CY7C1049BNV33

512K x 8 Static RAM

Features

- **High speed**
  - **— t_{AA} = 12 ns**
- **Low active power**
  - **— 504 mW (max.)**
- **Low CMOS standby power (Commercial L version)**
  - **— 1.8 mW (max.)**
- **2.0V Data Retention (660 µW at 2.0V retention)**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**

Functional Description[1]

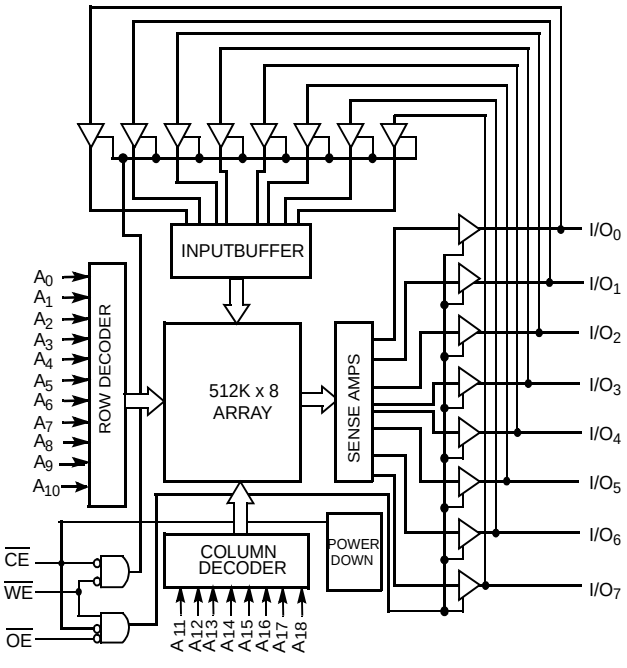
The CY7C1049BNV33 is a high-performance CMOS Static RAM organized as 524,288 words by 8 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers. Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{18}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

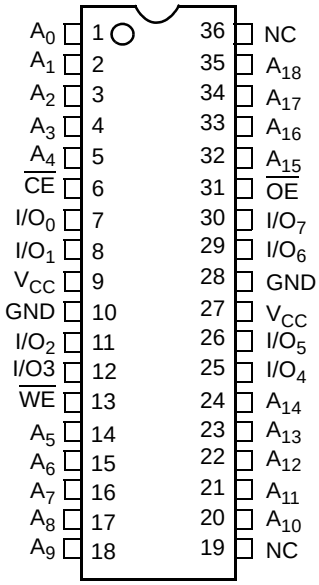
The CY7C1049BNV33 is available in a standard 400-mil-wide 36-pin SOJ and 44-pin TSOPII packages with center power and ground (revolutionary) pinout.

Logic Block Diagram

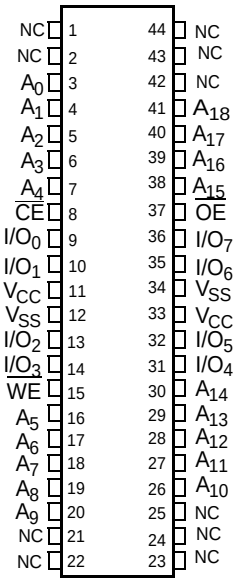


Pin Configuration

SOJ
Top View



TSOP
Top View



Selection Guide

			-12	-15	-20
Maximum Access Time (ns)			12	15	20
Maximum Operating Current (mA)	Com'l		200	180	160
	Ind'l		220	200	170
Maximum CMOS Standby Current (mA)	Com'l/Ind'l		8	8	8
	Com'l	L	0.5	0.5	0.5

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[2].....–0.5V to +4.6V

DC Voltage Applied to Outputs[2] in High Z State .....–0.5V to V_{CC} + 0.5V

DC Input Voltage[2] .....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.3V ± 0.3V
Industrial	–40°C to +85°C	

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-12 Min.	-12 Max.	-15 Min.	-15 Max.	-20 Min.	-20 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	2.2	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage[2]			–0.5	0.8	–0.5	0.8	–0.5	0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$	Com'l		200		180		160	mA
			Ind'l		220		200		170	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			30		30		30	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Com'l/Ind'l		8		8		8	mA
			Com'l L		0.5		0.5		0.5	mA

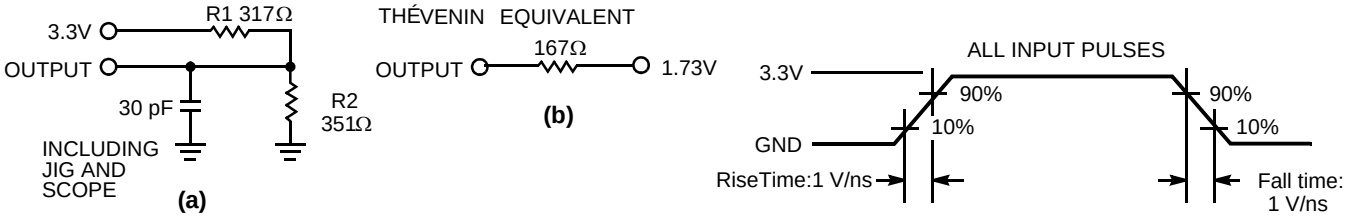
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	8	pF
C_{OUT}	I/O Capacitance		8	pF

Notes:
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.
2. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

[+] Feedback

AC Test Loads and Waveforms



AC Switching Characteristics[4] Over the Operating Range

Parameter	Description	-12		-15		-20		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{power}	V_{CC} (typical) to the First Access[5]	1		1		1		µs
t_{RC}	Read Cycle Time	12		15		20		ns
t_{AA}	Address to Data Valid		12		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		6		7		8	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z	0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[6, 7]		6		7		8	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[7]	3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6, 7]		6		7		8	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20	ns
Write Cycle[8, 9]								
t_{WC}	Write Cycle Time	12		15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	10		12		13		ns
t_{AW}	Address Set-Up to Write End	10		12		13		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	10		12		13		ns
t_{SD}	Data Set-Up to Write End	7		8		9		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z[7]	3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z[6, 7]		6		7		8	ns

Notes:

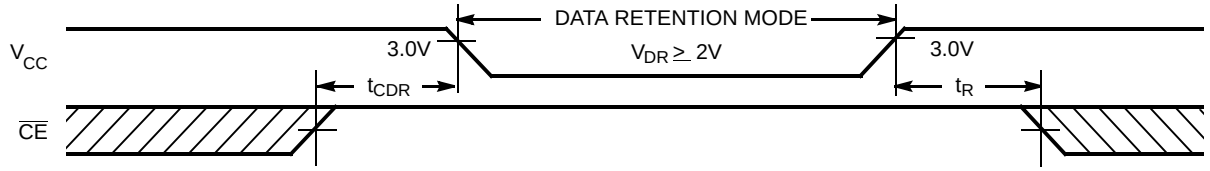
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
5. This part has a voltage regulator which steps down the voltage from 5V to 3.3V internally. T_{power} time has to be provided initially before a read/write operation is started.
6. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
7. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a write, and the transition of either of these signals can terminate the write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the write.
9. The minimum write cycle time for Write Cycle No. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. No input may exceed V_{CC} + 0.5V
11. .$t_r \leq 3$ ns for the -12 and -15 speeds. $t_r \leq 5$ ns for the -20 ns and slower speeds.

[+] Feedback

Data Retention Characteristics Over the Operating Range (For L version only)

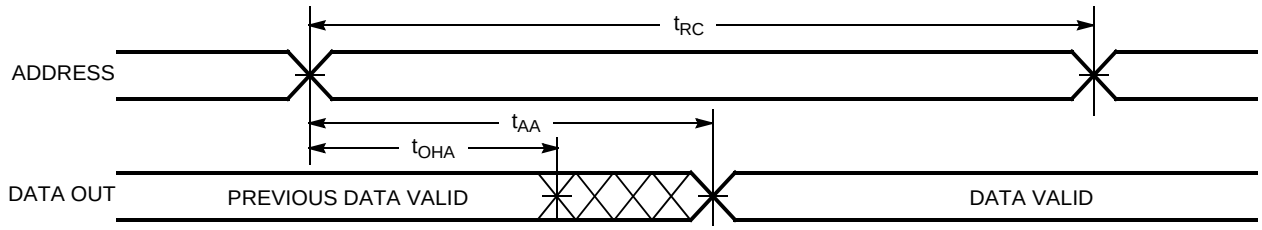
Parameter	Description	Conditions[10]	Min.	Max	Unit
V_{DR}	V_{CC} for Data Retention		2.0		V
I_{CCDR}	Data Retention Current	$\overline{V_{CC}} = V_{DR} = 2.0V$, $\overline{CE} \geq V_{CC} - 0.3V$ $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$		330	μA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0		ns
t_R[11]	Operation Recovery Time		t_{RC}		ns

Data Retention Waveform

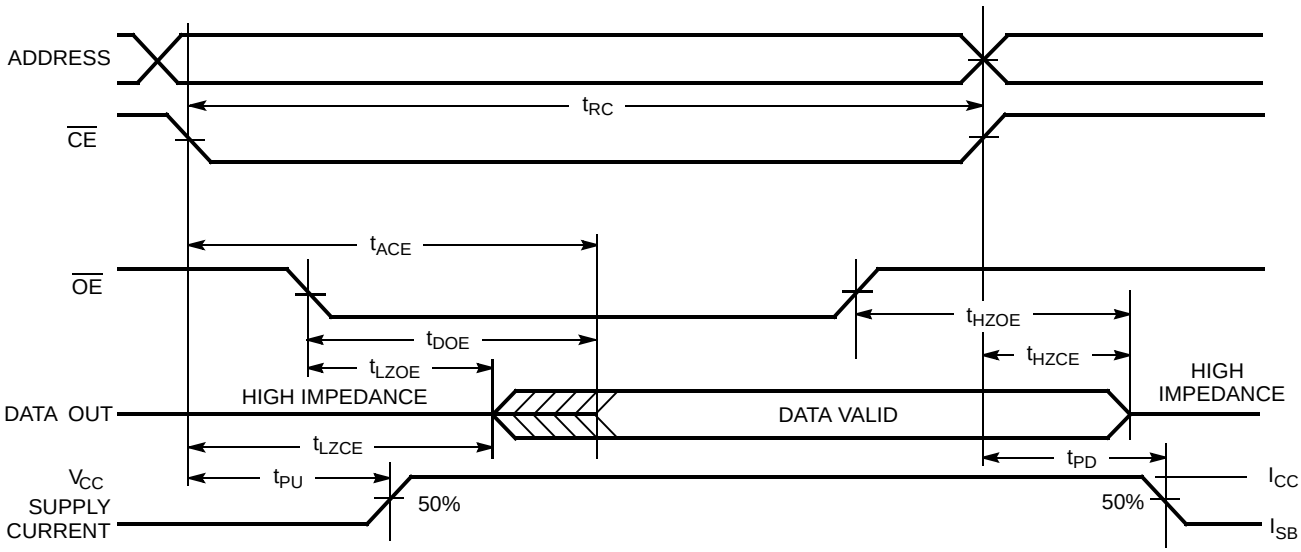


Switching Waveforms

Read Cycle No. 1[12, 13]



Read Cycle No. 2 ($\overline{OE}$ Controlled)[13, 14]

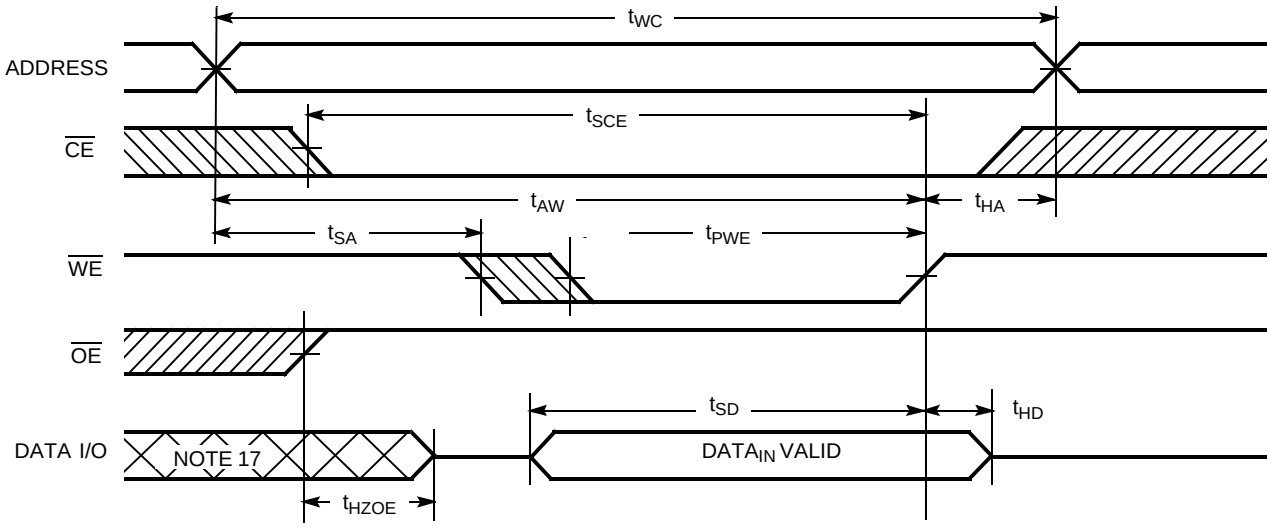


Notes:
12. Device is continuously selected. $\overline{OE}$, $\overline{CE} = V_{IL}$.
13. $\overline{WE}$ is HIGH for read cycle.
14. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

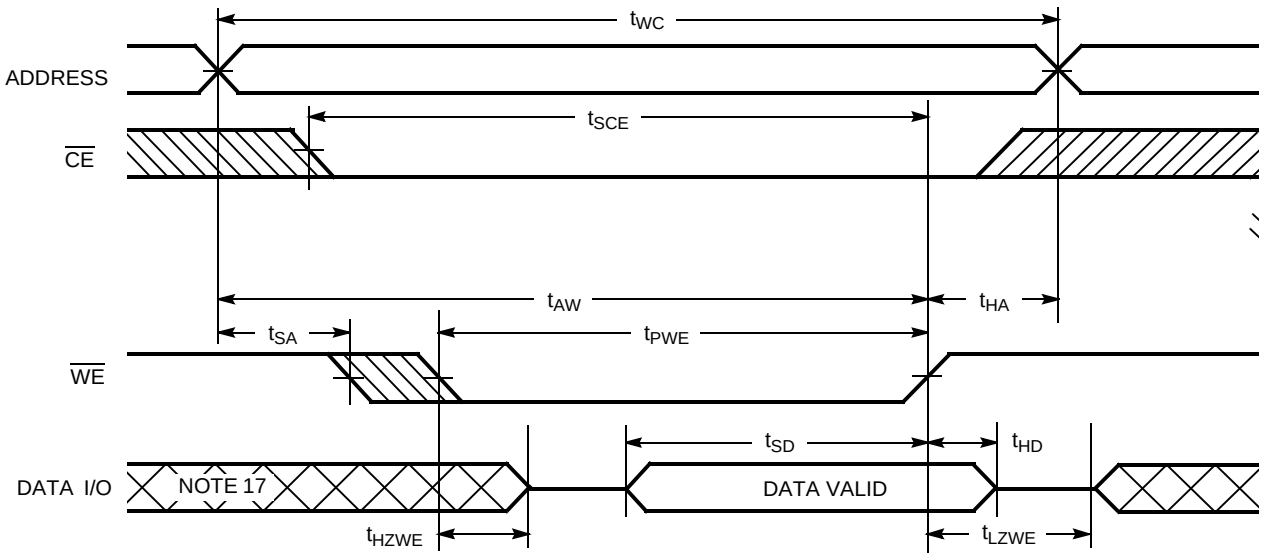
[+] Feedback

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[15, 16]



Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[16]



Truth Table

$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 – I/O_7$	Mode	Power
H	X	X	High Z	Power-Down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High Z	Selected, Outputs Disabled	Active (I_{CC})

Notes:
15. Data I/O is high-impedance if $\overline{OE}$ = V_{IH}.
16. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
17. During this period the I/Os are in the output state and input signals should not be applied.

[+] Feedback

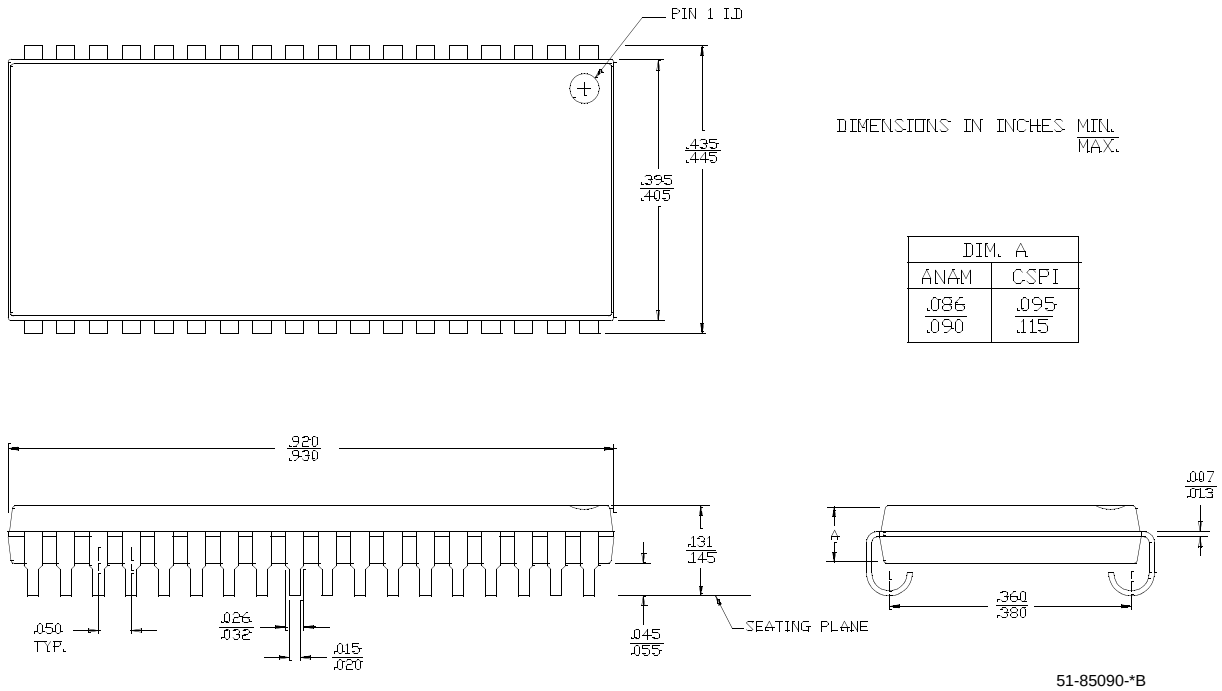
Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
12	CY7C1049BNV33-12ZC	51-85087	44-Pin TSOP II Z44	Commercial
	CY7C1049BNV33-12VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33-12VI	51-85090	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BNV33-12VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
15	CY7C1049BNV33-15VC	51-85090	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BNV33-15VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33L-15VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33-15ZC	51-85087	44-Pin TSOP II Z44	
	CY7C1049BNV33-15VI	51-85090	36-Lead (400-Mil) Molded SOJ	Industrial
	CY7C1049BNV33-15VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33-15ZI	51-85087	44-Pin TSOP II Z44	
20	CY7C1049BNV33-20VC	51-85090	36-Lead (400-Mil) Molded SOJ	Commercial
	CY7C1049BNV33-20VXC	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	
	CY7C1049BNV33-20VXI	51-85090	36-Lead (400-Mil) Molded SOJ (Pb-free)	Industrial

Please contact local sales representative regarding availability of these parts

Package Diagrams

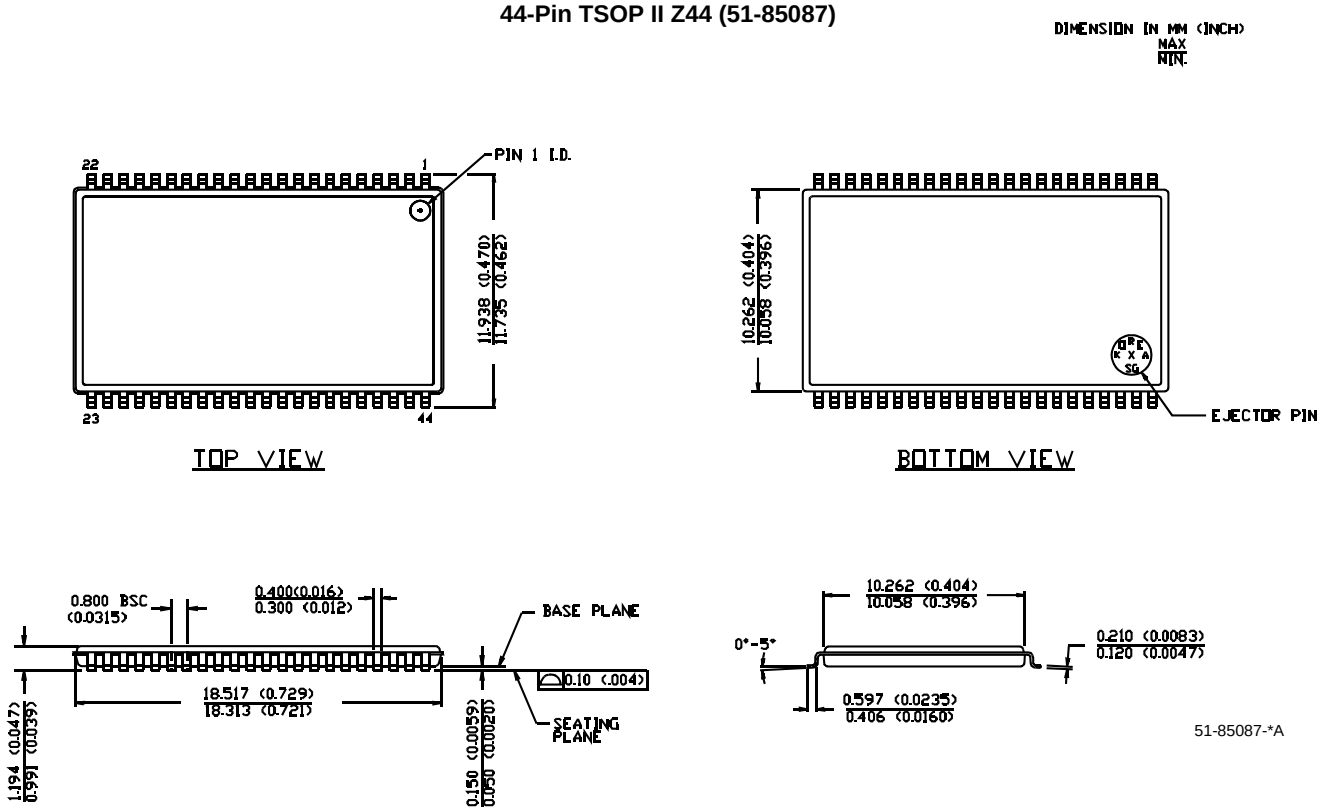
36-pin (400-Mil) Molded SOJ (51-85090)



[+] Feedback

Package Diagrams (continued)

44-Pin TSOP II Z44 (51-85087)



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Document History Page

Document Title: CY7C1049BNV33 512K x 8 Static RAM Document Number: 001-06432				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	423847	See ECN	NXR	New Data Sheet

[+] Feedback