

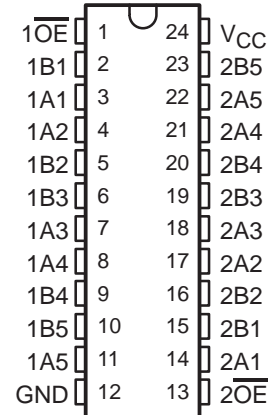
- 5-Ω Switch Connection Between Two Ports
- TTL-Compatible Input Levels

### description/ordering information

The SN74CBT3384A provides ten bits of high-speed TTL-compatible bus switching. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as two 5-bit switches with separate output-enable ( $\overline{OE}$ ) inputs. When  $\overline{OE}$  is low, the switch is on, and port A is connected to port B. When  $\overline{OE}$  is high, the switch is open, and the high-impedance state exists between the two ports.

DB, DBQ, DGV, DW, OR PW PACKAGE  
(TOP VIEW)



### ORDERING INFORMATION

| T <sub>A</sub> | PACKAGE†          |               | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|-------------------|---------------|-----------------------|------------------|
| –40°C to 85°C  | SOIC – DW         | Tube          | SN74CBT3384ADW        | CBT3384A         |
|                |                   | Tape and reel | SN74CBT3384ADWR       |                  |
|                | SSOP – DB         | Tape and reel | SN74CBT3384ADBR       | CU384A           |
|                | SSOP (QSOP) – DBQ | Tape and reel | SN74CBT3384ADBQR      | CBT3384A         |
|                | TSSOP – PW        | Tube          | SN74CBT3384APW        | CU384A           |
|                |                   | Tape and reel | SN74CBT3384APWR       |                  |
|                | TVSOP – DGV       | Tape and reel | SN74CBT3384ADGVR      | CU384A           |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

### FUNCTION TABLE (each 5-bit bus switch)

| INPUTS           |                  | INPUTS/OUTPUTS |         |
|------------------|------------------|----------------|---------|
| $\overline{1OE}$ | $\overline{2OE}$ | 1B1–1B5        | 2B1–2B5 |
| L                | L                | 1A1–1A5        | 2A1–2A5 |
| L                | H                | 1A1–1A5        | Z       |
| H                | L                | Z              | 2A1–2A5 |
| H                | H                | Z              | Z       |



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 **TEXAS  
INSTRUMENTS**

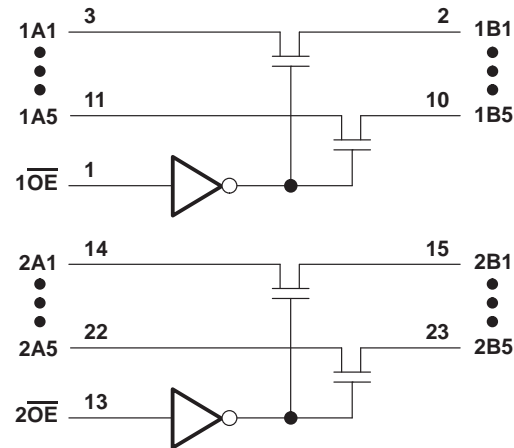
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SN74CBT3384A
10-BIT FET BUS SWITCH

SCDS004L – NOVEMBER 1992 – REVISED JANUARY 2004

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Table with 2 columns: Parameter and Rating. Parameters include Supply voltage range (VCC), Input voltage range (VI), Continuous channel current, Input clamp current (IJK), Package thermal impedance (thetaJA) for DBQ, DGV, DW, and PW packages, and Storage temperature range (Tstg).

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- 2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

Table with 4 columns: Parameter, MIN, MAX, and UNIT. Parameters include VCC (Supply voltage), VIH (High-level control input voltage), VIL (Low-level control input voltage), and TA (Operating free-air temperature).

NOTE 3: All unused control inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

| PARAMETER                |                | TEST CONDITIONS  |  | MIN | TYP† | MAX     | UNIT          |
|--------------------------|----------------|--|--|-----|------|---------|---------------|
| $V_{IK}$                 |                | $V_{CC} = 4.5\text{ V}$ ,<br>$I_I = -18\text{ mA}$                               |  |     |      | -1.2    | V             |
| $I_I$                    |                | $V_{CC} = 5.5\text{ V}$ ,<br>$V_I = 5.5\text{ V or GND}$                         |  |     |      | $\pm 1$ | $\mu\text{A}$ |
| $I_{CC}$                 |                | $V_{CC} = 5.5\text{ V}$ ,<br>$I_O = 0$ ,<br>$V_I = V_{CC} \text{ or GND}$        |  |     |      | 3       | $\mu\text{A}$ |
| $\Delta I_{CC}^\ddagger$ | Control inputs | $V_{CC} = 5.5\text{ V}$ ,<br>One input at 3.4 V, Other inputs at $V_{CC}$ or GND |  |     |      | 2.5     | mA            |
| $C_i$                    | Control inputs | $V_I = 3\text{ V or 0}$  |  |     |      | 4       | pF            |
| $C_{io(OFF)}$            |                | $V_O = 3\text{ V or 0}$ ,<br>$\overline{OE} = V_{CC}$                            |  |     |      | 4.5     | pF            |
| $r_{on}^\S$              |                | $V_{CC} = 4\text{ V}$ ,<br>TYP at $V_{CC} = 4\text{ V}$                          | $V_I = 2.4\text{ V}$ ,<br>$I_I = 15\text{ mA}$ |     |      | 14      | $\Omega$      |
|                          |                | $V_{CC} = 4.5\text{ V}$  | $V_I = 0$ ,<br>$I_I = 64\text{ mA}$            |     |      | 5       |               |
|                          |                |  | $I_I = 30\text{ mA}$                           |     |      | 5       |               |
|                          |                |  | $V_I = 2.4\text{ V}$ ,<br>$I_I = 15\text{ mA}$ |     |      | 10      |               |

† All typical values are at  $V_{CC} = 5\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

‡ This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lowest voltage of the two (A or B) terminals.

**switching characteristics over recommended operating free-air temperature range,  $C_L = 50\text{ pF}$  (unless otherwise noted) (see Figure 1)**

| PARAMETER          | FROM (INPUT)    | TO (OUTPUT) | $V_{CC} = 4\text{ V}$ |     | $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ |     | UNIT |
|--------------------|-----------------|-------------|-----------------------|-----|--|-----|------|
|                    |                 |             | MIN                   | MAX | MIN                                    | MAX |      |
| $t_{pd}^\parallel$ | A or B          | B or A      | 0.35                  |     | 0.25                                   |     | ns   |
| $t_{en}$           | $\overline{OE}$ | A or B      | 6.2                   |     | 1.9                                    | 5.7 | ns   |
| $t_{dis}$          | $\overline{OE}$ | A or B      | 5.5                   |     | 2.1                                    | 5.2 | ns   |

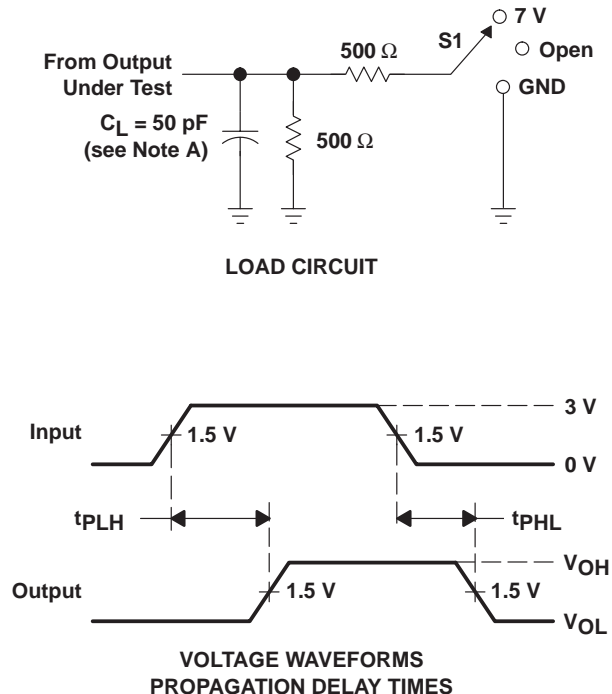
¶ The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

# SN74CBT3384A

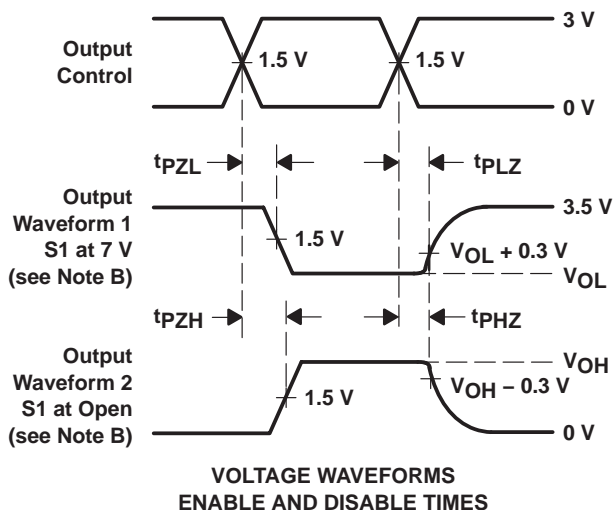
## 10-BIT FET BUS SWITCH

SCDS004L – NOVEMBER 1992 – REVISED JANUARY 2004

### PARAMETER MEASUREMENT INFORMATION



| TEST              | S1   |
|-------------------|------|
| $t_{pd}$          | Open |
| $t_{PLZ}/t_{PZL}$ | 7 V  |
| $t_{PHZ}/t_{PZH}$ | Open |



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5 \text{ ns}$ ,  $t_f \leq 2.5 \text{ ns}$ .
  - D. The outputs are measured one at a time with one transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

| Orderable Device   | Status <sup>(1)</sup> | Package Type  | Package Drawing | Pins | Package Qty | Eco Plan <sup>(2)</sup>    | Lead/Ball Finish | MSL Peak Temp <sup>(3)</sup> |
|--------------------|-----------------------|---------------|-----------------|------|-------------|----------------------------|------------------|------------------------------|
| SN74CBT3384ADBLE   | OBSOLETE              | SSOP          | DB              | 24   |             | TBD                        | Call TI          | Call TI                      |
| SN74CBT3384ADBQR   | ACTIVE                | SSOP/<br>QSOP | DBQ             | 24   | 2500        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-2-260C-1YEAR           |
| SN74CBT3384ADBQRE4 | ACTIVE                | SSOP/<br>QSOP | DBQ             | 24   | 2500        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-2-260C-1YEAR           |
| SN74CBT3384ADBQRG4 | ACTIVE                | SSOP/<br>QSOP | DBQ             | 24   | 2500        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-2-260C-1YEAR           |
| SN74CBT3384ADBR    | ACTIVE                | SSOP          | DB              | 24   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384ADBRE4  | ACTIVE                | SSOP          | DB              | 24   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384ADGVR   | ACTIVE                | TVSOP         | DGV             | 24   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384ADGVRE4 | ACTIVE                | TVSOP         | DGV             | 24   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384ADW     | ACTIVE                | SOIC          | DW              | 24   | 25          | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384ADWE4   | ACTIVE                | SOIC          | DW              | 24   | 25          | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384ADWR    | ACTIVE                | SOIC          | DW              | 24   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384ADWRE4  | ACTIVE                | SOIC          | DW              | 24   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384APW     | ACTIVE                | TSSOP         | PW              | 24   | 60          | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384APWE4   | ACTIVE                | TSSOP         | PW              | 24   | 60          | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384APWLE   | OBSOLETE              | TSSOP         | PW              | 24   |             | TBD                        | Call TI          | Call TI                      |
| SN74CBT3384APWR    | ACTIVE                | TSSOP         | PW              | 24   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |
| SN74CBT3384APWRE4  | ACTIVE                | TSSOP         | PW              | 24   | 2000        | Green (RoHS &<br>no Sb/Br) | CU NIPDAU        | Level-1-260C-UNLIM           |

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

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**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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## DGV (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

## DW (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE

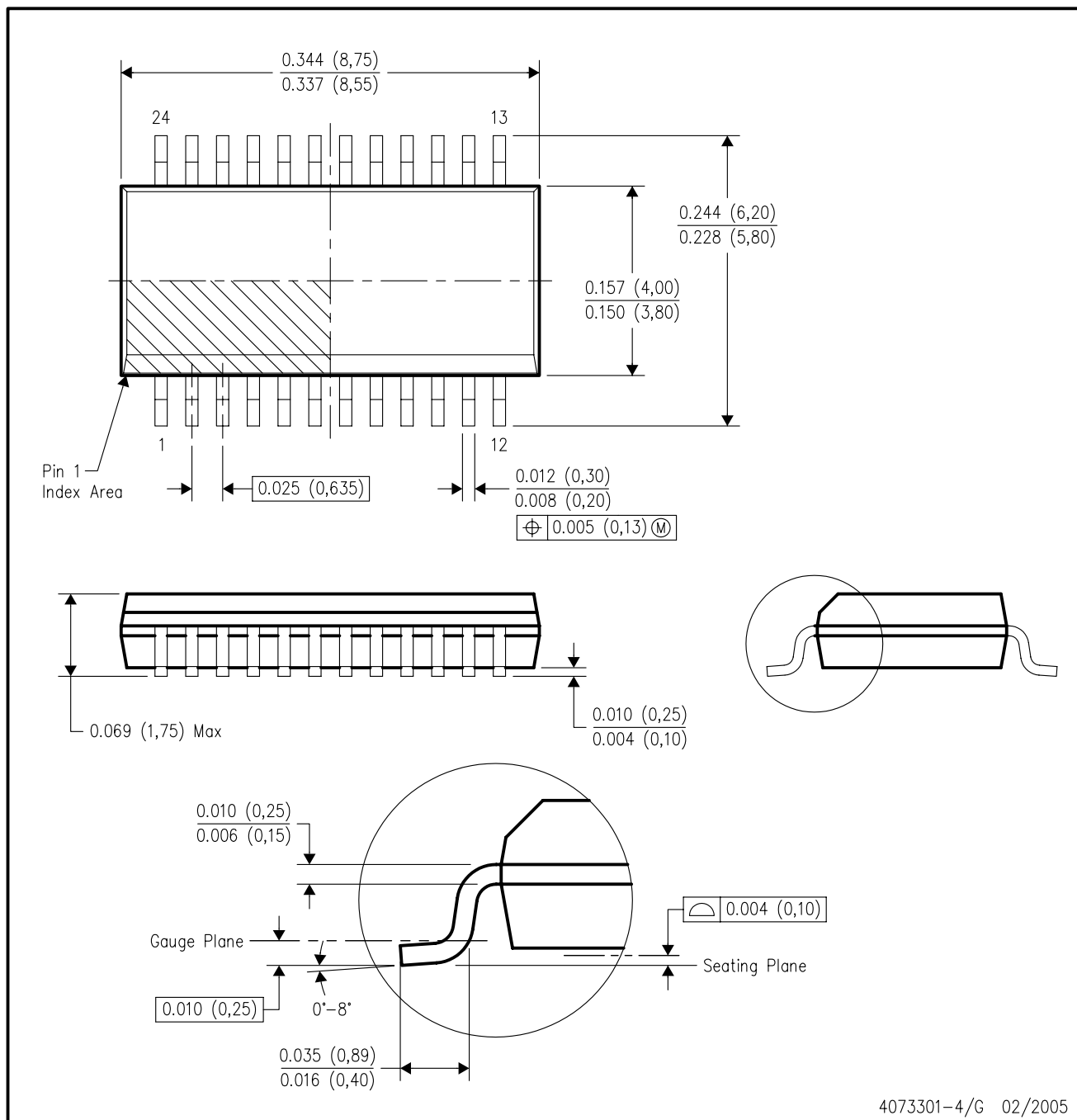


- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - Falls within JEDEC MS-013 variation AD.



## DBQ (R-PDSO-G24)

## PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
  - Falls within JEDEC MO-137 variation AE.

## DB (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## PW (R-PDSO-G\*\*)

## PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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