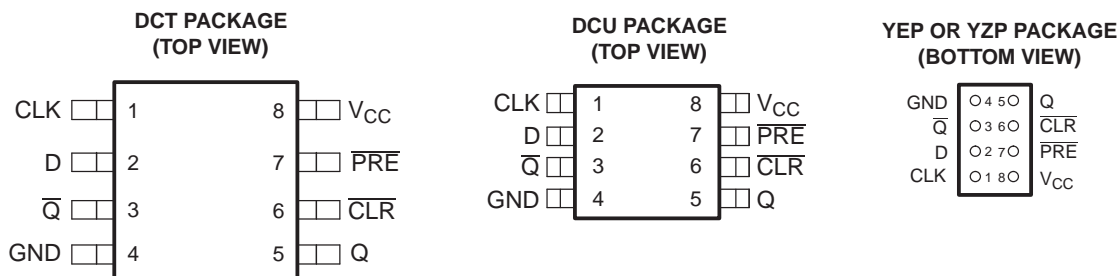


FEATURES

- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Low Static-Power Consumption:
 $I_{CC} = 0.9 \mu A$ Max
- Low Dynamic-Power Consumption:
 $C_{pd} = 4.3$ pF Typ at 3.3 V
- Low Input Capacitance: $C_i = 1.5$ pF Typ
- Low Noise – Overshoot and Undershoot
<10% of V_{CC}
- I_{off} Supports Partial-Power-Down Mode Operation
- Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the Input ($V_{hys} = 250$ mV Typ at 3.3 V)
- Wide Operating V_{CC} Range of 0.8 V to 3.6 V
- Optimized for 3.3-V Operation
- 3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation
- $t_{pd} = 4.3$ ns Max at 3.3 V
- Suitable for Point-to-Point Applications
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Performance Tested Per JESD 22
 - 2000-V Human-Body Model (A114-B, Class II)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)
- ESD Protection Exceeds ± 5000 V With Human-Body Model



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see the very low undershoot and overshoot characteristics shown in Figure 2).

ORDERING INFORMATION

T_A	PACKAGE ⁽¹⁾		ORDERABLE PART NUMBER	TOP-SIDE MARKING ⁽²⁾
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74AUP1G74YEPR	_ _ _ HS _
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)	Reel of 3000	SN74AUP1G74YZPR	
	SSOP – DCT	Reel of 3000	SN74AUP1G74DCTR	H74_ _ _
	VSSOP – DCU	Reel of 3000	SN74AUP1G74DCUR	H74_

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

(2) DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.
DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar, NanoFree are trademarks of Texas Instruments.

SN74AUP1G74

LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCES644A—MARCH 2006—REVISED SEPTEMBER 2006

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

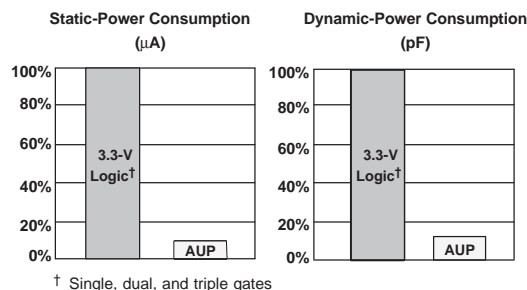


Figure 1. AUP – The Lowest-Power Family

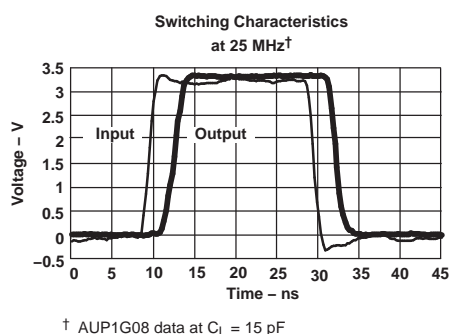


Figure 2. Excellent Signal Integrity

This single positive-edge-triggered D-type flip-flop is designed for 0.8-V to 3.6-V V_{CC} operation.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) input sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) input meeting the setup time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not related directly to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. To better optimize the flip-flop for higher frequencies, the \overline{CLR} input overrides the \overline{PRE} input when they are both low.

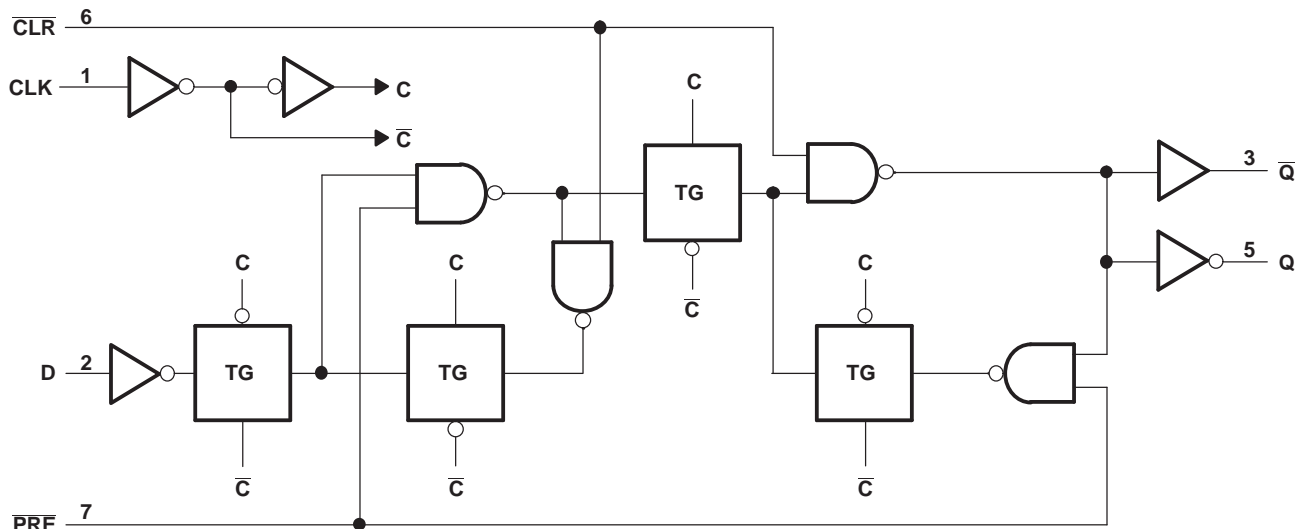
NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

FUNCTION TABLE

INPUTS				OUTPUTS	
\overline{PRE}	\overline{CLR}	CLK	D	Q	\overline{Q}
L	H	X	X	H	L
X	L	X	X	L	H
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q_0	\overline{Q}_0

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V _{CC}	Supply voltage range		−0.5	4.6	V
V _I	Input voltage range ⁽²⁾		−0.5	4.6	V
V _O	Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾		−0.5	4.6	V
V _O	Output voltage range in the high or low state ⁽²⁾		−0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	V _I < 0	−50		mA
I _{OK}	Output clamp current	V _O < 0	−50		mA
I _O	Continuous output current		±20		mA
Continuous current through V _{CC} or GND			±50		mA
θ _{JA}	Package thermal impedance ⁽³⁾	DCT package	220		°C/W
		DCU package	227		
		YEP/YZP package	102		
T _{std}	Storage temperature range		−65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		0.8	3.6	V
V _{IH}	High-level input voltage	V _{CC} = 0.8 V	V _{CC}		V
		V _{CC} = 1.1 V to 1.95 V	0.65 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	1.6		
		V _{CC} = 3 V to 3.6 V	2		
V _{IL}	Low-level input voltage	V _{CC} = 0.8 V	0		V
		V _{CC} = 1.1 V to 1.95 V	0.35 × V _{CC}		
		V _{CC} = 2.3 V to 2.7 V	0.7		
		V _{CC} = 3 V to 3.6 V	0.9		
V _I	Input voltage		0	3.6	V
V _O	Output voltage		0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 0.8 V	−20		mA
		V _{CC} = 1.1 V	−1.1		
		V _{CC} = 1.4 V	−1.7		
		V _{CC} = 1.65	−1.9		
		V _{CC} = 2.3 V	−3.1		
		V _{CC} = 3 V	−4		
I _{OL}	Low-level output current	V _{CC} = 0.8 V	20		mA
		V _{CC} = 1.1 V	1.1		
		V _{CC} = 1.4 V	1.7		
		V _{CC} = 1.65 V	1.9		
		V _{CC} = 2.3 V	3.1		
		V _{CC} = 3 V	4		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 0.8 V to 3.6 V	200		ns/V
T _A	Operating free-air temperature		−40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	T _A = 25°C			T _A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V _{OH}		I _{OH} = –20 μA	0.8 V to 3.6 V	V _{CC} – 0.1			V _{CC} – 0.1		V
		I _{OH} = –1.1 mA	1.1 V	0.75 × V _{CC}			0.7 × V _{CC}		
		I _{OH} = –1.7 mA	1.4 V	1.11			1.03		
		I _{OH} = –1.9 mA	1.65 V	1.32			1.3		
		I _{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I _{OH} = –3.1 mA		1.9			1.85		
		I _{OH} = –2.7 mA	3 V	2.72			2.67		
		I _{OH} = –4 mA		2.6			2.55		
V _{OL}		I _{OL} = 20 μA	0.8 V to 3.6 V	0.1			0.1		V
		I _{OL} = 1.1 mA	1.1 V	0.3 × V _{CC}			0.3 × V _{CC}		
		I _{OL} = 1.7 mA	1.4 V	0.31			0.37		
		I _{OL} = 1.9 mA	1.65 V	0.31			0.35		
		I _{OL} = 2.3 mA	2.3 V	0.31			0.33		
		I _{OL} = 3.1 mA		0.44			0.45		
		I _{OL} = 2.7 mA	3 V	0.31			0.33		
		I _{OL} = 4 mA		0.44			0.45		
I _I	A or B input	V _I = GND to 3.6 V	0 V to 3.6 V	0.1			0.5	μA	
I _{off}		V _I or V _O = 0 V to 3.6 V	0 V	0.2			0.6	μA	
ΔI _{off}		V _I or V _O = 0 V to 3.6 V	0 V to 0.2 V	0.2			0.6	μA	
I _{CC}		V _I = GND or (V _{CC} to 3.6 V), I _O = 0	0.8 V to 3.6 V	0.5			0.9	μA	
ΔI _{CC}		V _I = V _{CC} – 0.6 V ⁽¹⁾ , I _O = 0	3.3 V	40			50	μA	
C _i		V _I = V _{CC} or GND	0 V	1.5					pF
			3.6 V	1.5					
C _O		V _O = GND	0 V	3					pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

SN74AUP1G74

LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCES644A—MARCH 2006—REVISED SEPTEMBER 2006

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 3](#))

PARAMETER		V _{CC}	T _A = 25°C	T _A = –40°C to 85°C		UNIT
			TYP	MIN	MAX	
f _{clock}	Clock frequency	0.8 V	21			MHz
		1.2 V ± 0.1 V			40	
		1.5 V ± 0.1 V			50	
		1.8 V ± 0.15 V			60	
		2.5 V ± 0.2 V			90	
		3.3 V ± 0.3 V			90	
t _w	CLK high or low	0.8 V	3.5			ns
		1.2 V ± 0.1 V		2		
		1.5 V ± 0.1 V		2		
		1.8 V ± 0.15 V		2		
		2.5 V ± 0.2 V		2		
		3.3 V ± 0.3 V		2		
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ low	0.8 V	4.5			
		1.2 V ± 0.1 V		2		
		1.5 V ± 0.1 V		2		
		1.8 V ± 0.15 V		2		
		2.5 V ± 0.2 V		2		
		3.3 V ± 0.3 V		2		
t _{su}	Data high	0.8 V	3			ns
		1.2 V ± 0.1 V		1.3		
		1.5 V ± 0.1 V		1		
		1.8 V ± 0.15 V		1		
		2.5 V ± 0.2 V		0.5		
		3.3 V ± 0.3 V		0.5		
	Data low	0.8 V	1			
		1.2 V ± 0.1 V		1.2		
		1.5 V ± 0.1 V		1		
		1.8 V ± 0.15 V		1		
		2.5 V ± 0.2 V		1		
		3.3 V ± 0.3 V		1		
	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$ inactive	0.8 V	1			
		1.2 V ± 0.1 V		0.5		
		1.5 V ± 0.1 V		0.5		
		1.8 V ± 0.15 V		0.5		
		2.5 V ± 0.2 V		0.5		
		3.3 V ± 0.3 V		0.5		
t _h	Hold time, data after CLK↑	0.8 V	0			ns
		1.2 V ± 0.1 V		0		
		1.5 V ± 0.1 V		0		
		1.8 V ± 0.15 V		0		
		2.5 V ± 0.2 V		0		
		3.3 V ± 0.3 V		0		

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 5$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		60				MHz
			1.2 V \pm 0.1 V		80		60		
			1.5 V \pm 0.1 V		125		90		
			1.8 V \pm 0.15 V		150		120		
			2.5 V \pm 0.2 V		180		160		
			3.3 V \pm 0.3 V		190		180		
t_{pd}	CLK	Q	0.8 V		31				ns
			1.2 V \pm 0.1 V	2	10	20	2.7	20.4	
			1.5 V \pm 0.1 V	2	6	12	1.9	12.4	
			1.8 V \pm 0.15 V	2	5	9	1.4	9.5	
			2.5 V \pm 0.2 V	2	3	6	1.1	6.2	
			3.3 V \pm 0.3 V	2	3	4	1	4.7	
		\overline{Q}	0.8 V		28				
			1.2 V \pm 0.1 V	2	9	19	2.4	19	
			1.5 V \pm 0.1 V	2	6	11	1.6	11.8	
			1.8 V \pm 0.15 V	2	5	9	1.3	9	
			2.5 V \pm 0.2 V	2	3	6	1.1	6	
			3.3 V \pm 0.3 V	2	3	4	1	4.6	
	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	0.8 V		26				
			1.2 V \pm 0.1 V	2	9	20	2	20	
			1.5 V \pm 0.1 V	2	6	12	1.5	13	
			1.8 V \pm 0.15 V	2	5	9	1.3	10	
			2.5 V \pm 0.2 V	2	3	6	1	7	
			3.3 V \pm 0.3 V	2	3	5	1	5	

SN74AUP1G74

LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCES644A—MARCH 2006—REVISED SEPTEMBER 2006

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 10$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{\max}			0.8 V		46				MHz
			$1.2\text{ V} \pm 0.1\text{ V}$		65		50		
			$1.5\text{ V} \pm 0.1\text{ V}$		95		55		
			$1.8\text{ V} \pm 0.15\text{ V}$		110		60		
			$2.5\text{ V} \pm 0.2\text{ V}$		170		130		
			$3.3\text{ V} \pm 0.3\text{ V}$		180		160		
t_{pd}	CLK	Q	0.8 V		33				ns
			$1.2\text{ V} \pm 0.1\text{ V}$	2	10	22	3.4	21.8	
			$1.5\text{ V} \pm 0.1\text{ V}$	2	7	13	2.4	13.5	
			$1.8\text{ V} \pm 0.15\text{ V}$	2	6	10	1.9	10.4	
			$2.5\text{ V} \pm 0.2\text{ V}$	2	4	6	1.5	7	
			$3.3\text{ V} \pm 0.3\text{ V}$	2	3	5	1.2	5.3	
		\overline{Q}	0.8 V		30				
			$1.2\text{ V} \pm 0.1\text{ V}$	2	10	20	3	20.3	
			$1.5\text{ V} \pm 0.1\text{ V}$	2	7	12	2.2	12.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	2	5	9	1.8	9.9	
			$2.5\text{ V} \pm 0.2\text{ V}$	2	4	6	1.3	6.7	
			$3.3\text{ V} \pm 0.3\text{ V}$	2	3	5	1.1	5.2	
	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	0.8 V		29				
			$1.2\text{ V} \pm 0.1\text{ V}$	2	10	21	2	21.4	
			$1.5\text{ V} \pm 0.1\text{ V}$	2	7	13	2	13.8	
			$1.8\text{ V} \pm 0.15\text{ V}$	2	5	10	2	10.8	
			$2.5\text{ V} \pm 0.2\text{ V}$	2	4	7	1.5	7.4	
			$3.3\text{ V} \pm 0.3\text{ V}$	2	3	5	1.5	5.8	

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		41				MHz
			1.2 V \pm 0.1 V		75		50		
			1.5 V \pm 0.1 V		95		55		
			1.8 V \pm 0.15 V		100		60		
			2.5 V \pm 0.2 V		150		130		
			3.3 V \pm 0.3 V		200		160		
t_{pd}	CLK	Q	0.8 V		35				ns
			1.2 V \pm 0.1 V	2	12	23.1	4.1	23.2	
			1.5 V \pm 0.1 V	2	8	14.1	2.9	14.6	
			1.8 V \pm 0.15 V	2	6	10.7	2.4	11.3	
			2.5 V \pm 0.2 V	2	4	7	1.9	7.6	
			3.3 V \pm 0.3 V	2	4	5.4	1.6	5.9	
		\overline{Q}	0.8 V		32				
			1.2 V \pm 0.1 V	2	11	21.8	3.7	21.8	
			1.5 V \pm 0.1 V	2	7	13.5	2.6	14	
			1.8 V \pm 0.15 V	2	6	10.4	2.2	10.9	
			2.5 V \pm 0.2 V	2	4	7.1	1.7	7.5	
			3.3 V \pm 0.3 V	2	3	5.4	1.4	5.8	
	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	0.8 V		31				
			1.2 V \pm 0.1 V	2	11	23	2	22.9	
			1.5 V \pm 0.1 V	2	7	14	2	14.9	
			1.8 V \pm 0.15 V	2	6	11	2	11.7	
			2.5 V \pm 0.2 V	2	4	7	2	8.1	
			3.3 V \pm 0.3 V	2	4	6	1.5	6.4	

SN74AUP1G74

LOW-POWER SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

SCES644A—MARCH 2006—REVISED SEPTEMBER 2006

Switching Characteristics

over recommended operating free-air temperature range, $C_L = 30$ pF (unless otherwise noted) (see [Figure 3](#) and [Figure 4](#))

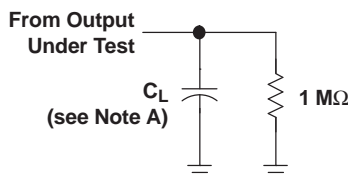
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	$T_A = 25^\circ\text{C}$			$T_A = -40^\circ\text{C to } 85^\circ\text{C}$		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{\max}			0.8 V		21				MHz
			1.2 V \pm 0.1 V		50		40		
			1.5 V \pm 0.1 V		60		50		
			1.8 V \pm 0.15 V		75		70		
			2.5 V \pm 0.2 V		100		90		
			3.3 V \pm 0.3 V		100		90		
t_{pd}	CLK	Q	0.8 V		32				ns
			1.2 V \pm 0.1 V	3	14	27	5.9	27	
			1.5 V \pm 0.1 V	3	10	17	4.4	17.2	
			1.8 V \pm 0.15 V	3	8	13	3.6	13.4	
			2.5 V \pm 0.2 V	3	6	9	3	9.2	
			3.3 V \pm 0.3 V	3	5	7	2.6	7.2	
		\overline{Q}	0.8 V		40				
			1.2 V \pm 0.1 V	3	13	26	5.5	25.9	
			1.5 V \pm 0.1 V	3	9	16	4.1	16.8	
			1.8 V \pm 0.15 V	3	7	13	3.5	13.2	
			2.5 V \pm 0.2 V	3	5	9	2.7	9.2	
			3.3 V \pm 0.3 V	3	5	7	2.4	7.2	
	\overline{PRE} or \overline{CLR}	Q or \overline{Q}	0.8 V		38				
			1.2 V \pm 0.1 V	3	13	26	3	27	
			1.5 V \pm 0.1 V	3	9	17	3	17.4	
			1.8 V \pm 0.15 V	3	8	13	3	14	
			2.5 V \pm 0.2 V	3	6	9	3	10	
			3.3 V \pm 0.3 V	3	5	7	2.5	8	

Operating Characteristics

$T_A = 25^\circ\text{C}$

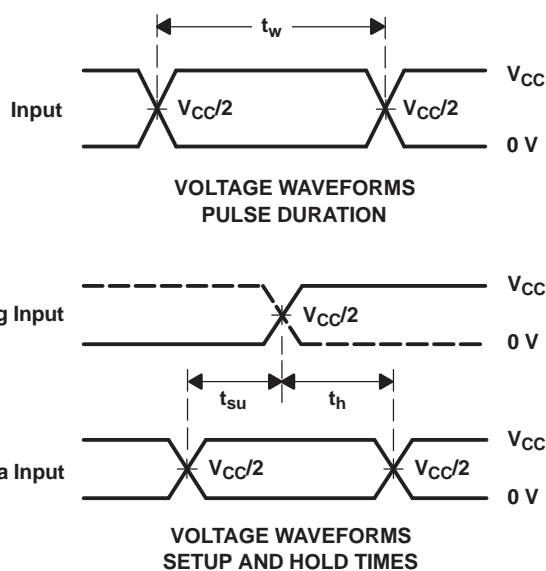
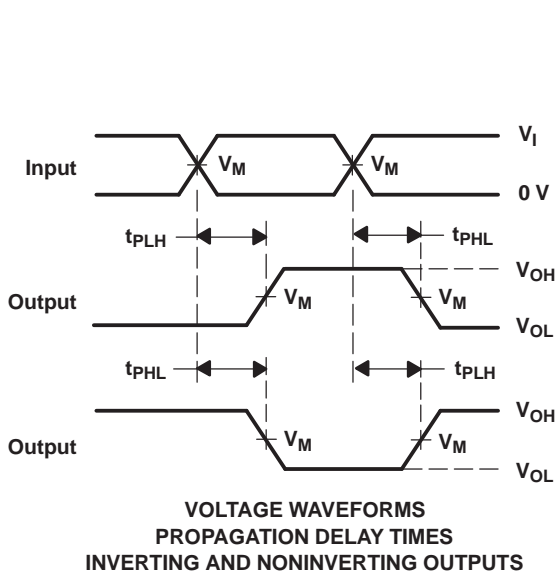
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	$f = 10$ MHz	0.8 V	5.5	pF
			1.2 V \pm 0.1 V	5.5	
			1.5 V \pm 0.1 V	5.5	
			1.8 V \pm 0.15 V	5.5	
			2.5 V \pm 0.2 V	5.5	
			3.3 V \pm 0.3 V	5.5	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Width)



LOAD CIRCUIT

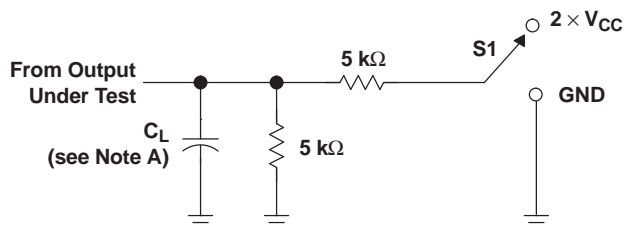
	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



- NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd} .
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

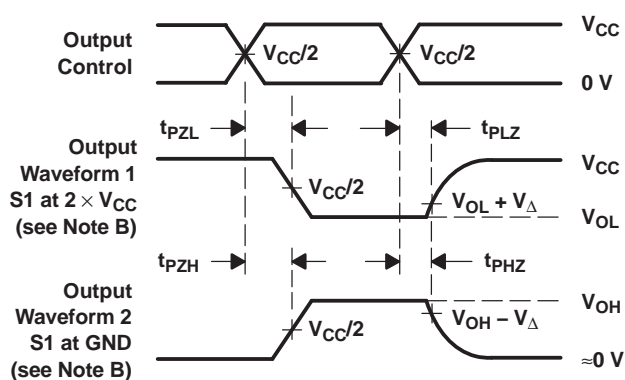
PARAMETER MEASUREMENT INFORMATION (Enable and Disable Times)



TEST	S1
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PHL}	GND

LOAD CIRCUIT

	$V_{CC} = 0.8 \text{ V}$	$V_{CC} = 1.2 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.5 \text{ V}$ $\pm 0.1 \text{ V}$	$V_{CC} = 1.8 \text{ V}$ $\pm 0.15 \text{ V}$	$V_{CC} = 2.5 \text{ V}$ $\pm 0.2 \text{ V}$	$V_{CC} = 3.3 \text{ V}$ $\pm 0.3 \text{ V}$
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_{Δ}	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r/t_f = 3 \text{ ns}$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AUP1G74DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G74DCURG4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

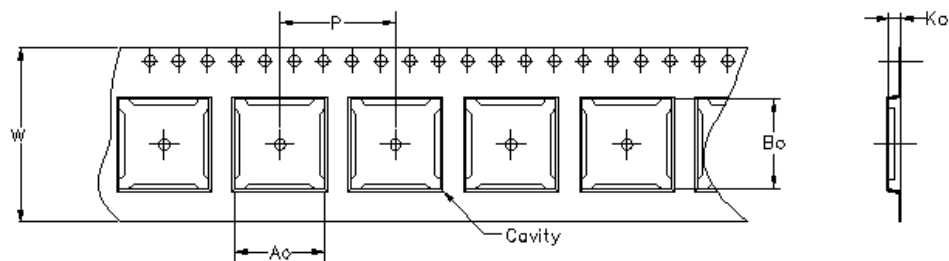
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

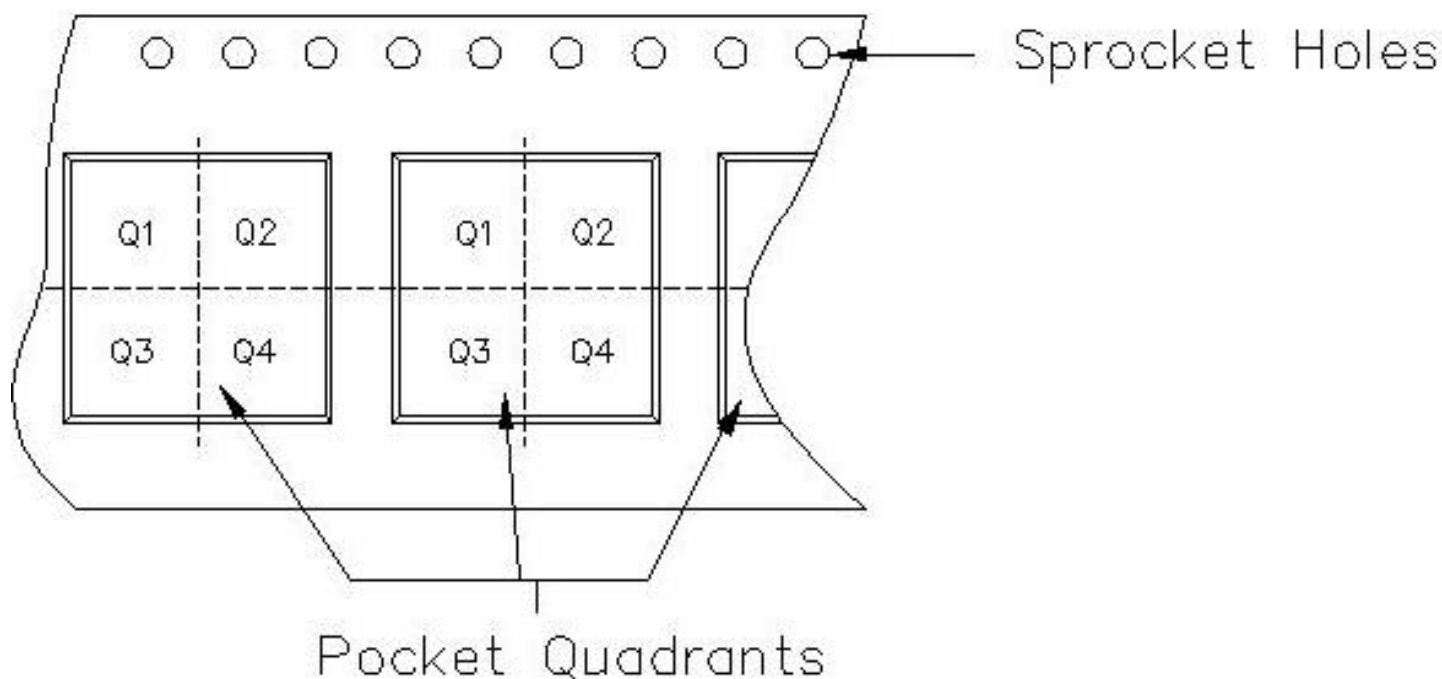
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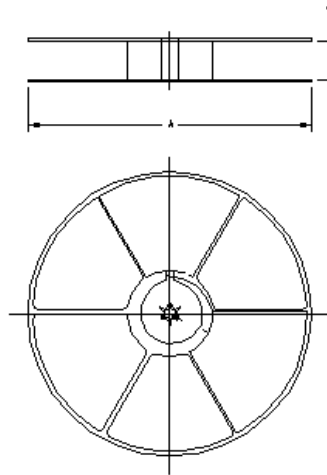
Carrier tape design is defined largely by the component length, width, and thickness.

A_0 = Dimension designed to accommodate the component width.
B_0 = Dimension designed to accommodate the component length.
K_0 = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



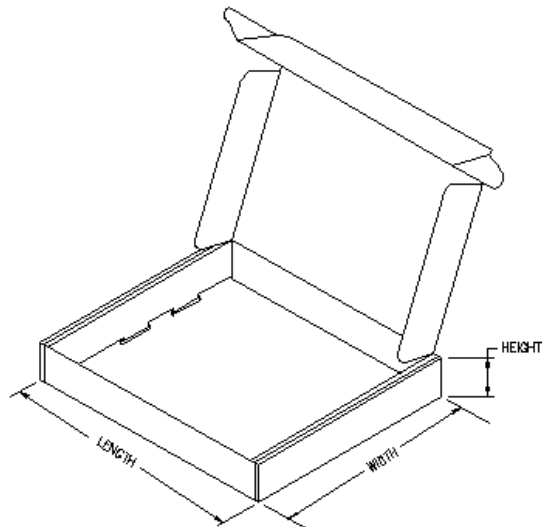
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AUP1G74DCUR	DCU	8	HNT	180	9	2.25	3.35	1.05	4	8	NONE



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74AUP1G74DCUR	DCU	8	HNT	202.0	201.0	28.0



DCU (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.

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