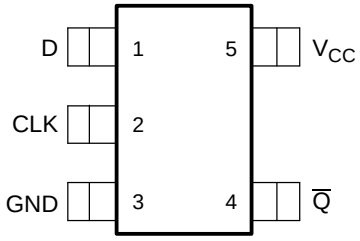
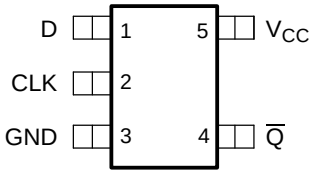
FEATURES

- **Available in the Texas Instruments NanoStar™ and NanoFree™ Packages**
- **Low Static-Power Consumption (I_{CC} = 0.9 μA Max)**
- **Low Dynamic-Power Consumption (C_{pd} = 4.3 pF Typ at 3.3 V)**
- **Low Input Capacitance (C_i = 1.5 pF Typ)**
- **Low Noise – Overshoot and Undershoot <10% of V_{CC}**
- **I_{off} Supports Partial-Power-Down Mode Operation**
- **Schmitt-Trigger Action Allows Slow Input Transition and Better Switching Noise Immunity at the Input (V_{hys} = 250 mV Typ at 3.3 V)**
- **Wide Operating V_{CC} Range of 0.8 V to 3.6 V**
- **Optimized for 3.3-V Operation**
- **3.6-V I/O Tolerant to Support Mixed-Mode Signal Operation**
- **t_{pd} = 4.3 ns Max at 3.3 V**
- **Suitable for Point-to-Point Applications**
- **Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human-Body Model (A114-B, Class II)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**
- **ESD Protection Exceeds ±5000 V With Human-Body Model**

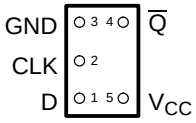
DBV PACKAGE
(TOP VIEW)



DCK PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



See mechanical drawings for dimensions.

DESCRIPTION/ORDERING INFORMATION

The AUP family is TI's premier solution to the industry's low-power needs in battery-powered portable applications. This family ensures a very low static- and dynamic-power consumption across the entire V_{CC} range of 0.8 V to 3.6 V, resulting in increased battery life (see Figure 1). This product also maintains excellent signal integrity (see Figure 2).

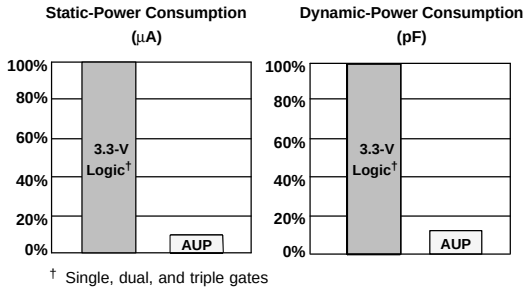


Figure 1. AUP – The Lowest-Power Family

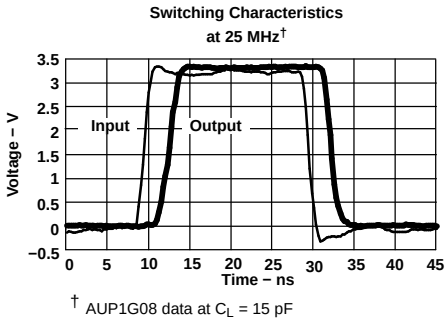


Figure 2. Excellent Signal Integrity

DESCRIPTION/ORDERING INFORMATION (CONTINUED)

This is a single positive-edge-triggered D-type flip-flop. When data at the data (D) input meets the setup time requirement, the data is transferred to the Q output on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

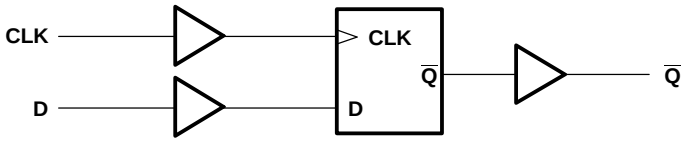
T_A	PACKAGE(1)		ORDERABLE PART NUMBER	TOP-SIDE MARKING(2)
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74AUP1G80YEPR	_ _ _HX_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74AUP1G80YZPR	
	SOT (SOT-23) – DBV	Reel of 3000	SN74AUP1G80DBVR	H80_
		Reel of 250	SN74AUP1G80DBVT	
	SOT (SC-70) – DCK	Reel of 3000	SN74AUP1G80DCKR	HX_
		Reel of 250	SN74AUP1G80DCKT	

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.
(2) DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.
YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, · = Pb-free).

FUNCTION TABLE

INPUTS		OUTPUT
CLK	D	$\overline{Q}$
↑	H	L
↑	L	H
L or H	X	$\overline{Q}_0$

LOGIC DIAGRAM (POSITIVE LOGIC)



Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	4.6	V
V_I	Input voltage range(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high-impedance or power-off state(2)		–0.5	4.6	V
V_O	Voltage range applied to any output in the high or low state(2)		–0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0		–50	mA
I_{OK}	Output clamp current	V_O < 0		–50	mA
I_O	Continuous output current			±20	mA
	Continuous current through V_{CC} or GND			±50	mA
θ_{JA}	Package thermal impedance(3)	DBV package		206	°C/W
		DCK package		252	
		YEP/YZP package		132	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		0.8	3.6	V
V_{IH}	High-level input voltage	V_{CC} = 0.8 V	V_{CC}		V
		V_{CC} = 1.1 V to 1.95 V	0.65 × V_{CC}		
		V_{CC} = 2.3 V to 2.7 V	1.6		
		V_{CC} = 3 V to 3.6 V	2		
V_{IL}	Low-level input voltage	V_{CC} = 0.8 V		0	V
		V_{CC} = 1.1 V to 1.95 V		0.35 × V_{CC}	
		V_{CC} = 2.3 V to 2.7 V		0.7	
		V_{CC} = 3 V to 3.6 V		0.9	
V_I	Input voltage		0	3.6	V
V_O	Output voltage		0	V_{CC}	V
I_{OH}	High-level output current(2)	V_{CC} = 0.8 V		–20	µA
		V_{CC} = 1.1 V		–1.1	mA
		V_{CC} = 1.4 V		–1.7	
		V_{CC} = 1.65		–1.9	
		V_{CC} = 2.3 V		–3.1	
		V_{CC} = 3 V		–4	
I_{OL}	Low-level output current(2)	V_{CC} = 0.8 V		20	µA
		V_{CC} = 1.1 V		1.1	mA
		V_{CC} = 1.4 V		1.7	
		V_{CC} = 1.65 V		1.9	
		V_{CC} = 2.3 V		3.1	
		V_{CC} = 3 V		4	
$\Delta t/\Delta v$	Input transition rise or fall rate	V_{CC} = 0.8 V to 3.6 V		200	ns/V
T_A	Operating free-air temperature		–40	85	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.
(2) Defined by the signal integrity requirements and design-goal priorities.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
V_{OH}		I_{OH} = –20 μA	0.8 V to 3.6 V	V_{CC} – 0.1			V_{CC} – 0.1		V
		I_{OH} = –1.1 mA	1.1 V	0.75 × V_{CC}			0.7 × V_{CC}		
		I_{OH} = –1.7 mA	1.4 V	1.11			1.03		
		I_{OH} = –1.9 mA	1.65 V	1.32			1.3		
		I_{OH} = –2.3 mA	2.3 V	2.05			1.97		
		I_{OH} = –3.1 mA		1.9			1.85		
		I_{OH} = –2.7 mA	3 V	2.72			2.67		
		I_{OH} = –4 mA		2.6			2.55		
V_{OL}		I_{OL} = 20 μA	0.8 V to 3.6 V			0.1		0.1	V
		I_{OL} = 1.1 mA	1.1 V			0.3 × V_{CC}		0.3 × V_{CC}	
		I_{OL} = 1.7 mA	1.4 V			0.31		0.37	
		I_{OL} = 1.9 mA	1.65 V			0.31		0.35	
		I_{OL} = 2.3 mA	2.3 V			0.31		0.33	
		I_{OL} = 3.1 mA				0.44		0.45	
		I_{OL} = 2.7 mA	3 V			0.31		0.33	
		I_{OL} = 4 mA				0.44		0.45	
I_I	D or CLK input	V_I = GND to 3.6 V	0 V to 3.6 V			0.1		0.5	μA
I_{off}		V_I or V_O = 0 V to 3.6 V	0 V			0.2		0.6	μA
ΔI_{off}		V_I or V_O = 0 V to 3.6 V	0 V to 0.2 V			0.2		0.6	μA
I_{CC}		V_I = GND or V_{CC} to 3.6 V, I_O = 0	0.8 V to 3.6 V			0.5		0.9	μA
ΔI_{CC}		V_I = V_{CC} – 0.6 V,(1) I_O = 0	3.3 V			40		50	μA
C_i		V_I = V_{CC} or GND	0 V		1.5				pF
			3.6 V		1.5				
C_o		V_O = GND	0 V		3				pF

(1) One input at V_{CC} – 0.6 V, other input at V_{CC} or GND

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

			V_{CC}	T_A = 25°C	T_A = –40°C to 85°C		UNIT
				TYP	MIN	MAX	
f_{clock}	Clock frequency		0.8 V			20	MHz
			1.2 V ± 0.1 V			80	
			1.5 V ± 0.1 V			120	
			1.8 V ± 0.15 V			160	
			2.5 V ± 0.2 V			220	
			3.3 V ± 0.3 V			260	
t_w	Pulse duration, CLK high or low		0.8 V		5.5		
			1.2 V ± 0.1 V		2.5		
			1.5 V ± 0.1 V		1.5		
			1.8 V ± 0.15 V		1.6		
			2.5 V ± 0.2 V		1.7		
			3.3 V ± 0.3 V		1.9		
t_{su}	Setup time before CLK↑	Data high	0.8 V	3.4	6.7		ns
			1.2 V ± 0.1 V		2.4		
			1.5 V ± 0.1 V		1.2		
			1.8 V ± 0.15 V		0.8		
			2.5 V ± 0.2 V		0.6		
			3.3 V ± 0.3 V		0.4		
		Data low	0.8 V	3.4	8.9		ns
			1.2 V ± 0.1 V		2		
			1.5 V ± 0.1 V		1.3		
			1.8 V ± 0.15 V		1.1		
			2.5 V ± 0.2 V		0.8		
			3.3 V ± 0.3 V		0.7		
t_h	Hold time, data after CLK↑		0.8 V	0	1		ns
			1.2 V ± 0.1 V		0		
			1.5 V ± 0.1 V		0		
			1.8 V ± 0.15 V		0		
			2.5 V ± 0.2 V		0		
			3.3 V ± 0.3 V		0		

Switching Characteristics

over recommended operating free-air temperature range, C_L = 5 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		91		90		MHz
			1.2 V ± 0.1 V		175		220		
			1.5 V ± 0.1 V		237		230		
			1.8 V ± 0.15 V		269		240		
			2.5 V ± 0.2 V		280		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		17.2				ns
			1.2 V ± 0.1 V	3.2	7.1	14.9	2.7	16.3	
			1.5 V ± 0.1 V	1.9	5	9.8	2.1	10.3	
			1.8 V ± 0.15 V	1.7	3.9	7.6	1.6	8.1	
			2.5 V ± 0.2 V	1.4	2.8	5.3	1.2	5.6	
			3.3 V ± 0.3 V	1.2	2.2	4.1	1	4.4	

Switching Characteristics

over recommended operating free-air temperature range, C_L = 10 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		68		70		MHz
			1.2 V ± 0.1 V		128		170		
			1.5 V ± 0.1 V		189		220		
			1.8 V ± 0.15 V		234		240		
			2.5 V ± 0.2 V		273		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		19.4				ns
			1.2 V ± 0.1 V	4.4	8.2	16.2	3.4	17.7	
			1.5 V ± 0.1 V	3.6	5.8	10.7	2.6	11.3	
			1.8 V ± 0.15 V	2.9	4.6	8.4	2.1	3	
			2.5 V ± 0.2 V	2.2	3.3	5.9	1.7	6.3	
			3.3 V ± 0.3 V	1.9	2.7	4.7	1.4	4.9	

Switching Characteristics

over recommended operating free-air temperature range, C_L = 15 pF (unless otherwise noted) (see Figure 3 and Figure 4)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		52		50		MHz
			1.2 V ± 0.1 V		98		130		
			1.5 V ± 0.1 V		148		180		
			1.8 V ± 0.15 V		196		240		
			2.5 V ± 0.2 V		249		250		
			3.3 V ± 0.3 V		280		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		21.5				ns
			1.2 V ± 0.1 V	3	9.1	17.4	4.1	19	
			1.5 V ± 0.1 V	3.2	6.5	11.7	3.2	12.3	
			1.8 V ± 0.15 V	2.7	4.2	9.2	2.6	9.8	
			2.5 V ± 0.2 V	2.2	3.8	6.5	2.1	6.9	
			3.3 V ± 0.3 V	1.9	3.1	5.1	1.8	5.5	

Switching Characteristics

over recommended operating free-air temperature range, C_L = 30 pF (unless otherwise noted) (see Figure 3 and Figure 4)

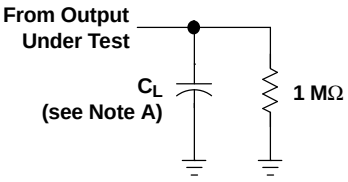
PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC}	T_A = 25°C			T_A = –40°C to 85°C		UNIT
				MIN	TYP	MAX	MIN	MAX	
f_{max}			0.8 V		32		20		MHz
			1.2 V ± 0.1 V		71		80		
			1.5 V ± 0.1 V		104		120		
			1.8 V ± 0.15 V		133		160		
			2.5 V ± 0.2 V		181		220		
			3.3 V ± 0.3 V		257		260		
t_{pd}	CLK	$\overline{Q}$	0.8 V		28.4				ns
			1.2 V ± 0.1 V	5.1	11.8	20.7	6.2	28.7	
			1.5 V ± 0.1 V	4.8	8.5	14.1	6.9	16.7	
			1.8 V ± 0.15 V	4	6.9	11.2	2	13.3	
			2.5 V ± 0.2 V	3.3	5.1	7.9	3.2	9.3	
			3.3 V ± 0.3 V	2.9	4.2	6.4	2.8	7.5	

Operating Characteristics

T_A = 25°C

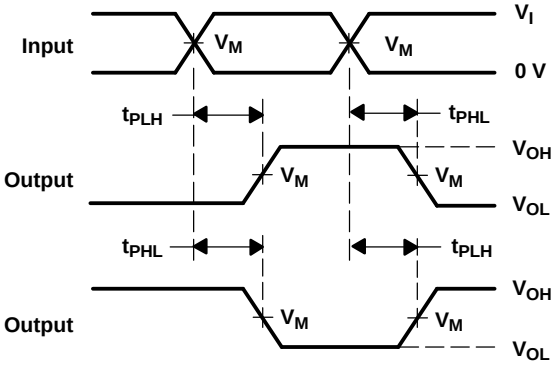
PARAMETER		TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	Power dissipation capacitance	f = 10 MHz	0.8 V	2.5	pF
			1.2 V ± 0.1 V	2.5	
			1.5 V ± 0.1 V	2.5	
			1.8 V ± 0.15 V	2.5	
			2.5 V ± 0.2 V	3	
			3.3 V ± 0.3 V	3	

PARAMETER MEASUREMENT INFORMATION
(Propagation Delays, Setup and Hold Times, and Pulse Duration)



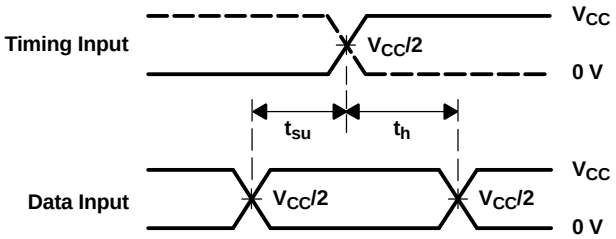
LOAD CIRCUIT

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

VOLTAGE WAVEFORMS
PULSE DURATION

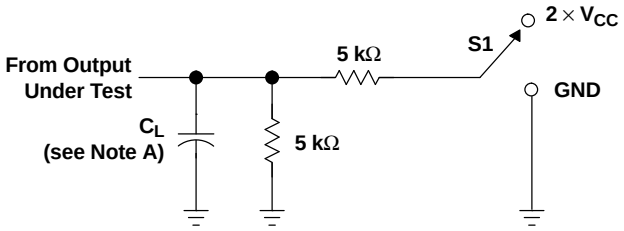


VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
C. The outputs are measured one at a time, with one transition per measurement.
D. t_{PLH} and t_{PHL} are the same as t_{pd}.
E. All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

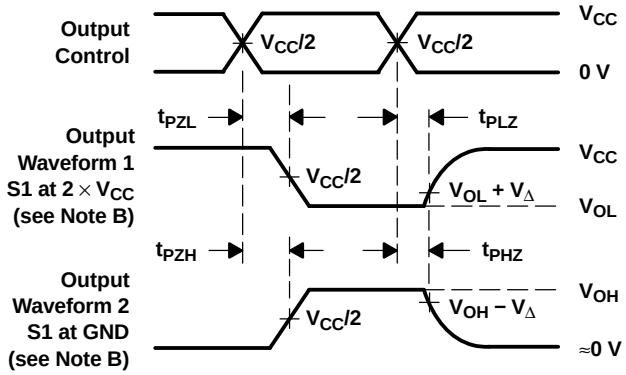
PARAMETER MEASUREMENT INFORMATION
(Enable and Disable Times)



LOAD CIRCUIT

TEST	S1
t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	$2 \times V_{CC}$ GND

	V_{CC} = 0.8 V	V_{CC} = 1.2 V ± 0.1 V	V_{CC} = 1.5 V ± 0.1 V	V_{CC} = 1.8 V ± 0.15 V	V_{CC} = 2.5 V ± 0.2 V	V_{CC} = 3.3 V ± 0.3 V
C_L	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF	5, 10, 15, 30 pF
V_M	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$	$V_{CC}/2$
V_I	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}	V_{CC}
V_Δ	0.1 V	0.1 V	0.1 V	0.15 V	0.15 V	0.3 V



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f = 3 ns.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. All parameters and waveforms are not applicable to all devices.

Figure 4. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

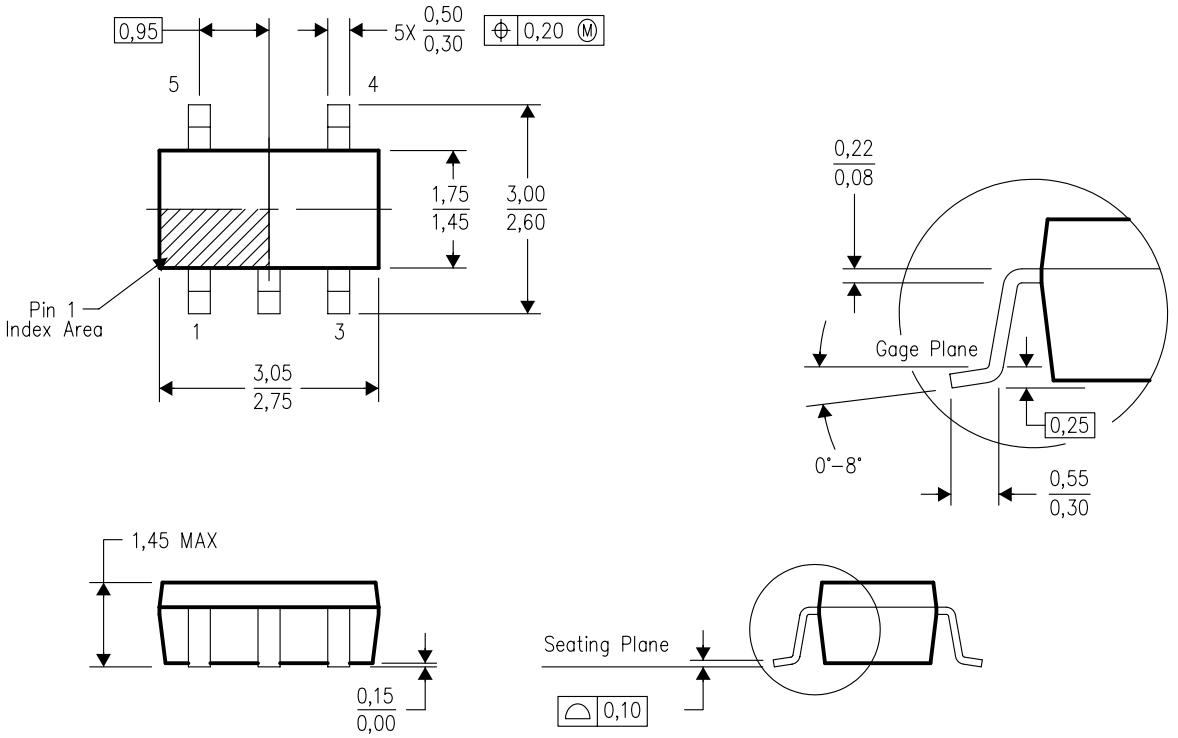
Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74AUP1G80DBVR	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G80DBVRE4	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G80DBVT	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G80DBVTE4	ACTIVE	SOT-23	DBV	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G80DCKR	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G80DCKRE4	ACTIVE	SC70	DCK	5	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G80DCKT	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G80DCKTE4	ACTIVE	SC70	DCK	5	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AUP1G80YZPR	ACTIVE	WCSP	YZP	5	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

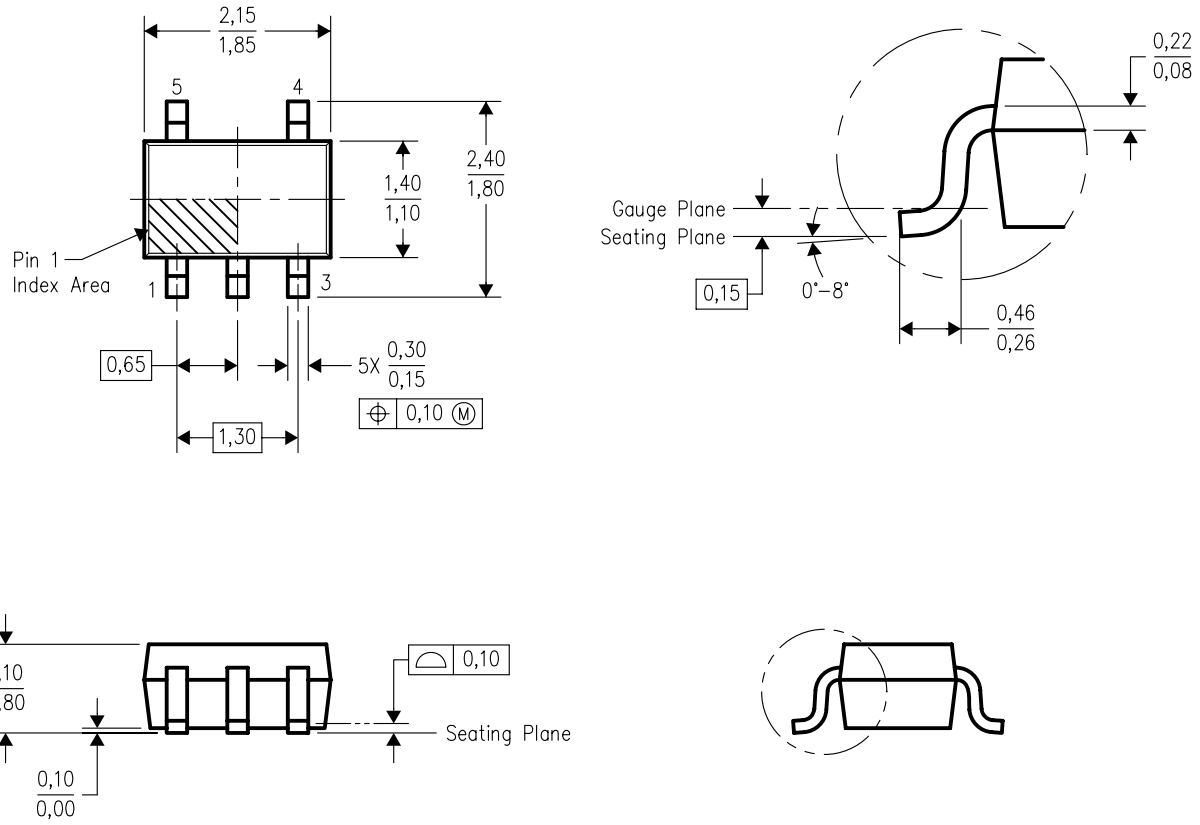
DBV (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4073253–4/K 03/2006

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–178 Variation AA.

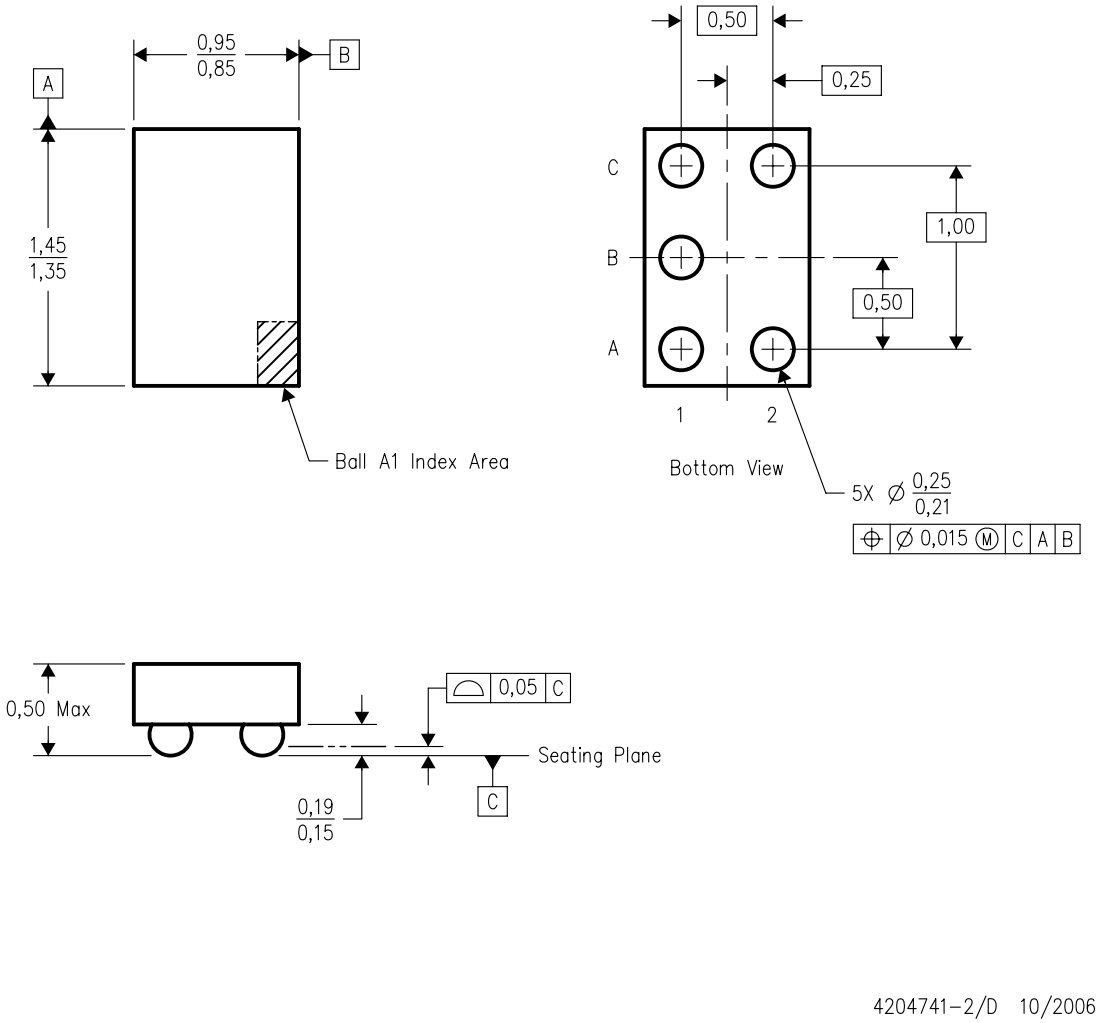
DCK (R–PDSO–G5) PLASTIC SMALL–OUTLINE PACKAGE



4093553–3/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AA.

YZP (R–XBGA–N5) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. This package is lead–free. Refer to the 5 YEP package (drawing 4204725) for tin–lead (SnPb).

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