SN55LVDS32, SN65LVDS32, SN65LVDS3486, SN65LVDS9637
HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

- **Meets or Exceeds the Requirements of ANSI TIA/EIA-644 Standard**
- **Operates with a Single 3.3-V Supply**
- **Designed for Signaling Rate of Up To 400 Mbps**
- **Differential Input Thresholds ±100 mV Max**
- **Typical Propagation Delay Time of 2.1 ns**
- **Power Dissipation 60 mW Typical per Receiver at 200 MHz**
- **Bus-Terminal ESD Protection Exceeds 8 kV**
- **Low-Voltage TTL (LVTTL) Logic Output Levels**
- **Pin-Compatible with the AM26LS32, MC3486, and μA9637**
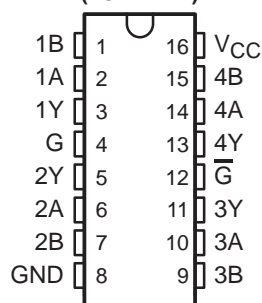- **Open-Circuit Fail Safe**

description

The SN55LVDS32, SN65LVDS32, SN65LVDS3486, and SN65LVDS9637 are differential line receivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). This signaling technique lowers the output voltage levels of 5-V differential standard levels (such as EIA/TIA-422B) to reduce the power, increase the switching speeds, and allow operation with a 3.3-V supply rail. Any of the four differential receivers provides a valid logical output state with a ±100 mV differential input voltage within the input common-mode voltage range. The input common-mode voltage range allows 1 V of ground potential difference between two LVDS nodes.
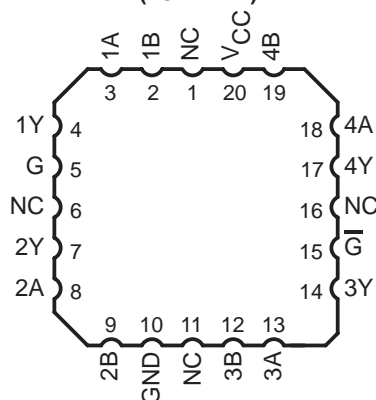
The intended application of these devices and signaling technique is both point-to-point and multidrop (one driver and multiple receivers) data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media and the noise coupling to the environment.

The SN65LVDS32, SN65LVDS3486, and SN65LVDS9637 are characterized for operation from $-40°$C to $85°$C. The SN55LVDS32 is characterized for operation from $-55°$C to $125°$C.
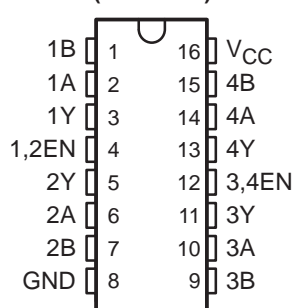
SN55LVDS32 . . . J OR W
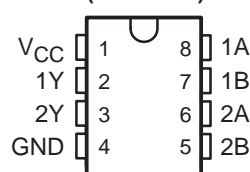**SN65LVDS32D**
(Marked as **LVDS32** or **65LVDS32**)
(TOP VIEW)

1B	1	16	V_{CC}
1A	2	15	4B
1Y	3	14	4A
G	4	13	4Y
2Y	5	12	$\overline{G}$
2A	6	11	3Y
2B	7	10	3A
GND	8	9	3B

SN55LVDS32FK
(TOP VIEW)

SN65LVDS3486D (Marked as **LVDS3486**)
(TOP VIEW)

1B	1	16	V_{CC}
1A	2	15	4B
1Y	3	14	4A
1,2EN	4	13	4Y
2Y	5	12	3,4EN
2A	6	11	3Y
2B	7	10	3A
GND	8	9	3B

SN65LVDS9637D (Marked as **DK637** or **LVDS37**)
SN65LVDS9637DGN (Marked as **L37**)
(TOP VIEW)

V_{CC}	1	8	1A
1Y	2	7	1B
2Y	3	6	2A
GND	4	5	2B

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SN55LVDS32, SN65LVDS32, SN65LVDS3486, SN65LVDS9637
HIGH-SPEED DIFFERENTIAL LINE RECEIVERS

AVAILABLE OPTIONS

T$_A$	PACKAGE				
	SMALL OUTLINE (D)	MSOP (DGN)	CHIP CARRIER (FK)	CERAMIC DIP (J)	FLAT PACK (W)
−40°C to 85°C	SN65LVDS32D	—	—	—	—
	SN65LVDS3486D	—	—	—	—
	SN65LVDS9637D	SN65LVDS9637DGN	—	—	—
−55°C to 125°C	—	—	SN55LVDS32FK	SN55LVDS32J	SN55LVDS32W
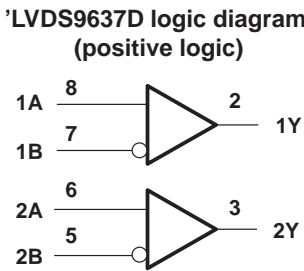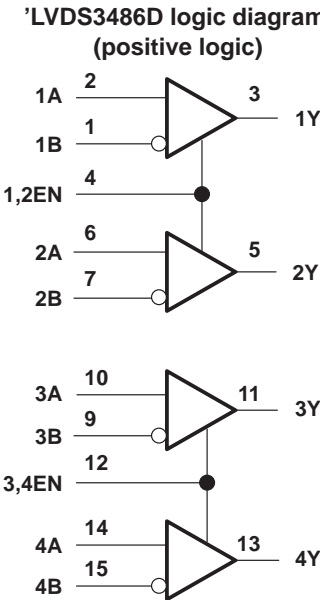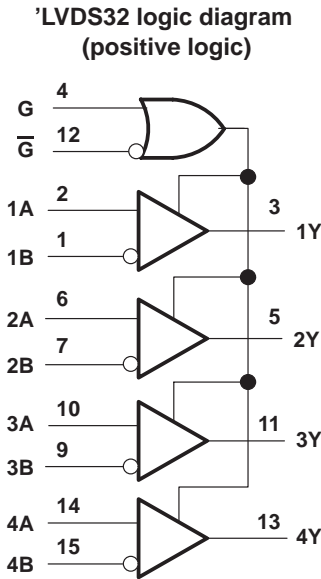
'LVDS32 logic diagram (positive logic)

'LVDS3486D logic diagram (positive logic)

'LVDS9637D logic diagram (positive logic)

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Function Tables

SN55LVDS32, SN65LVDS32

DIFFERENTIAL INPUT	ENABLES		OUTPUT
A, B	G	$\overline{G}$	Y
$V_{ID} \geq 100$ mV	H X	X L	H H
-100 mV $< V_{ID} < 100$ mV	H X	X L	? ?
$V_{ID} \leq -100$ mV	H X	X L	L L
X	L	H	Z
Open	H X	X L	H H

SN65LVDS3486

DIFFERENTIAL INPUT	ENABLE	OUTPUT
A, B	EN	Y
$V_{ID} \geq 100$ mV	H X	H H
-100 mV $< V_{ID} < 100$ mV	H X	? ?
$V_{ID} \leq -100$ mV	H X	L L
X	L	Z
Open	H X	H H

H = high level, L = low level, X = irrelevant, Z = high impedance (off), ? = indeterminate

logic symbol†

SN55LVDS32, SN65LVDS32
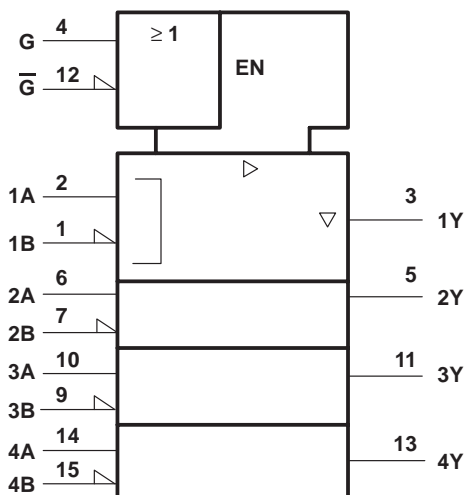
SN65LVDS3486

† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Function Table

SN65LVDS9637

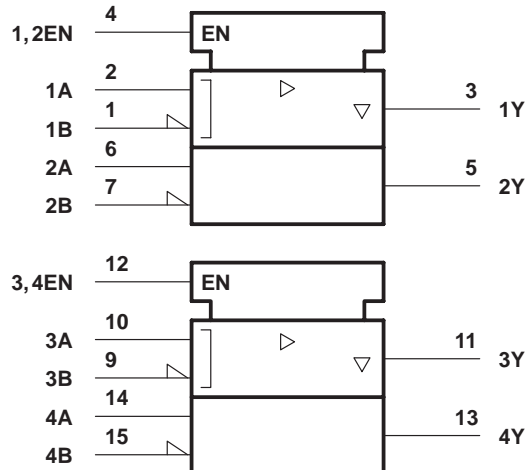| DIFFERENTIAL INPUT	OUTPUT
A, B	Y
$V_{ID} \geq 100$ mV	H
-100 mV $< V_{ID} < 100$ mV	?
$V_{ID} \leq -100$ mV	L
Open	H

H = high level, L = low level, ? = indeterminate

logic symbol†

SN65LVDS9637
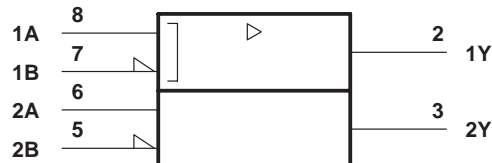
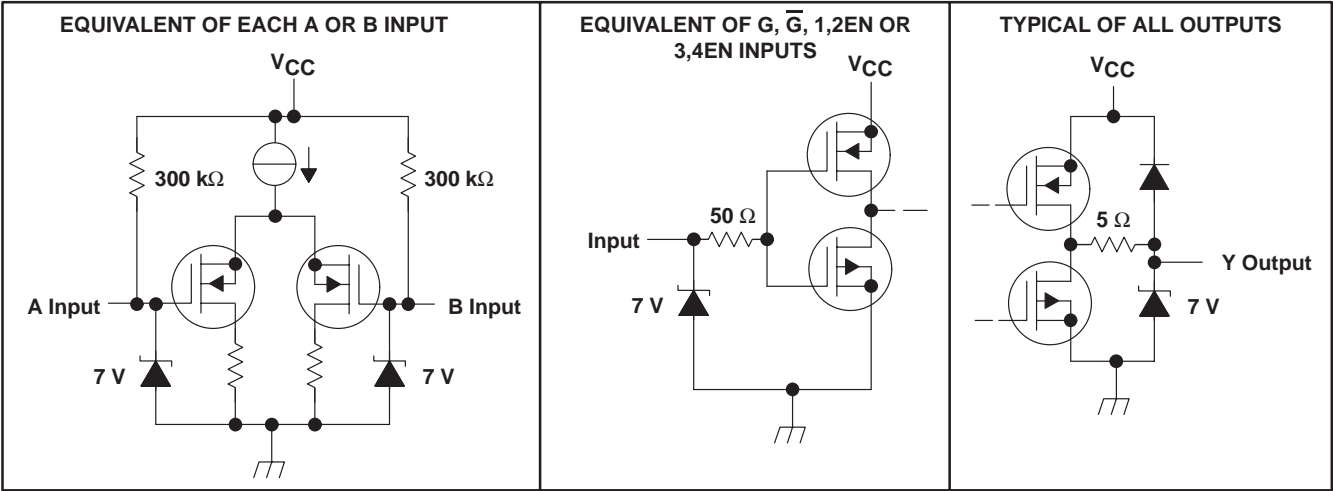† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

equivalent input and output schematic diagrams

EQUIVALENT OF EACH A OR B INPUT	EQUIVALENT OF G, $\overline{G}$, 1,2EN OR 3,4EN INPUTS	TYPICAL OF ALL OUTPUTS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	−0.5 V to 4 V
Input voltage range, V_I	−0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (A or B)	−0.5 V to 4 V
Continuous total power dissipation	See Dissipation Rating Table
Storage temperature range, T_{stg}	−65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds	260°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1:   All voltages, except differential I/O bus voltages, are with respect to the network ground terminal.

DISSIPATION RATING TABLE

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR‡ ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D (8)	725 mW	5.8 mW/°C	464 mW	377 mW	—
D (16)	950 mW	7.6 mW/°C	608 mW	494 mW	—
DGN	2.14 W	17.1 mW/°C	1.37 W	1.11 W	—
FK	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
J	1375 mW	11.0 mW/°C	880 mW	715 mW	275 mW
W	1000 mW	8.0 mW/°C	640 mW	520 mW	200 mW

‡ This is the inverse of the junction-to-ambient thermal resistance when board mounted and with no air flow.

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recommended operating conditions

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
High-level input voltage, V_{IH}	G, $\overline{G}$, 1,2EN, or 3,4EN	2			V
Low-level input voltage, V_{IL}	G, $\overline{G}$, 1,2EN, or 3,4EN			0.8	V
Magnitude of differential input voltage, $|V_{ID}|$		0.1		0.6	V
Common-mode input voltage, V_{IC} (see Figure 1)		$\dfrac{|V_{ID}|}{2}$		$2.4 - \dfrac{|V_{ID}|}{2}$	V
				$V_{CC} - 0.8$	V
Operating free-air temperature, T_A	SN65 prefix	−40		85	°C
	SN55 prefix	−55		125	
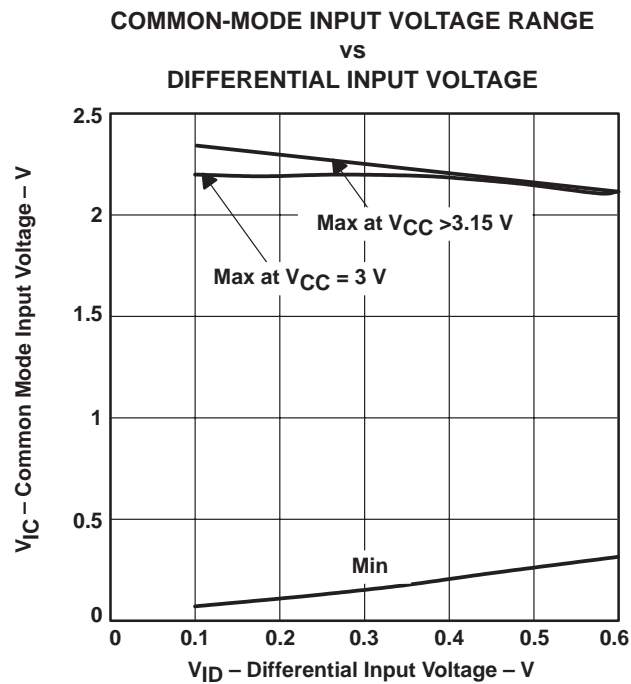
COMMON-MODE INPUT VOLTAGE RANGE
vs
DIFFERENTIAL INPUT VOLTAGE

Figure 1. V_{IC} Versus V_{ID} and V_{CC}

SN65LVDSxxxx electrical characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		SN65LVDS32, SN65LVDS3486, SN65LVDS9637			UNIT
				MIN	TYP[†]	MAX	
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 2 and Table 1				100	mV
V_{ITH-}	Negative-going differential input voltage threshold[‡]			−100			mV
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA		2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA				0.4	V
I_{CC}	Supply current	SN65LVDS32, SN65LVDS3486	Enabled, No load		10	18	mA
			Disabled		0.25	0.5	
		SN65LVDS9637	No load		5.5	10	
I_I	Input current (A or B inputs)	$V_I = 0$		−2	−10	−20	μA
		$V_I = 2.4$ V		−1.2	−3		
$I_{I(OFF)}$	Power-off input current (A or B inputs)	$V_{CC} = 0$, $V_I = 3.6$ V			6	20	μA
I_{IH}	High-level input current (EN, G, or $\overline{G}$ inputs)	$V_{IH} = 2$ V				10	μA
I_{IL}	Low-level input current (EN, G, or $\overline{G}$ inputs)	$V_{IL} = 0.8$ V				10	μA
I_{OZ}	High-impedance output current	$V_O = 0$ or V_{CC}				±10	μA

[†] All typical values are at $T_A = 25°C$ and with $V_{CC} = 3.3$ V.

[‡] The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.

SN65LVDSxxxx switching characteristics over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SN65LVDS32, SN65LVDS3486, SN65LVDS9637			UNIT
			MIN	TYP	MAX	
t_{pLH}	Propagation delay time, low-to-high-level output	$C_L = 10$ pF, See Figure 3	1.5	2.1	3	ns
t_{pHL}	Propagation delay time, high-to-low-level output		1.5	2.1	3	ns
$t_{sk(p)}$	Pulse skew ($|t_{PHL} - t_{PLH}|$)			0	0.4	ns
$t_{sk(o)}$	Channel-to-channel output skew[†]			0.1	0.3	ns
$t_{sk(pp)}$	Part-to-part skew[‡]				1	ns
t_r	Output signal rise time, 20% to 80%			0.6		ns
t_f	Output signal fall time, 80% to 20%			0.7		ns
t_{pHZ}	Propagation delay time, high-level-to-high-impedance output	See Figure 4		6.5	12	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output			5.5	12	ns
t_{pZH}	Propagation delay time, high-impedance-to-high-level output			8	12	ns
t_{pZL}	Propagation delay time, high-impedance-to-low-level output			3	12	ns

[†] $t_{sk(o)}$ is the skew between specified outputs of a single device with all driving inputs connected together and the outputs switching in the same direction while driving identical specified loads.

[‡] $t_{sk(pp)}$ is the magnitude of the different in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, same temperature, and have identical packages and test circuits.

SN55LVDS32 Selectrical characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	SN55LVDS32 MIN	SN55LVDS32 TYP†	SN55LVDS32 MAX	UNIT
V_{ITH+}	Positive-going differential input voltage threshold	See Figure 2, Table 1, and Note 2			100	mV
V_{ITH-}	Negative-going differential input voltage threshold‡		−100			mV
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA	2.4			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA			0.4	V
I_{CC}	Supply current	Enabled, No load		10	18	mA
		Disabled		0.25	0.5	
I_I	Input current (A or B inputs)	$V_I = 0$	−2	−10	−20	µA
		$V_I = 2.4$ V	−1.2	−3		
$I_{I(OFF)}$	Power-off input current (A or B inputs)	$V_{CC} = 0$, $V_I = 2.4$ V		6	20	µA
I_{IH}	High-level input current (EN, G, or $\overline{G}$ inputs)	$V_{IH} = 2$ V			10	µA
I_{IL}	Low-level input current (EN, G, or $\overline{G}$ inputs)	$V_{IL} = 0.8$ V			10	µA
I_{OZ}	High-impedance output current	$V_O = 0$ or V_{CC}			±12	µA

† All typical values are at $T_A = 25°C$ and with $V_{CC} = 3.3$ V.
‡ The algebraic convention, in which the less positive (more negative) limit is designated minimum, is used in this data sheet for the negative-going differential input voltage threshold only.
NOTE 2: $|V_{ITH}| = 200$ mV for operation at $-55°C$.

SN55LVDS32 switching characteristics over recommended operating conditions (unless otherwise noted)

	PARAMETER	TEST CONDITIONS	SN55LVDS32 MIN	SN55LVDS32 TYP	SN55LVDS32 MAX	UNIT
t_{pLH}	Propagation delay time, low-to-high-level output		1.3	2.3	6	ns
t_{pHL}	Propagation delay time, high-to-low-level output	$C_L = 10$ pF, See Figure 3	1.4	2.2	6.1	ns
$t_{sk(o)}$	Channel-to-channel output skew†			0.1		ns
t_r	Output signal rise time, 20% to 80%	$C_L = 10$ pF, See Figure 3		0.6		ns
t_f	Output signal fall time, 80% to 20%			0.7		ns
t_{pHZ}	Propagation delay time, high-level-to-high-impedance output			6.5	12	ns
t_{pLZ}	Propagation delay time, low-level-to-high-impedance output	See Figure 4		5.5	12	ns
t_{pZH}	Propagation delay time, high-impedance-to-high-level output			8	14	ns
t_{pZL}	Propagation delay time, high-impedance-to-low-level output			3	12	ns

† $t_{sk(o)}$ is the maximum delay time difference between drivers on the same device.

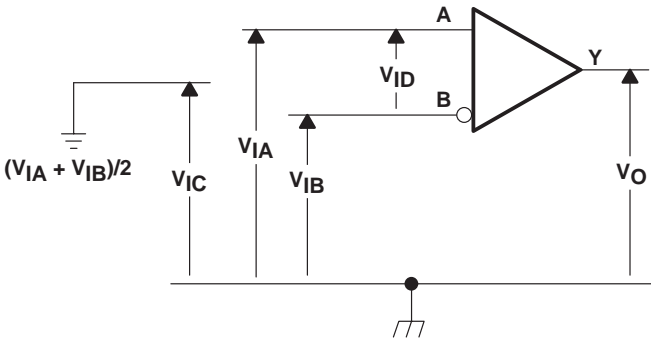## PARAMETER MEASUREMENT INFORMATION

Figure 2. Voltage Definitions

Table 1. Receiver Minimum and Maximum Input Threshold Test Voltages

| APPLIED VOLTAGES		RESULTING DIFFERENTIAL INPUT VOLTAGE	RESULTING COMMON-MODE INPUT VOLTAGE
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25 V	1.15 V	100 mV	1.2 V
1.15 V	1.25 V	−100 mV	1.2 V
2.4 V	2.3 V	100 mV	2.35 V
2.3 V	2.4 V	−100 mV	2.35 V
0.1 V	0 V	100 mV	0.05 V
0 V	0.1 V	−100 mV	0.05 V
1.5 V	0.9 V	600 mV	1.2 V
0.9 V	1.5 V	−600 mV	1.2 V
2.4 V	1.8 V	600 mV	2.1 V
1.8 V	2.4 V	−600 mV	2.1 V
0.6 V	0 V	600 mV	0.3 V
0 V	0.6 V	−600 mV	0.3 V

PARAMETER MEASUREMENT INFORMATION
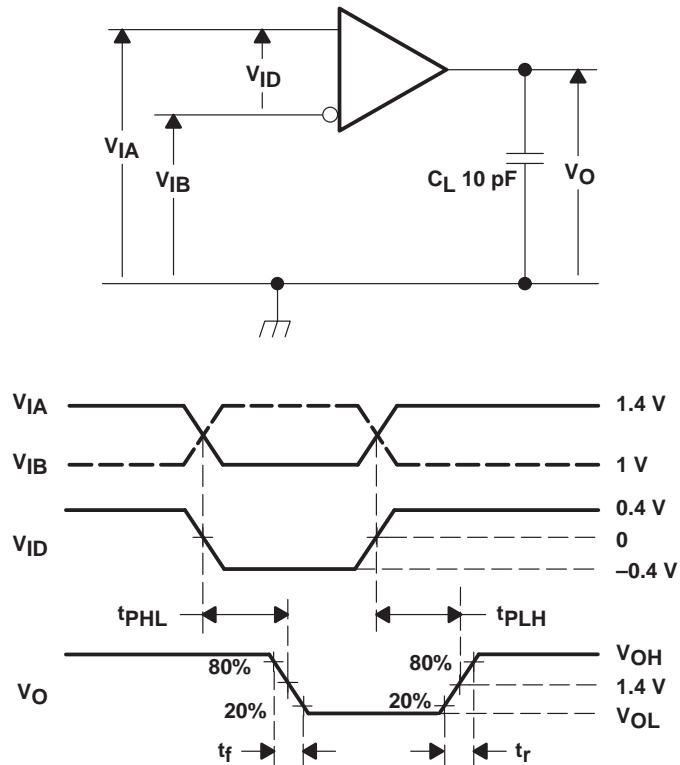
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 50 Mpps, pulse width = 10 ± 0.2 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 3. Timing Test Circuit and Wave Forms

PARAMETER MEASUREMENT INFORMATION
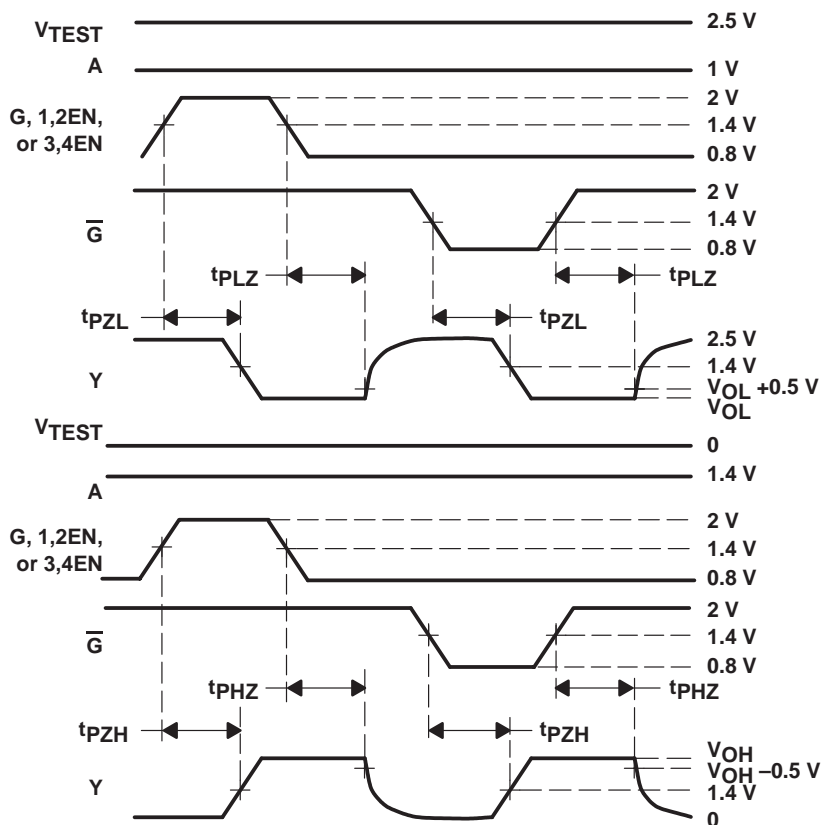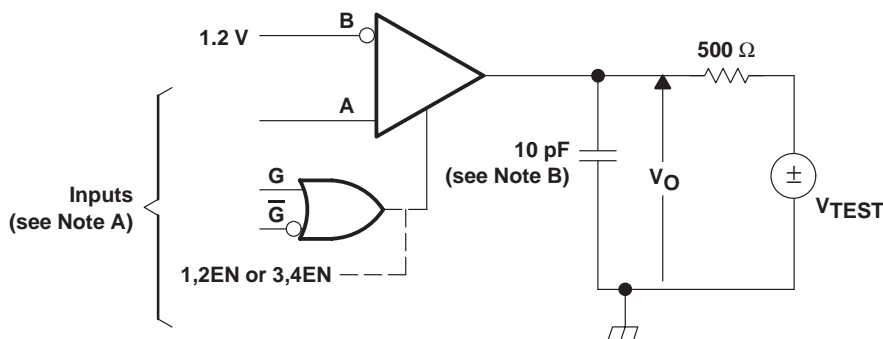
NOTES: A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq 1$ ns, pulse repetition rate (PRR) = 0.5 Mpps, pulse width = 500 $\pm$ 10 ns.
B. C_L includes instrumentation and fixture capacitance within 6 mm of the D.U.T.

Figure 4. Enable/Disable Time Test Circuit and Wave Forms
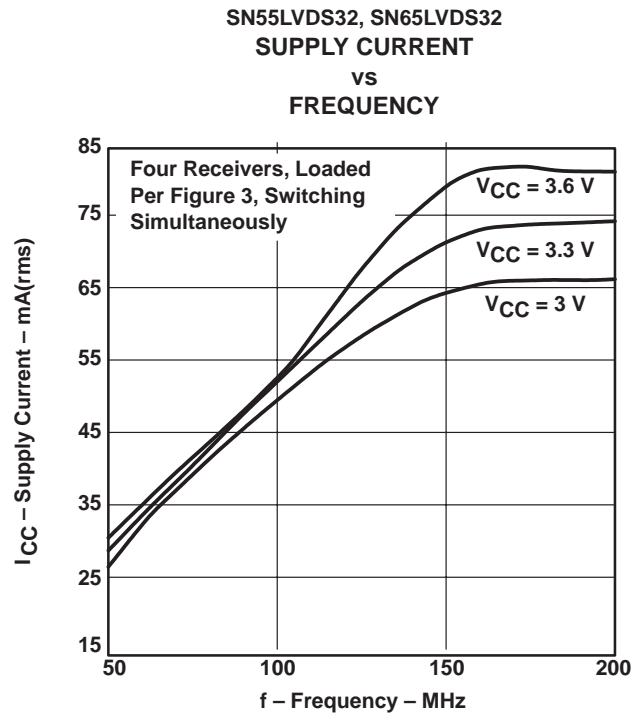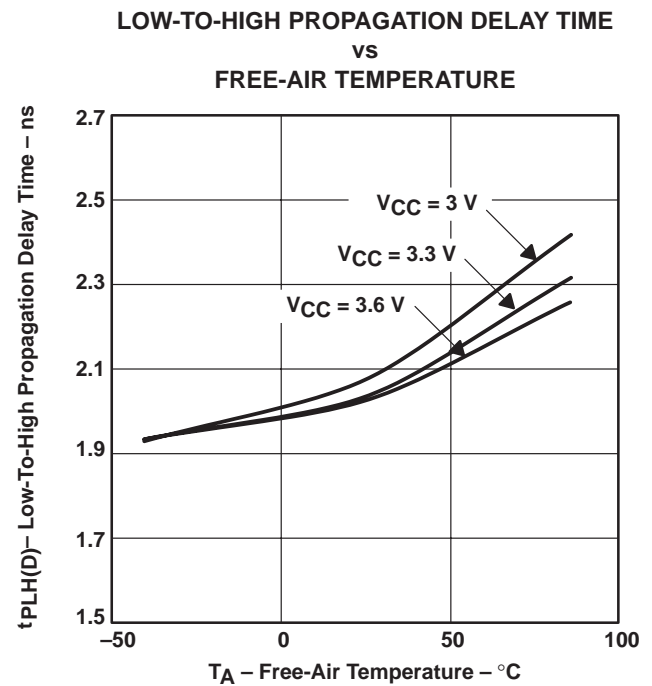
TYPICAL CHARACTERISTICS

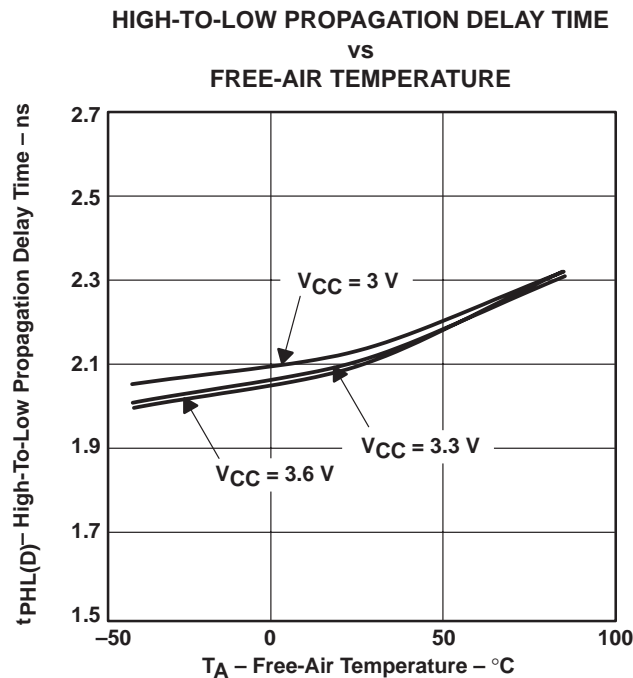**SN55LVDS32, SN65LVDS32
SUPPLY CURRENT
vs
FREQUENCY**

Figure 5

**LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE**

Figure 6

**HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE**


Figure 7

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APPLICATION INFORMATION

using an LVDS receiver with RS-422 data

Receipt of data from a TIA/EIA-422 line driver may be accomplished using a TIA/EIA-644 line receiver with the addition of an attenuator circuit. This technique gives the user a very high-speed and low-power 422 receiver.

If the ground noise between the transmitter and receiver is not a concern (less than ± 1 V), the answer can be as simple as shown below in Figure 8. The use of a resistor divider circuit in front of the LVDS receiver attenuates the 422 differential signal to LVDS levels.

The resistors present a total differential load of 100 Ω to match the characteristic impedance of the transmission line and to reduce the signal 10:1. The maximum 422 differential output signal or 6 V is reduced to 600 mV. The high input impedance of the LVDS receiver prevents input bias offsets and maintains a better than 200-mV differential input voltage threshold at the inputs to the divider. This circuit is used in front of each LVDS channel that also receives 422 signals.
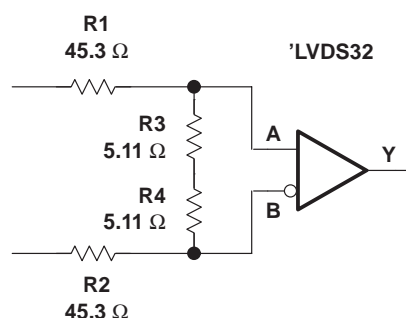
NOTE A: The components used were standard values.
        R1, R2 = NRC12F45R3TR, NIC Components, 45.3 Ohm, 1/8W, 1%, 1206 Package
        R3, R4 = NRC12F5R11TR, NIC Components, 5.11 Ohm, 1/8W, 1%, 1206 Package

        The resistor values do not need to be 1% tolerance. However, it can be difficult locating a supplier of resistors having values less than 100 Ω in stock and readily available. The user may find other suppliers with comparable parts having tolerances of 5% or even 10%. These parts are adequate for use in this circuit.

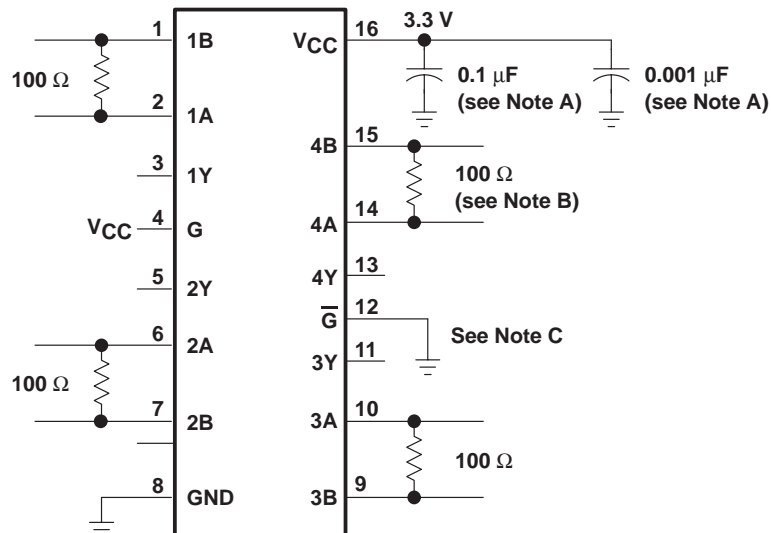**Figure 8. RS-422 Data Input to an LVDS Receiver Under Low Ground Noise Conditions**

If ground noise between the RS-422 driver and LVDS receiver is a concern, then the common-mode voltage must be attenuated. The circuit must then be modified to connect the node between R3 and R4 to the LVDS receiver ground. This modification to the circuit increases the common-mode voltage from ± 1 V to greater than ± 4.5 V.

APPLICATIONS INFORMATION

The devices are generally used as building blocks for high-speed point-to-point data transmission where ground differences are less than 1 V. Devices can interoperate with RS-422, PECL, and IEEE-P1596. Drivers/receivers approach ECL speeds without the power and dual supply requirements.

TRANSMISSION DISTANCE vs SIGNALING RATE

NOTE A: This parameter is the percentage of distortion of the unit interval (UI) with a pseudo-random data pattern.

Figure 9. Typical Transmission Distance Versus Signaling Rate

NOTES: A. Place a 0.1 µF and a 0.001 µF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitors should be located as close as possible to the device terminals.
B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.
C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 10. Typical Application Circuit Schematic

APPLICATION INFORMATION
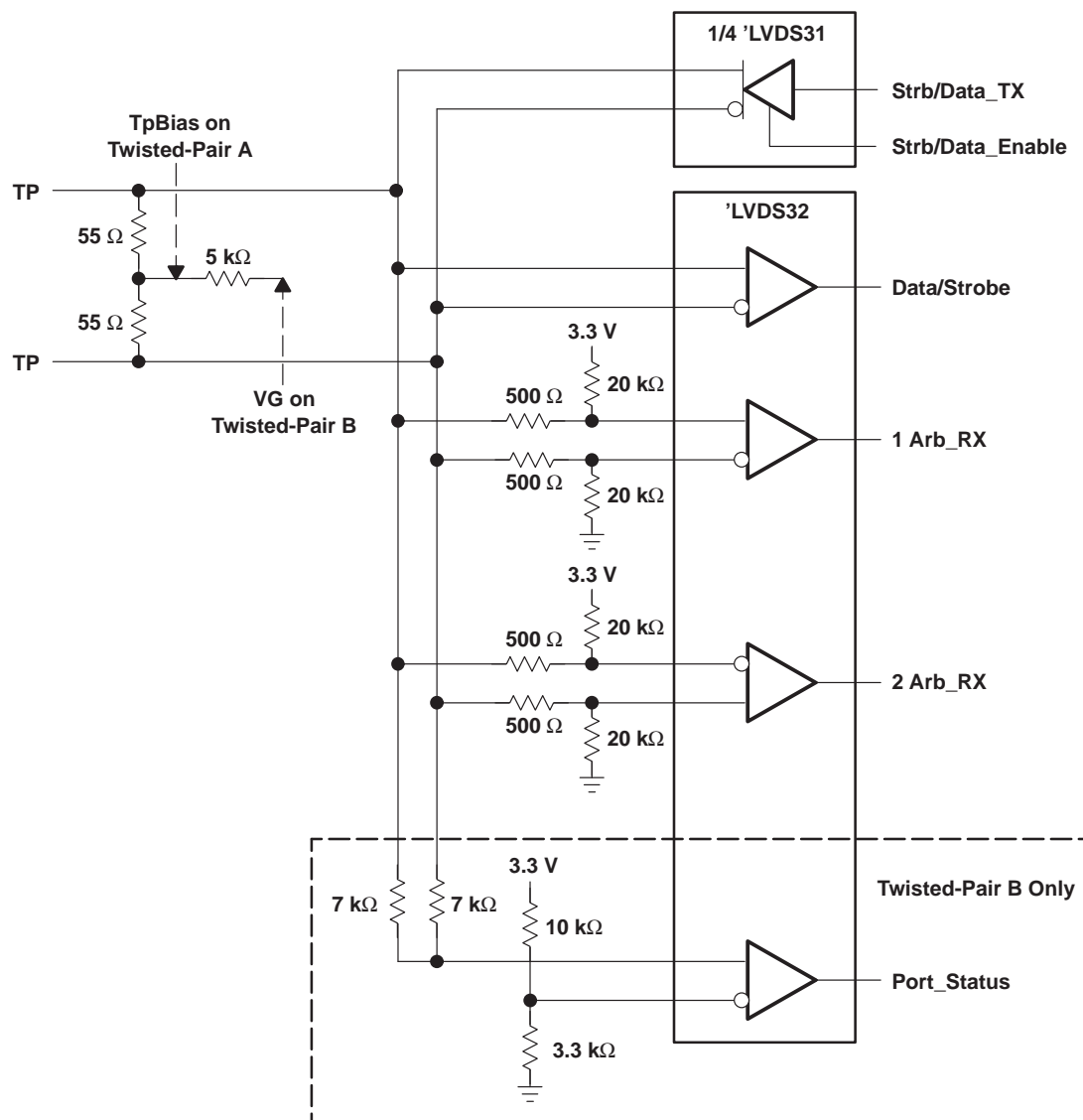
NOTES: A. Resistors are leadless thick-film (0603) 5% tolerance.
B. Decoupling capacitance is not shown but recommended.
C. V_{CC} is 3 V to 3.6 V.
D. The differential output voltage of the 'LVDS31 can exceed that allowed by IEEE1394.

Figure 11. 100-Mbps IEEE 1394 Transceiver

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APPLICATION INFORMATION

fail safe

One of the most common problems with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV if it is within its recommended input common-mode voltage range. TI's LVDS receiver is different in how it handles the open-input circuit situation, however.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver will pull each line of the signal pair to near V_{CC} through 300-kΩ resistors as shown in Figure 11. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high level, regardless of the differential input voltage.
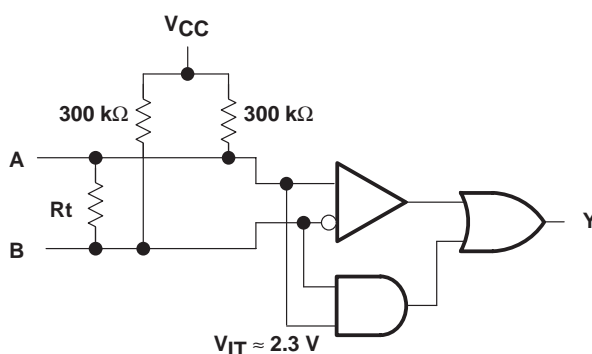

Figure 12. Open-Circuit Fail Safe of the LVDS Receiver

It is only under these conditions that the output of the receiver will be valid with less than a 100-mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in the figure. Other termination circuits may allow a dc current to ground that could defeat the pull-up currents from the receiver and the fail-safe feature.

APPLICATION INFORMATION
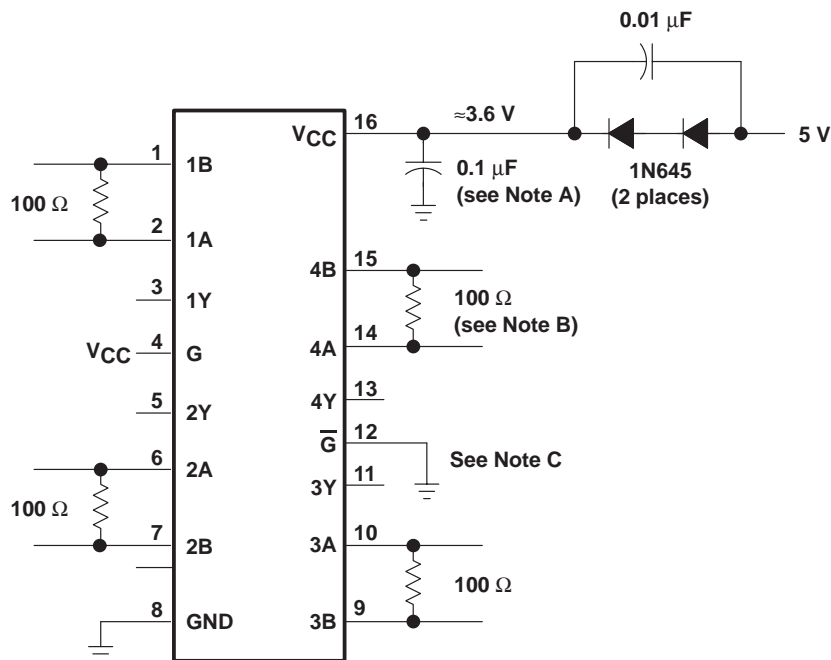
NOTES: A. Place a 0.1 μF Z5U ceramic, mica or polystyrene dielectric, 0805 size, chip capacitor between V_{CC} and the ground plane. The capacitor should be located as close as possible to the device terminals.

B. The termination resistance value should match the nominal characteristic impedance of the transmission media with ±10%.

C. Unused enable inputs should be tied to V_{CC} or GND as appropriate.

Figure 13. Operation with 5-V Supply

related information

IBIS modeling is available for this device. Please contact the local TI sales office or the TI Web site at *www.ti.com* for more information.

For more application guidelines, please see the following documents:

● *Low-Voltage Differential Signalling Design Notes* (TI literature number SLLA014)

● *Interface Circuits for TIA/EIA-644* (LVDS) (SLLA038)

● *Reducing EMI with LVDS* (SLLA030)

● *Slew Rate Control of LVDS Circuits* (SLLA034)

● *Using an LVDS Receiver with RS-422 Data* (SLLA031)

● *Evaluating the LVDS EVM* (SLLA033)

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

MECHANICAL INFORMATION

D (R-PDSO-G**)   **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN
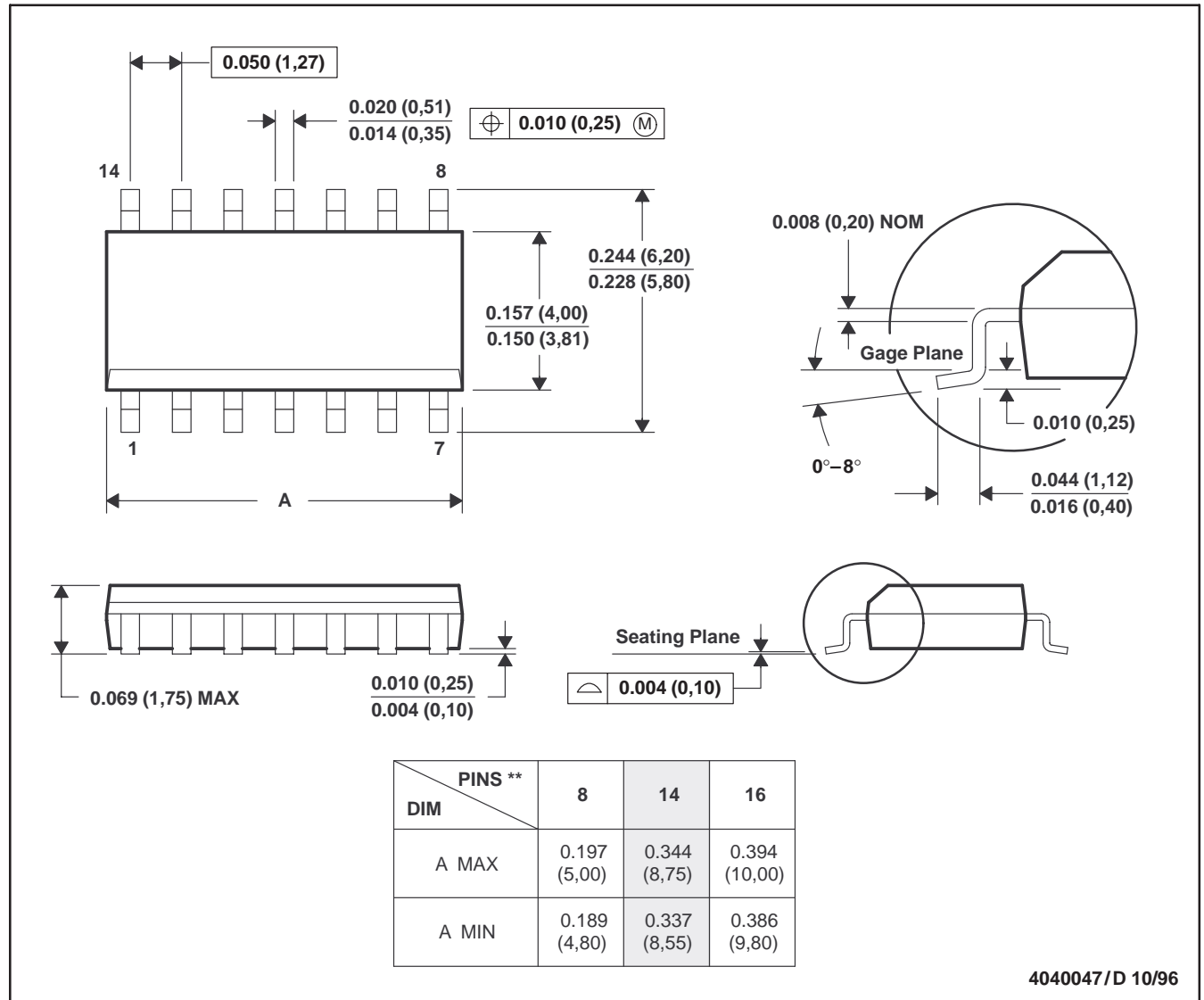
PINS ** DIM	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047 / D 10/96

NOTES: A.   All linear dimensions are in inches (millimeters).
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
         D.   Falls within JEDEC MS-012

TEXAS INSTRUMENTS

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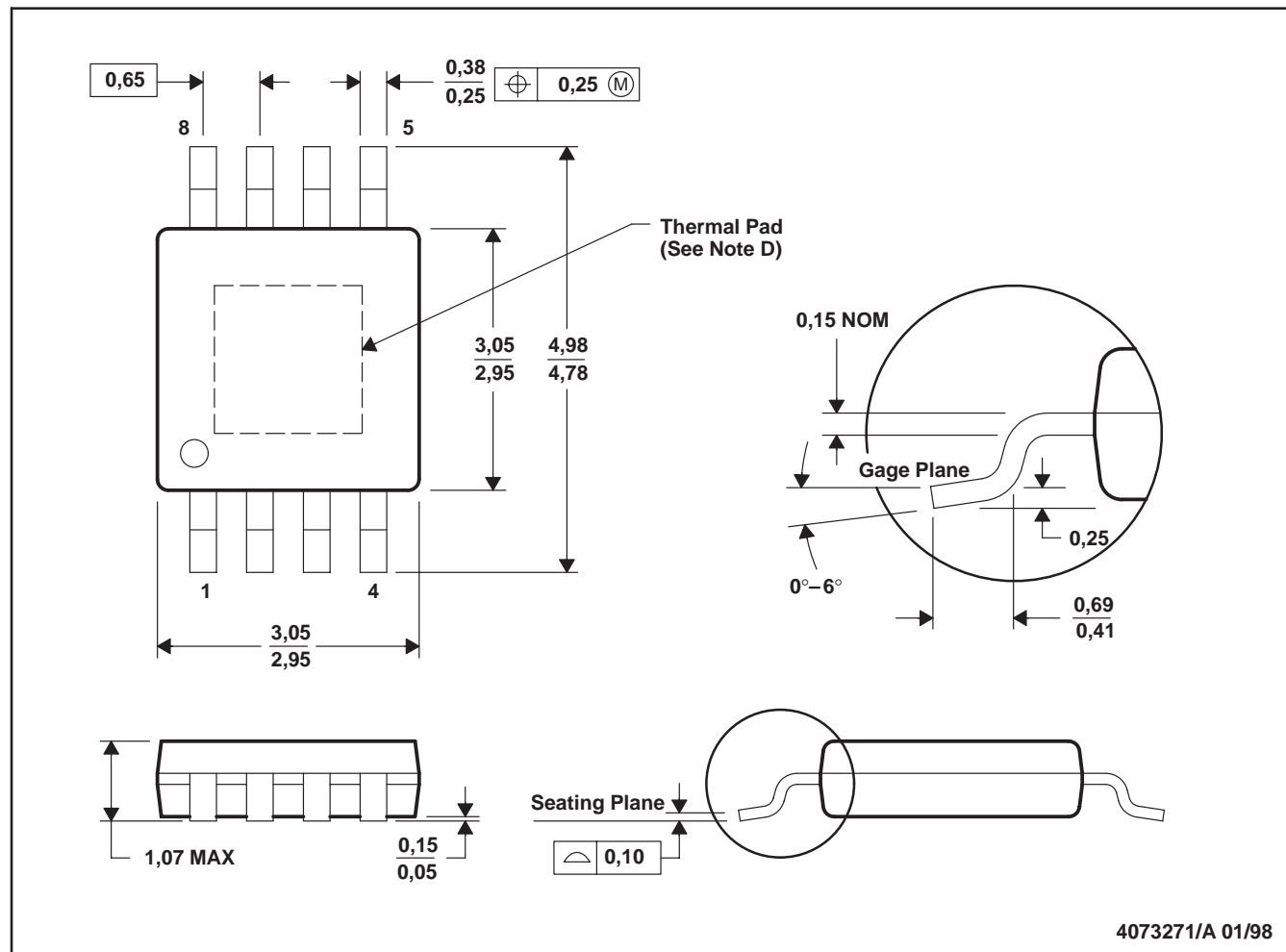
17

MECHANICAL INFORMATION

DGN (S-PDSO-G8)　　　　　　　　　　　　　　　　　　**PowerPAD™ PLASTIC SMALL-OUTLINE PACKAGE**

4073271/A 01/98

NOTES:　A.　All linear dimensions are in millimeters.
　　　　　B.　This drawing is subject to change without notice.
　　　　　C.　Body dimensions include mold flash or protrusions.
　　　　　D.　The package thermal performance may be enhanced by attaching an external heat sink to the thermal pad. This pad is electrically and thermally connected to the backside of the die and possibly selected leads.
　　　　　E.　Falls within JEDEC MO-187

PowerPAD is a trademark of Texas Instruments Incorporated.

TEXAS INSTRUMENTS

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MECHANICAL INFORMATION

FK (S-CQCC-N**)   **LEADLESS CERAMIC CHIP CARRIER**

28 TERMINAL SHOWN
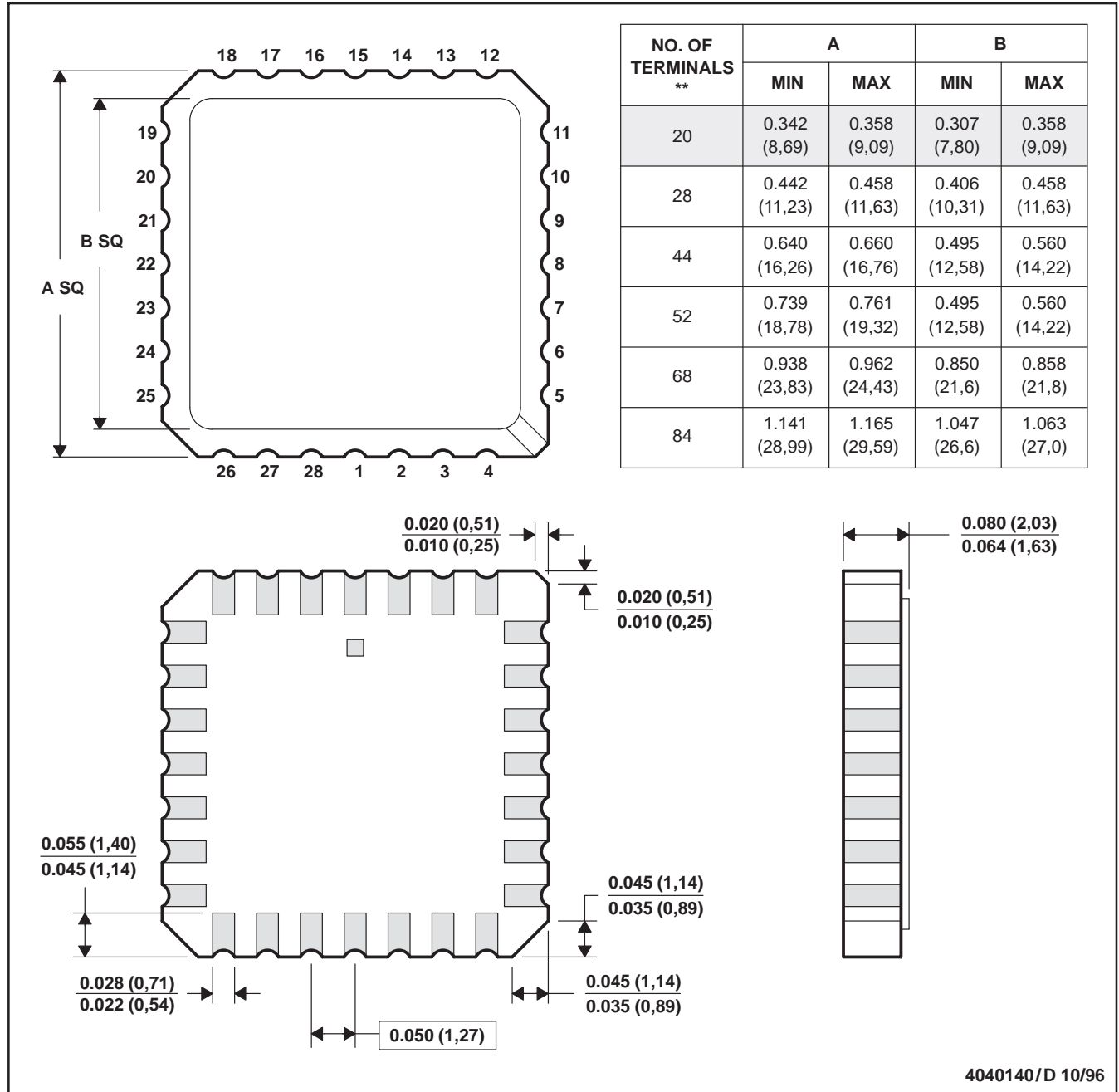
NO. OF TERMINALS **	A		B	
	MIN	**MAX**	**MIN**	**MAX**
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.739 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)

4040140 / D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
       B. This drawing is subject to change without notice.
       C. This package can be hermetically sealed with a metal lid.
       D. The terminals are gold plated.
       E. Falls within JEDEC MS-004

TEXAS INSTRUMENTS

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MECHANICAL INFORMATION

J (R-GDIP-T**)

CERAMIC DUAL-IN-LINE PACKAGE

14 PIN SHOWN
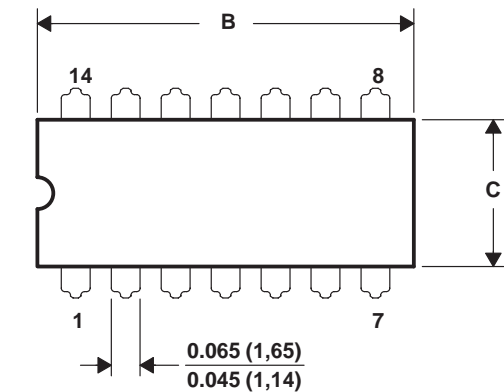
PINS ** DIM	14	16	18	20
A MAX	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)	0.310 (7,87)
A MIN	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)	0.290 (7,37)
B MAX	0.785 (19,94)	0.785 (19,94)	0.910 (23,10)	0.975 (24,77)
B MIN	0.755 (19,18)	0.755 (19,18)	——	0.930 (23,62)
C MAX	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)	0.245 (6,22)
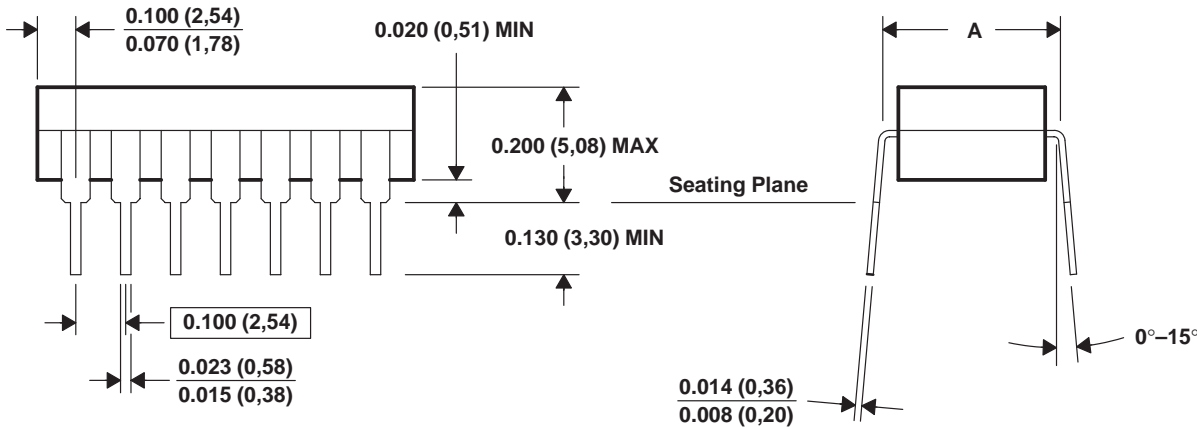
4040083/D 08/98

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
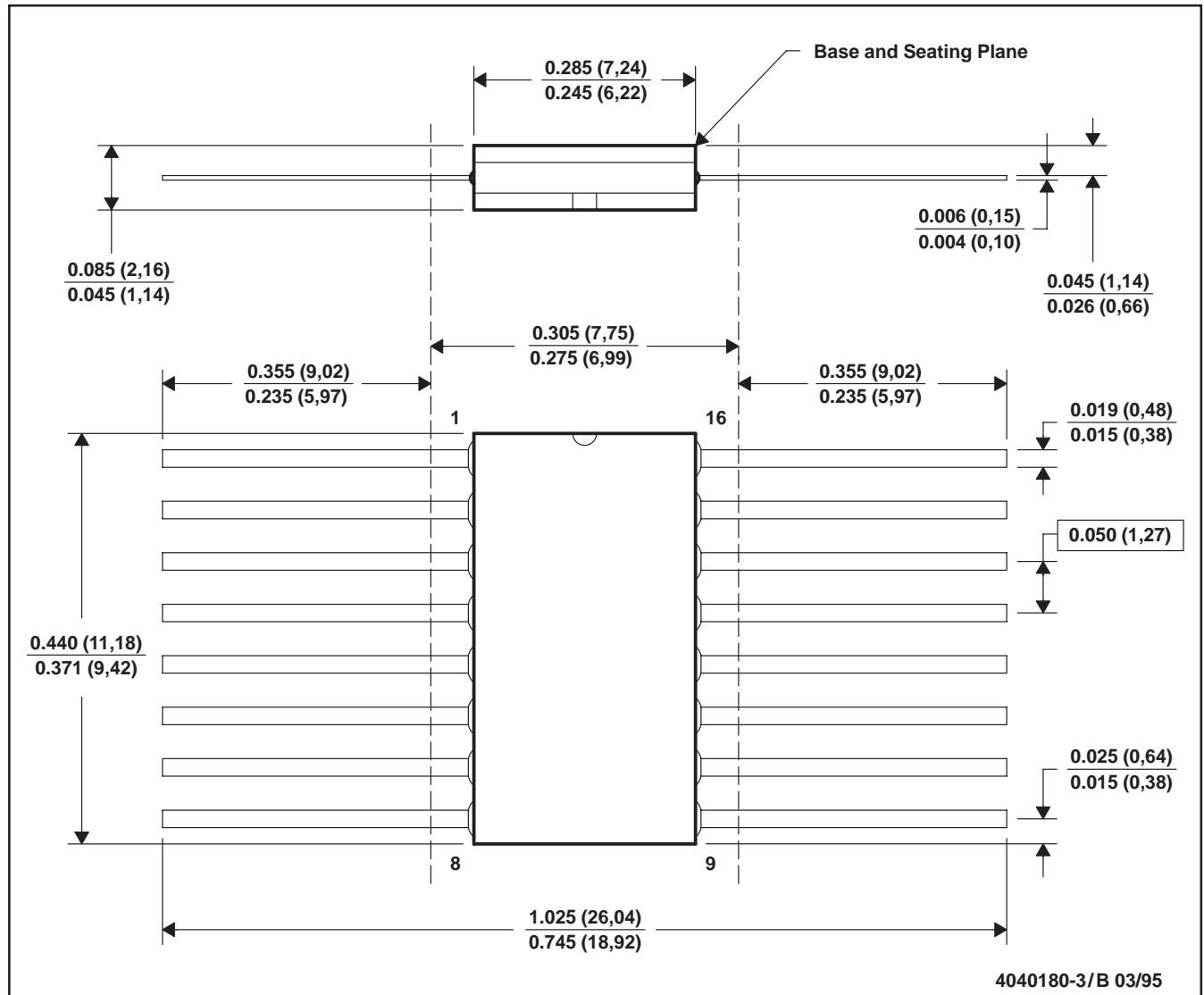E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18, GDIP1-T20, and GDIP1-T22.

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MECHANICAL INFORMATION

W (R-GDFP-F16)   **CERAMIC DUAL FLATPACK**

0.285 (7,24) / 0.245 (6,22)

Base and Seating Plane

0.085 (2,16) / 0.045 (1,14)

0.006 (0,15) / 0.004 (0,10)

0.045 (1,14) / 0.026 (0,66)

0.305 (7,75) / 0.275 (6,99)

0.355 (9,02) / 0.235 (5,97)

0.355 (9,02) / 0.235 (5,97)

1   16

0.019 (0,48) / 0.015 (0,38)

0.050 (1,27)

0.440 (11,18) / 0.371 (9,42)

0.025 (0,64) / 0.015 (0,38)

8   9

1.025 (26,04) / 0.745 (18,92)

4040180-3 / B 03/95

NOTES: A. All linear dimensions are in inches (millimeters).
          B. This drawing is subject to change without notice.
          C. This package can be hermetically sealed with a ceramic lid using glass frit.
          D. Index point is provided on cap for terminal identification only.
          E. Falls within MIL-STD-1835 GDFP1-F16 and JEDEC MO-092AC

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