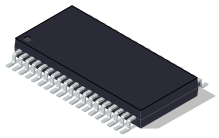


LVDS 4x4 CROSSPOINT SWITCH

FEATURES

- **Greater Than 2.0 Gbps Operation**
- **Nonblocking Architecture Allows Each Output to be Connected to Any Input**
- **Pk-Pk Jitter:**
  - **– 60 ps Typical at 2.0 Gbps**
  - **– 110 ps Typical at 2.5 Gbps**
- **Compatible With ANSI TIA/EIA-644-A LVDS Standard**
- **Available Packaging 38-Pin TSSOP**
- **25 mV of Input Voltage Threshold Hysteresis**
- **Propagation Delay Times: 800 ps Typical**
- **Inputs Electrically Compatible With LVPECL, CML and LVDS Signal Levels**
- **Operates From a Single 3.3-V Supply**
- **Low Power: 110 mA Typical**
- **Integrated 110-Ω Line Termination Resistors Available With SN65LVDT250**

APPLICATIONS

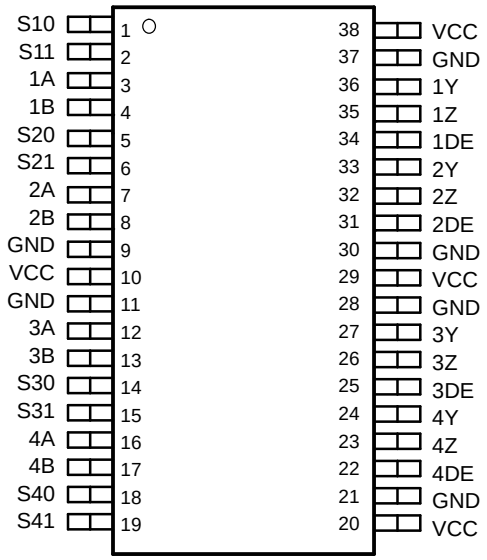
- **Clock Buffering/Clock Muxing**
- **Wireless Base Stations**
- **High-Speed Network Routing**
- **Telecom/Datacom**

DESCRIPTION

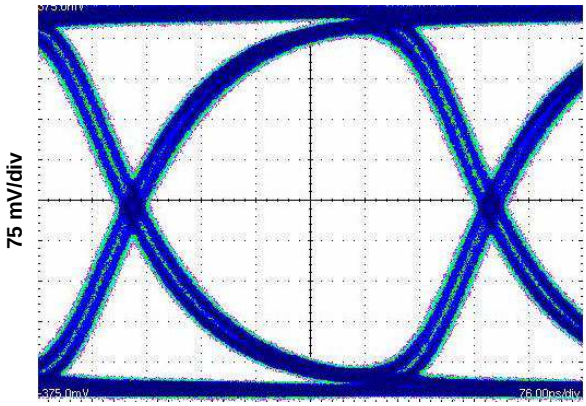
The SN65LVDS250 and SN65LVDT250 are 4x4 nonblocking crosspoint switches in a flow-through pin-out allowing for ease in PCB layout. Low-voltage differential signaling (LVDS) is used to achieve a high-speed data throughput while using low power. Each of the output drivers includes a 4:1 multiplexer to allow any input to be routed to any output. Internal signal paths are fully differential to achieve the high signaling speeds while maintaining low signal skews. The SN65LVDT250 incorporates 110-Ω termination resistors for those applications where board space is a premium.

The SN65LVDS250 and SN65LVDT250 are characterized for operation from -40°C to 85°C.

SN65LVDS250DBT (Marked as LVDS250)
SN65LVDT250DBT (Marked as LVDT250)
(TOP VIEW)



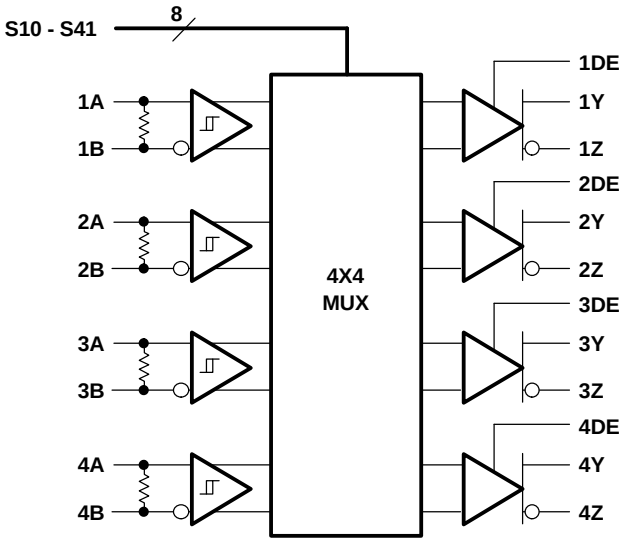
EYE PATTERN



V_{IC}= 1.2 V
$|V_{ID}|$ = 200 mV
2 Gbps
Input = PRBS 2^{23} –1
V_{CC} = 3.3 V

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

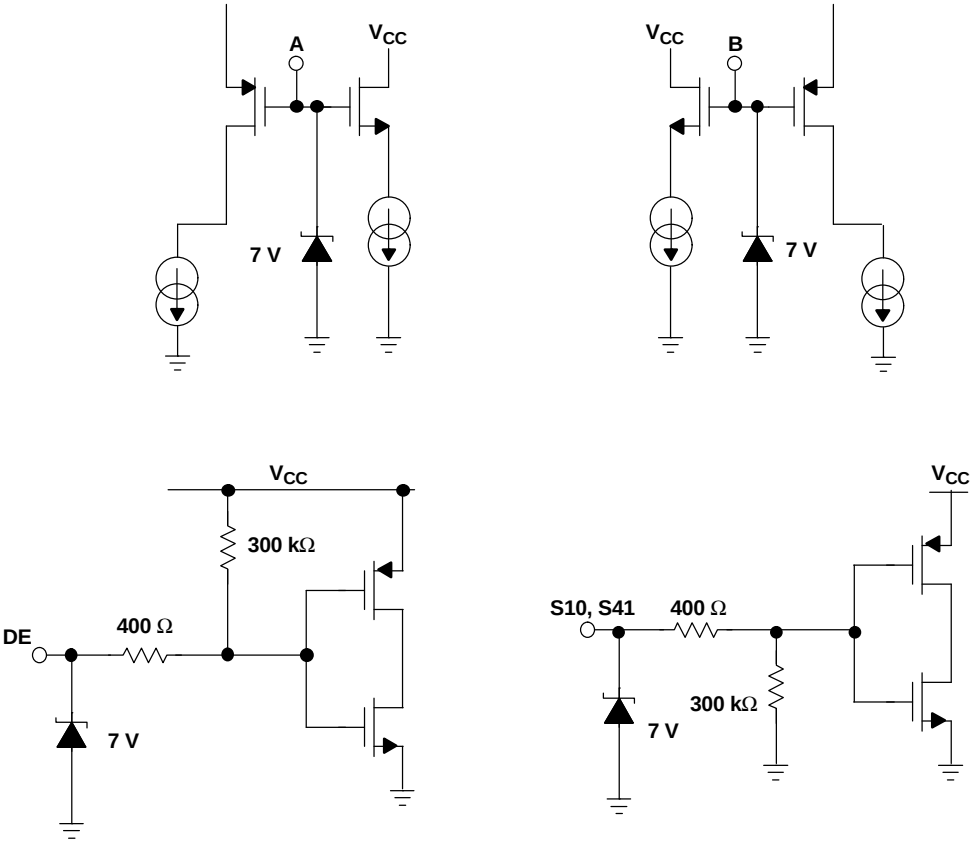
LOGIC DIAGRAM



Integrated Termination on LVDT Only

EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

INPUT LVDS250



OUTPUT LVDS250

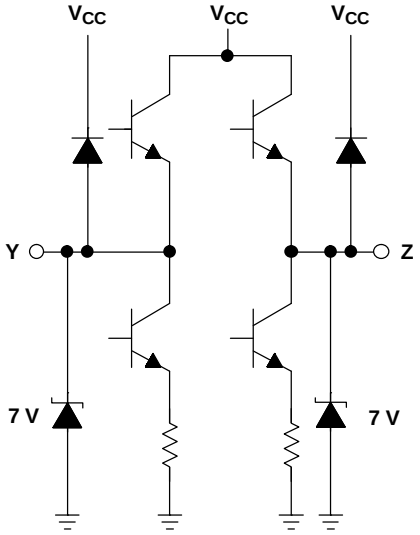


Table 1. CROSSPOINT LOGIC TABLES

OUTPUT CHANNEL 1			OUTPUT CHANNEL 2			OUTPUT CHANNEL 3			OUTPUT CHANNEL 4		
CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED	CONTROL PINS		INPUT SELECTED
S10	S11	1Y/1Z	S20	S21	2Y/2Z	S30	S31	3Y/3Z	S40	S41	4Y/4Z
0	0	1A/1B	0	0	1A/1B	0	0	1A/1B	0	0	1A/1B
0	1	2A/2B	0	1	2A/2B	0	1	2A/2B	0	1	2A/2B
1	0	3A/3B	1	0	3A/3B	1	0	3A/3B	1	0	3A/3B
1	1	4A/4B	1	1	4A/4B	1	1	4A/4B	1	1	4A/4B

PACKAGE DISSIPATION RATINGS

PACKAGE	CIRCUIT BOARD MODEL	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR(1) ABOVE $T_A = 25°C$	$T_A = 85°C$ POWER RATING
TSSOP (DBT)	Low-K(2)	1038 mW	9.0 mW/°C	496 mW
TSSOP (DBT)	High-K(3)	1772 mW	15.4 mW/°C	847 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounded and with no air flow.
(2) In accordance with the Low-K thermal metric definitions of EIA/JESD51-6
(3) In accordance with the High-K thermal metric definitions of EIA/JESD51-6

THERMAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	VALUE	UNITS
Θ_{JB}	Junction-to-board thermal resistance		40.3	°C/W
Θ_{JC}	Junction-to-case thermal resistance		8.5	°C/W
P_D	Device power dissipation	V_{CC} = 3.3 V, T_A = 25°C, 1 GHz	356	mW
		V_{CC} = 3.6 V, T_A = 85°C, 1 GHz	522	mW

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

			UNITS
Supply voltage range, V_{CC}			-0.5 V to 4 V
Voltage range(2)	S, DE		-0.5 V to 4 V
	A, B		-0.5 V to 4 V
	$\lvert V_A - V_B \rvert$ (LVDT only)		1 V
	Y, Z		-0.5 V to 4 V
Electrostatic discharge	Human body model(3)	All pins	±3 kV
	Charged-device model(4)	All pins	±500 V
Continuous power dissipation			See Dissipation Rating Table

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with JEDEC Standard 22, Test Method A114-A.
(4) Tested in accordance with JEDEC Standard 22, Test Method C101.

RECOMMENDED OPERATING CONDITIONS

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3	3.3	3.6	V
V_{IH}	High-level input voltage	S10-S41, 1DE-4DE	2		V_{CC}	V
V_{IL}	Low-level input voltage	S10-S41, 1DE-4DE	0		0.8	V
$\|V_{ID}\|$	Magnitude of differential input voltage	LVDS	0.1		1	V
		LVDT	0.1		0.8	V
	Input voltage (any combination of common-mode or input signals)		0		3.3	V
T_J	Junction temperature				140	°C
T_A (1)	Operating free-air temperature		-40		85	°C

(1) Maximum free-air temperature operation is allowed as long as the device maximum junction temperature is not exceeded.

TIMING SPECIFICATIONS

PARAMETER			MIN	NOM	MAX	UNIT
t_{SET}	Input to select setup time	See Figure 7		0.6		ns
t_{HOLD}	Input to select hold time			0.2		ns
t_{SWITCH}	Select to switch output			1.2	1.6	ns

INPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted(1)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input voltage threshold		See Figure 1			100	mV
V_{IT-}	Negative-going differential input voltage threshold		See Figure 1	-100			mV
$V_{ID(HYS)}$	Differential input voltage hysteresis				25		mV
I_{IH}	High-level input current	1DE-4DE	V_{IH} = 2 V	-10			µA
		S10-S41				20	
I_{IL}	Low-level input current	1DE-4DE	V_{IL} = 0.8 V	-10			µA
		S10-S41				20	
I_I	Input current (A or B inputs)		V_I = 0 V or 3.3 V, second input at 1.2 V (other input open for LVDT)	-20		20	µA
$I_{I(OFF)}$	Input current (A or B inputs)		$V_{CC} \leq$ 1.5 V, V_I = 0 V or 3.3 V, second input at 1.2 V(other input open for LVDT)	-20		20	µA
I_{IO}	Input offset current ($\|I_{IA} - I_{IB}\|$) (LVDS)		$V_{IA} = V_{IB}$, $0 \leq V_{IA} \leq$ 3.3 V	-6		6	µA
R_T	Termination resistance (LVDT)		V_{ID} = 300 mV, V_{IC} = 0 V to 3.3 V	90	110	132	Ω
	Termination resistance (LVDT with power-off)		V_{ID} = 300 mV, V_{IC} = 0 V to 3.3 V, V_{CC} = 1.5 V	90	110	132	
C_I	Differential input capacitance				2.5		pF

(1) All typical values are at 25°C and with a 3.3 V supply.

OUTPUT ELECTRICAL CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage magnitude	See Figure 2 V_{ID} = ±100 mV	247	350	454	mV
$\Delta\|V_{OD}\|$	Change in differential output voltage magnitude between logic states		-50		50	mV
$V_{OC(SS)}$	Steady-state common-mode output voltage	See Figure 3	1.125		1.375	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage between logic states		-50		50	mV
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			50	150	mV
I_{CC}	Supply current	R_L=100 Ω		110	145	mA
I_{OS}	Short-circuit output current	V_{OY} or V_{OZ} = 0 V	-27		27	mA
I_{OSD}	Differential short circuit output current	V_{OD} = 0 V	-12		12	mA
I_{OZ}	High-impedance output current	V_O = 0 V or V_{CC}			±1	µA
C_O	Differential output capacitance			2		pF

SWITCHING CHARACTERISTICS

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	See Figure 4	700	800	1200	ps
t_{PHL}	Propagation delay time, high-to-low-level output		700	800	1200	
t_r	Differential output signal rise time (20%-80%)			200	245	
t_f	Differential output signal fall time (20%-80%)			200	245	
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$) (1)			0	50	ps
$t_{sk(o)}$	Channel-to-channel output skew (2)				175	ps
$t_{sk(pp)}$	Part-to-part skew (3)				300	ps
$t_{jit(per)}$	Period jitter, rms (1 standard deviation) (4)	See Figure 6		1	3	ps
$t_{jit(cc)}$	Cycle-to-cycle jitter (peak) (5)	See Figure 6		8	17	ps
$t_{jit(pp)}$	Peak-to-peak jitteR (6)	See Figure 6		60	110	ps
$t_{jit(det)}$	Deterministic jitter, peak-to-peak (7)	See Figure 6		48	65	ps
t_{PHZ}	Propagation delay, high-level-to-high-impedance output	See Figure 5			6	ns
t_{PLZ}	Propagation delay, low-level-to-high-impedance output				6	
t_{PZH}	Propagation delay, high-impedance -to-high-level output				300	
t_{PZL}	Propagation delay, high-impedance-to-low-level output				300	

(1) $t_{sk(p)}$ is the magnitude of the time difference between the t_{PLH} and t_{PHL} of any output of a single device.
(2) $t_{sk(o)}$ is the maximum delay time difference between drivers over temperature, V_{CC}, and process.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.
(4) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 1.0 GHz, t_r = t_f= 50 ps (20% to 80%), measured over 1000 samples.
(5) Input voltage = V_{ID} = 200 mV, 50% duty cycle at 1.0 GHz, t_r = t_f= 50 ps (20% to 80%).
(6) Input voltage = V_{ID} = 200 mV, 2^{23}-1 PRBS pattern at 2.0 Gbps, t_r = t_f = 50 ps (20% to 80%), measured over 200k samples.
(7) Input voltage = V_{ID} = 200 mV, 2^7-1 PRBS pattern at 2.0 Gbps, t_r= t_f = 50 ps (20% to 80%).

PARAMETER MEASUREMENT INFORMATION

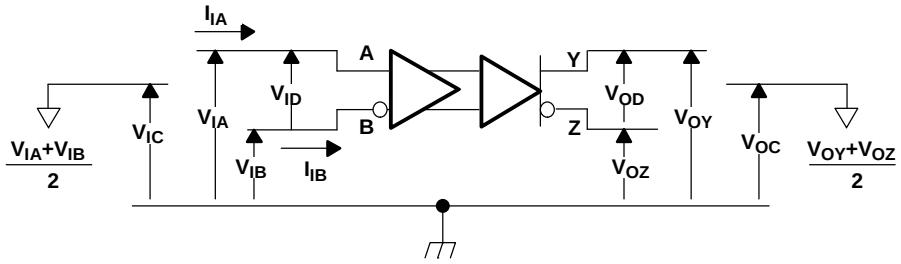


Figure 1. Voltage and Current Definitions

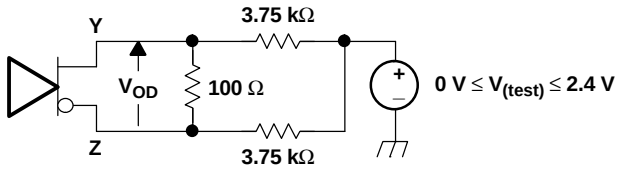
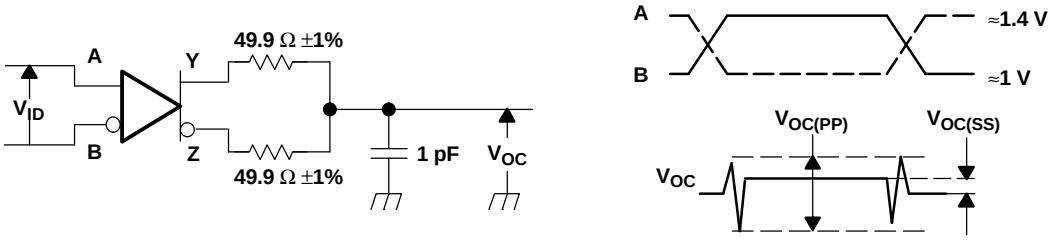
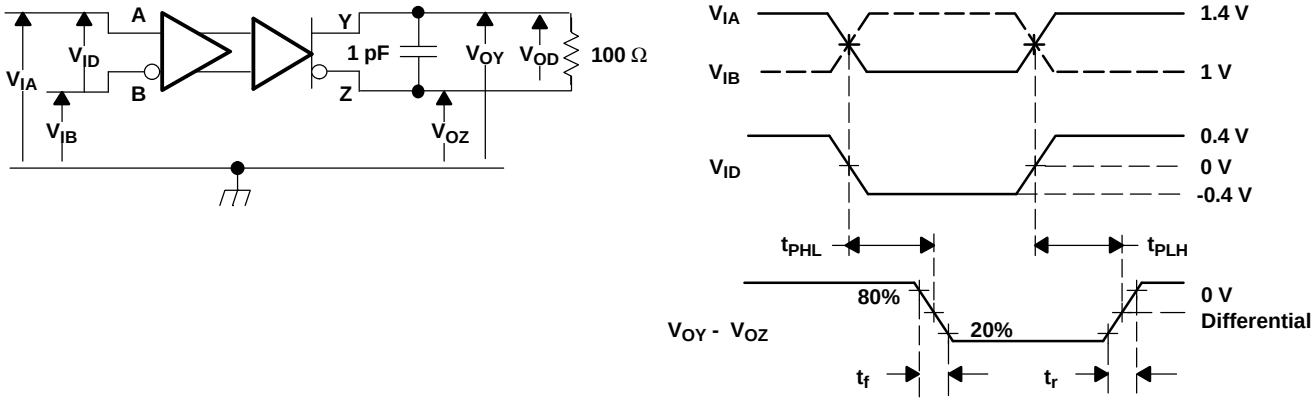


Figure 2. Differential Output Voltage (V_{OD}) Test Circuit



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 1 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ±10 ns; R_L = 100Ω ; C_L includes instrumentation and fixture capacitance within 0,06 mm of the DUT; the measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

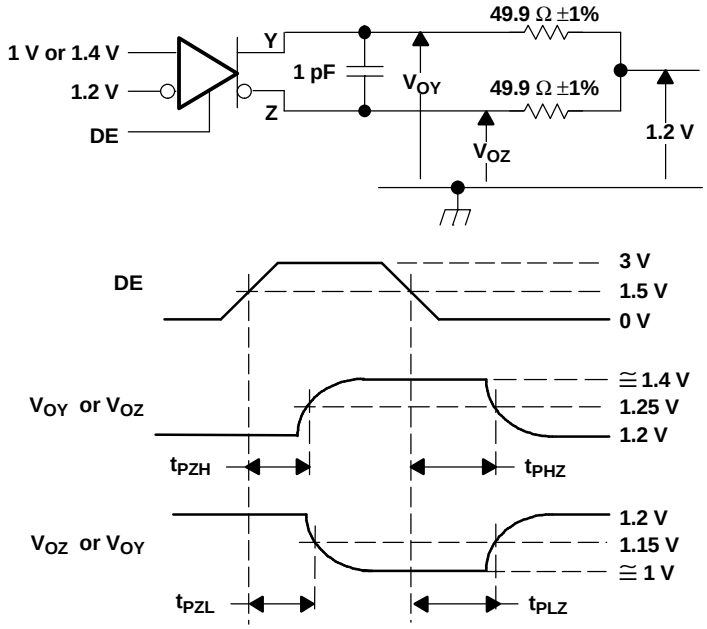
Figure 3. Test Circuit and Definitions fot the Driver Common-Mode Output Voltage



A. All input pulses are supplied by a generator having the following characteristics: t_r or t_f≤ 0.25 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns . C_L includes instrumentation and fixture capacitance within 0,06 mm of the DUT.

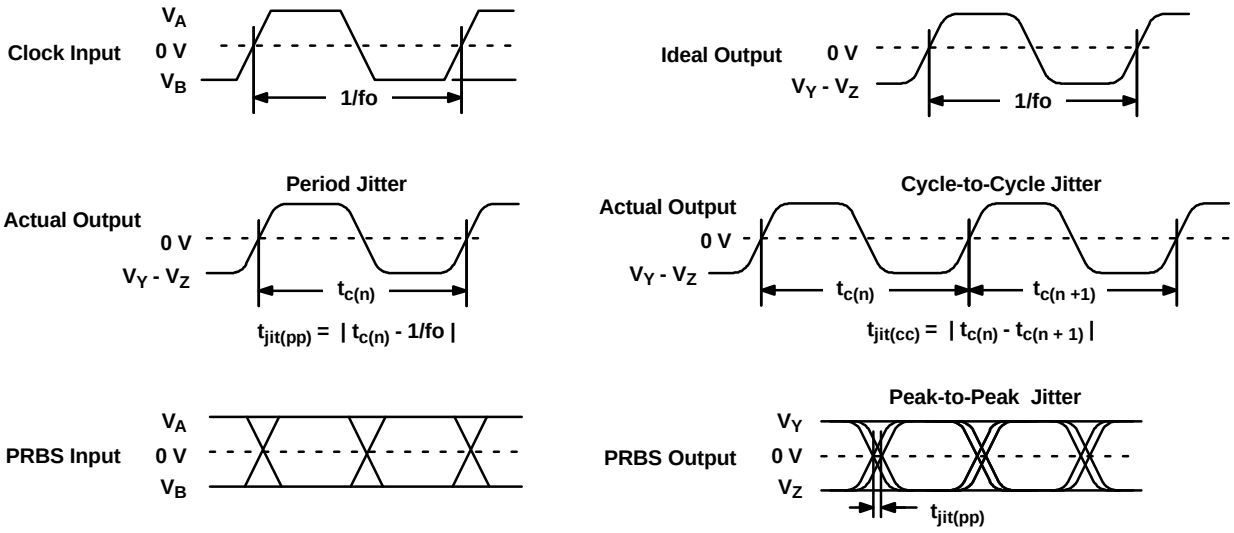
Figure 4. Timing Test Circuit and Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



A. All input pulses are supplied by a generator having the following characteristics: t_r or $t_f \leq$ 1 ns, pulse-repetition rate (PRR) = 0.5 Mpps, pulse width = 500 ± 10 ns. C_L includes instrumentation and fixture capacitance within 0,06 mm of the DUT.

Figure 5. Enable and Disable Time Circuit and Definitions

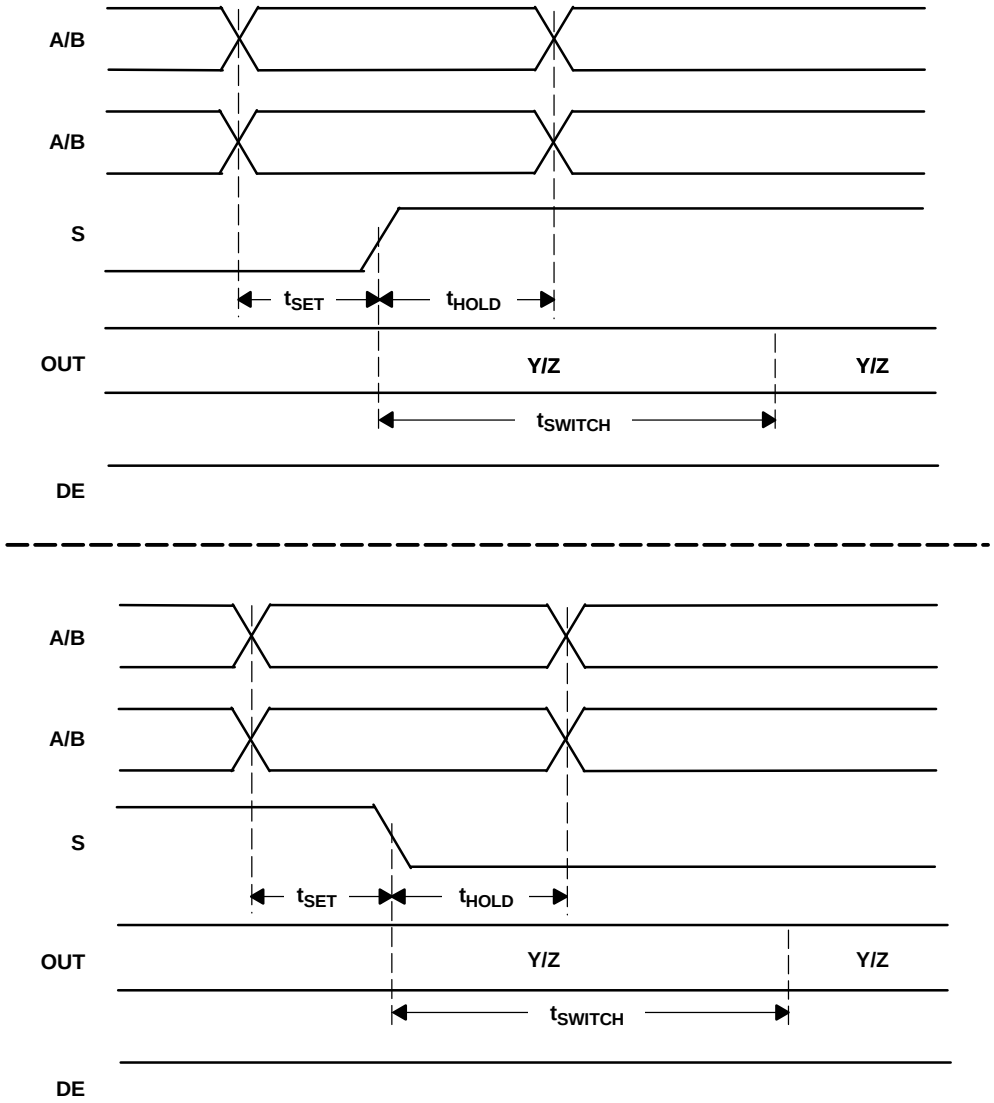


A. All input pulses are supplied by an Agilent 81250 Stimulus System.

B. The measurement is made on a TEK TDS6604 running TDSJIT3 application software.

Figure 6. Driver Jitter Measurement Waveforms

PARAMETER MEASUREMENT INFORMATION (continued)



A. t_{SET} and t_{HOLD} times specify that data must be in a stable state before and after mux control switches.

Figure 7. Input to Select for Both Rising and Falling Edge Setup and Hold Times

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREQUENCY

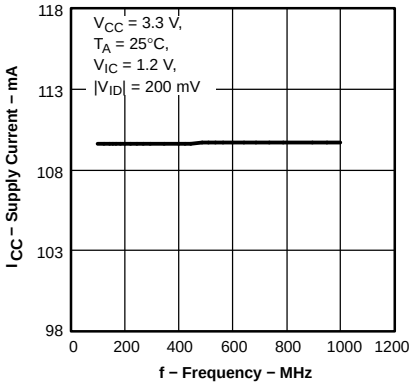


Figure 8.

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

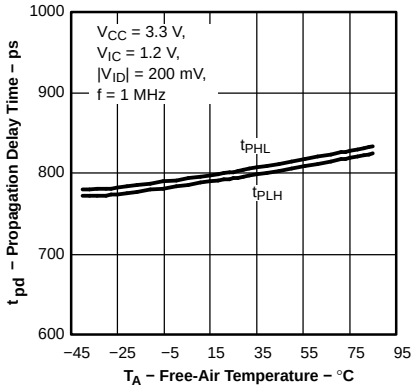


Figure 9.

PROPAGATION DELAY TIME vs COMMON-MODE INPUT VOLTAGE

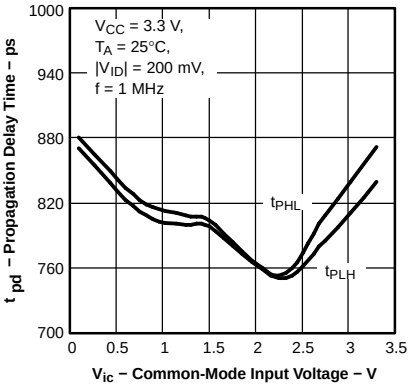


Figure 10.

PEAK-TO-PEAK JITTER vs FREQUENCY

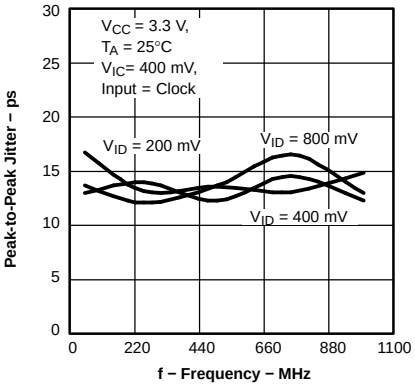


Figure 11.

PEAK-TO-PEAK JITTER vs DATA RATE

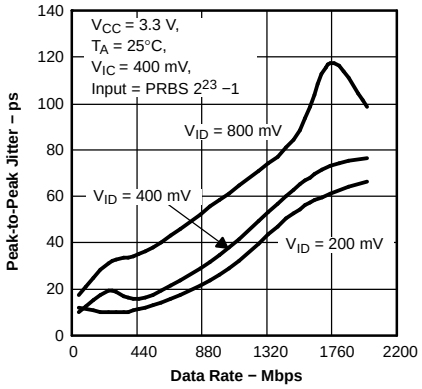


Figure 12.

PEAK-TO-PEAK JITTER vs FREQUENCY

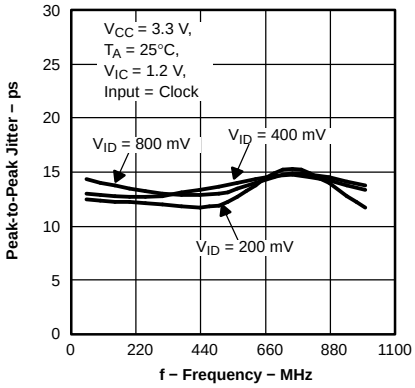


Figure 13.

PEAK-TO-PEAK JITTER vs DATA RATE

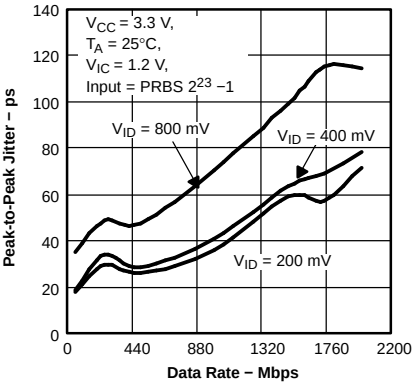


Figure 14.

PEAK-TO-PEAK JITTER vs FREQUENCY

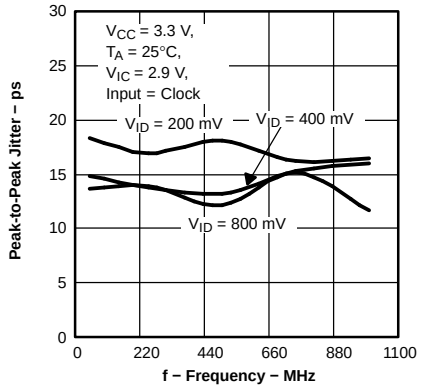


Figure 15.

PEAK-TO-PEAK JITTER vs DATA RATE

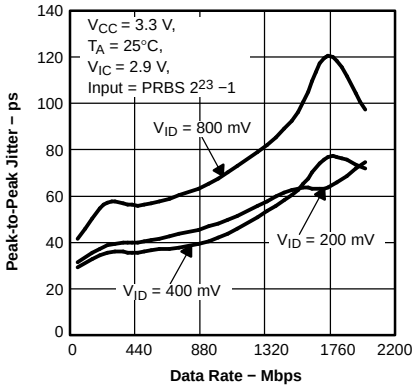


Figure 16.

TYPICAL CHARACTERISTICS (continued)

PEAK-TO-PEAK JITTER vs FREE-AIR TEMPERATURE

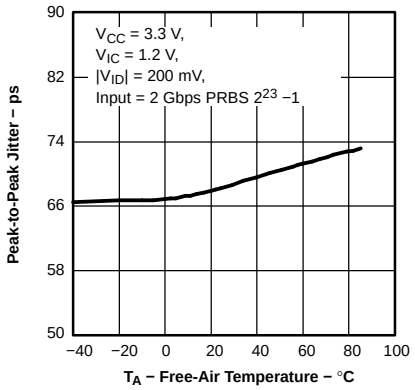


Figure 17.

PEAK-TO-PEAK JITTER vs DATA RATE

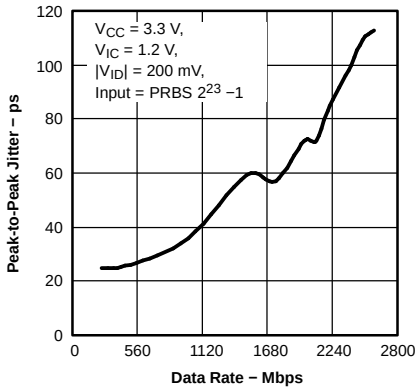


Figure 18.

DIFFERENTIAL OUTPUT VOLTAGE vs FREQUENCY

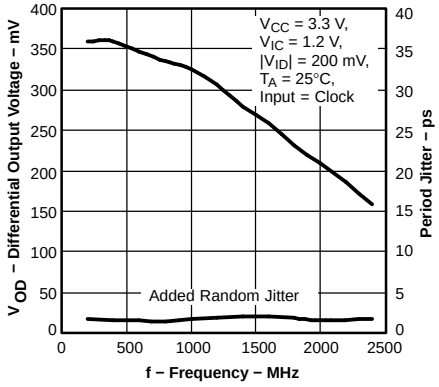
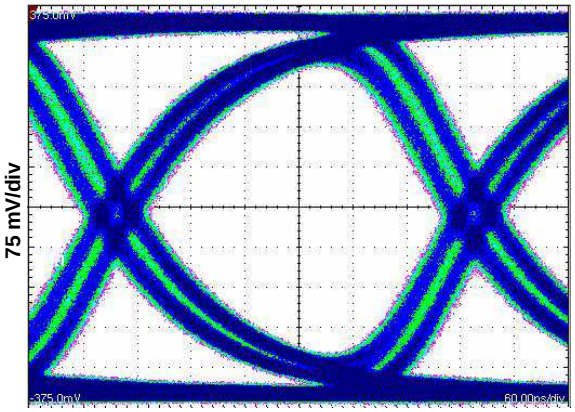


Figure 19.

EYE PATTERN



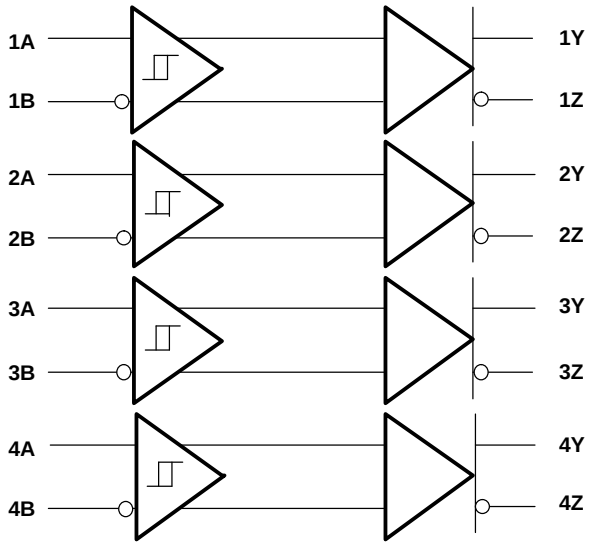
V_{IC}= 1.2 V, $|V_{ID}|$ = 200 mV, 2.5 Gbps, Input = PRBS 2^{23} –1, V_{CC} = 3.3 V

Figure 20.

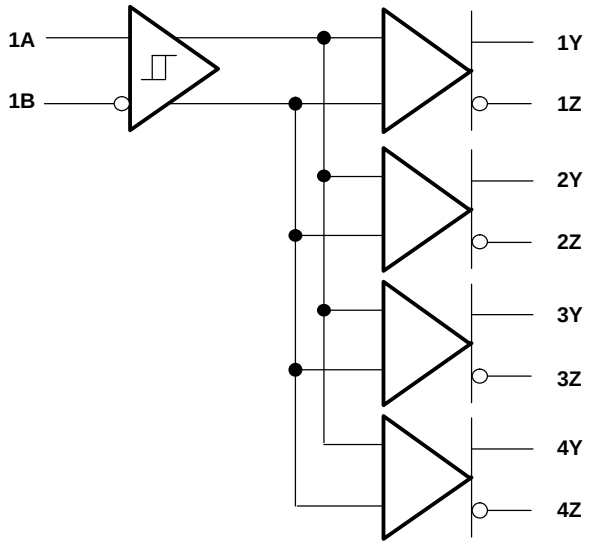
APPLICATION INFORMATION

CONFIGURATION EXAMPLES

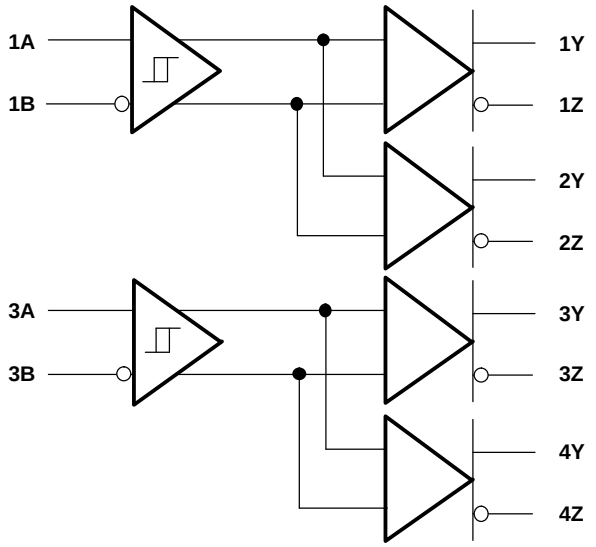
S10	S11	S20	S21
0	0	0	1
S30	S31	S40	S41
1	0	1	1



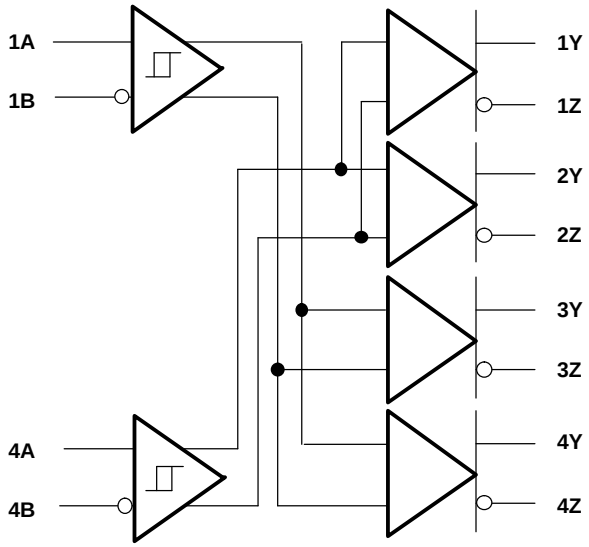
S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
0	0	0	0



S10	S11	S20	S21
0	0	0	0
S30	S31	S40	S41
1	0	1	0



S10	S11	S20	S21
1	1	1	1
S30	S31	S40	S41
0	0	0	0



APPLICATION INFORMATION (continued)

TYPICAL APPLICATION CIRCUITS (ECL, PECL, LVDS, etc.)

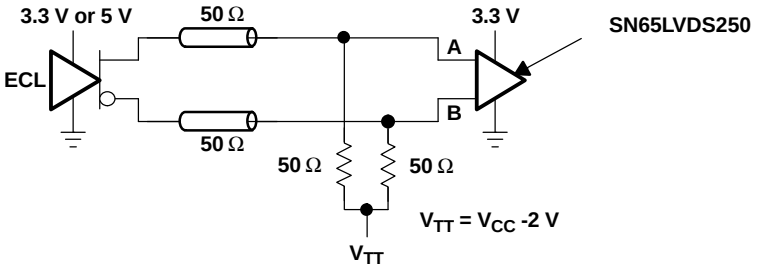


Figure 21. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)

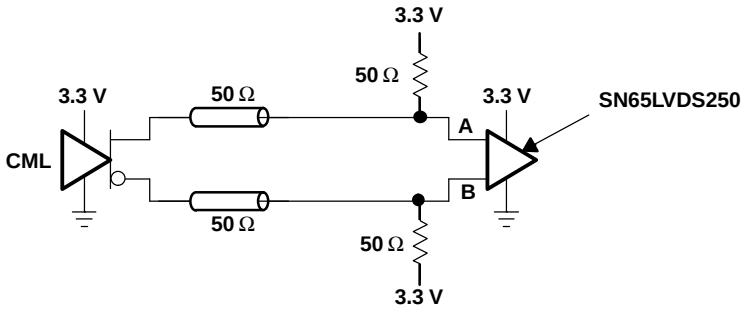


Figure 22. Current-Mode Logic (CML)

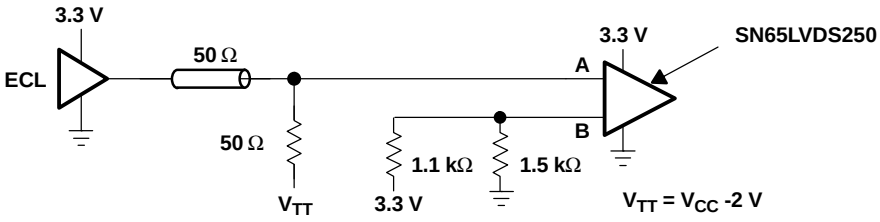


Figure 23. Single-Ended (LVPECL)

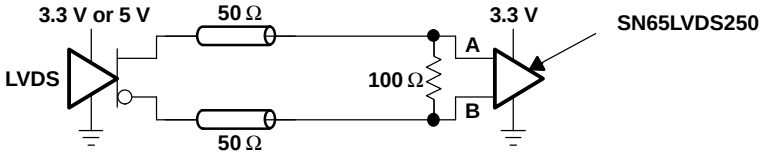


Figure 24. Low-Voltage Differential Signaling (LVDS)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN65LVDS250DBT	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS250DBTG4	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS250DBTR	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDS250DBTRG4	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDT250DBT	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDT250DBTG4	ACTIVE	SM8	DBT	38	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDT250DBTR	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
SN65LVDT250DBTRG4	ACTIVE	SM8	DBT	38	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

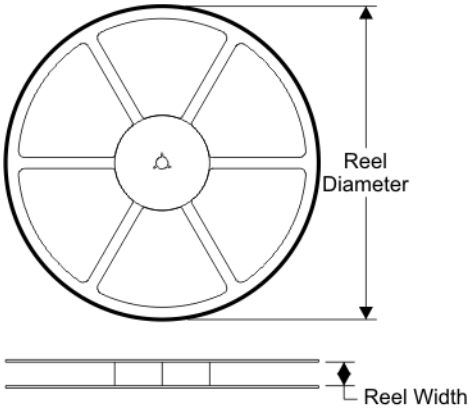
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

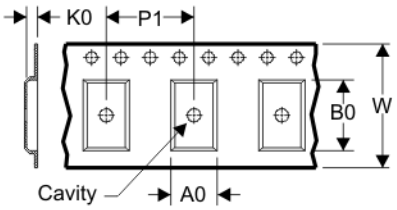
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL BOX INFORMATION

REEL DIMENSIONS

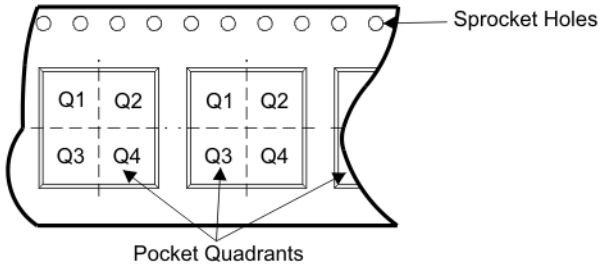


TAPE DIMENSIONS



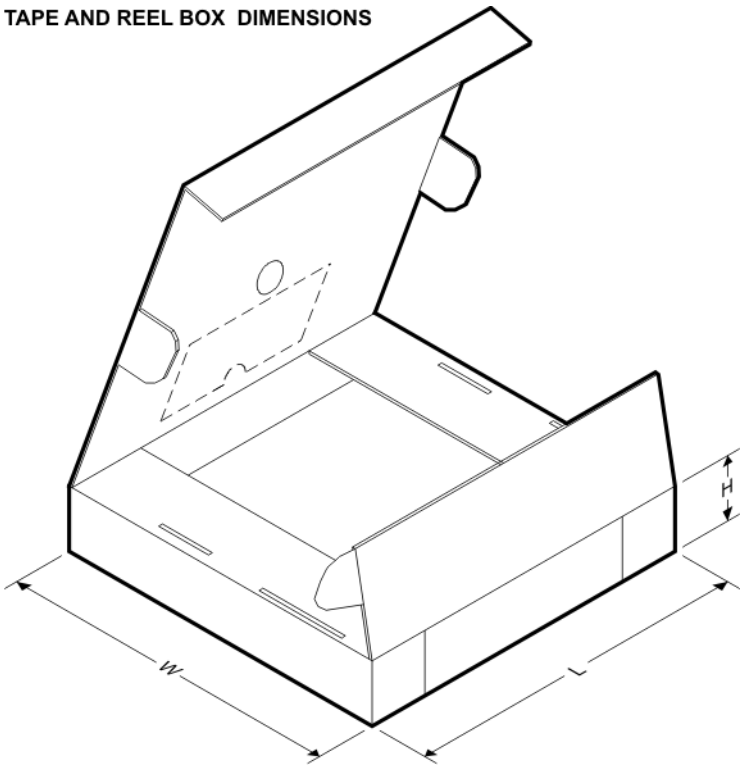
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65LVDS250DBTR	DBT	38	SITE 60	330	16	6.9	10.2	1.8	12	16	Q1
SN65LVDT250DBTR	DBT	38	SITE 60	330	16	6.9	10.2	1.8	12	16	Q1

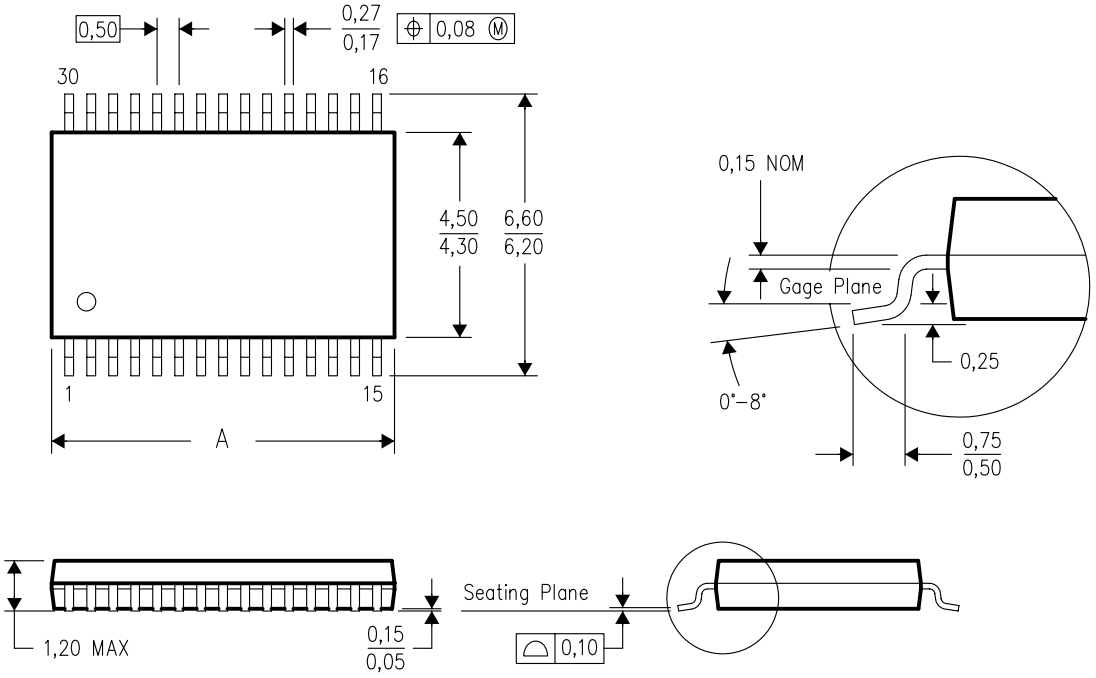
TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN65LVDS250DBTR	DBT	38	SITE 60	346.0	346.0	33.0
SN65LVDT250DBTR	DBT	38	SITE 60	346.0	346.0	33.0

DBT (R–PDSO–G**) PLASTIC SMALL–OUTLINE PACKAGE

30 PINS SHOWN



DIM \ PINS **	20	24	28	30	38	44	50
A MAX	5,10	6,60	7,90	7,90	9,80	11,40	12,60
A MIN	4,90	6,40	7,70	7,70	9,60	11,20	12,40

4073252/F 09/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–153 except 44 pin package length.

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of TI information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation. Information of third parties may be subject to additional restrictions.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

TI products are not authorized for use in safety-critical applications (such as life support) where a failure of the TI product would reasonably be expected to cause severe personal injury or death, unless officers of the parties have executed an agreement specifically governing such use. Buyers represent that they have all necessary expertise in the safety and regulatory ramifications of their applications, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of TI products in such safety-critical applications, notwithstanding any applications-related information or support that may be provided by TI. Further, Buyers must fully indemnify TI and its representatives against any damages arising out of the use of TI products in such safety-critical applications.

TI products are neither designed nor intended for use in military/aerospace applications or environments unless the TI products are specifically designated by TI as military-grade or "enhanced plastic." Only products designated by TI as military-grade meet military specifications. Buyers acknowledge and agree that any such use of TI products which TI has not designated as military-grade is solely at the Buyer's risk, and that they are solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI products are neither designed nor intended for use in automotive applications or environments unless the specific TI products are designated by TI as compliant with ISO/TS 16949 requirements. Buyers acknowledge and agree that, if they use any non-designated products in automotive applications, TI will not be responsible for any failure to meet such requirements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
RFID	www.ti-rfid.com	Telephony	www.ti.com/telephony
Low Power Wireless	www.ti.com/lpw	Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265