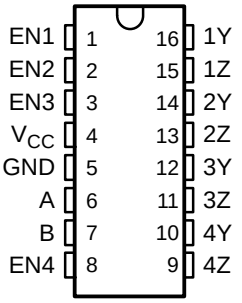
# 4-PORT LVDS AND 4-PORT TTL-TO-LVDS REPEATERS

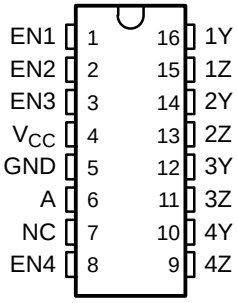
## FEATURES

- **Receiver and Drivers Meet or Exceed the Requirements of ANSI EIA/TIA-644 Standard**
  - **SN65LVDS105 Receives Low-Voltage TTL (LVTTL) Levels**
  - **SN65LVDS104 Receives Differential Input Levels, ±100 mV**
- **Typical Data Signaling Rates to 400 Mbps or Clock Frequencies to 400 MHz**
- **Operates From a Single 3.3-V Supply**
- **Low-Voltage Differential Signaling With Typical Output Voltage of 350 mV and a 100-Ω Load**
- **Propagation Delay Time**
  - **SN65LVDS105 – 2.2 ns (Typ)**
  - **SN65LVDS104 – 3.1 ns (Typ)**
- **LVTTL Levels Are 5-V Tolerant**
- **Electrically Compatible With LVDS, PECL, LVPECL, LVTTL, LVCMOS, GTL, BTL, CTT, SSTL, or HSTL Outputs With External Networks**
- **Driver Outputs Are High Impedance When Disabled or With $V_{CC}$ <1.5 V**
- **Bus-Pin ESD Protection Exceeds 16 kV**
- **SOIC and TSSOP Packaging**

**SN65LVDS104**
**D OR PW PACKAGE**
**(Marked as LVDS104)**
**(TOP VIEW)**

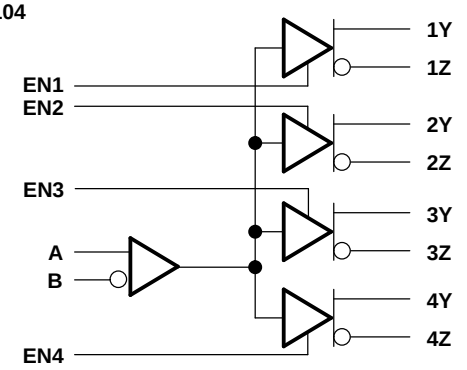



**SN65LVDS105**
**D OR PW PACKAGE**
**(Marked as LVDS105)**
**(TOP VIEW)**

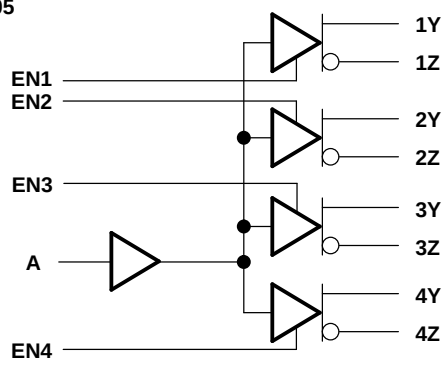



### logic diagram (positive logic)

**'LVDS104**




**'LVDS105**




## DESCRIPTION

The SN65LVDS104 and SN65LVDS105 are a differential line receiver and a LVTTL input (respectively) connected to four differential line drivers that implement the electrical characteristics of low-voltage differential signaling (LVDS). LVDS, as specified in EIA/TIA-644 is a data signaling technique that offers low-power, low-noise coupling, and switching speeds to transmit data at relatively long distances. (Note: The ultimate rate and distance of data transfer is dependent upon the attenuation characteristics of the media, the noise coupling to the environment, and other system characteristics.)

The intended application of this device and signaling technique is for point-to-point baseband data transmission over controlled impedance media of approximately 100 Ω. The transmission media may be printed-circuit board traces, backplanes, or cables. Having the drivers integrated into the same substrate, along with the low pulse skew of balanced signaling, allows extremely precise timing alignment of the signals repeated from the input. This is particularly advantageous in distribution or expansion of signals such as clock or serial data stream.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## DESCRIPTION (CONTINUED)

The SN65LVDS104 and SN65LVDS105 are characterized for operation from –40°C to 85°C.

The SN65LVDS104 and SN65LVDS105 are members of a family of LVDS repeaters. A brief overview of the family is provided in the table below.

**Selection Guide to LVDS Repeaters**

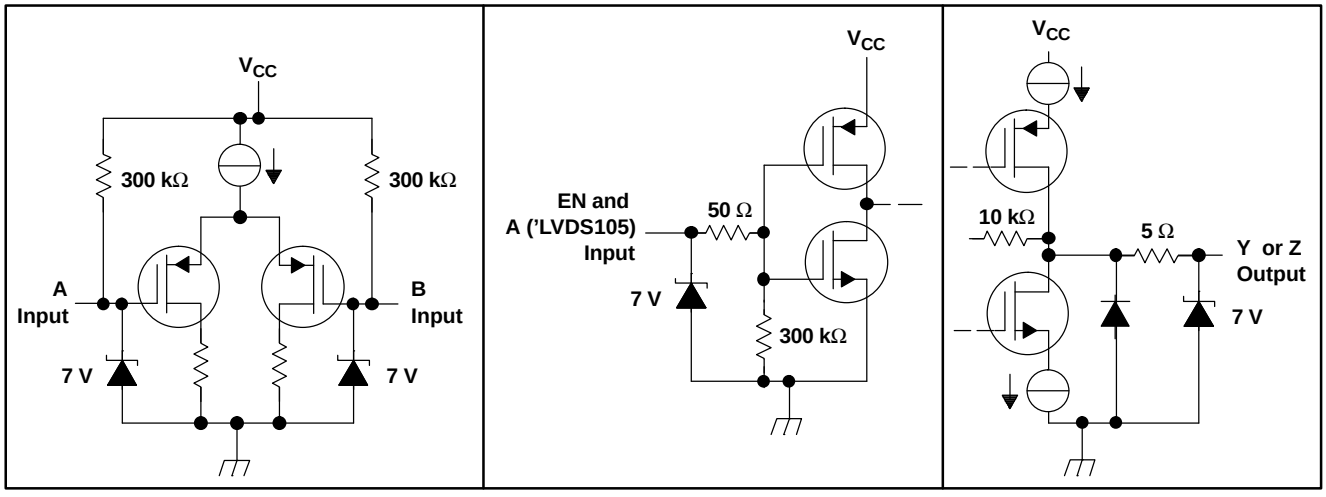
| DEVICE | NO. INPUTS | NO. OUTPUTS | PACKAGE | COMMENT |
|---|---|---|---|---|
| SN65LVDS22 | 2 LVDS | 2 LVDS | 16-pin D | Dual multiplexed LVDS repeater |
| SN65LVDS104 | 1 LVDS | 4 LVDS | 16-pin D | 4-Port LVDS repeater |
| SN65LVDS105 | 1 LVTTL | 4 LVDS | 16-pin D | 4-Port TTL-to-LVDS repeater |
| SN65LVDS108 | 1 LVDS | 8 LVDS | 38-pin DBT | 8-Port LVDS repeater |
| SN65LVDS109 | 2 LVDS | 8 LVDS | 38-pin DBT | Dual 4-port LVDS repeater |
| SN65LVDS116 | 1 LVDS | 16 LVDS | 64-pin DGG | 16-Port LVDS repeater |
| SN65LVDS117 | 2 LVDS | 16 LVDS | 64-pin DGG | Dual 8-port LVDS repeater |

**Function Tables(1)**

| SN65LVDS104 | | | | SN65LVDS105 | | | |
|---|---|---|---|---|---|---|---|
| INPUT | | OUTPUT | | INPUT | | OUTPUT | |
| $V_{ID} = V_A - V_B$ | xEN | xY | xZ | A | ENx | xY | xZ |
| X | X | Z | Z | L | H | L | H |
| X | L | Z | Z | H | H | H | L |
| $V_{ID} \geq 100$ mV | H | H | L | Open | H | L | H |
| –100 mV < $V_{ID}$ < 100 mV | H | ? | ? | X | L | Z | Z |
| $V_{ID} \leq$ –100 mV | H | L | H | X | X | Z | Z |

(1) H = high level, L = low level, Z = high impedance, ? = indeterminate, X = don't care

## EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS



## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)

| | | UNIT |
|---|---|---|
| Supply voltage range, $V_{CC}$ (2) | | –0.5 to 4 V |
| Voltage range | Enables, A ('LVDS105) | –0.5 to 6 V |
| | A, B, Y or Z | –0.5 to 4 V |
| Electrostatic discharge (3) | A, B, Y, Z, and GND | Class 3, A:16 kV, B: 400 V |
| Continuous power dissipation | | See Dissipation Rating Table |
| Storage temperature range | | –65°C to 150°C |
| Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds | | 260°C |

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.
(3) Tested in accordance with MIL-STD-883C Method 3015.7

## DISSIPATION RATING TABLE

| PACKAGE | $T_A \leq 25°C$ POWER RATING | OPERATING FACTOR (1) ABOVE $T_A = 25°C$ | $T_A = 85°C$ POWER RATING |
|---|---|---|---|
| D | 950 mW | 7.6 mW/°C | 494 mW |
| PW | 774 mW | 6.2 mW/°C | 402 mW |

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted (low-k) and with no air flow.

## RECOMMENDED OPERATING CONDITIONS

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | 3 | 3.3 | 3.6 | V |
| $V_{IH}$ | High-level input voltage | 2 | | | V |
| $V_{IL}$ | Low-level input voltage | | | 0.8 | V |
| $V_I$ or $V_{IC}$ | Voltage at any bus terminal (separately or common-mode) | 0 | | $V_{CC}$–0.8 | |
| $T_A$ | Operating free-air temperature | –40 | | 85 | °C |

## SN65LVDS104 ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IT+}$ | Positive-going differential input voltage threshold | See Figure 1 and Table 1 | | | 100 | mV |
| $V_{IT-}$ | Negative-going differential input voltage threshold | | –100 | | | |
| $\|V_{OD}\|$ | Differential output voltage magnitude | $R_L$ = 100 Ω, $V_{ID}$ = ± 100 mV, See Figure 1 and Figure 2 | 247 | 340 | 454 | mV |
| $\Delta\|V_{OD}\|$ | Change in differential output voltage magnitude between logic states | | –50 | | 50 | |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | See Figure 3 | 1.125 | | 1.375 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic states | | –50 | | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | | 25 | 150 | mV |
| $I_{CC}$ | Supply current | Enabled, $R_L$ = 100 Ω | | 23 | 35 | mA |
| | | Disabled | | 3 | 8 | mA |
| $I_I$ | Input current (A or B inputs) | $V_I$ = 0 V | –2 | –11 | –20 | µA |
| | | $V_I$ = 2.4 V | –1.2 | –3 | | |
| $I_{I(OFF)}$ | Power-off Input current | $V_{CC}$ = 1.5 V, $V_I$ = 2.4 V | | | 20 | µA |
| $I_{IH}$ | High-level input current (enables) | $V_{IH}$ = 2 V | | | 20 | µA |
| $I_{IL}$ | Low-level input current (enables) | $V_{IL}$ = 0.8 V | | | 10 | µA |
| $I_{OS}$ | Short-circuit output current | $V_{OY}$ or $V_{OZ}$ = 0 V | | | ±10 | mA |
| | | $V_{OD}$ = 0 V | | | ±10 | mA |
| $I_{OZ}$ | High-impedance output current | $V_O$ = 0 V or 2.4 V | | | ±1 | µA |
| $I_{O(OFF)}$ | Power-off output current | $V_{CC}$ = 1.5 V, $V_O$ = 2.4 V | | | ±1 | µA |
| $C_{IN}$ | Input capacitance (A or B inputs) | $V_I$ = 0.4 sin (4E6πt) + 0.5 V | | 3 | | pF |
| $C_O$ | Output capacitance (Y or Z outputs) | $V_I$ = 0.4 sin (4E6πt) + 0.5 V, Disabled | | 9.4 | | pF |

(1) All typical values are at 25°C and with a 3.3-V supply.

## SN65LVDS104 SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $R_L$ = 100 Ω, $C_L$ = 10 pF, See Figure 4 | 2.4 | 3.2 | 4.2 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 2.2 | 3.1 | 4.2 | ns |
| $t_r$ | Differential output signal rise time | | 0.3 | 0.8 | 1.2 | ns |
| $t_f$ | Differential output signal fall time | | 0.3 | 0.8 | 1.2 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{PHL} - t_{PLH}\|$) | | | 150 | 500 | ps |
| $t_{sk(o)}$ | Channel-to-channel output skew(2) | | | 20 | 100 | ps |
| $t_{sk(pp)}$ | Part-to-part skew(3) | | | | 1.5 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | See Figure 5 | | 7.2 | 15 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | 8.4 | 15 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | | | 3.6 | 15 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | 6 | 15 | ns |

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the $t_{PLH}$ or $t_{PHL}$ of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## SN65LVDS105 ELECTRICAL CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $\|V_{OD}\|$ | Differential output voltage magnitude | $R_L$ = 100 Ω, $V_{ID}$ = ±100 mV, See Figure 6 and Figure 7 | 247 | 340 | 454 | mV |
| $\Delta\|V_{OD}\|$ | Change in differential output voltage magnitude between logic states | | –50 | | 50 | |
| $V_{OC(SS)}$ | Steady-state common-mode output voltage | See Figure 8 | 1.125 | | 1.375 | V |
| $\Delta V_{OC(SS)}$ | Change in steady-state common-mode output voltage between logic states | | –50 | | 50 | mV |
| $V_{OC(PP)}$ | Peak-to-peak common-mode output voltage | | | 25 | 150 | mV |
| $I_{CC}$ | Supply current | Enabled, $R_L$ = 100 Ω | | 23 | 35 | mA |
| | | Disabled | | 0.7 | 6.4 | mA |
| $I_{IH}$ | High-level input current | $V_{IH}$ = 2 V | | | 20 | µA |
| $I_{IL}$ | Low-level input current | $V_{IL}$ = 0.8 V | | | 10 | µA |
| $I_{OS}$ | Short-circuit output current | $V_{OY}$ or $V_{OZ}$ = 0 V | | | ±10 | mA |
| | | $V_{OD}$ = 0 V | | | ±10 | mA |
| $I_{OZ}$ | High-impedance output current | $V_O$ = 0 V or 2.4 V | | | ±1 | µA |
| $I_{O(OFF)}$ | Power-off output current | $V_{CC}$ = 1.5 V, $V_O$ = 2.4 V | | 0.3 | ±1 | µA |
| $C_{IN}$ | Input capacitance | $V_I$ = 0.4 sin (4E6πt) + 0.5 V | | 5 | | pF |
| $C_O$ | Output capacitance (Y or Z outputs) | $V_I$ = 0.4 sin (4E6πt) + 0.5 V, Disabled | | 9.4 | | pF |

(1) All typical values are at 25°C and with a 3.3-V supply.

## SN65LVDS105 SWITCHING CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $t_{PLH}$ | Propagation delay time, low-to-high-level output | $R_L$ = 100 Ω, $C_L$ = 10 pF, See Figure 9 | 1.7 | 2.2 | 3 | ns |
| $t_{PHL}$ | Propagation delay time, high-to-low-level output | | 1.4 | 2.3 | 3.5 | ns |
| $t_r$ | Differential output signal rise time | | 0.3 | 0.8 | 1.2 | ns |
| $t_f$ | Differential output signal fall time | | 0.3 | 0.8 | 1.2 | ns |
| $t_{sk(p)}$ | Pulse skew ($\|t_{PHL} - t_{PLH}\|$) | | | 150 | 500 | ps |
| $t_{sk(o)}$ | Channel-to-channel output skew(2) | | | 20 | 100 | ps |
| $t_{sk(pp)}$ | Part-to-part skew(3) | | | | 1.5 | ns |
| $t_{PZH}$ | Propagation delay time, high-impedance-to-high-level output | See Figure 10 | | 7.2 | 15 | ns |
| $t_{PZL}$ | Propagation delay time, high-impedance-to-low-level output | | | 8.4 | 15 | ns |
| $t_{PHZ}$ | Propagation delay time, high-level-to-high-impedance output | | | 3.6 | 15 | ns |
| $t_{PLZ}$ | Propagation delay time, low-level-to-high-impedance output | | | 6 | 15 | ns |

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(o)}$ is the magnitude of the time difference between the $t_{PLH}$ or $t_{PHL}$ of all drivers of a single device with all of their inputs connected together.
(3) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

## PARAMETER MEASUREMENT INFORMATION

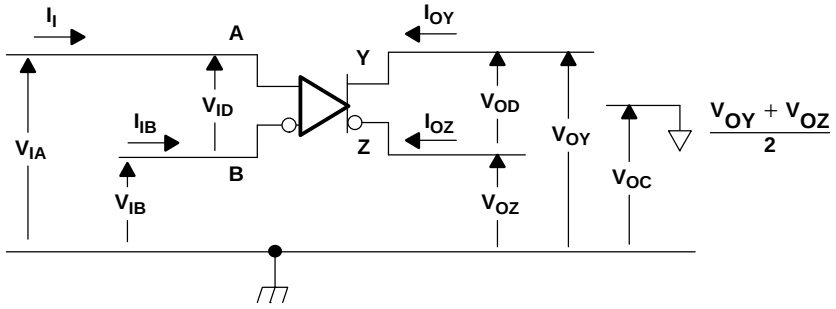



**Figure 1. 'LVDS104 Voltage and Current Definitions**

**Table 1. SN65LVDS104 Minimum and Maximum Input Threshold Test Voltages**

| APPLIED VOLTAGES | | RESULTING DIFFERENTIAL INPUT VOLTAGE | RESULTING COMMON-MODE INPUT VOLTAGE |
|---|---|---|---|
| $V_{IA}$ | $V_{IB}$ | $V_{ID}$ | $V_{IC}$ |
| 1.25 V | 1.15 V | 100 mV | 1.2 V |
| 1.15 V | 1.25 V | –100 mV | 1.2 V |
| 2.4 V | 2.3 V | 100 mV | 2.35 V |
| 2.3 V | 2.4 V | –100 mV | 2.35 V |
| 0.1 V | 0 V | 100 mV | 0.05 V |
| 0 V | 0.1 V | –100 mV | 0.05 V |
| 1.5 V | 0.9 V | 600 mV | 1.2 V |
| 0.9 V | 1.5 V | –600 mV | 1.2 V |
| 2.4 V | 1.8 V | 600 mV | 2.1 V |
| 1.8 V | 2.4 V | –600 mV | 2.1 V |
| 0.6 V | 0 V | 600 mV | 0.3 V |
| 0 V | 0.6 V | –600 mV | 0.3 V |

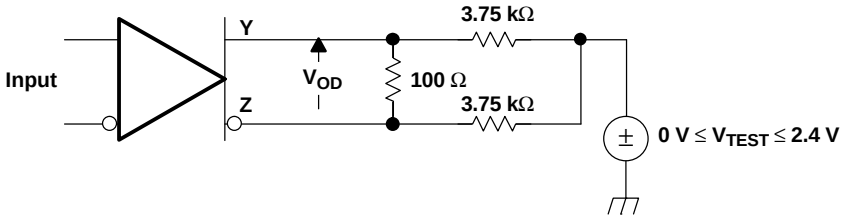
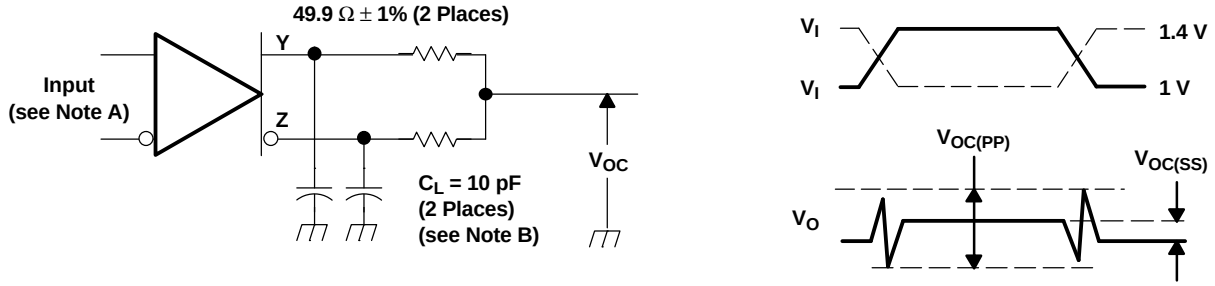


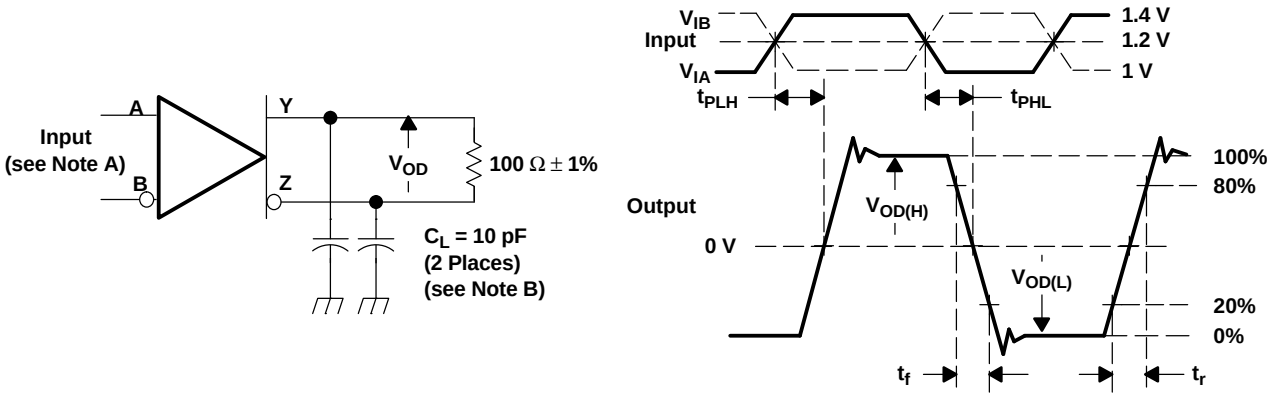

**Figure 2. 'LVDS104 $V_{OD}$ Test Circuit**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns.

B. $C_L$ includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a –3 dB bandwidth of at least 300 MHz.

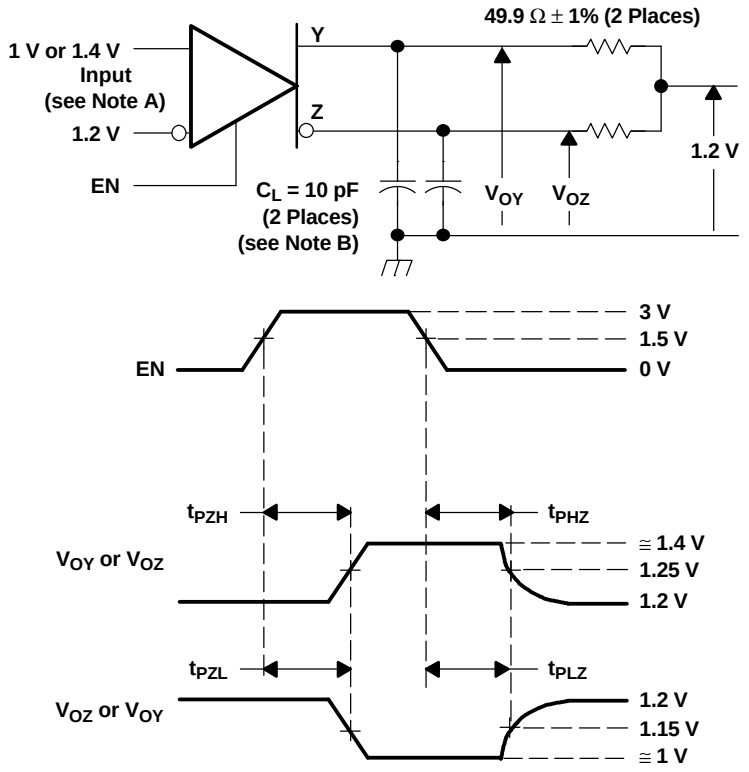
**Figure 3. 'LVDS104 Test Circuit and Definitions for the Driver Common-Mode Output Voltage**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ± 0.2 ns.

B. $C_L$ includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

**Figure 4. 'LVDS104 Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns.

B. $C_L$ includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

**Figure 5. 'LVDS104 Enable and Disable Time Circuit and Definitions**

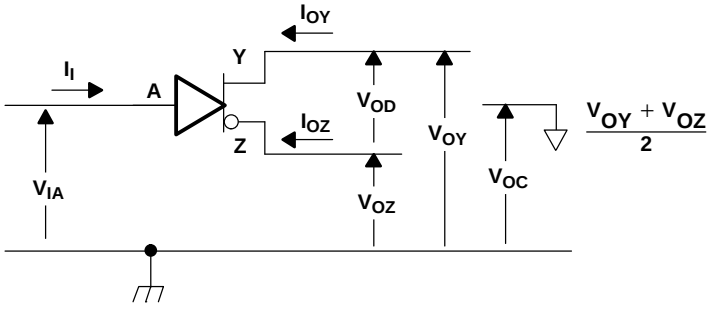



**Figure 6. 'LVDS105 Voltage and Current Definitions**

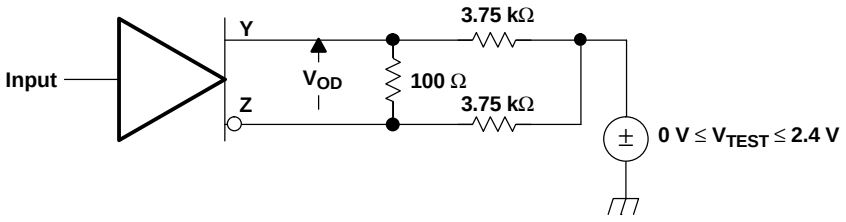
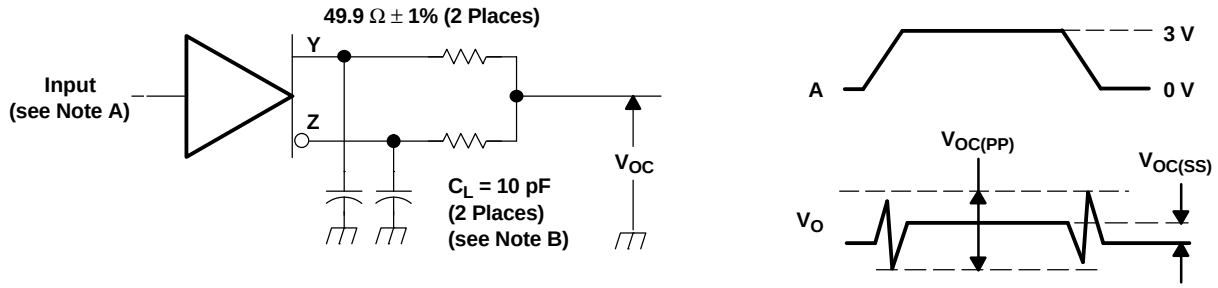


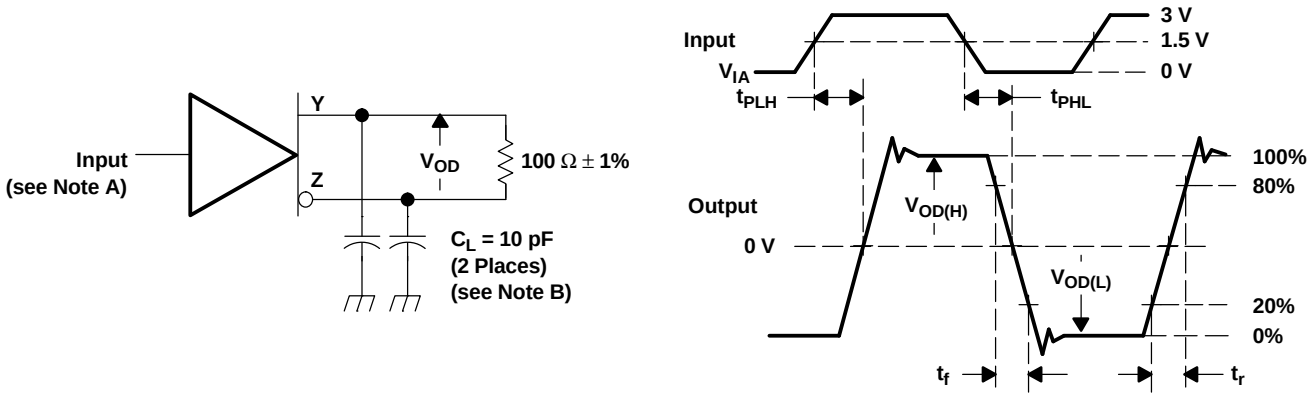

**Figure 7. 'LVDS105 VOD Test Circuit**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns.

B. $C_L$ includes instrumentation and fixture capacitance within 0,06 m of the D.U.T. The measurement of $V_{OC(PP)}$ is made on test equipment with a -3 dB bandwidth of at least 300 MHz.

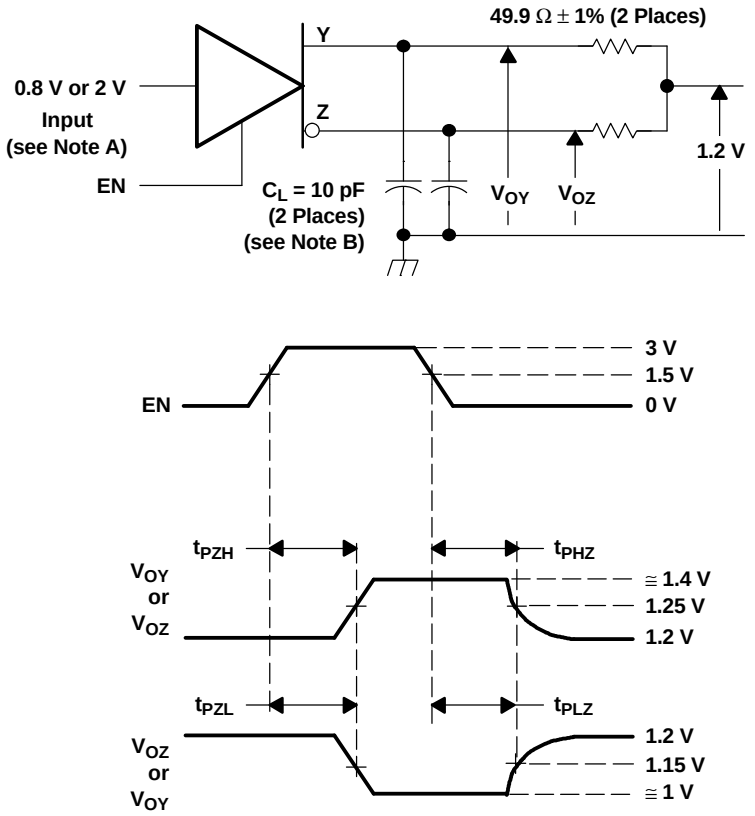
**Figure 8. 'LVDS105 Test Circuit and Definitions for the Driver Common-Mode Output Voltage**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 50 Mpps, pulsewidth = 10 ± 0.2 ns.

B. $C_L$ includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

**Figure 9. 'LVDS105 Test Circuit, Timing, and Voltage Definitions for the Differential Output Signal**




A. All input pulses are supplied by a generator having the following characteristics: $t_r$ or $t_f \leq$ 1 ns, pulse repetition rate (PRR) = 0.5 Mpps, pulsewidth = 500 ± 10 ns.

B. $C_L$ includes instrumentation and fixture capacitance within 0,06 m of the D.U.T.

**Figure 10. 'LVDS105 Enable and Disable Time Circuit and Definitions**

## TYPICAL CHARACTERISTIC

SN65LVDS104
SUPPLY CURRENT
vs
FREQUENCY

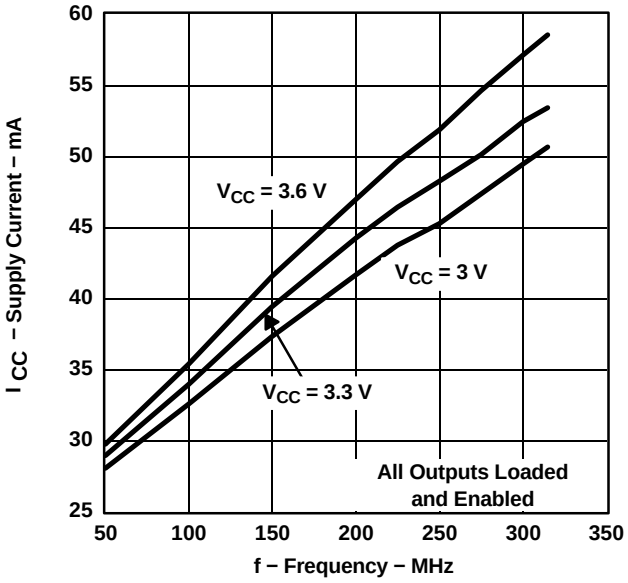



Figure 11.

SN65LVDS105
SUPPLY CURRENT
vs
FREQUENCY

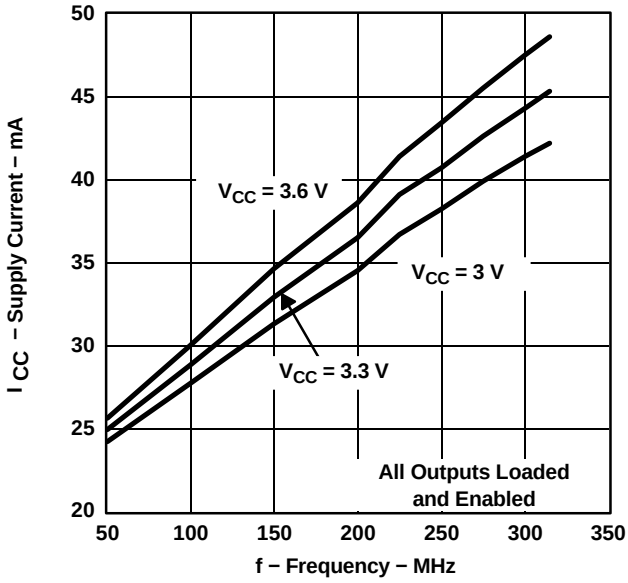



Figure 12.

DRIVER
LOW-LEVEL OUTPUT VOLTGE
vs
LOW-LEVEL OUTPUT CURRENT

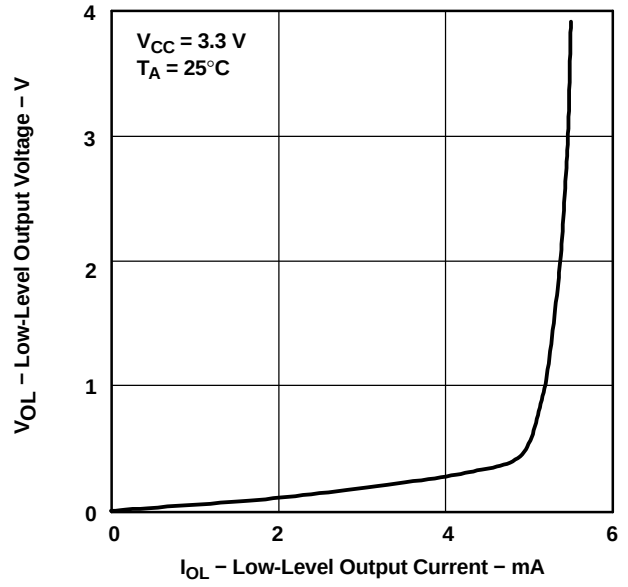



Figure 13.

DRIVER
HIGH-LEVEL OUTPUT VOLTGE
vs
HIGH-LEVEL OUTPUT CURRENT

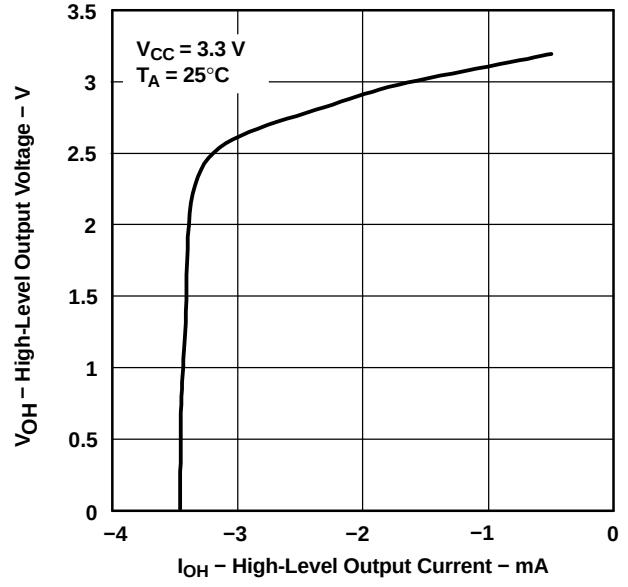



Figure 14.

## TYPICAL CHARACTERISTIC (continued)

SN65LVDS104
LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

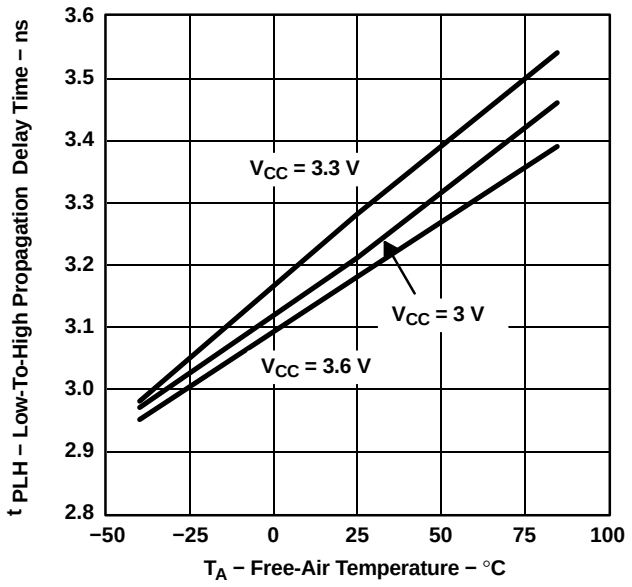



Figure 15.

SN65LVDS104
HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

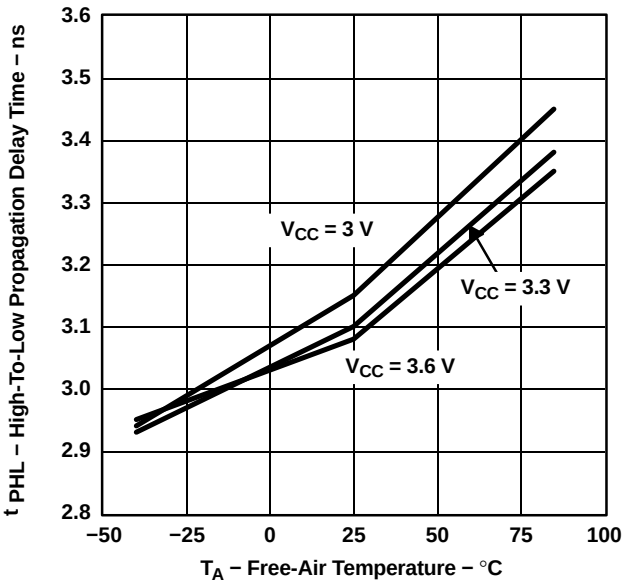



Figure 16.

SN65LVDS105
LOW-TO-HIGH PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

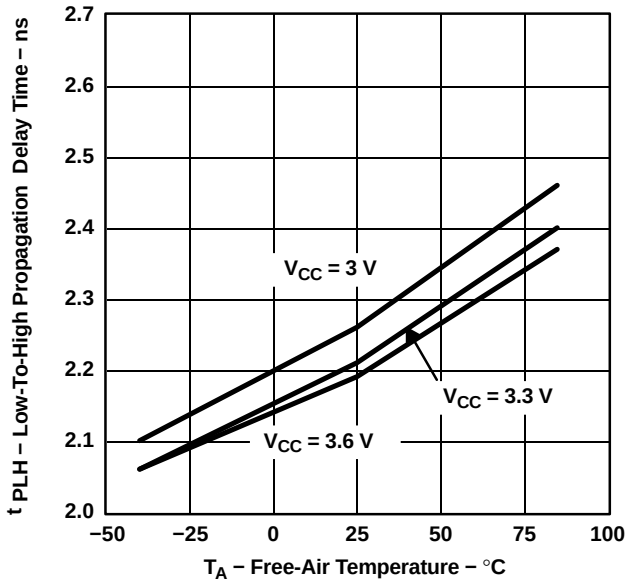



Figure 17.

SN65LVDS105
HIGH-TO-LOW PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

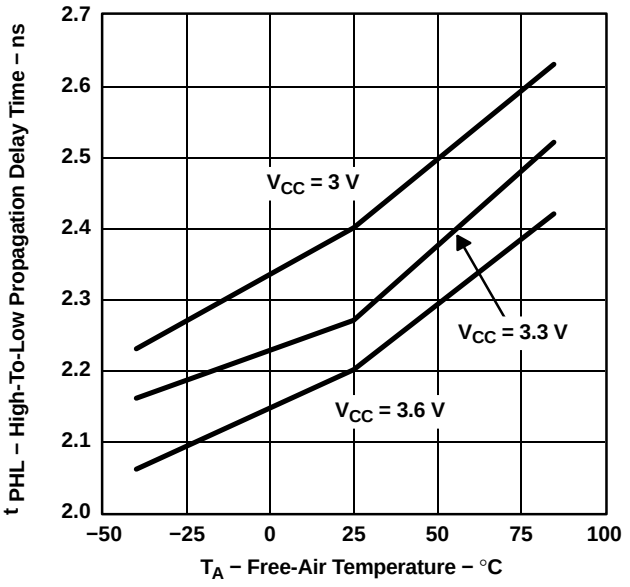
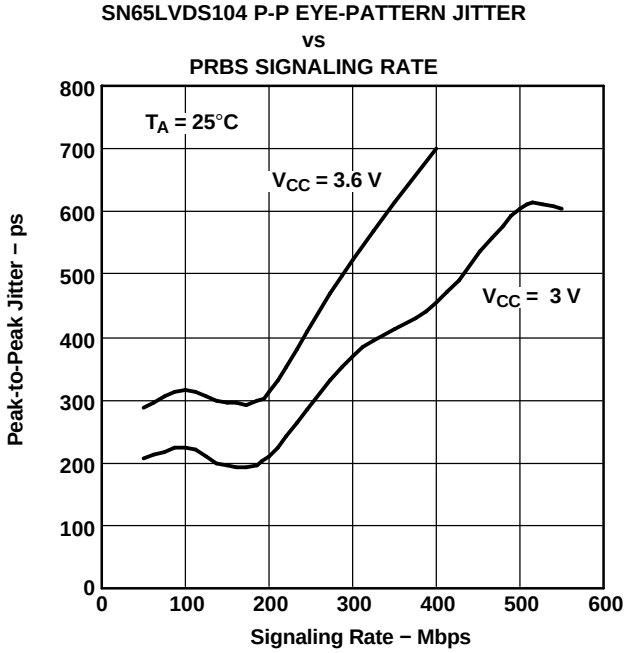


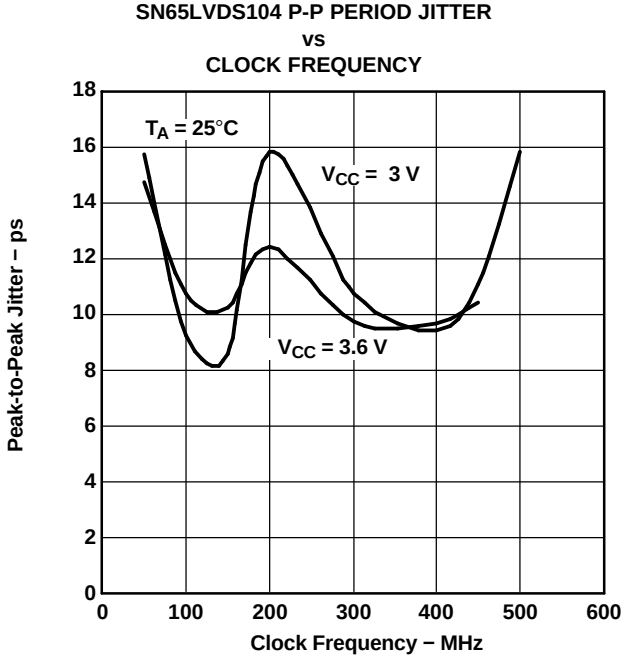

Figure 18.

## TYPICAL CHARACTERISTIC (continued)




NOTES: Input: $2^{15}$ PRBS with peak-to-peak jitter <115 ps at 100 Mbps. Test board adds about 70 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF ceramic 0603-style capacitors 1 cm from the device.

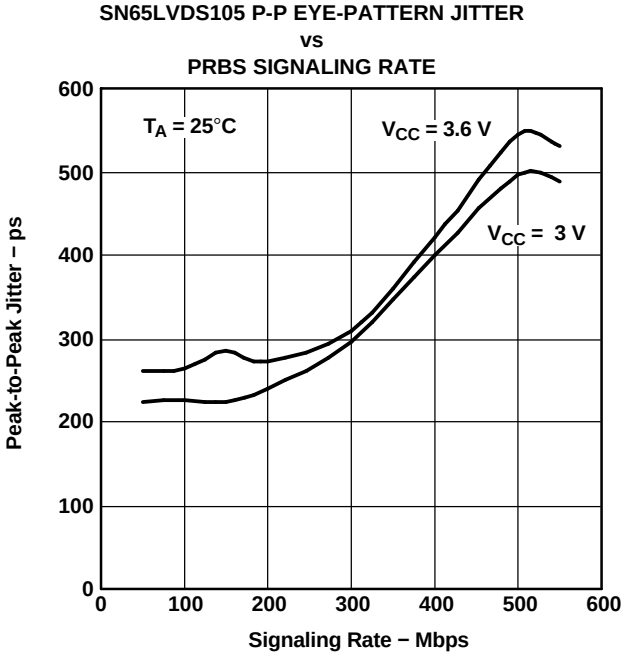
**Figure 19.**




NOTES: Input: 50% duty cycle square wave with period jitter < 9 ps at 100 MHz. Test board adds about 5 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

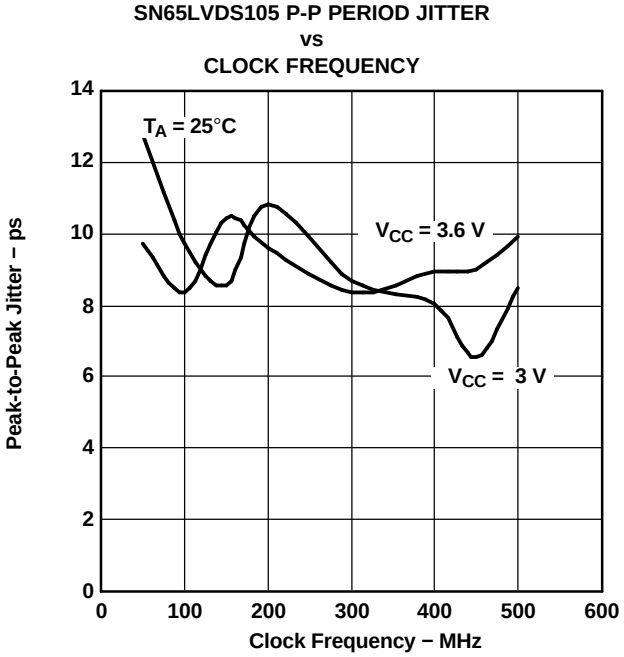
**Figure 20.**

## TYPICAL CHARACTERISTIC (continued)




NOTES: Input: $2^{15}$ PRBS with peak-to-peak Jitter < 147 ps at 100 Mbps, Test board adds about 43 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

**Figure 21.**




NOTES: Input: 50% duty cycle square wave with period jitter < 10 ps at 100 MHz. Test board adds about 5 ps p-p jitter. All outputs enabled and loaded with differential 100-Ω loads, worst-case output, supply decoupled with 0.1-µF and 0.001-µF ceramic 0603-style capacitors 1 cm from the device.

**Figure 22.**

## APPLICATION INFORMATION

### INPUT LEVEL TRANSLATION

An LVDS receiver can be used to receive various other types of logic signals. Figure 23 through Figure 32 show the termination circuits for SSTL, HSTL, GTL, BTL, LVPECL, PECL, CMOS, and TTL.

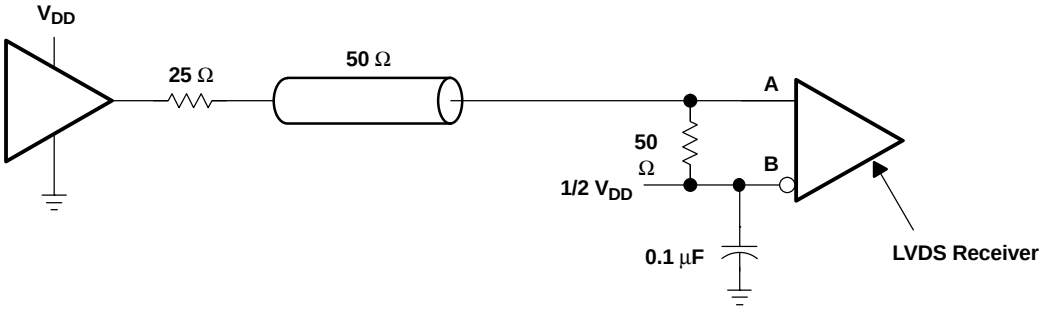



**Figure 23. Stub-Series Terminated (SSTL) or High-Speed Transceiver Logic (HSTL)**

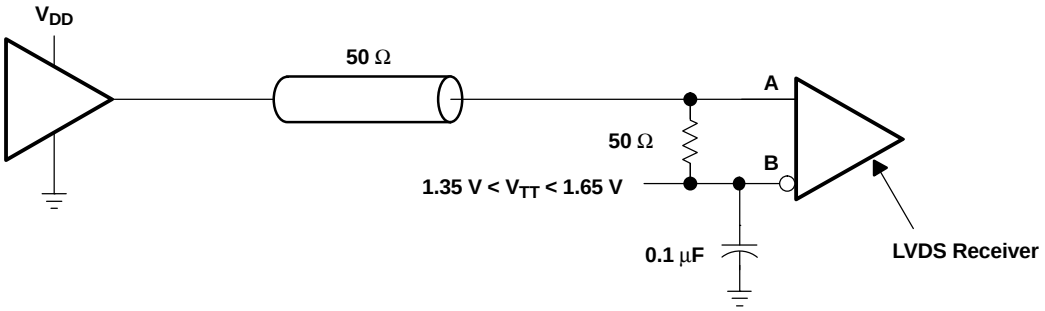



**Figure 24. Center-Tap Termination (CTT)**

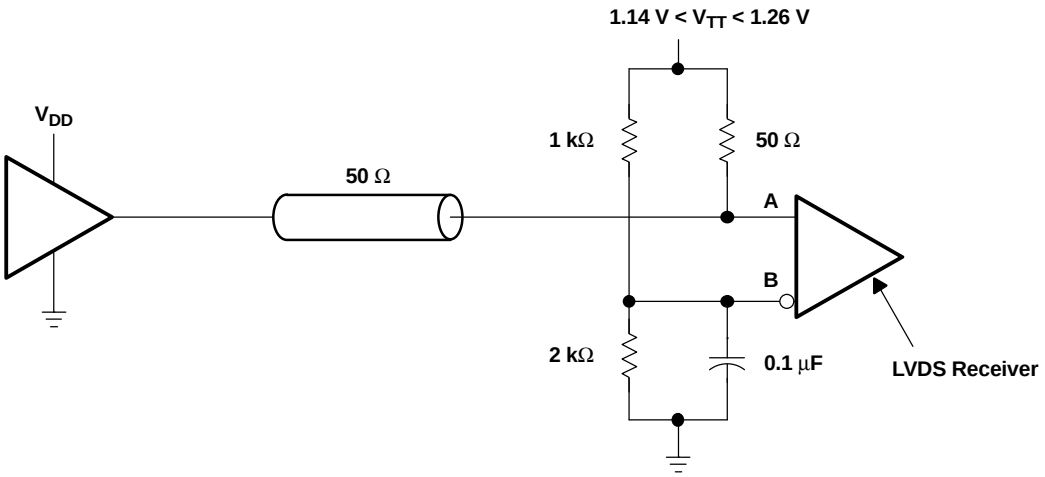



**Figure 25. Gunning Transceiver Logic (GTL)**

## APPLICATION INFORMATION (continued)

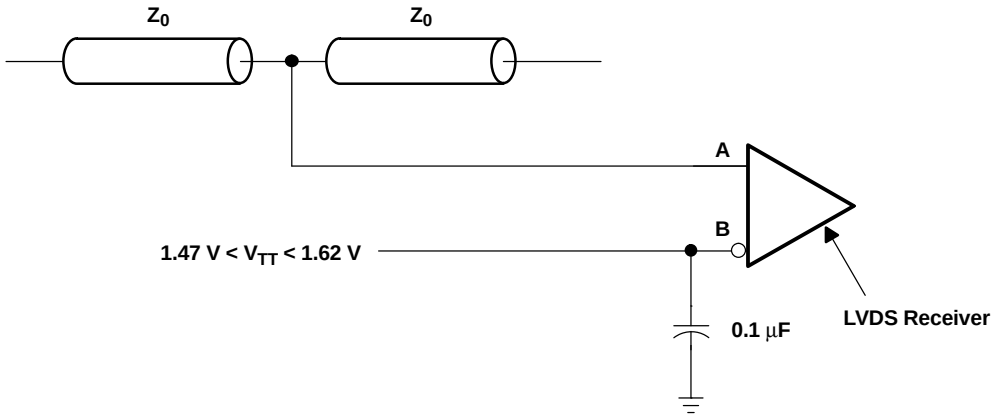



**Figure 26. Backplane Transceiver Logic (BTL)**

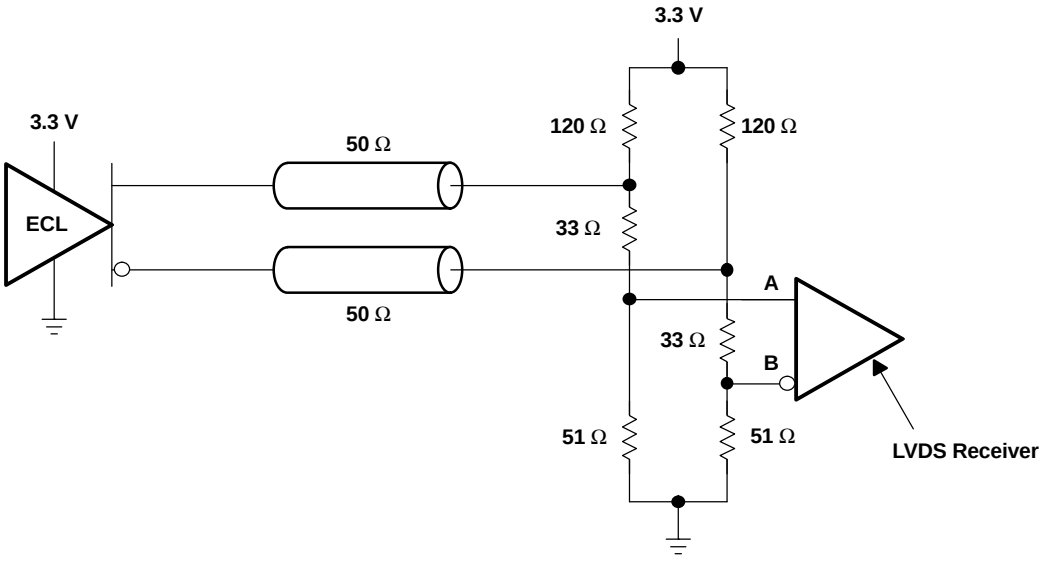



**Figure 27. Low-Voltage Positive Emitter-Coupled Logic (LVPECL)**

## APPLICATION INFORMATION (continued)

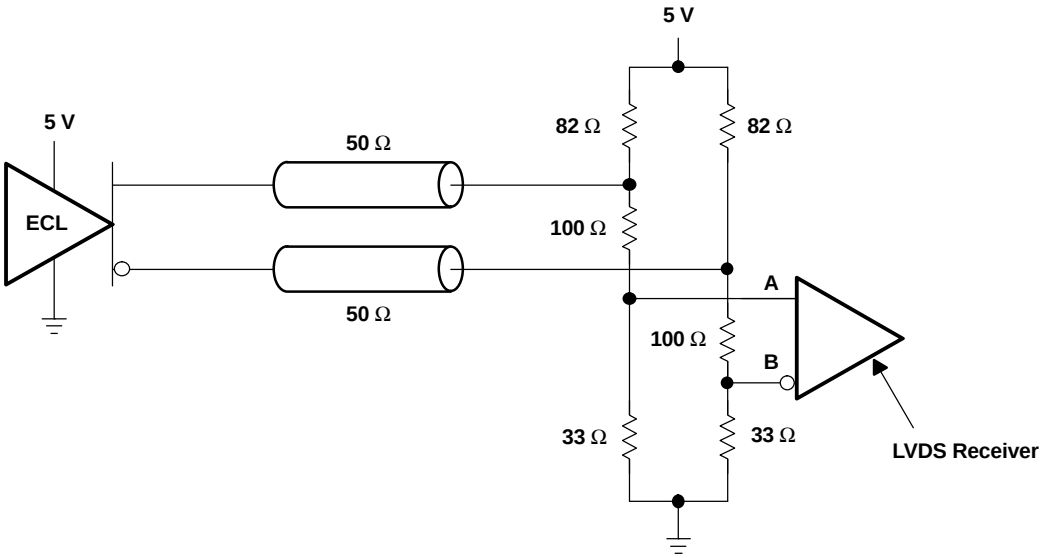



**Figure 28. Positive Emitter-Coupled Logic (PECL)**

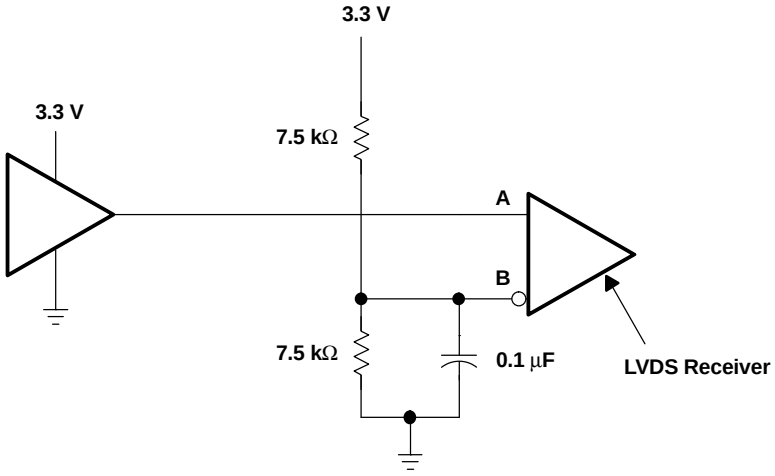



**Figure 29. 3.3-V CMOS**

## APPLICATION INFORMATION (continued)

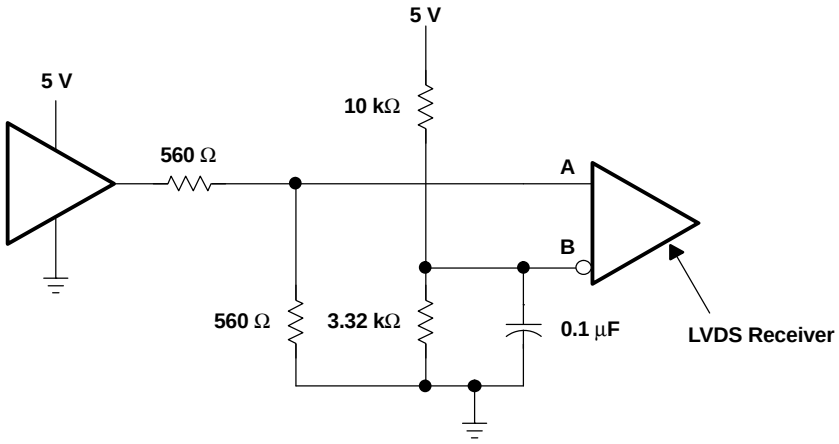



**Figure 30. 5-V CMOS**

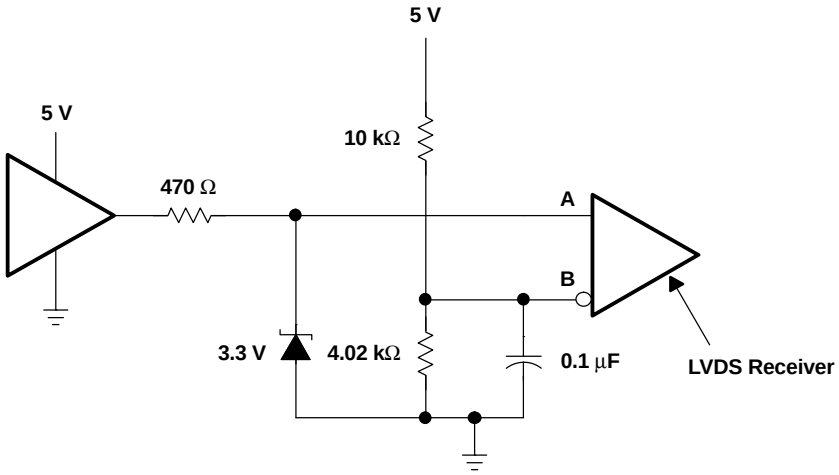



**Figure 31. 5-V TTL**

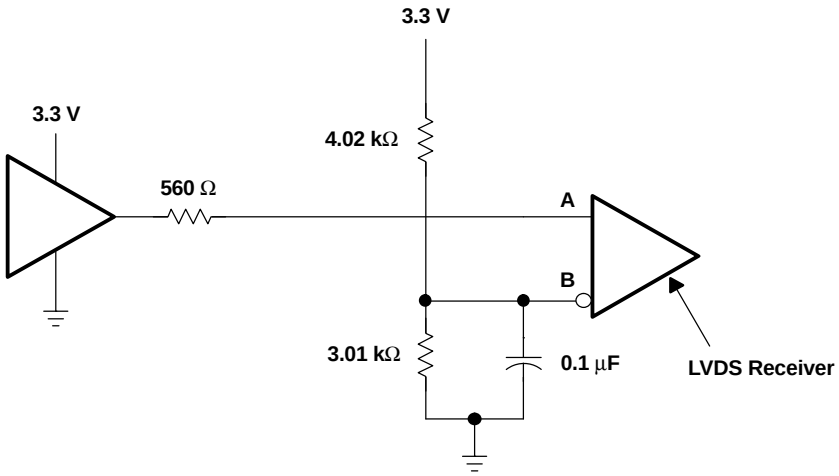



**Figure 32. LVTTL**

## APPLICATION INFORMATION (continued)

### FAIL SAFE

A common problem with differential signaling applications is how the system responds when no differential voltage is present on the signal pair. The LVDS receiver is like most differential line receivers, in that its output logic state can be indeterminate when the differential input voltage is between –100 mV and 100 mV and within its recommended input common-mode voltage range. Hovever, TI LVDS receivers handles the open-input circuit situation differently.

Open-circuit means that there is little or no input current to the receiver from the data line itself. This could be when the driver is in a high-impedance state or the cable is disconnected. When this occurs, the LVDS receiver pulls each line of the signal pair to near $V_{CC}$ through 300-kΩ resistors as shown in Figure 33. The fail-safe feature uses an AND gate with input voltage thresholds at about 2.3 V to detect this condition and force the output to a high-level regardless of the differential input voltage.

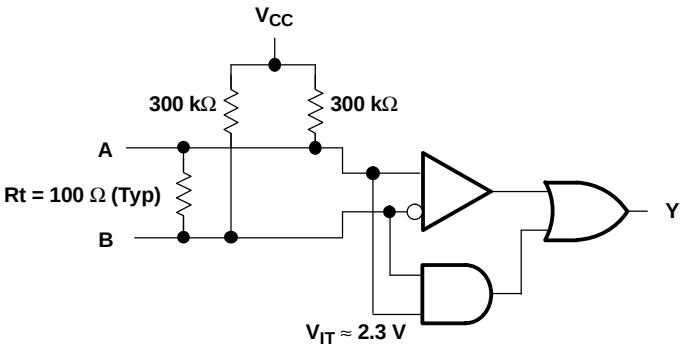



**Figure 33. Open-Circuit Fail Safe of the LVDS Receiver**

It is only under these conditions that the output of the receiver will be valid with less than a 100 mV differential input voltage magnitude. The presence of the termination resistor, Rt, does not affect the fail-safe function as long as it is connected as shown in Figure 33. Other termination circuits may allow a dc current to ground that could defeat the pullup currents from the receiver and the fail-safe feature.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) |
|---|---|---|---|---|---|---|---|---|
| SN65LVDS104D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS104DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS104DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS104DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS104PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS104PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS104PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS104PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS105D | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS105DG4 | ACTIVE | SOIC | D | 16 | 40 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS105DR | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS105DRG4 | ACTIVE | SOIC | D | 16 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS105PW | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS105PWG4 | ACTIVE | TSSOP | PW | 16 | 90 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS105PWR | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN65LVDS105PWRG4 | ACTIVE | TSSOP | PW | 16 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |

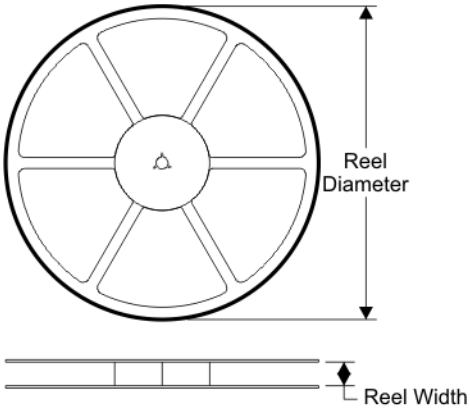
(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

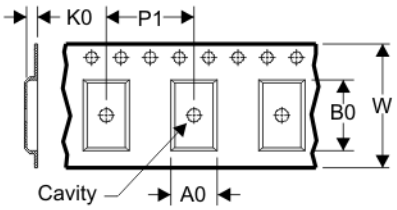
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

## TAPE AND REEL BOX INFORMATION

**REEL DIMENSIONS**

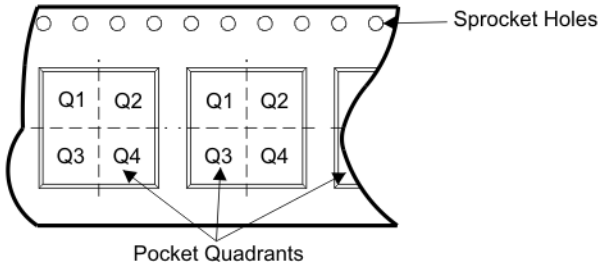



**TAPE DIMENSIONS**



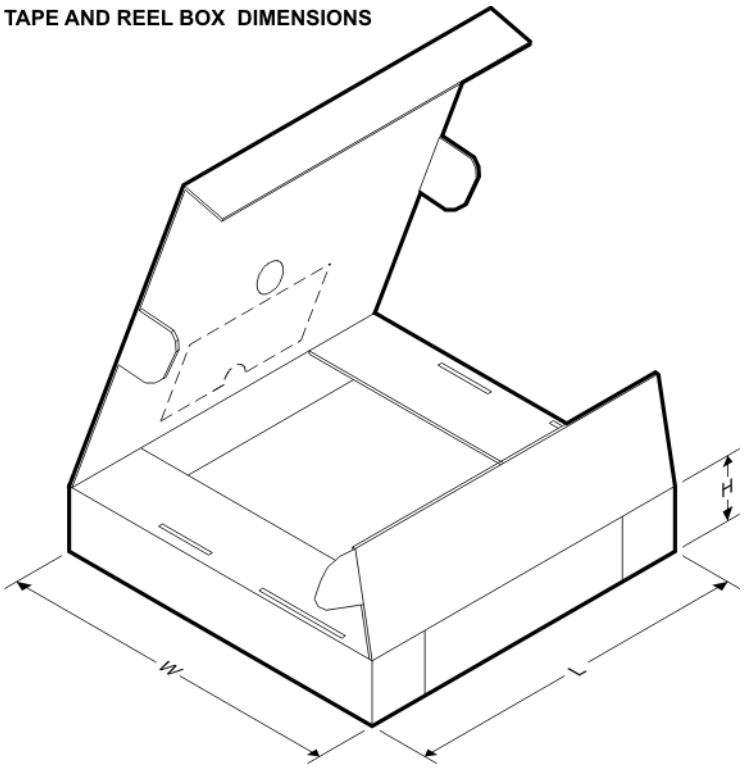

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



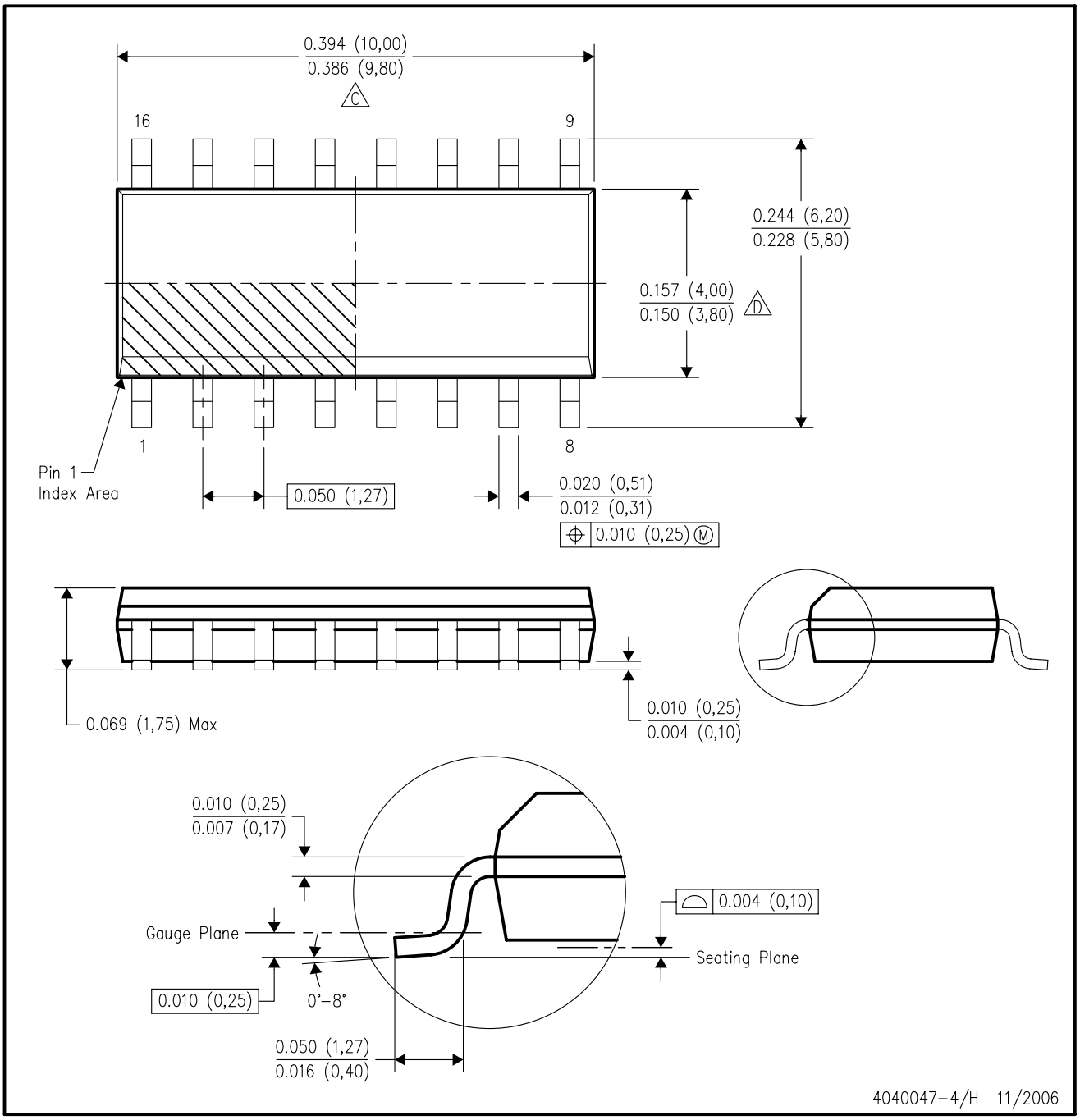

| Device | Package | Pins | Site | Reel Diameter (mm) | Reel Width (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65LVDS104DR | D | 16 | SITE 60 | 330 | 16 | 6.5 | 10.3 | 2.1 | 8 | 16 | Q1 |
| SN65LVDS104PWR | PW | 16 | SITE 41 | 330 | 12 | 7.0 | 5.6 | 1.6 | 8 | 12 | Q1 |
| SN65LVDS105DR | D | 16 | SITE 60 | 330 | 16 | 6.5 | 10.3 | 2.1 | 8 | 16 | Q1 |
| SN65LVDS105PWR | PW | 16 | SITE 41 | 330 | 12 | 7.0 | 5.6 | 1.6 | 8 | 12 | Q1 |

**TAPE AND REEL BOX DIMENSIONS**




| Device | Package | Pins | Site | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|
| SN65LVDS104DR | D | 16 | SITE 60 | 346.0 | 346.0 | 33.0 |
| SN65LVDS104PWR | PW | 16 | SITE 41 | 346.0 | 346.0 | 29.0 |
| SN65LVDS105DR | D | 16 | SITE 60 | 346.0 | 346.0 | 33.0 |
| SN65LVDS105PWR | PW | 16 | SITE 41 | 346.0 | 346.0 | 29.0 |

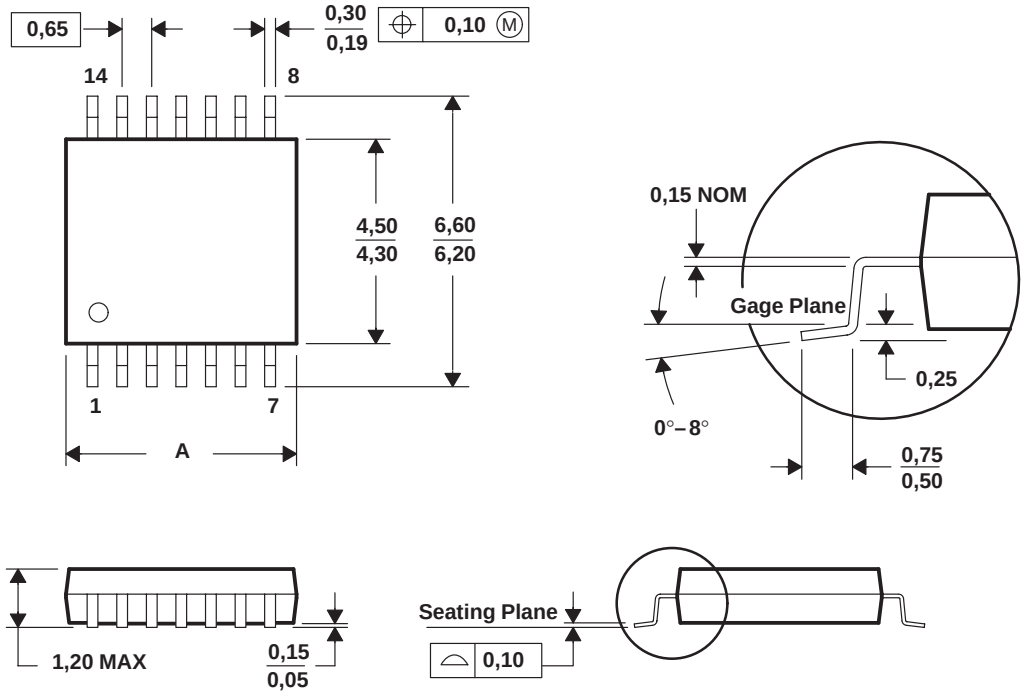
## D (R–PDSO–G16) PLASTIC SMALL–OUTLINE PACKAGE




NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AC.

**PW (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14 PINS SHOWN**




| DIM \ PINS ** | 8 | 14 | 16 | 20 | 24 | 28 |
|---|---|---|---|---|---|---|
| A MAX | 3,10 | 5,10 | 5,10 | 6,60 | 7,90 | 9,80 |
| A MIN | 2,90 | 4,90 | 4,90 | 6,40 | 7,70 | 9,60 |

**4040064/F 01/97**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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| Logic | logic.ti.com | Military | www.ti.com/military |
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| RFID | www.ti-rfid.com | Telephony | www.ti.com/telephony |
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