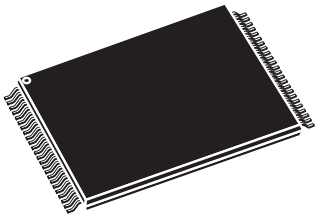
NAND01G-B2B
NAND02G-B2C

1-Gbit, 2-Gbit, 2112-byte/1056-word page, 1.8 V/3 V, NAND flash memory

Features

- High density NAND flash memories
  - Up to 2 Gbits of memory array
  - Cost effective solutions for mass storage applications
- NAND interface
  - x8 or x16 bus width
  - Multiplexed address/ data
  - Pinout compatibility for all densities
- Supply voltage: 1.8 V/3.0 V
- Page size
  - x8 device: (2048 + 64 spare) bytes
  - x16 device: (1024 + 32 spare) words
- Block size
  - x8 device: (128 K + 4 K spare) bytes
  - x16 device: (64 K + 2 K spare) words
- Page read/program
  - Random access: 25 µs (max)
  - Sequential access: 30 ns (min)
  - Page program time: 200 µs (typ)
- Copy back program mode
- Cache program and cache read modes
- Fast block erase: 2 ms (typ)
- Status register
- Electronic signature
- Chip enable ‘don’t care’



TSOP48 12 x 20 mm

VFBGA63 9.5 x 12 x 1 mm
VFBGA63 9 x 11 x 1 mm

- Serial number option
- Data protection
  - Hardware block locking
  - Hardware program/erase locked during power transitions
- Data integrity
  - 100 000 program/erase cycles per block (with ECC)
  - 10 years data retention
- ECOPACK® packages
- Development tools
  - Error correction code models
  - Bad blocks management and wear leveling algorithms
  - Hardware simulation models

Table 1. Device summary

Reference	Part number
NAND01G-B2B	NAND01GR3B2B, NAND01GW3B2B
	NAND01GR4B2B, NAND01GW4B2B(1)
NAND02G-B2C	NAND02GR3B2C, NAND02GW3B2C
	NAND02GR4B2C, NAND02GW4B2C(1)

1. x16 organization only available for MCP products.

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1 Description

NAND01G-B2B and NAND02G-B2C flash 2112-byte/1056-word page is a family of non-volatile flash memories that uses NAND cell technology. The devices range from 1 Gbit to 2 Gbits and operate with either a 1.8 V or 3 V voltage supply. The size of a page is either 2112 bytes (2048 + 64 spare) or 1056 words (1024 + 32 spare) depending on whether the device has a x8 or x16 bus width.

The address lines are multiplexed with the Data Input/Output signals on a multiplexed x8 or x16 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased over 100 000 cycles (with ECC on). To extend the lifetime of NAND flash devices it is strongly recommended to implement an error correction code (ECC).

The devices feature a write protect pin that allows performing hardware protection against program and erase operations.

The devices feature an open-drain ready/busy output that can be used to identify if the program/erase/read (P/E/R) controller is currently active. The use of an open-drain output allows the ready/busy pins from several memories to be connected to a single pull-up resistor.

A Copy Back Program command is available to optimize the management of defective blocks. When a page program operation fails, the data can be programmed in another page without having to resend the data to be programmed.

Each device has cache program and cache read features which improve the program and read throughputs for large files. During cache programming, the device loads the data in a cache register while the previous data is transferred to the page buffer and programmed into the memory array. During cache reading, the device loads the data in a cache register while the previous data is transferred to the I/O buffers to be read.

All devices have the chip enable don’t care feature, which allows code to be directly downloaded by a microcontroller, as chip enable transitions during the latency time do not stop the read operation.

All devices have the option of a unique identifier (serial number), which allows each device to be uniquely identified.

The unique identifier options is subject to an NDA (non disclosure agreement) and so not described in the datasheet. For more details of this option contact your nearest Numonyx sales office.

The devices are available in the following packages:

- TSOP48 (12 x 20 mm)
- VFBGA63 (9.5 x 12 x 1 mm, 0.8 mm pitch) for NAND02G-B2C devices
- VFBGA63 (9 x 11 x 1 mm, 0.8 mm pitch) for NAND01G-B2B devices.

For information on how to order these options refer to *Table 29: Ordering information scheme*. Devices are shipped from the factory with Block 0 always valid and the memory content bits, in valid blocks, erased to ’1’.

See *Table 2: Product description*, for all the devices available in the family.

Table 2. Product description

Reference	Part number	Density	Bus width	Page size	Block size	Memory array	Operating voltage	Timings				Package
								Random access time (max)	Sequential access time (min)	Page Program time (typ)	Block erase (typ)	
NAND01G-B2B	NAND01GR3B2B	1Gbit	x8	2048 +64 bytes	128K +4K bytes	64 pages x 1024 blocks	1.7 to 1.95 V	25 µs	50 ns	200 µs	2 ms	VFBGA63 9 x 11 mm
	NAND01GW3B2B						2.7 to 3.6 V	25 µs	30 ns			TSOP48
	NAND01GR4B2B		x16	1024 +32 words	64K+ 2K words		1.7 to 1.95 V	25 µs	50 ns			(1)
	NAND01GW4B2B						2.7 to 3.6 V	25 µs	30 ns			(1)
NAND02G-B2C	NAND02GR3B2C	2Gbits	x8	2048 +64 bytes	128K +4K bytes	64 pages x 2048 blocks	1.7 to 1.95 V	25 µs	50 ns		2 ms	VFBGA63 9.5 x 12 mm
	NAND02GW3B2C						2.7 to 3.6 V	25 µs	30 ns			TSOP48
	NAND02GR4B2C		x16	1024 +32 words	64K+ 2K words		1.7 to 1.95 V	25 µs	50 ns			(1)
	NAND02GW4B2C						2.7 to 3.6 V	25 µs	30 ns			(1)

1. x16 organization only available for MCP.

Figure 1. Logic block diagram

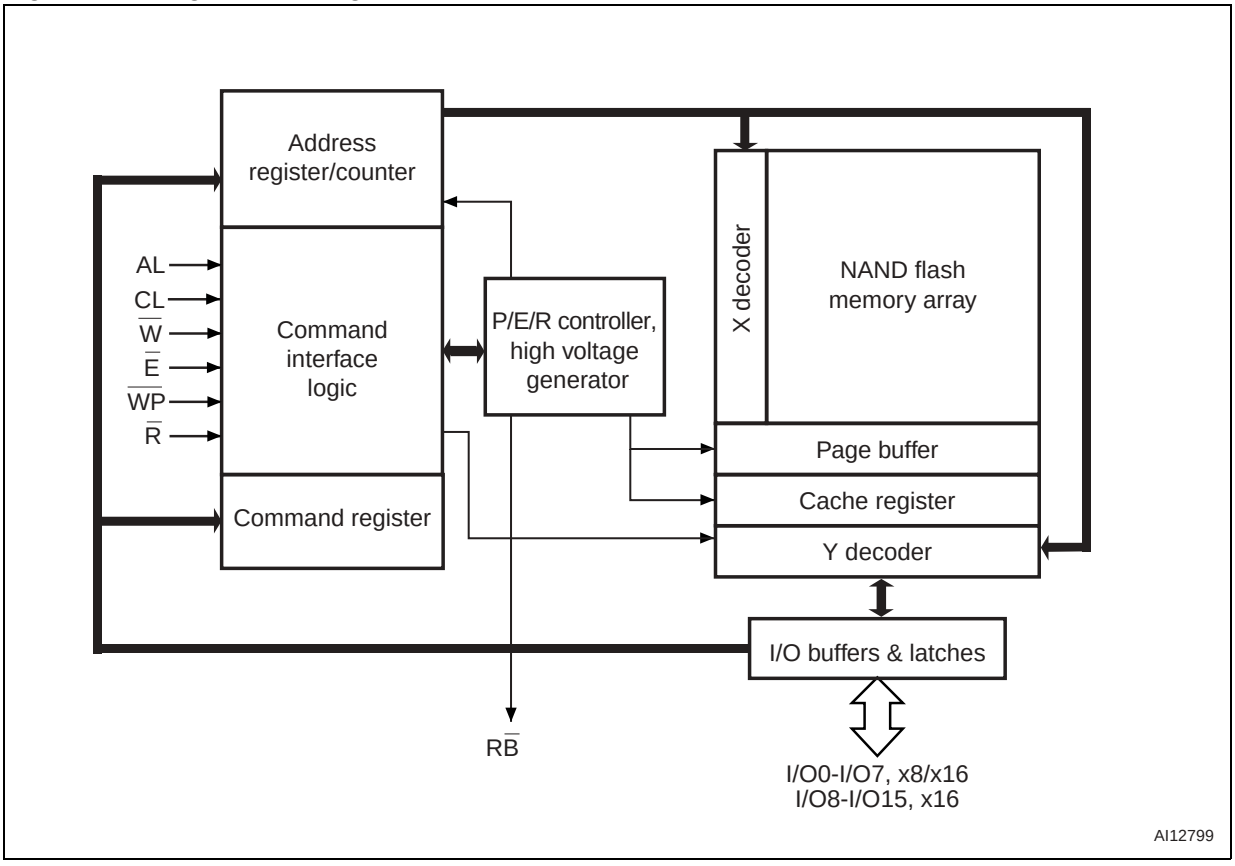
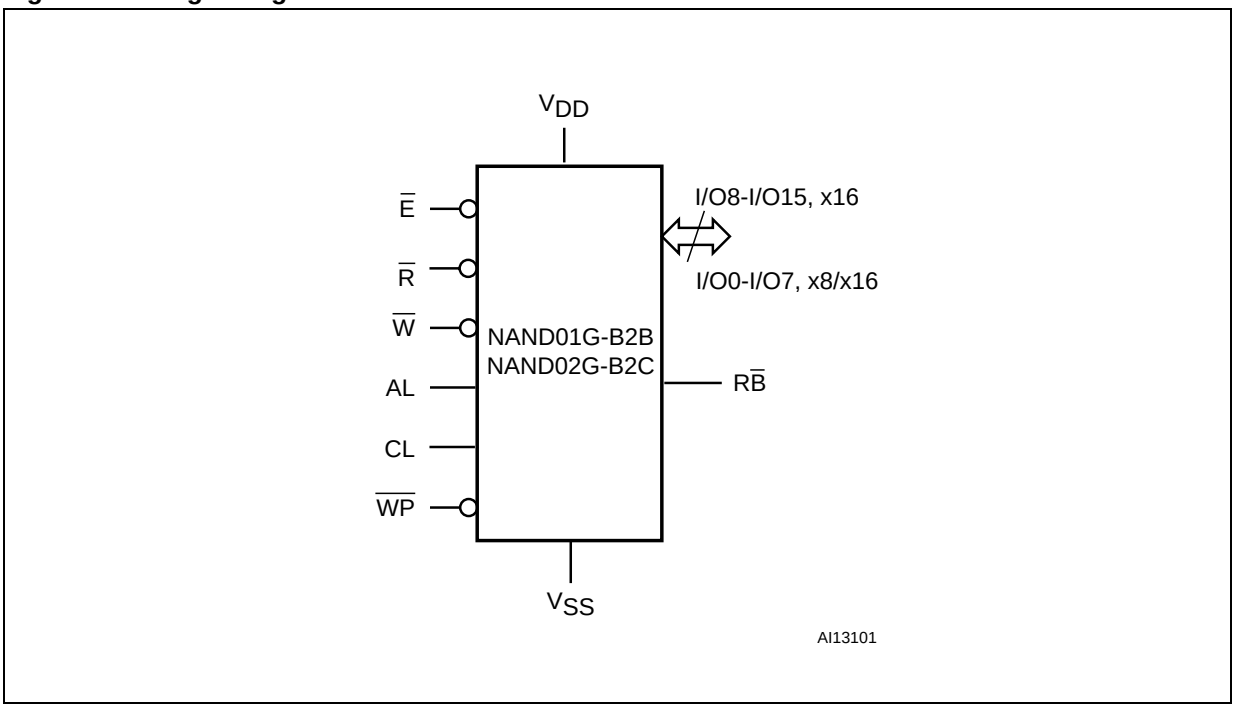


Figure 2. Logic diagram

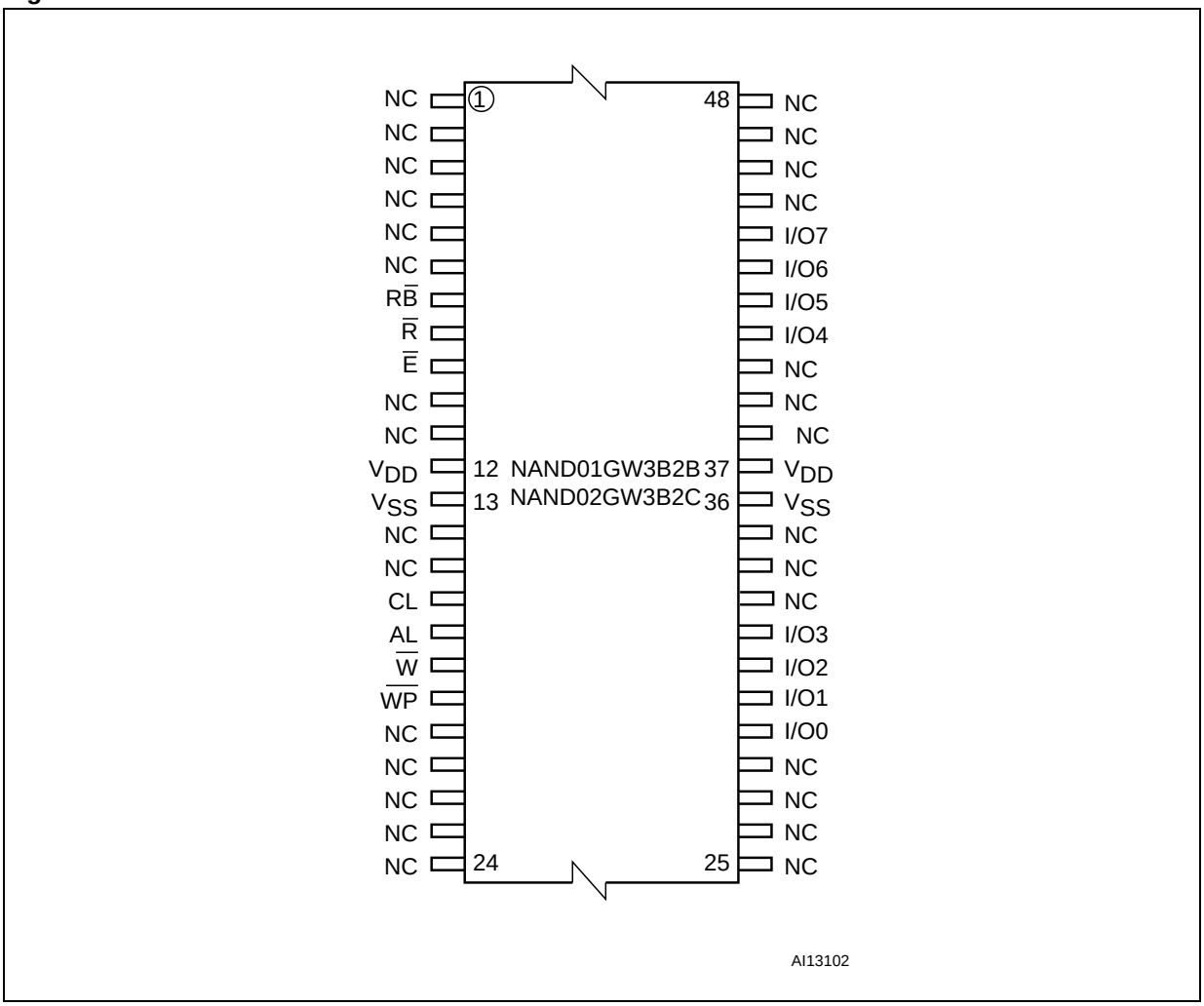


1. x16 organization only available for MCP.

Table 3. Signal names

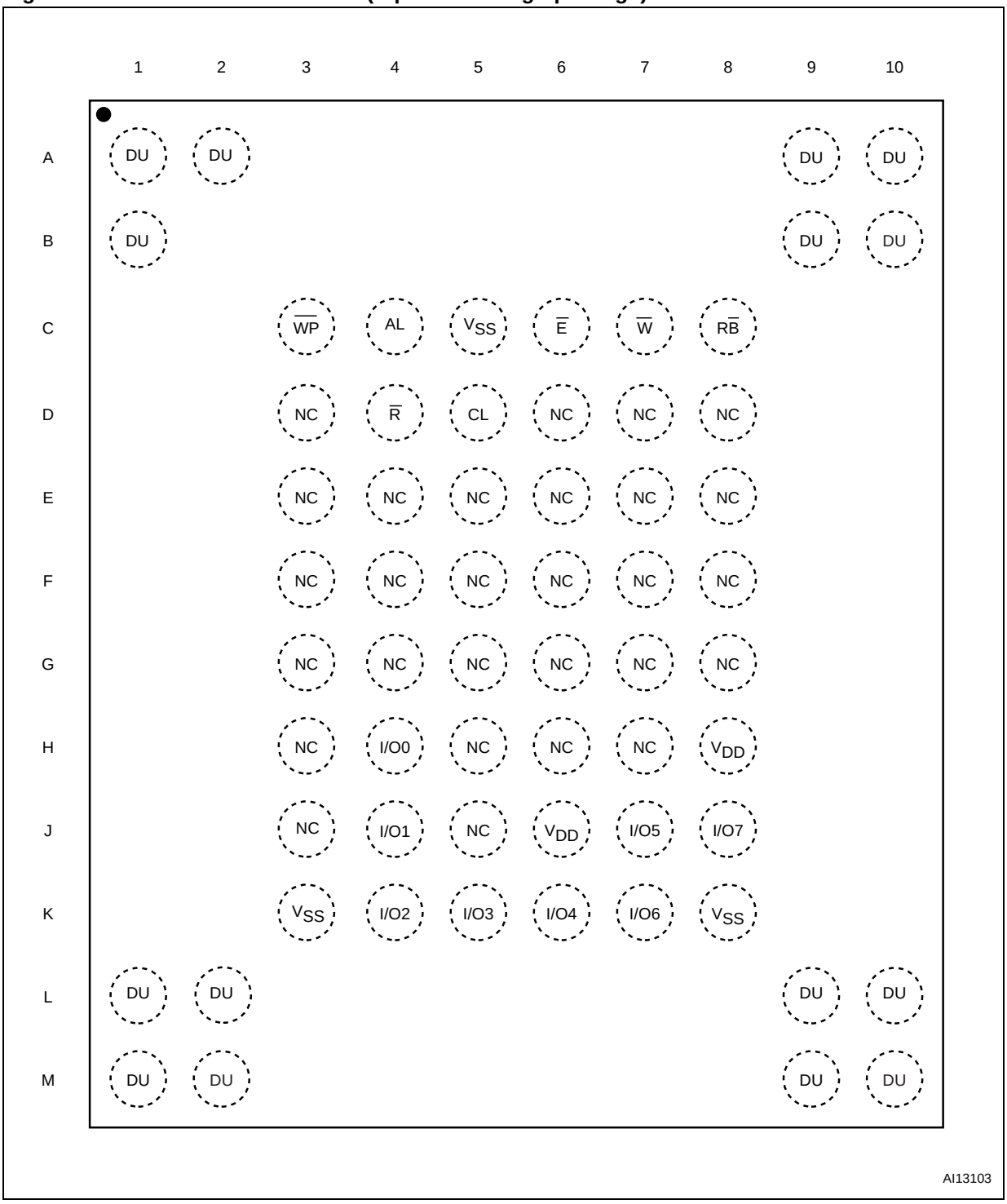
Signal	Function	Direction
I/O8-15	Data input/outputs for x16 devices	I/O
I/O0-7	Data input/outputs, address inputs, or command inputs for x8 and x16 devices	I/O
AL	Address Latch Enable	Input
CL	Command Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$R\overline{B}$	Ready/Busy (open-drain output)	Output
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
V_{DD}	Supply voltage	Supply
V_{SS}	Ground	Supply
NC	Not connected internally	–
DU	Do not use	–

Figure 3. TSOP48 connections



1. Available only for NAND01GW3B2B and NAND02GW3B2C 8-bit devices.

Figure 4. VFBGA63 connections (top view through package)



1. Available only for NAND01GR3B2B and NAND02GR3B2C 8-bit devices.

2 Memory array organization

The memory array is made up of NAND structures where 32 cells are connected in series.

The memory array is organized in blocks where each block contains 64 pages. The array is split into two areas, the main area and the spare area. The main area of the array is used to store data whereas the spare area is typically used to store error correction codes, software flags or bad block identification.

In x8 devices the pages are split into a 2048-byte main area and a spare area of 64 bytes. In the x16 devices the pages are split into a 1,024-word main area and a 32-word spare area. Refer to *Figure 5: Memory array organization*.

2.1 Bad blocks

The NAND flash 2112-byte/1056-word page devices may contain bad blocks, that is blocks that contain one or more invalid bits whose reliability is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block Information is written prior to shipping (refer to *Section 8.1: Bad block management* for more details).

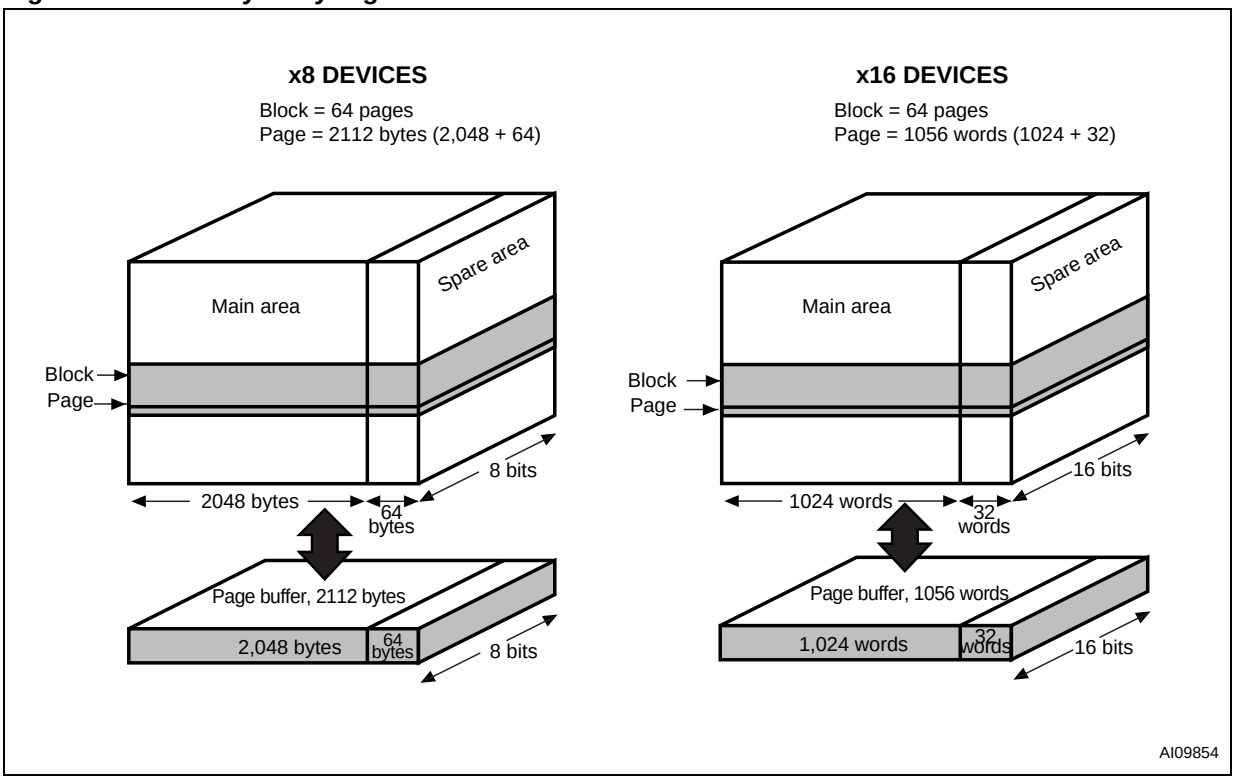
Table 4: Valid blocks shows the minimum number of valid blocks in each device. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

These blocks need to be managed using bad blocks management, block replacement or error correction codes (refer to *Section 8: Software algorithms*).

Table 4. Valid blocks

Density of device	Min	Max
2 Gbits	2008	2048
1 Gbit	1004	1024

Figure 5. Memory array organization



3 Signals description

See *Figure 2: Logic diagram*, and *Table 3: Signal names*, for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used to input the selected address, output the data during a read operation or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Inputs/outputs (I/O8-I/O15)

Input/outputs 8 to 15 are only available in x16 devices. They are used to output the data during a read operation or input data during a write operation. Command and address Inputs only require I/O0 to I/O7.

The inputs are latched on the rising edge of Write Enable. I/O8-I/O15 are left floating when the device is deselected or the outputs are disabled.

3.3 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

3.4 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

3.5 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, v_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.6 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.7 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the command interface, input address and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.8 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.9 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can be used to identify if the P/E/R controller is currently active. When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low will then indicate that one, or more, of the memories is busy.

Refer to the *Section 11.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

During power-up and power-down a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the $R\overline{B}$ signal is Low, V_{OL}.

3.10 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 22* and *Table 23*) to protect the device from any involuntary program/erase during power-transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.11 V_{SS} ground

Ground, V_{SS}, is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section, see *Table 5: Bus operations*, for a summary.

Typically, glitches of less than 5 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command input

Command input bus operations are used to give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 19* and *Table 24* for details of the timings requirements.

4.2 Address input

Address input bus operations are used to input the memory addresses. Four bus cycles are required to input the addresses for 1-Gbit devices whereas five bus cycles are required for the 2-Gbit device (refer to *Table 6* and *Table 7*, Address insertion).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See *Figure 20* and *Table 24* for details of the timings requirements.

4.3 Data input

Data input bus operations are used to input the data to be programmed.

Data is accepted only when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 21* and *Table 24* and *Table 25* for details of the timings requirements.

4.4 Data output

Data output bus operations are used to read: the data in the memory array, the status register, the lock status, the electronic signature and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low. The data is output sequentially using the Read Enable signal.

See *Figure 22* and *Table 25* for details of the timings requirements.

4.5 Write Protect

Write Protect bus operations are used to protect the memory against program or erase operations. When the Write Protect signal is Low the device will not accept program or erase operations and so the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection even during power-up.

4.6 Standby

When Chip Enable is High the memory enters standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 5. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7	I/O8 - I/O15(1)
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(2)	Command	X
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address	X
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data input	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output	Data output
Write Protect	X	X	X	X	X	V_{IL}	X	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X	X

1. Only for x16 devices.
2. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 6. Address insertion, x8 devices

Bus cycle(1)	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A11	A10	A9	A8
3rd	A19	A18	A17	A16	A15	A14	A13	A12
4th	A27	A26	A25	A24	A23	A22	A21	A20
5th(2)	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A28

1. Any additional address input cycles will be ignored.
2. The fifth cycle is valid for 2-Gbit devices. A28 is for 2-Gbit devices only.

Table 7. Address insertion, x16 devices

Bus cycle(1)	I/O8-I/O15	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	X	A7	A6	A5	A4	A3	A2	A1	A0
2nd	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A10	A9	A8
3rd	X	A18	A17	A16	A15	A14	A13	A12	A11
4th	X	A26	A25	A24	A23	A22	A21	A20	A19
5th(2)	X	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A27

1. Any additional address input cycles will be ignored.
2. The fifth cycle is valid for 2-Gbit devices. A27 is for 2-Gbit devices only.

Table 8. Address definitions, x8

Address	Definition	
A0 - A11	Column address	
A12 - A17	Page address	
A18 - A27	Block address	1-Gbit device
A18 - A28	Block address	2-Gbit device

Table 9. Address definitions, x16

Address	Definition	
A0 - A10	Column address	
A11 - A16	Page address	
A17 - A26	Block address	1-Gbit device
A17 - A27	Block address	2-Gbit device

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is High. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The commands are summarized in *Table 10: Commands*.

Table 10. Commands

Command	Bus write operations(1)				Commands accepted during busy
	1st cycle	2nd cycle	3rd cycle	4th cycle	
Read	00h	30h	–	–	
Random Data Output	05h	E0h	–	–	
Cache Read	00h	31h	–	–	
Exit Cache Read	34h	–	–	–	Yes(2)
Page Program (Sequential Input default)	80h	10h	–	–	
Random Data Input	85h	–	–	–	
Copy Back Program	00h	35h	85h	10h	
Cache Program	80h	15h	–	–	
Block Erase	60h	D0h	–	–	
Reset	FFh	–	–	–	Yes
Read Electronic Signature	90h	–	–	–	
Read Status Register	70h	–	–	–	Yes

1. The bus cycles are only shown for issuing the codes. The cycles required to input the addresses or input/output data are not shown.
2. Only during Cache Read busy.

6 Device operations

The following section gives the details of the device operations.

6.1 Read memory array

At power-up the device defaults to read mode. To enter read mode from another mode the Read command must be issued, see *Table 10: Commands*.

Once a Read command is issued two types of operations are available: random read and page read.

6.1.1 Random read

Each time the Read command is issued the first read is random read.

6.1.2 Page read

After the first random read access, the page data (2112 bytes or 1056 words) is transferred to the page buffer in a time of t_{WHBH} (refer to *Table 25* for value). Once the transfer is complete the Ready/Busy signal goes High. The data can then be read out sequentially (from selected column address to last column address) by pulsing the Read Enable signal.

The device can output random data in a page, instead of the consecutive sequential data, by issuing a Random Data Output command.

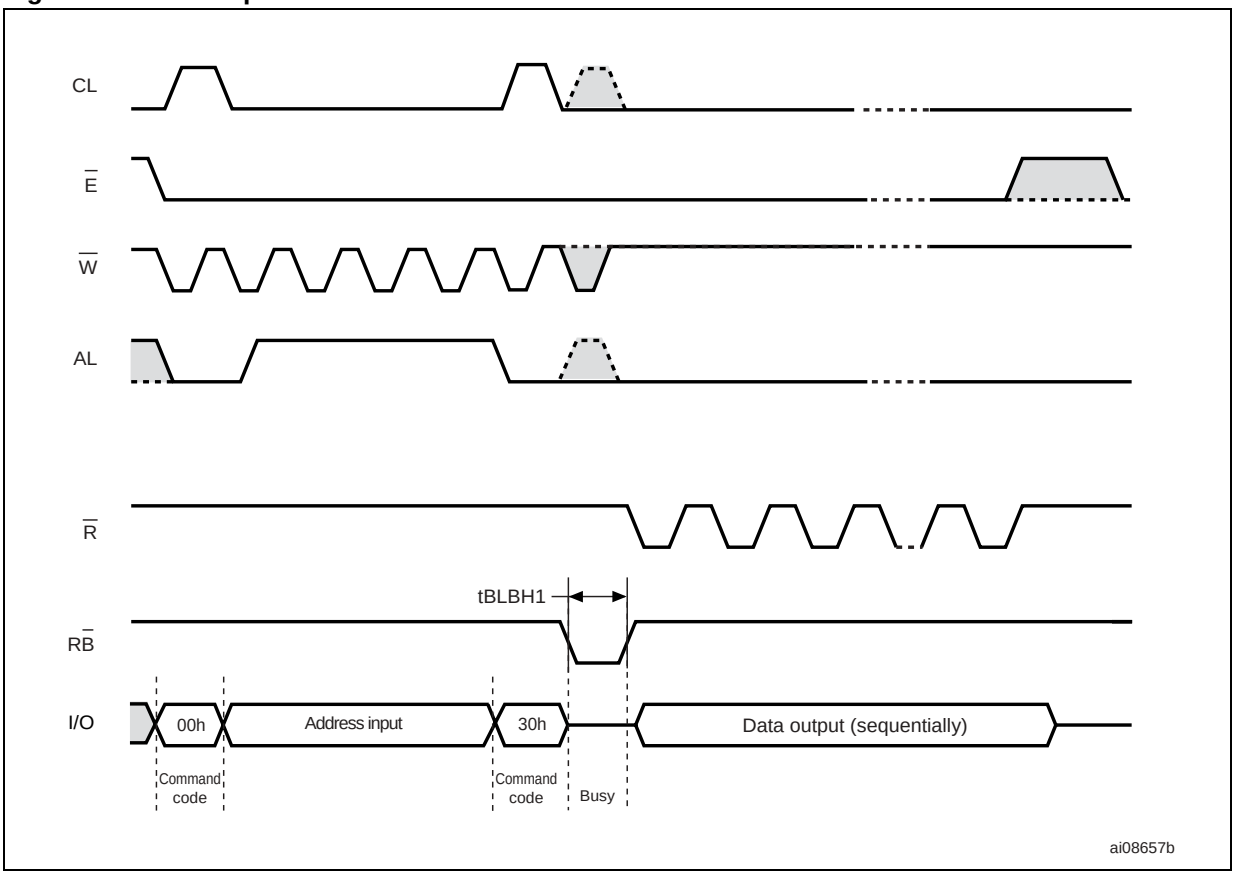
The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command.

The Random Data Output command can be issued as many times as required within a page.

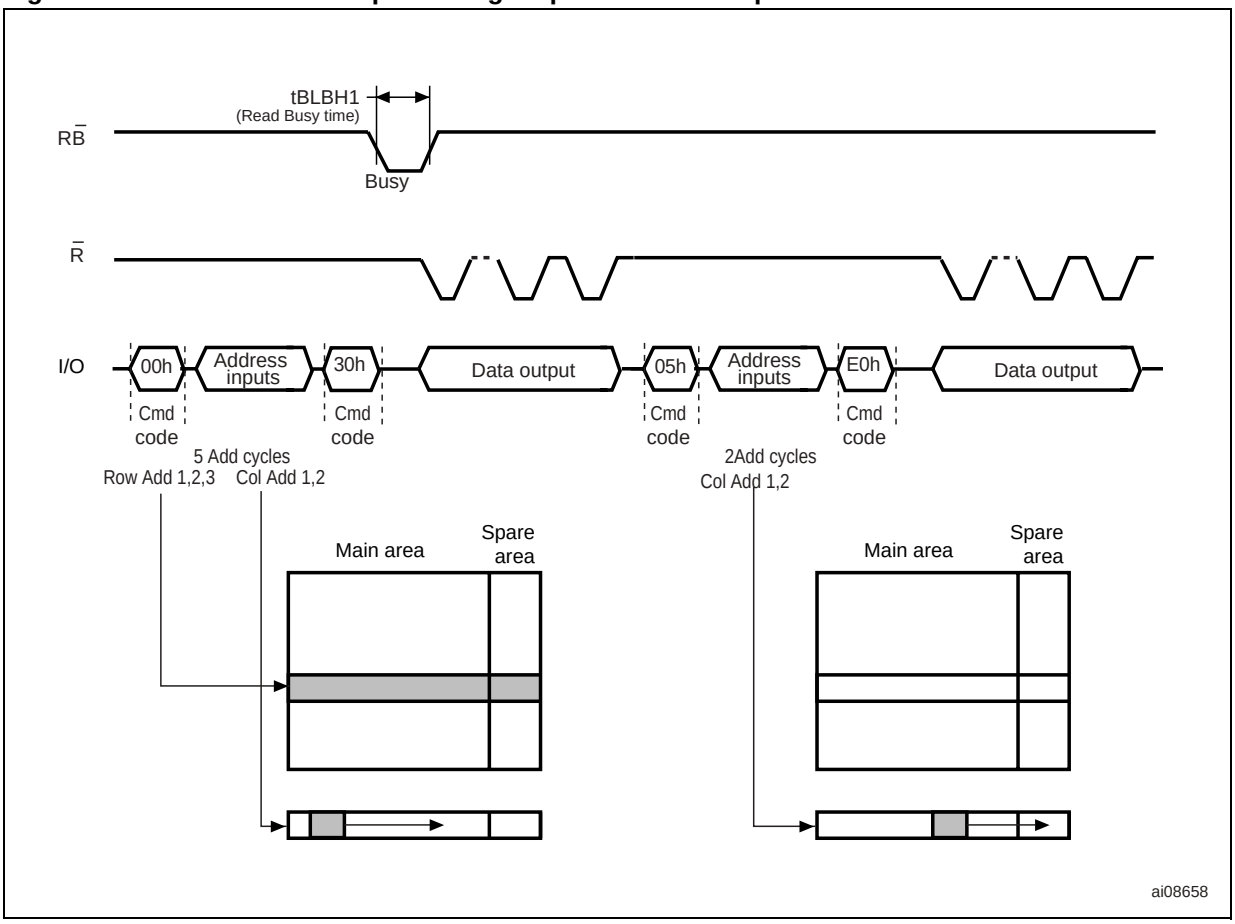
The Random Data Output command is not accepted during cache read operations.

Figure 6. Read operations



1. Highest address depends on device density.

Figure 7. Random data output during sequential data output



6.2 Cache read

The cache read operation is used to improve the read throughput by reading data using the cache register. As soon as the user starts to read one page, the device automatically loads the next page into the cache register.

A cache read operation consists of three steps (see *Table 10: Commands*):

1. One bus cycle is required to setup the Cache Read command (the same as the standard Read command)
2. Four or five (refer to *Table 6* and *Table 7*) bus cycles are then required to input the start address
3. One bus cycle is required to issue the Cache Read Confirm command to start the P/E/R controller.

The start address must be at the beginning of a page (column address = 00h, see *Table 8* and *Table 9*). This allows the data to be output uninterrupted after the latency time (t_{BLBH1}), see *Figure 8*.

The Ready/Busy signal can be used to monitor the start of the operation. During the latency period the Ready/Busy signal goes Low, after this the Ready/Busy signal goes High, even if the device is internally downloading page n+1.

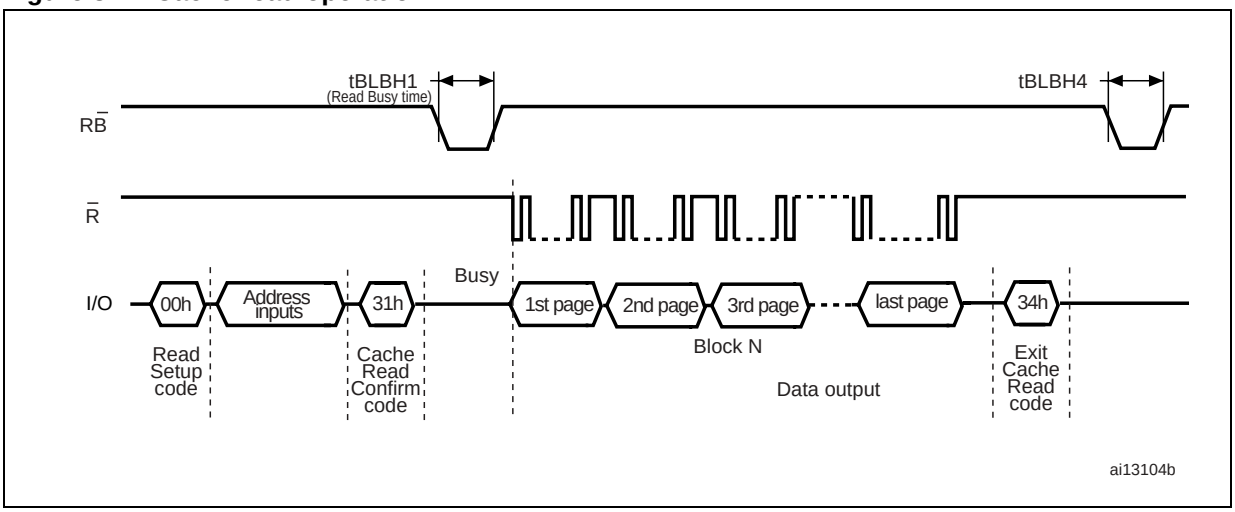
Once the cache read operation has started, the status register can be read using the Read Status Register command.

During the operation, SR5 can be read, to find out whether the internal reading is ongoing (SR5 = '0'), or has completed (SR5 = '1'), while SR6 indicates whether the cache register is ready to download new data.

To exit the cache read operation an Exit Cache Read command must be issued (see *Table 10*).

If the Exit Cache Read command is issued while the device is internally reading page n+1, pages n and n+1 will not be output.

Figure 8. Cache read operation



6.3 Page program

The page program operation is the standard operation to program data to the memory array. Generally, the page is programmed sequentially, however the device does support random input within a page. It is recommended to address pages sequentially within a given block.

The memory array is programmed by page, however partial page programming is allowed where any number of bytes (1 to 2112) or words (1 to 1056) can be programmed.

The maximum number of consecutive partial page program operations allowed in the same page is four. After exceeding this a Block Erase command must be issued before any further program operations can take place in that page.

6.3.1 Sequential input

To input data sequentially the addresses must be sequential and remain in one block.

For sequential input each page program operation consists of five steps (see *Figure 9*):

1. one bus cycle is required to setup the Page Program (sequential input) command (see *Table 10*)
2. four or five bus cycles are then required to input the program address (refer to *Table 6* and *Table 7*)
3. the data is then loaded into the data registers
4. one bus cycle is required to issue the Page Program Confirm command to start the P/E/R controller. The P/E/R will only start if the data has been loaded in step 3
5. the P/E/R controller then programs the data into the array.

6.3.2 Random data input in a page

During a sequential input operation, the next sequential address to be programmed can be replaced by a random address, by issuing a Random Data Input command. The following two steps are required to issue the command:

1. one bus cycle is required to setup the Random Data Input command (see *Table 10*)
2. two bus cycles are then required to input the new column address (refer to *Table 6*).

Random Data Input can be repeated as often as required in any given page.

Once the program operation has started the status register can be read using the Read Status Register command. During program operations the status register will only flag errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High.

The device remains in read status register mode until another valid command is written to the command interface.

Figure 9. Page program operation

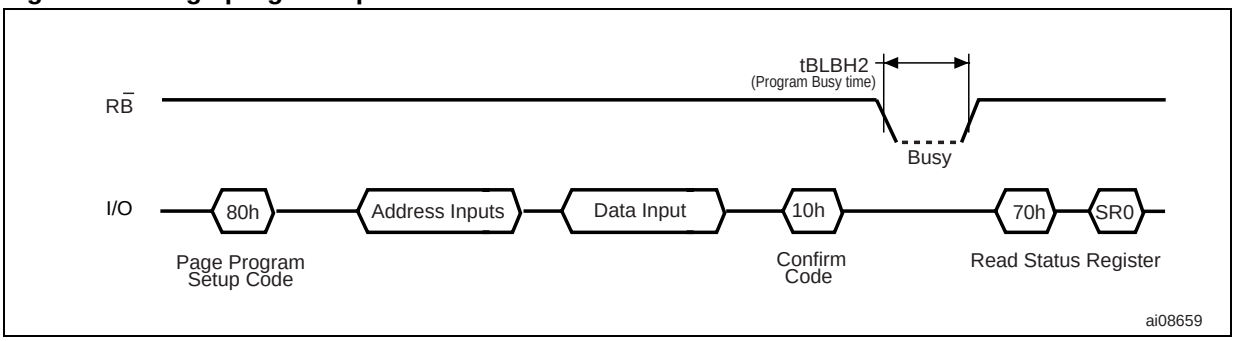
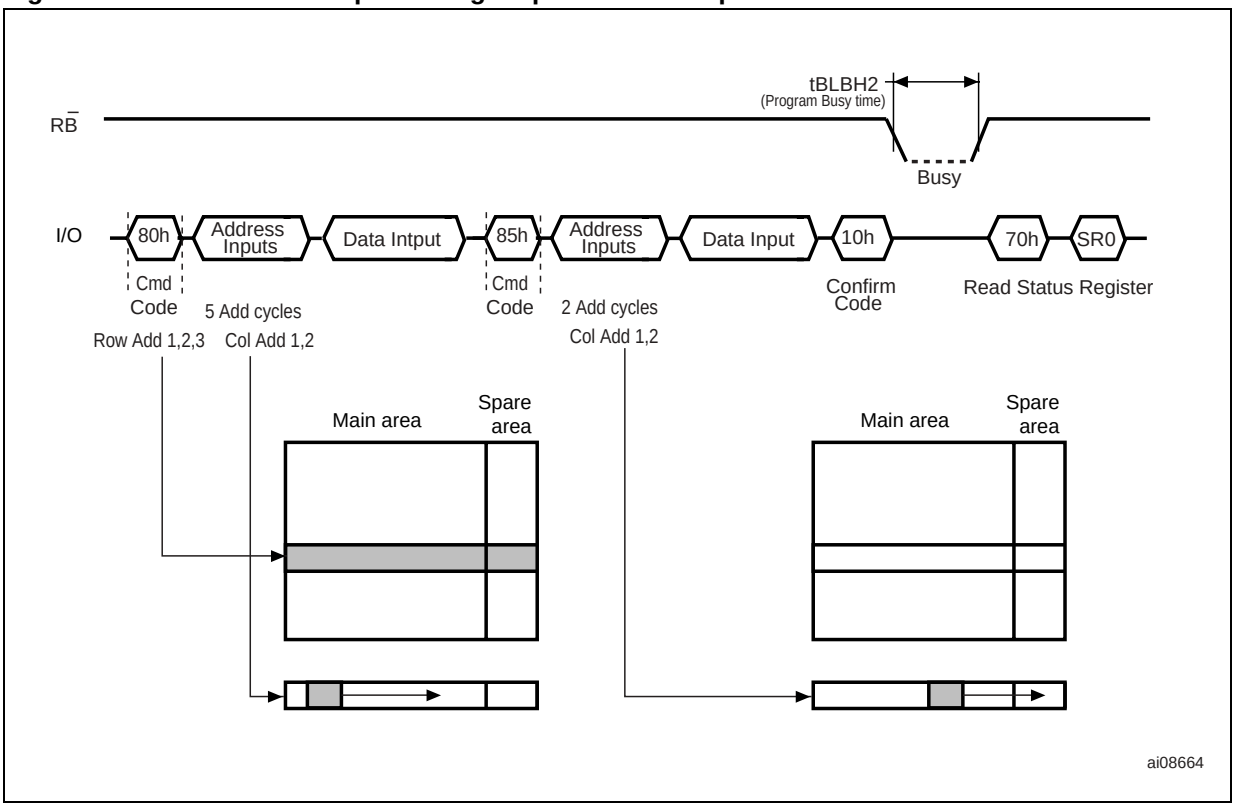


Figure 10. Random data input during sequential data input



6.4 Copy back program

The copy back program operation is used to copy the data stored in one page and reprogram it in another page.

The copy back program operation does not require external memory and so the operation is faster and more efficient because the reading and loading cycles are not required. The operation is particularly useful when a portion of a block is updated and the rest of the block needs to be copied to the newly assigned block.

If the copy back program operation fails an error is signalled in the status register. However as the standard external ECC cannot be used with the copy back program operation bit error due to charge loss cannot be detected. For this reason it is recommended to limit the number of copy back program operations on the same data and or to improve the performance of the ECC.

The copy back program operation requires four steps:

1. The first step reads the source page. The operation copies all 1056 words/ 2112 bytes from the page into the data buffer. It requires:
   - one bus write cycle to setup the command
   - 4 or 5 bus write cycles to input the source page address (see *Table 6* and *Table 7*)
   - one bus write cycle to issue the confirm command code
2. When the device returns to the ready state (Ready/Busy High), the next bus write cycle of the command is given with the 4 or 5 bus cycles to input the target page address (see *Table 6* and *Table 7*). Refer to *Table 11* for the addresses that must be the same for the source and target pages
3. Then the confirm command is issued to start the P/E/R controller.

To see the data input cycle for modifying the source page and an example of the copy back program operation refer to *Figure 11*.

A data input cycle to modify a portion or a multiple distant portion of the source page, is shown in *Figure 12*.

Table 11. Copy back program x8 addresses

Density	Same address for source and target pages
1 Gbit	no constraint
2 Gbits	A28

Table 12. Copy back program x16 addresses

Density	Same address for source and target pages
1 Gbit	no constraint
2 Gbits	A27

Figure 11. Copy back program

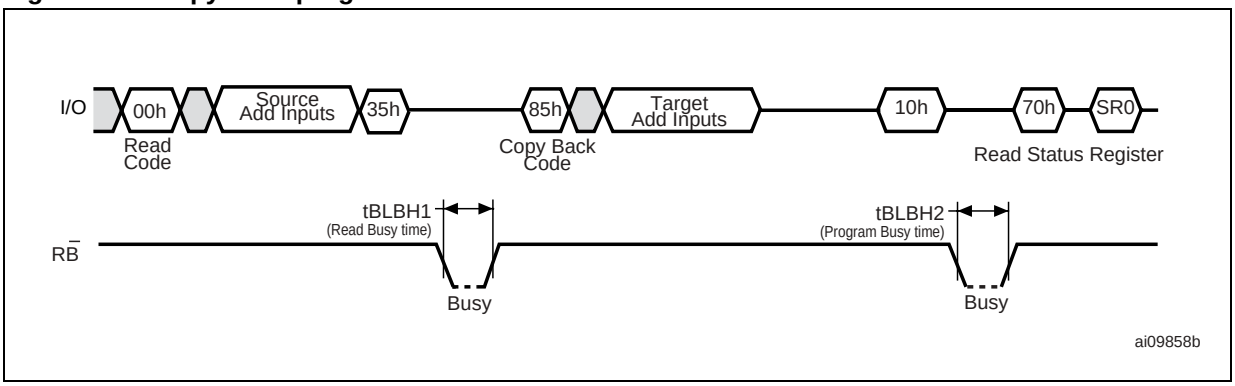
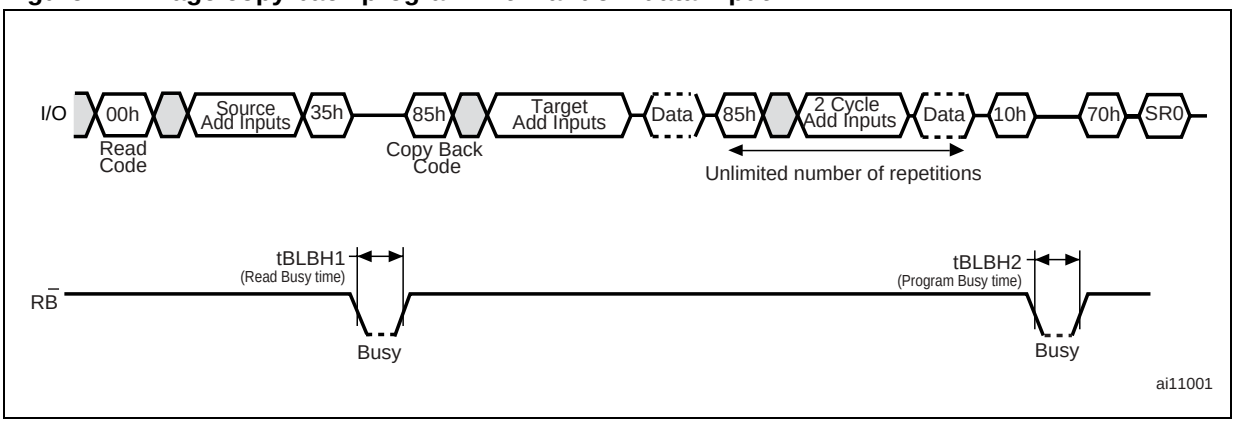


Figure 12. Page copy back program with random data input



6.5 Cache program

The cache program operation is used to improve the programming throughput by programming data using the cache register. The cache program operation can only be used within one block. The cache register allows new data to be input while the previous data that was transferred to the page buffer is programmed into the memory array.

The following sequence is required to issue a cache program operation (refer to *Figure 13*):

1. First of all the program setup command is issued: one bus cycle to issue the program setup command then 4 or 5 bus write cycles to input the address (see *Table 6* and *Table 7*). The data is then input (up to 2112 bytes/1056 words) and loaded into the cache register
2. One bus cycle is required to issue the confirm command to start the P/E/R controller
3. The P/E/R controller then transfers the data to the page buffer. During this the device is busy for a time of t_{BLBH5}
4. Once the data is loaded into the page buffer the P/E/R controller programs the data into the memory array. As soon as the cache registers are empty (after t_{BLBH5}) a new Cache Program command can be issued, while the internal programming is still executing.

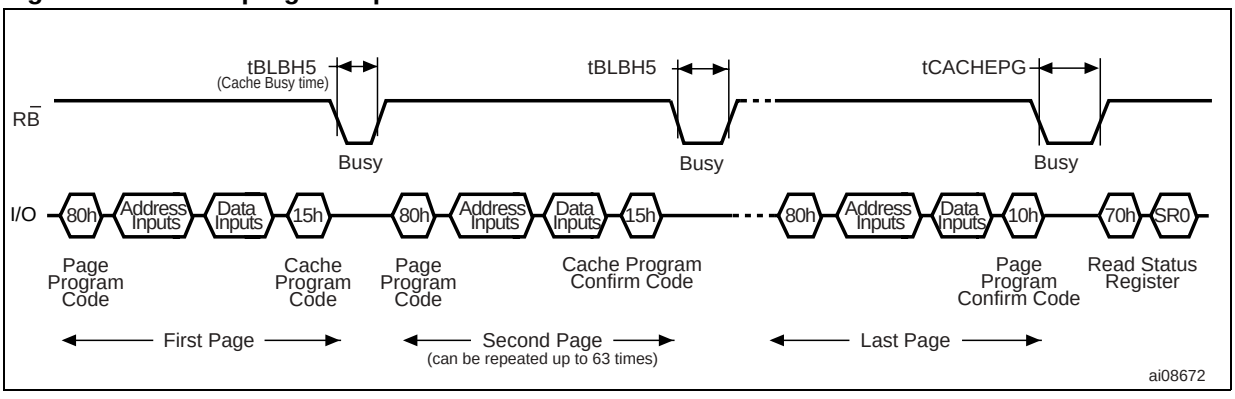
Once the program operation has started the status register can be read using the Read Status Register command. During cache program operations SR5 can be read to find out whether the internal programming is ongoing (SR5 = ‘0’) or has completed (SR5 = ‘1’) while SR6 indicates whether the cache register is ready to accept new data. If any errors have been detected on the previous page (Page N-1), the cache program error bit SR1 will be set to ‘1', while if the error has been detected on page N the error bit SR0 will be set to '1’.

When the next page (Page N) of data is input with the Cache Program command, t_{BLBH5} is affected by the pending internal programming. The data will only be transferred from the cache register to the page buffer when the pending program cycle is finished and the page buffer is available.

If the system monitors the progress of the operation using only the Ready/Busy signal, the last page of data must be programmed with the Page Program Confirm command (10h).

If the Cache Program Confirm command (15h) is used instead, status register bit SR5 must be polled to find out if the last programming is finished before starting any other operations.

Figure 13. Cache program operation



1. Up to 64 pages can be programmed in one cache program operation.
2. $t_{CACHEPG}$ is the program time for the last page + the program time for the (last – 1)th page – (Program command cycle time + Last page data loading time).

6.6 Block erase

Erase operations are done one block at a time. An erase operation sets all of the bits in the addressed block to ‘1’. All previous data in the block is lost.

An erase operation consists of three steps (refer to *Figure 14*):

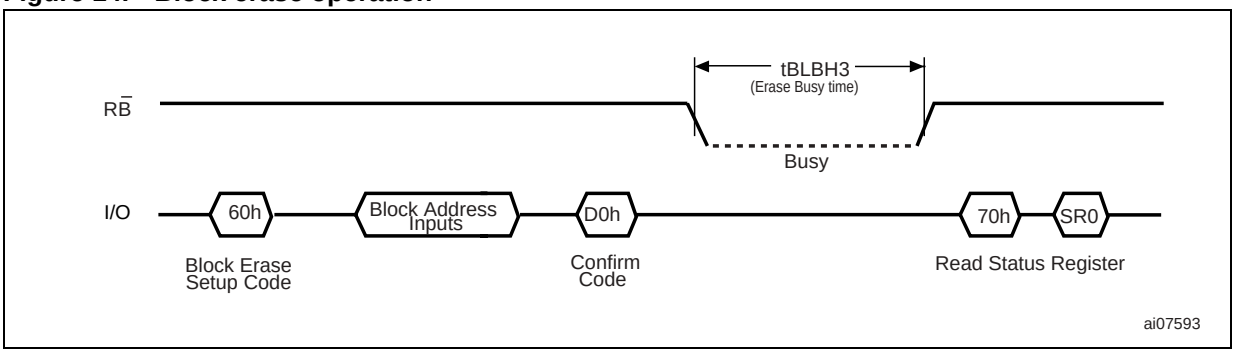
1. One bus cycle is required to setup the Block Erase command. Only addresses A18-A28 (x8) or A17-A27 (x16) are used, the other address inputs are ignored
2. Two or three bus cycles are then required to load the address of the block to be erased. Refer to *Table 8* and *Table 9* for the block addresses of each device
3. One bus cycle is required to issue the Block Erase Confirm command to start the P/E/R controller.

The operation is initiated on the rising edge of write Enable, $\overline{W}$, after the Confirm command is issued. The P/E/R controller handles block erase and implements the verify process.

During the block erase operation, only the Read Status Register and Reset commands will be accepted, all other commands will be ignored.

Once the program operation has completed the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High. If the operation completed successfully, the write status bit SR0 is ‘0’, otherwise it is set to ‘1’.

Figure 14. Block erase operation



6.7 Reset

The Reset command is used to reset the command interface and status register. If the Reset command is issued during any operation, the operation will be aborted. If it was a program or erase operation that was aborted, the contents of the memory locations being modified will no longer be valid as the data will be partially programmed or erased.

If the device has already been reset then the new Reset command will not be accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued, refer to *Table 25: AC characteristics for operations* for the values.

6.8 Read status register

The device contains a status register which provides information on the current or previous program or erase operation. The various bits in the status register convey information and errors on the operation.

The status register is read by issuing the Read Status Register command. The status register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the status register.

After the Read Status Register command has been issued, the device remains in read status register mode until another command is issued. Therefore if a Read Status Register command is issued during a random read cycle a new Read command must be issued to continue with a page read operation.

The Status Register bits are summarized in *Table 13: Status register bits*,. Refer to *Table 13* in conjunction with the following text descriptions.

6.8.1 Write protection bit (SR7)

The write protection bit can be used to identify if the device is protected or not. If the write protection bit is set to ‘1’ the device is not protected and program or erase operations are allowed. If the write protection bit is set to ‘0’ the device is protected and program or erase operations are not allowed.

6.8.2 P/E/R controller and cache ready/busy bit (SR6)

Status register bit SR6 has two different functions depending on the current operation.

During cache program operations SR6 acts as a cache program ready/busy bit, which indicates whether the cache register is ready to accept new data. When SR6 is set to '0', the cache register is busy and when SR6 is set to '1', the cache register is ready to accept new data.

During all other operations SR6 acts as a P/E/R controller bit, which indicates whether the P/E/R controller is active or inactive. When the P/E/R controller bit is set to ‘0’, the P/E/R controller is active (device is busy); when the bit is set to ‘1’, the P/E/R controller is inactive (device is ready).

6.8.3 P/E/R controller bit (SR5)

The program/erase/read controller bit indicates whether the P/E/R controller is active or inactive. When the P/E/R controller bit is set to ‘0’, the P/E/R controller is active (device is busy); when the bit is set to ‘1’, the P/E/R controller is inactive (device is ready).

6.8.4 Cache program error bit (SR1)

The cache program error bit can be used to identify if the previous page (page N-1) has been successfully programmed or not in a cache program operation. SR1 is set to ’1’ when the cache program operation has failed to program the previous page (page N-1) correctly. If SR1 is set to ‘0’ the operation has completed successfully.

The cache program error bit is only valid during cache program operations, during other operations it is don’t care.

6.8.5 Error bit (SR0)

The error bit is used to identify if any errors have been detected by the P/E/R controller. The error bit is set to ’1’ when a program or erase operation has failed to write the correct data to the memory. If the error bit is set to ‘0’ the operation has completed successfully. The error bit SR0, in a cache program operation, indicates a failure on page N.

6.8.6 SR4, SR3 and SR2 are reserved

Table 13. Status register bits

Bit	Name	Logic level	Definition
SR7	Write protection	'1'	Not protected
		'0'	Protected
SR6	Program/ erase/ read controller	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
	Cache ready/busy	'1'	Cache register ready (cache operation only)
		'0'	Cache register busy (cache operation only)
SR5	Program/ erase/ read controller(1)	'1'	P/E/R C inactive, device ready
		'0'	P/E/R C active, device busy
SR4, SR3, SR2	Reserved	Don’t care	
SR1	Cache program error(2)	'1'	Page N-1 failed in cache program operation
		'0'	Page N-1 programmed successfully
SR0	Generic error	‘1’	Error – operation failed
		‘0’	No Error – operation successful
	Cache program error	‘1’	Page N failed in cache program operation
		‘0’	Page N programmed successfully

1. Only valid for cache program operations, for other operations it is same as SR6.
2. Only valid for cache operations, for other operations it is don’t care.

6.9 Read electronic signature

The device contains a manufacturer code and device code. To read these codes three steps are required:

1. One bus write cycle to issue the Read Electronic Signature command (90h)
2. One bus write cycle to input the address (00h)
3. Four bus read cycles to sequentially output the data (as shown in *Table 14: Electronic signature*).

Table 14. Electronic signature

Part number	byte/word 1	byte/word 2	byte/word 3 (see *Table 15*)	byte/word 4 (see *Table 16*)
	Manufacturer code	Device code		
NAND01GR3B2B	20h	A1h	80h	15h
NAND01GW3B2B		F1h		1Dh
NAND01GR4B2B	0020h	B1h		55h
NAND01GW4B2B		C1h		5Dh
NAND02GR3B2C	20h	AAh		15h
NAND02GW3B2C		DAh		1Dh
NAND02GR4B2C	0020h	BAh		55h
NAND02GW42C		CAh		5Dh

Table 15. Electronic signature byte 3

I/O	Definition	Value	Description
I/O1-I/O0	Internal chip number	0 0 0 1 1 0 1 1	1 2 4 8
I/O3-I/O2	Cell type	0 0 0 1 1 0 1 1	2-level cell 4-level cell 8-level cell 16-level cell
I/O5-I/O4	Number of simultaneously programmed pages	0 0 0 1 1 0 1 1	1 2 4 8
I/O6	Interleaved programming between multiple devices	0 1	Not supported supported
I/O7	Cache program	0 1	Not supported supported

Table 16. Electronic signature byte/word 4

I/O	Definition	Value	Description
I/O1-I/O0	Page size (without spare area)	0 0 0 1 1 0 1 1	1 Kbyte 2 Kbytes Reserved Reserved
I/O2	Spare area size (byte / 512-byte)	0 1	8 16
I/O7, I/O3	Minimum sequential access time	0 0 0 1 1 0 1 1	50 ns 30 ns 25 ns Reserved
I/O5-I/O4	Block size (without spare area)	0 0 0 1 1 0 1 1	64 Kbytes 128 Kbytes 256 Kbytes Reserved
I/O6	Organization	0 1	X8 X16

7 Data protection

The device has hardware features to protect against program and erase operations.

It features a Write Protect, $\overline{WP}$, pin, which can be used to protect the device against program and erase operations. It is recommended to keep $\overline{WP}$ at V_{IL} during power-up and power-down.

In addition, to protect the memory from any involuntary program/erase operations during power-transitions, the device has an internal voltage detector which disables all functions whenever V_{DD} is below V_{LKO} (see *Table 22* and *Table 23*).

8 Software algorithms

This section gives information on the software algorithms that Numonyx recommends to implement to manage the bad blocks and extend the lifetime of the NAND device.

NAND flash memories are programmed and erased by Fowler-Nordheim tunneling using a high voltage. Exposing the device to a high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 18* for value) and it is recommended to implement garbage collection, a wear-leveling algorithm and an error correction code, to extend the number of program and erase cycles and increase the data retention.

To help integrate a NAND memory into an application, Numonyx can provide a file system OS native reference software, which supports the basic commands of file management.

Contact the nearest Numonyx sales office for more details.

8.1 Bad block management

Devices with bad blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A bad block does not affect the performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The bad block information is written prior to shipping. Any block, where the 1st and 6th bytes, or 1st word, in the spare area of the 1st page, does not contain FFh, is a bad block.

The bad block Information must be read before any erase is attempted as the bad block information may be erased. For the system to be able to recognize the bad blocks based on the original information it is recommended to create a bad block table following the flowchart shown in *Figure 15*.

8.2 NAND flash memory failure modes

Over the lifetime of the device additional bad blocks may develop.

To implement a highly reliable system, all the possible failure modes must be considered:

- **Program/erase failure:** in this case the block has to be replaced by copying the data to a valid block. These additional bad blocks can be identified as attempts to program or erase them will give errors in the status register
  As the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block. See *Section 6.4: Copy back program* for more details
- **Read failure:** in this case, ECC correction must be implemented. To efficiently use the memory space, it is recommended to recover single-bit error in read by ECC, without replacing the whole block.

Refer to *Table 17* for the procedure to follow if an error occurs during an operation.

Table 17. NAND flash failure modes

Operation	Procedure
Erase	Block replacement
Program	Block replacement or ECC
Read	ECC

Figure 15. Bad block management flowchart

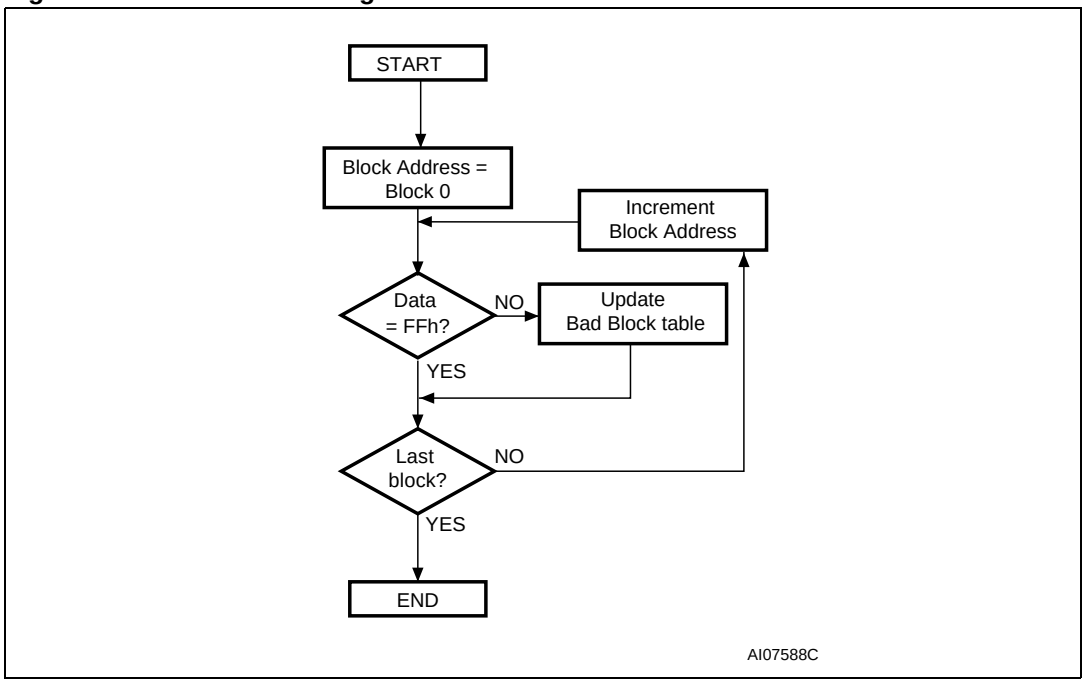
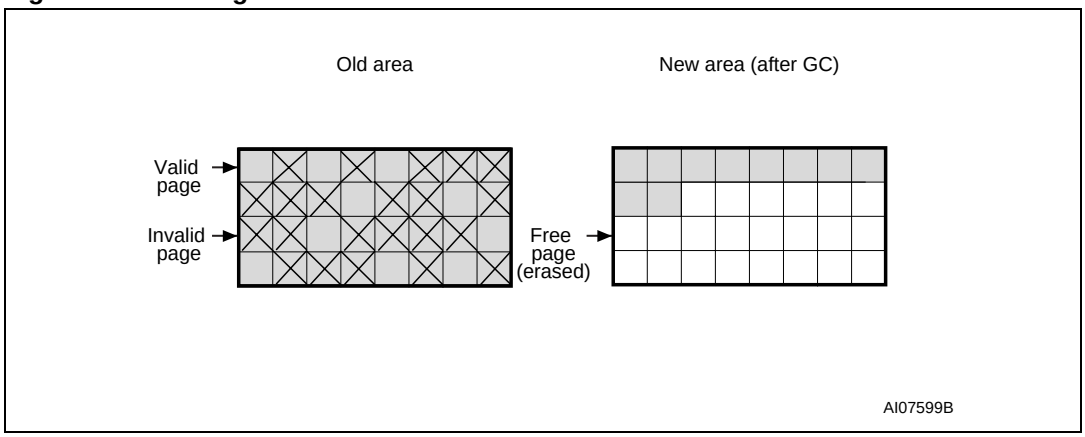


Figure 16. Garbage collection



8.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page, and the previous page is marked as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations it is recommended to implement a garbage collection algorithm. In a garbage collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 16*).

8.4 Wear-leveling algorithm

For write-intensive applications, it is recommended to implement a wear-leveling algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a wear-leveling algorithm not all blocks get used at the same rate. Blocks with long-lived data do not endure as many write cycles as the blocks with frequently-changed data.

The wear-leveling algorithm ensures that equal use is made of all the available write cycles for each block. There are two wear-leveling levels:

- First level wear-leveling, new data is programmed to the free blocks that have had the fewest write cycles
- Second level wear-leveling, long-lived data is copied to another block so that the original block can be used for more frequently-changed data.

The second level wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

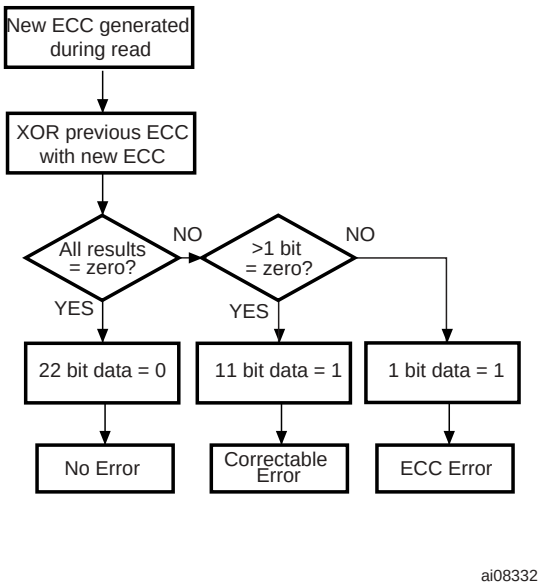
8.5 Error correction code

An error correction code (ECC) can be implemented in the NAND flash memories to identify and correct errors in the data.

For every 2048 bits in the device it is recommended to implement 22 bits of ECC (16 bits for line parity plus 6 bits for column parity).

An ECC model is available in VHDL or Verilog. Contact the nearest Numonyx sales office for more details.

Figure 17. Error detection



8.6 Hardware simulation models

8.6.1 Behavioral simulation models

Denali Software Corporation models are platform independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND flash devices, and so allow software to be developed before hardware.

8.6.2 IBIS simulations models

IBIS (I/O buffer information specification) models describe the behavior of the I/O buffers and electrical characteristics of flash devices.

These models provide information such as AC characteristics, rise/fall times and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models are used to simulate PCB connections and can be used to resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

9 Program and erase times and endurance cycles

The program and erase times and the number of program/erase cycles per block are shown in *Table 18*.

Table 18. Program, erase times and program erase endurance cycles

Parameters	NAND flash			Unit
	Min	Typ	Max	
Page program time		200	700	µs
Block erase time		2	3	ms
Program/erase cycles per block (with ECC)	100 000			cycles
Data retention	10			years

10 Maximum ratings

Stressing the device above the ratings listed in *Table 19: Absolute maximum ratings*, may cause permanent damage to the device. These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 19. Absolute maximum ratings

Symbol	Parameter		Value		Unit
			Min	Max	
T_{BIAS}	Temperature under bias		– 50	125	°C
T_{STG}	Storage temperature		– 65	150	°C
V_{IO}(1)	Input or output voltage	1.8 V devices	– 0.6	2.7	V
		3 V devices	– 0.6	4.6	V
V_{DD}	Supply voltage	1.8 V devices	– 0.6	2.7	V
		3 V devices	– 0.6	4.6	V

1. Minimum voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2 V for less than 20 ns during transitions on I/O pins.

11 DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristics tables that follow, are derived from tests performed under the measurement conditions summarized in *Table 20: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 20. Operating and AC measurement conditions

Parameter		NAND flash		Units
		Min	Max	
Supply voltage (V_{DD})	1.8 V devices	1.7	1.95	V
	3 V devices	2.7	3.6	V
Ambient temperature (T_A)	Grade 1	0	70	°C
	Grade 6	–40	85	°C
Load capacitance (C_L) (1 TTL GATE and C_L)	1.8 V devices	30		pF
	3 V devices (2.7 - 3.6 V)	50		pF
Input pulses voltages	1.8 V devices	0	V_{DD}	V
	3 V devices	0.4	2.4	V
Input and output timing ref. voltages		$V_{DD}/2$		V
Output circuit resistor R_{ref}		8.35		kΩ
Input rise and fall times		5		ns

Table 21. Capacitance(1)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		10	pF
$C_{I/O}$	Input/output capacitance(2)	V_{IL} = 0 V		10	pF

1. T_A = 25 °C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.
2. Input/output capacitances double in stacked devices.

Figure 18. Equivalent testing circuit for AC characteristics measurement

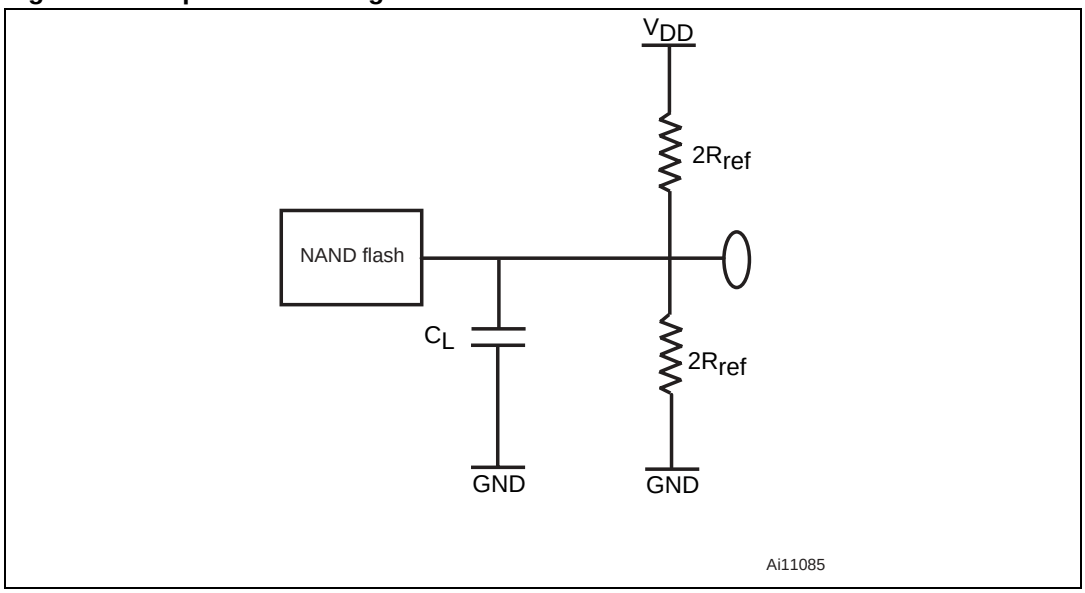


Table 22. DC characteristics, 1.8 V devices

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential read	$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA	-	8	15	mA
I_{DD2}		Program	–	-	8	15	mA
I_{DD3}		Erase	–	-	8	15	mA
I_{DD5}	Standby current (CMOS)(1)		$\overline{E}$ = V_{DD} – 0.2, $\overline{WP}$ = 0/V_{DD}	-	10	50	µA
I_{LI}	Input leakage current(1)		V_{IN} = 0 to V_{DD}max	-	–	±10	µA
I_{LO}	Output leakage current(1)		V_{OUT} = 0 to V_{DD}max	-	–	±10	µA
V_{IH}	Input high voltage		–	V_{DD} - 0.4	–	V_{DD} + 0.3	V
V_{IL}	Input low voltage		–	-0.3	–	0.4	V
V_{OH}	Output high voltage level		I_{OH} = –100 µA	V_{DD} - 0.1	–	–	V
V_{OL}	Output low voltage level		I_{OL} = 100 µA	–	–	0.1	V
I_{OL} ($R\overline{B}$)	Output low current ($R\overline{B}$)		V_{OL} = 0.1 V	3	4		mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		–	–	–	1.1	V

1. Leakage current and standby current double in stacked devices.

Table 23. DC characteristics, 3 V devices

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential Read	$\overline{E}$ = V_{IL}, I_{OUT} = 0 mA	–	10	20	mA
I_{DD2}		Program	–	–	10	20	mA
I_{DD3}		Erase	–	–	10	20	mA
I_{DD4}	Standby current (TTL)(1)		$\overline{E}$ = V_{IH}, $\overline{WP}$ = 0/V_{DD}			1	mA
I_{DD5}	Standby current (CMOS)(1)		$\overline{E}$ = V_{DD} – 0.2, $\overline{WP}$ = 0/V_{DD}	–	10	50	µA
I_{LI}	Input leakage current(1)		V_{IN} = 0 to V_{DD}max	–	–	±10	µA
I_{LO}	Output leakage current(1)		V_{OUT} = 0 to V_{DD}max	–	–	±10	µA
V_{IH}	Input high voltage		–	0.8V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input low voltage		–	-0.3	–	0.2V_{DD}	V
V_{OH}	Output high voltage level		I_{OH} = –400 µA	2.4	–	–	V
V_{OL}	Output low voltage level		I_{OL} = 2.1 mA	–	–	0.4	V
I_{OL} ($R\overline{B}$)	Output low current ($R\overline{B}$)		V_{OL} = 0.4 V	8	10		mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		–	–	–	1.7	V

1. Leakage current and standby current double in stacked devices.

Table 24. AC characteristics for command, address, data input

Symbol	Alt. symbol	Parameter			1.8 V devices	3 V devices	Unit
t_{ALLWH}	t_{ALS}	Address Latch Low to Write Enable High	AL setup time	Min	25	15	ns
t_{ALHWH}		Address Latch High to Write Enable High					
t_{CLHWH}	t_{CLS}	Command Latch High to Write Enable High	CL setup time	Min	25	15	ns
t_{CLLWH}		Command Latch Low to Write Enable High					
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data setup time	Min	20	15	ns
t_{ELWH}	t_{CS}	Chip Enable Low to Write Enable High	$\overline{E}$ setup time	Min	35	20	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL hold time	Min	10	5	ns
t_{WHALL}		Write Enable High to Address Latch Low	AL hold time	Min			
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	10	5	ns
t_{WHCLL}		Write Enable High to Command Latch Low					
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data hold time	Min	10	5	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ hold time	Min	10	5	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High hold time	Min	15	10	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ pulse width	Min	25	15	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write cycle time	Min	45	30	ns

Table 25. AC characteristics for operations(1)

Symbol	Alt. symbol	Parameter			1.8 V devices	3 V devices	Unit
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read electronic signature	Min	10	10	ns
t_{ALLRL2}			Read cycle	Min	10	10	ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		Min	20	20	ns
t_{BLBH1}		Ready/Busy Low to Ready/Busy High	Read busy time	Max	25	25	µs
t_{BLBH2}	t_{PROG}		Program busy time	Max	700	700	µs
t_{BLBH3}	t_{BERS}		Erase busy time	Max	3	3	ms
t_{BLBH4}	t_{RST}		Reset busy time, during ready	Max	5	5	µs
			Reset busy time, during read	Max	5	5	µs
			Reset busy time, during program	Max	10	10	µs
			Reset busy time, during erase	Max	500	500	µs
t_{BLBH5}	t_{CBSY}		Cache busy time	Typ	3	3	µs
				Max	700	700	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		Min	10	10	ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		Min	0	0	ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z		Max	30	30	ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-z		Max	30	30	ns
t_{WHWH}	t_{ADL}(2)	Last address latched to data loading time during program operations		Min	100	100	ns
t_{VHWH} t_{VLWH}	t_{WW}(3)	Write protection time		Min	100	100	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid		Max	45	25	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High hold time	Min	15	10	ns
t_{EHQX} t_{RHQX}	T_{OH}	Chip Enable High or Read Enable high to Output Hold		Min	10	10	ns
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable pulse width	Min	25	15	ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read cycle time	Min	50	30	ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable access time	Max	30	20	ns
			Read ES access time(4)				
t_{WHBH}	t_R	Write Enable High to Ready/Busy High	Read busy time	Max	25	25	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low		Max	100	100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		Min	60	60	ns

1. The time to ready depends on the value of the pull-up resistor tied to the ready/busy pin. See *Figure 31*, *Figure 32* and *Figure 33*.
2. t_{WHWH} is the time from $\overline{W}$ rising edge during the final address cycle to $\overline{W}$ rising edge during the first data cycle.
3. During a program/erase enable operation, t_{WW} is the delay from $\overline{WP}$ high to $\overline{W}$ High.
   During a program/erase disable Operation, t_{WW} is the delay from $\overline{WP}$ Low to $\overline{W}$ High.
4. ES = electronic signature.

Figure 19. Command latch AC waveforms

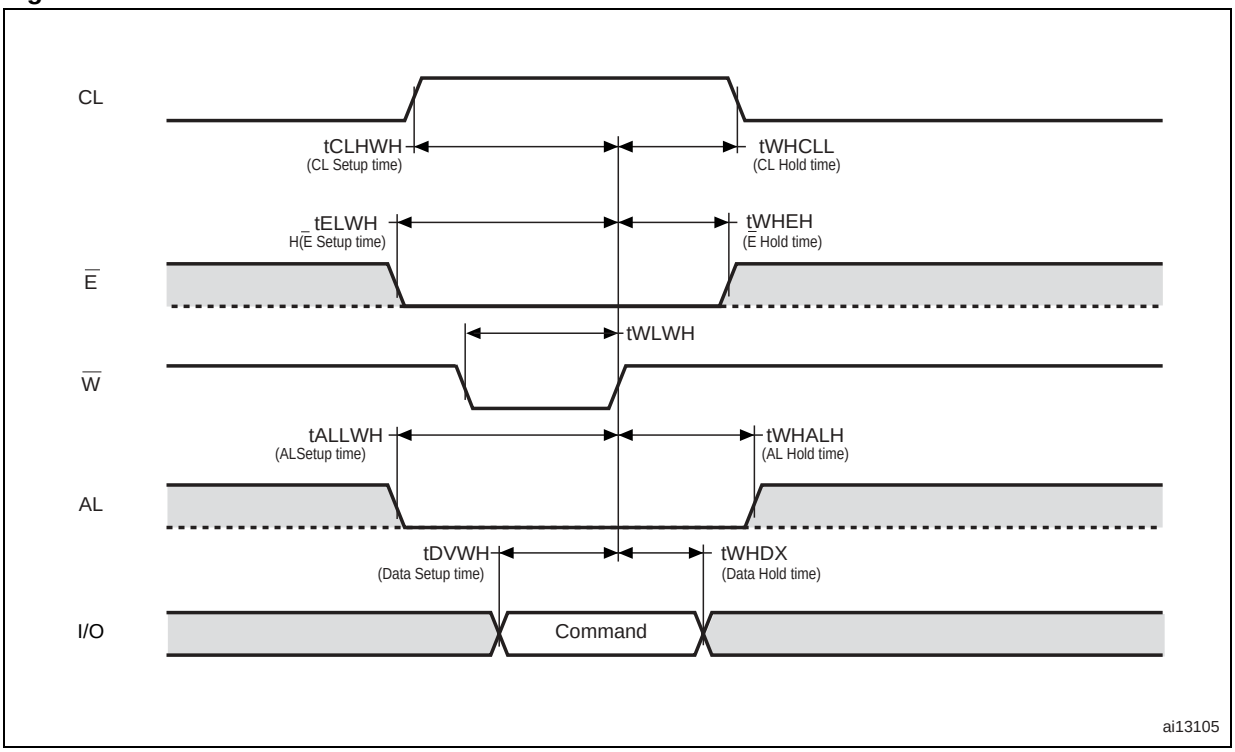
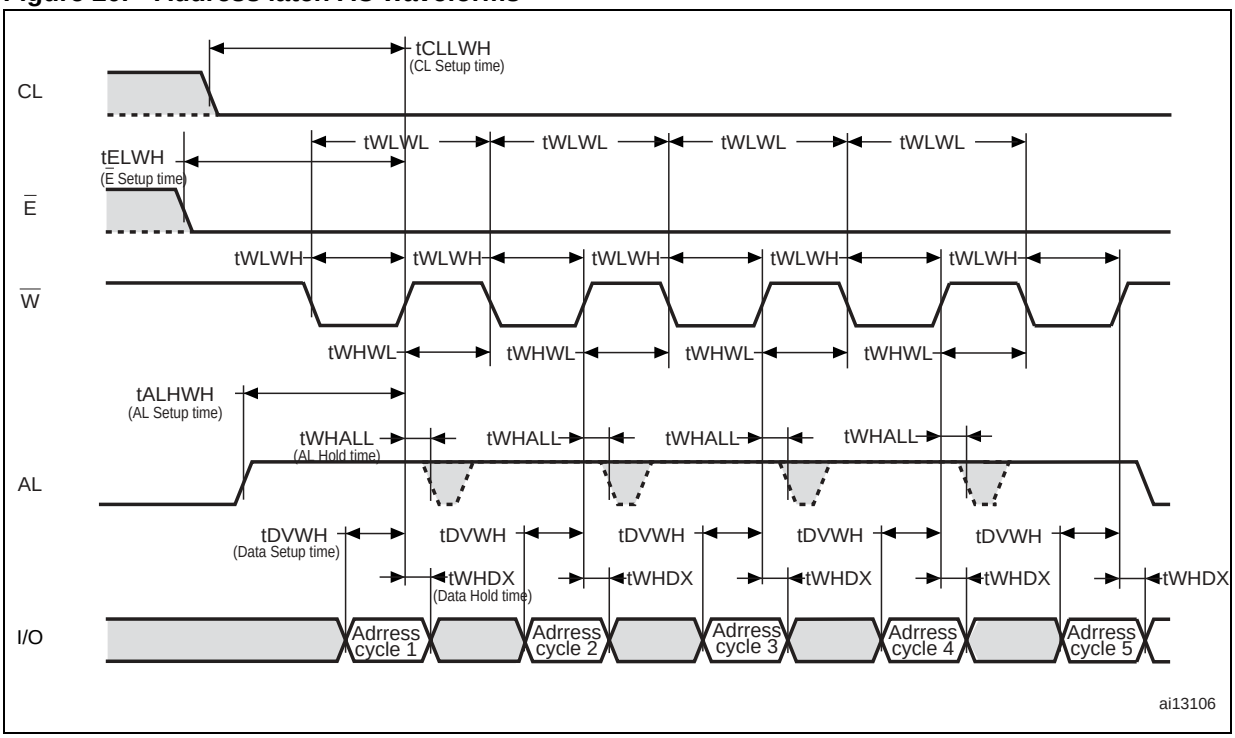
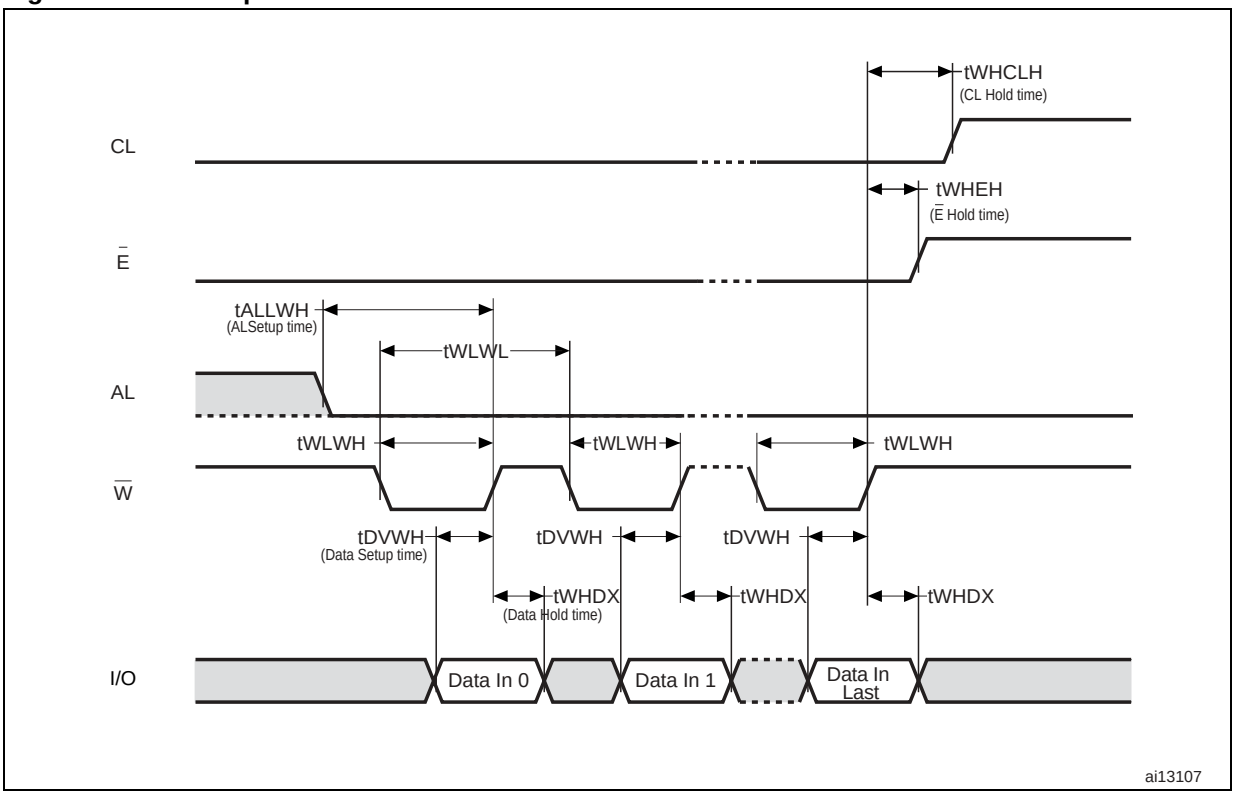


Figure 20. Address latch AC waveforms



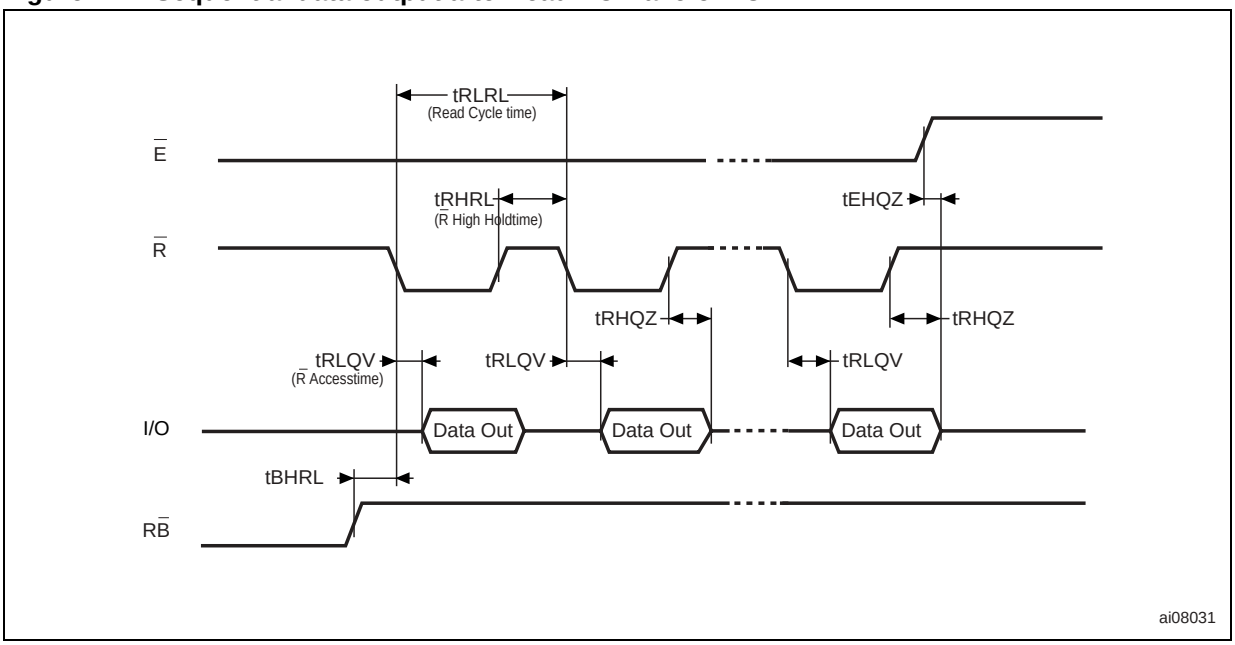
1. A fifth address cycle is required for 2-Gbit devices only.

Figure 21. Data Input Latch AC waveforms



1. Data in last is 2112 in x8 devices and 1056 in x16 devices.

Figure 22. Sequential data output after read AC waveforms



1. CL = Low, AL = Low, W = High.

Figure 23. Read status register AC waveforms

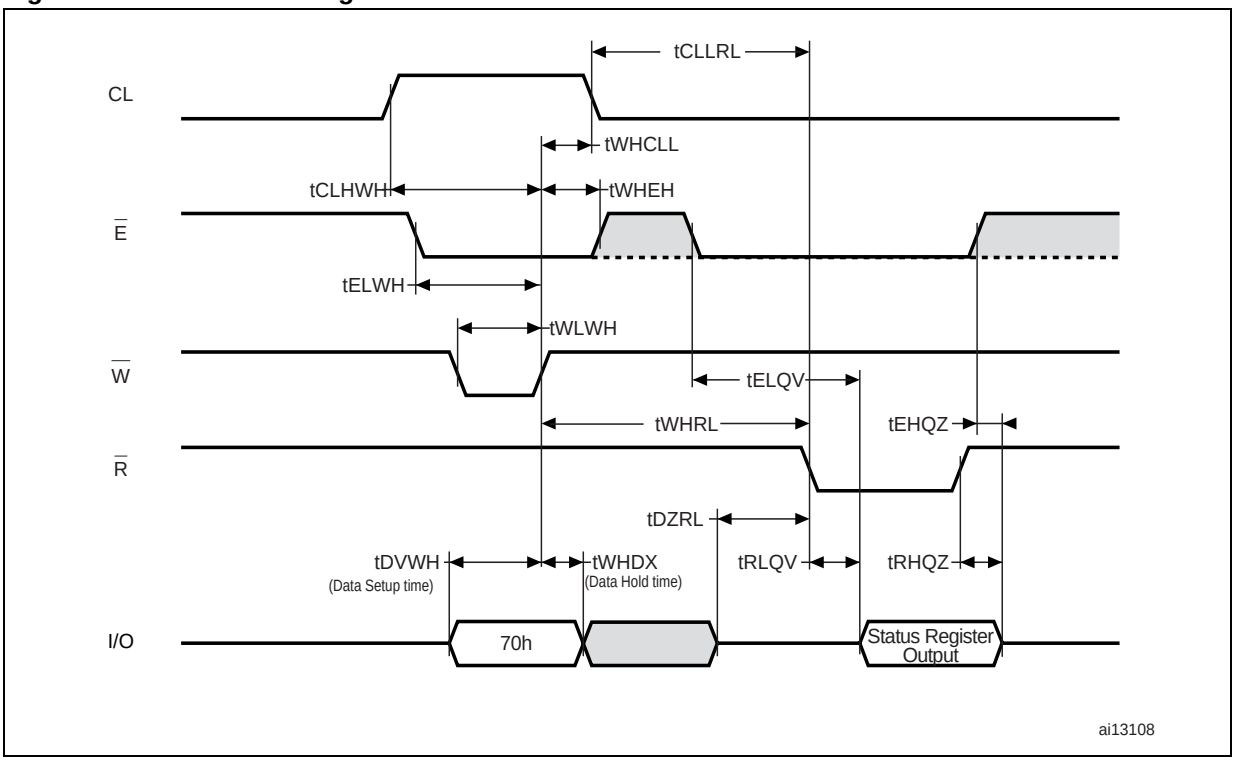
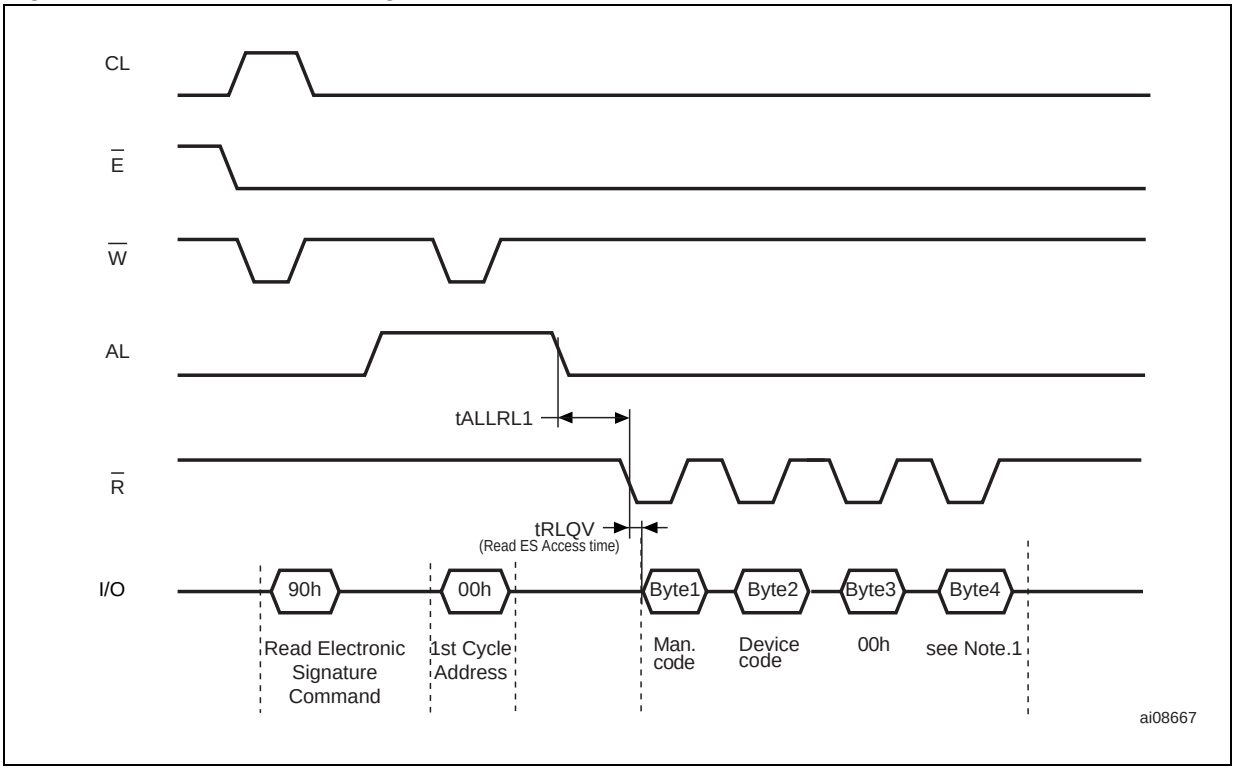
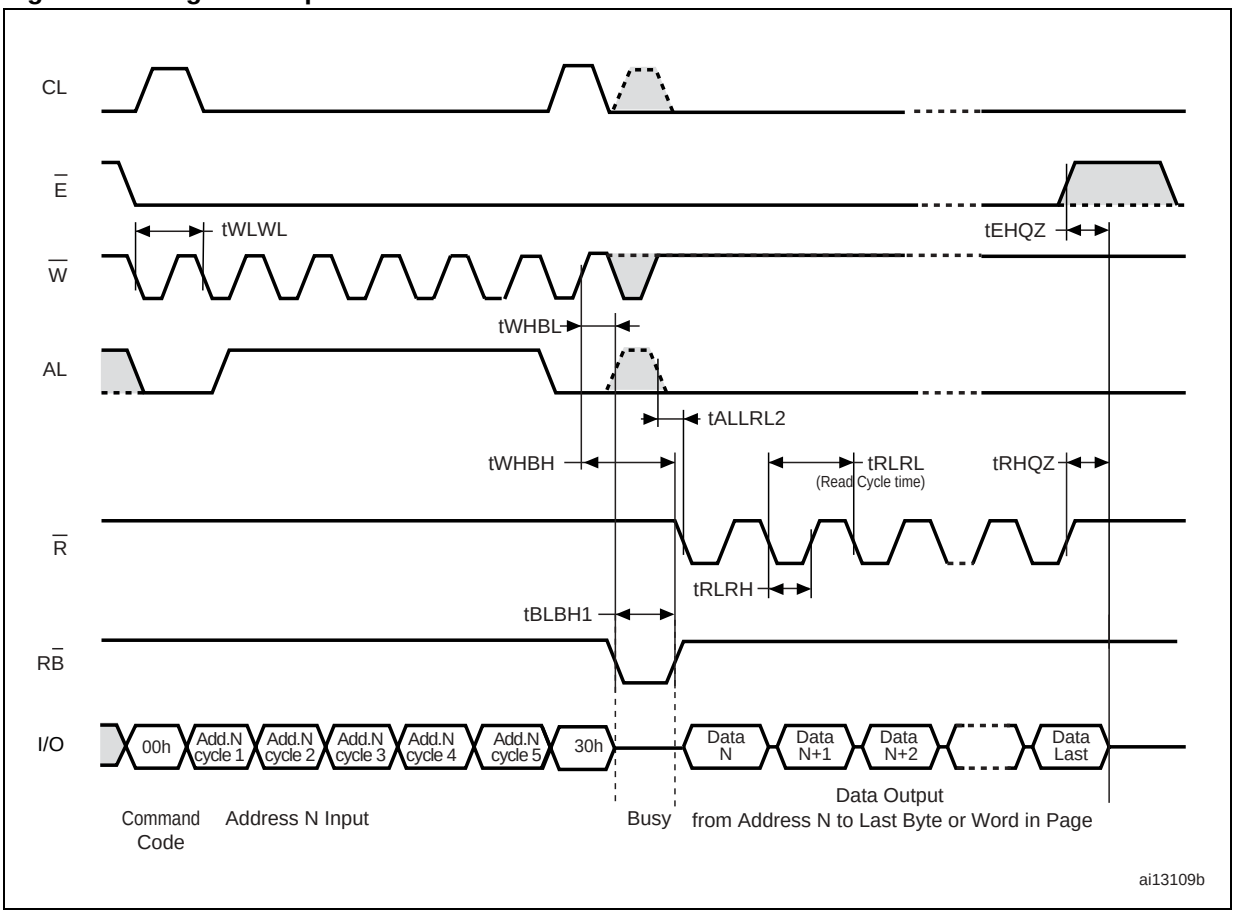


Figure 24. Read electronic signature AC waveforms



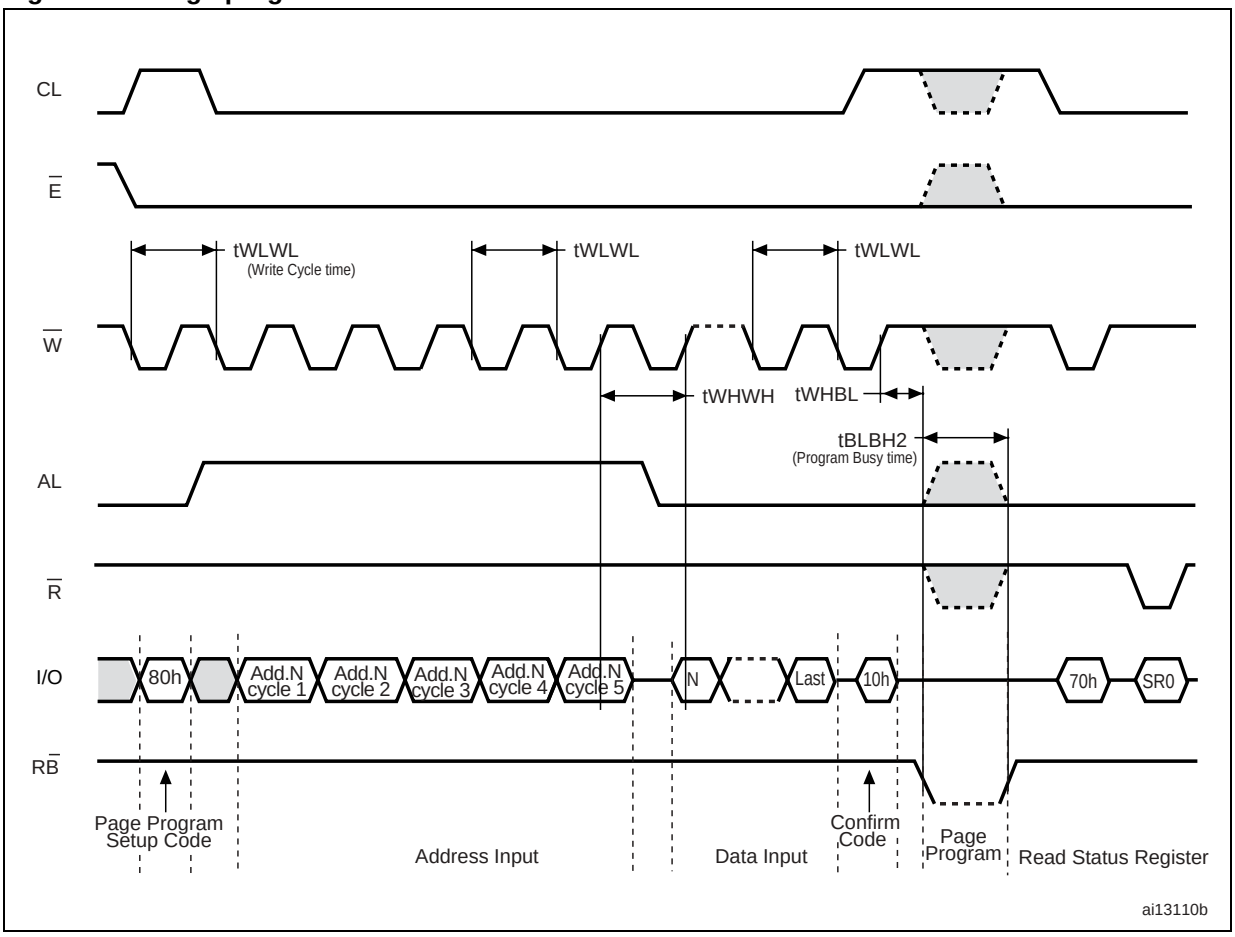
1. Refer to *Table 14* for the values of the manufacturer and device codes, and to *Table 15* and *Table 16* for the information contained in byte 3 and 4.

Figure 25. Page read operation AC waveforms



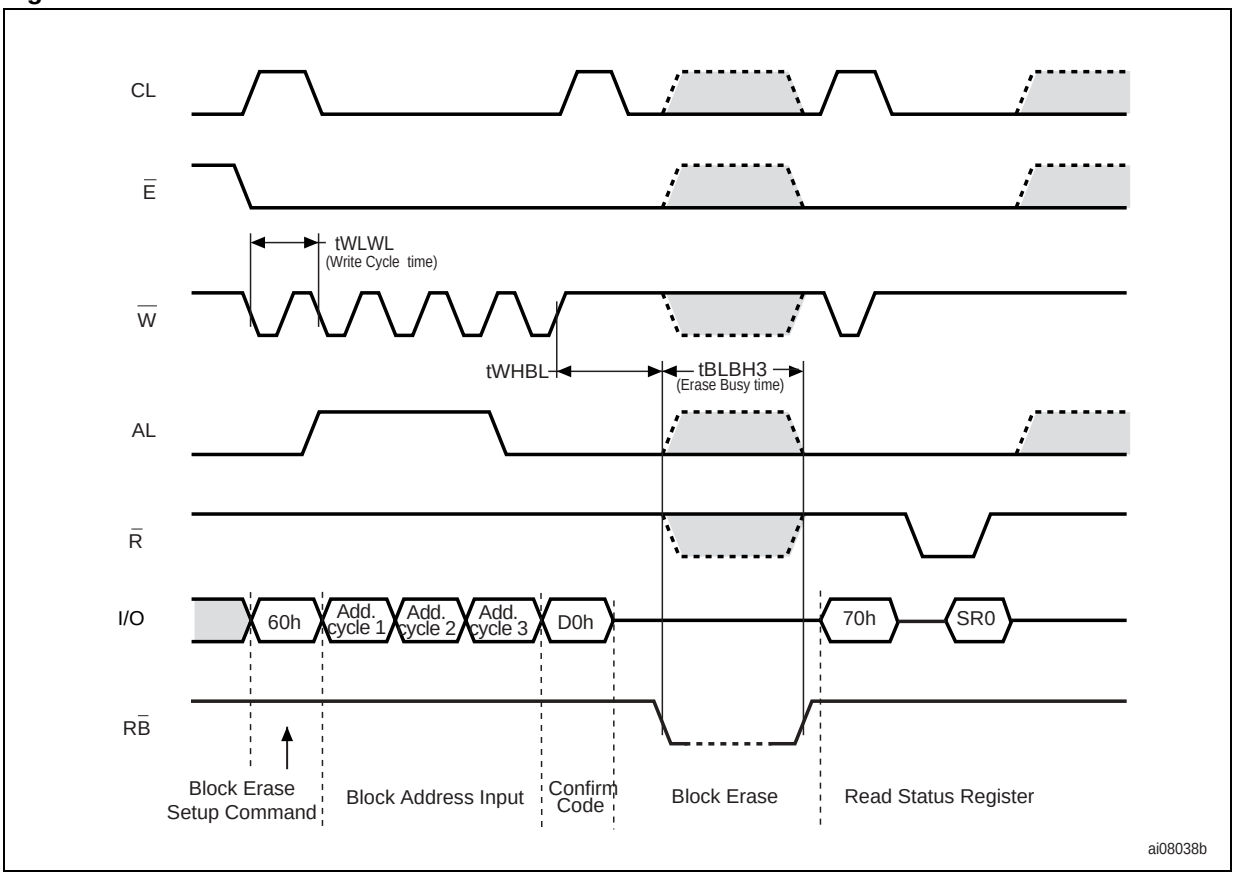
1. A fifth address cycle is required for 2-Gbit devices only.

Figure 26. Page program AC waveforms



1. A fifth address cycle is required for 2-Gbit devices only.

Figure 27. Block erase AC waveforms



1. Address cycle 3 is required for 2-Gbit devices only.

Figure 28. Reset AC waveforms

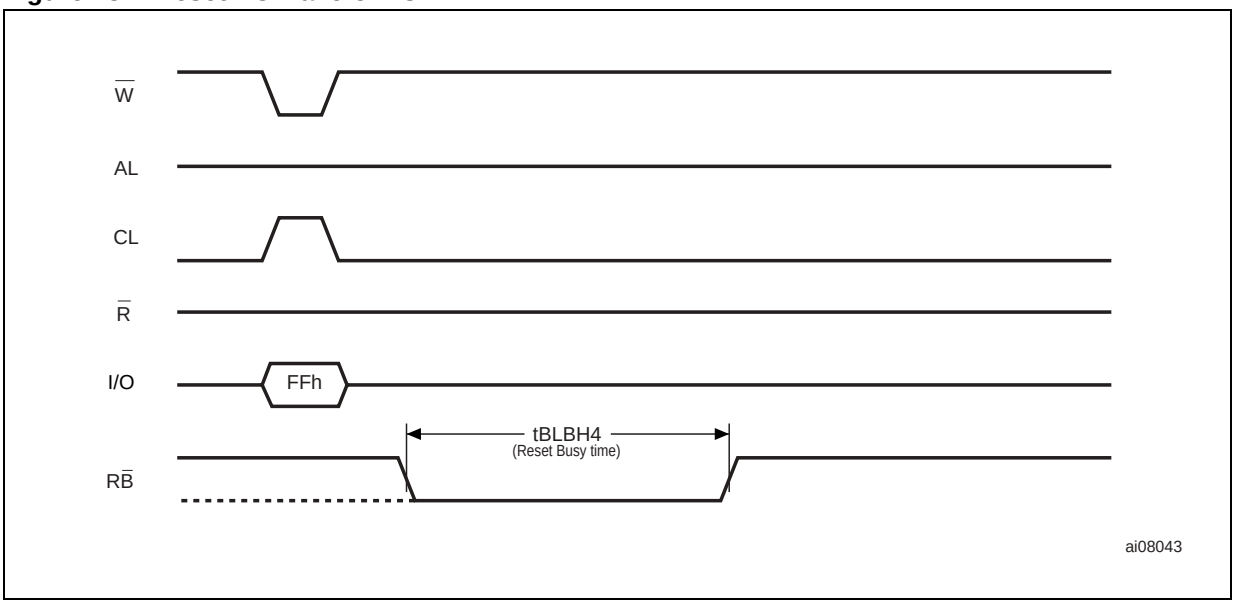


Figure 29. Program/erase enable waveforms

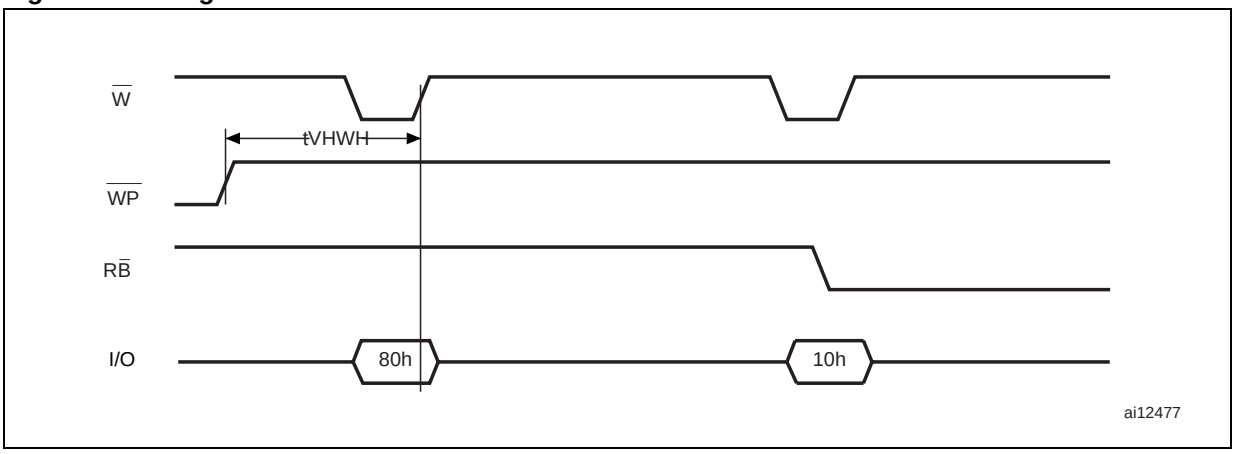
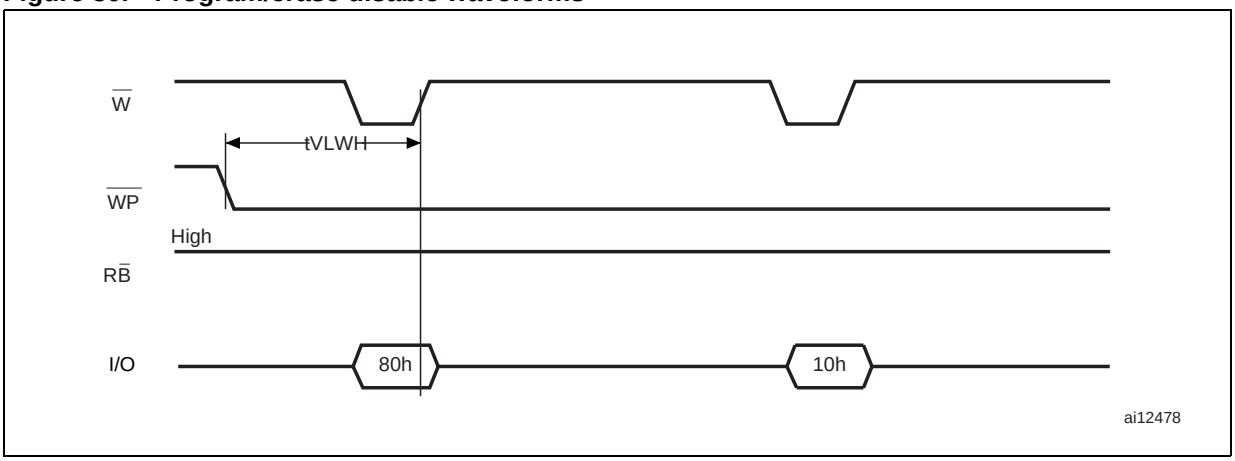


Figure 30. Program/erase disable waveforms



11.1 Ready/Busy signal electrical characteristics

Figure 32, *Figure 31* and *Figure 33* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min(1.8V) = \frac{1.85V}{3mA + I_L}$$

$$R_P min(3V) = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 31. Ready/Busy AC waveform

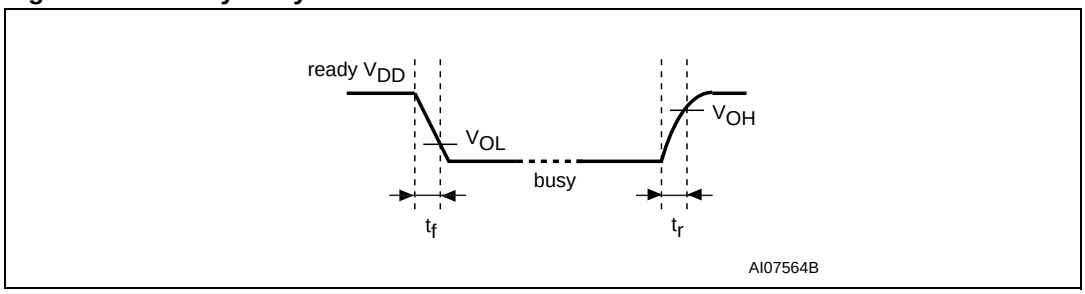


Figure 32. Ready/Busy load circuit

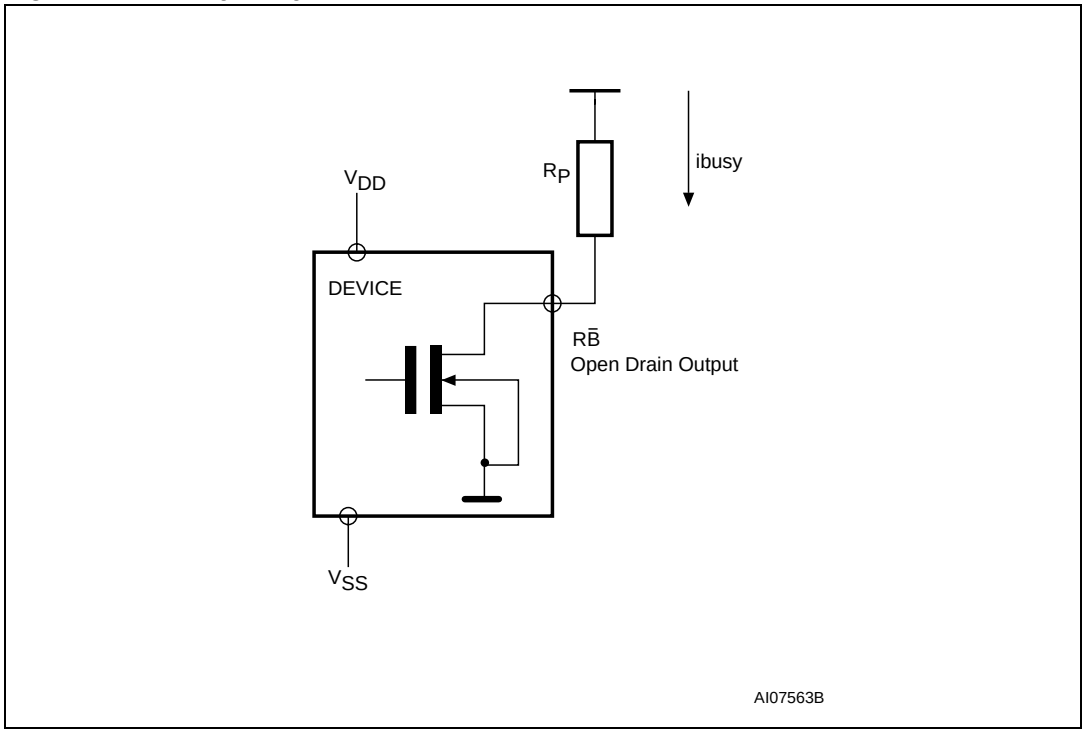
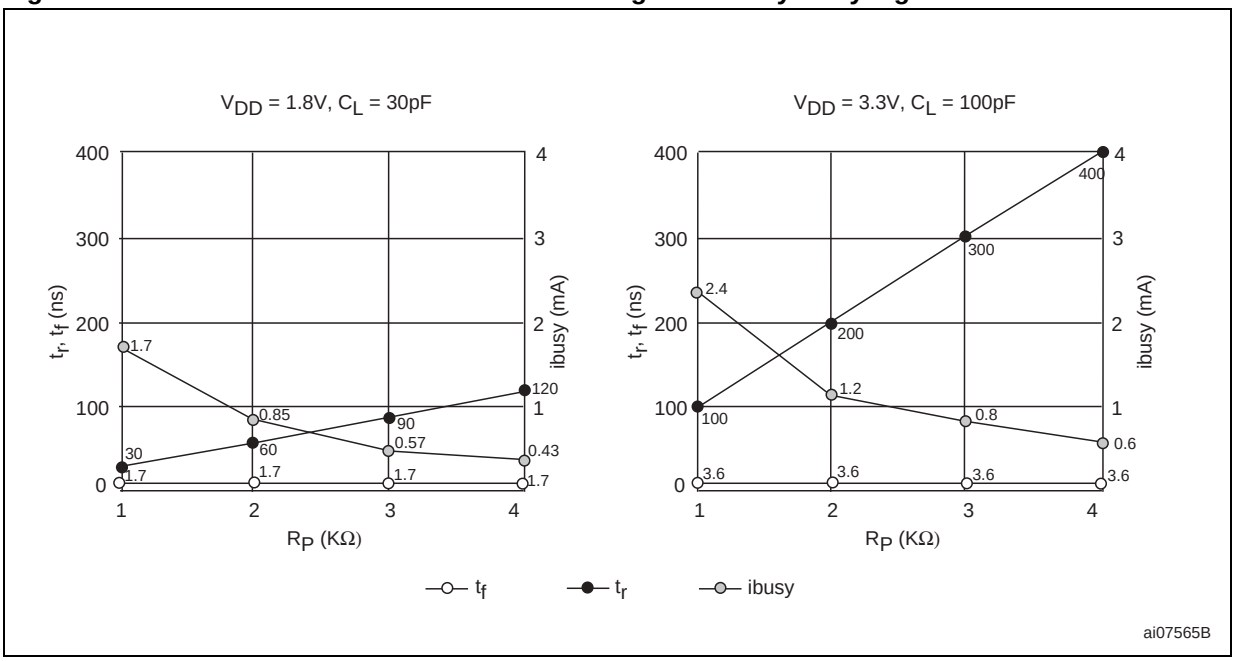


Figure 33. Resistor value versus waveform timings for Ready/Busy signal



1. T = 25°C.

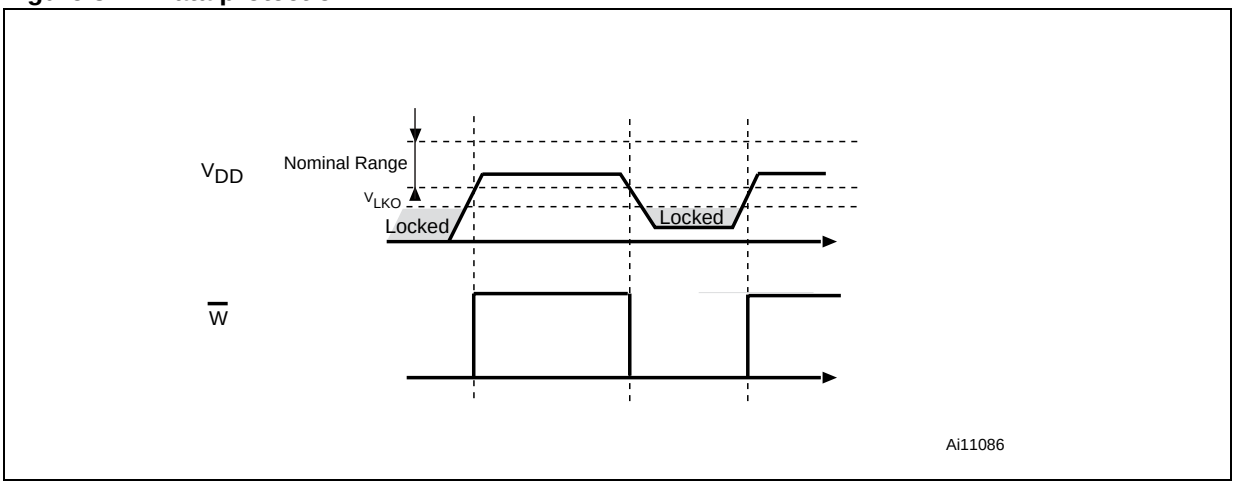
11.2 Data protection

The Numonyx NAND device is designed to guarantee data protection during power transitions.

A V_{DD} detection circuit disables all NAND operations, if V_{DD} is below the V_{LKO} threshold.

In the V_{DD} range from V_{LKO} to the lower limit of nominal range, the $\overline{WP}$ pin should be kept low (V_{IL}) to guarantee hardware protection during power transitions as shown in the below figure.

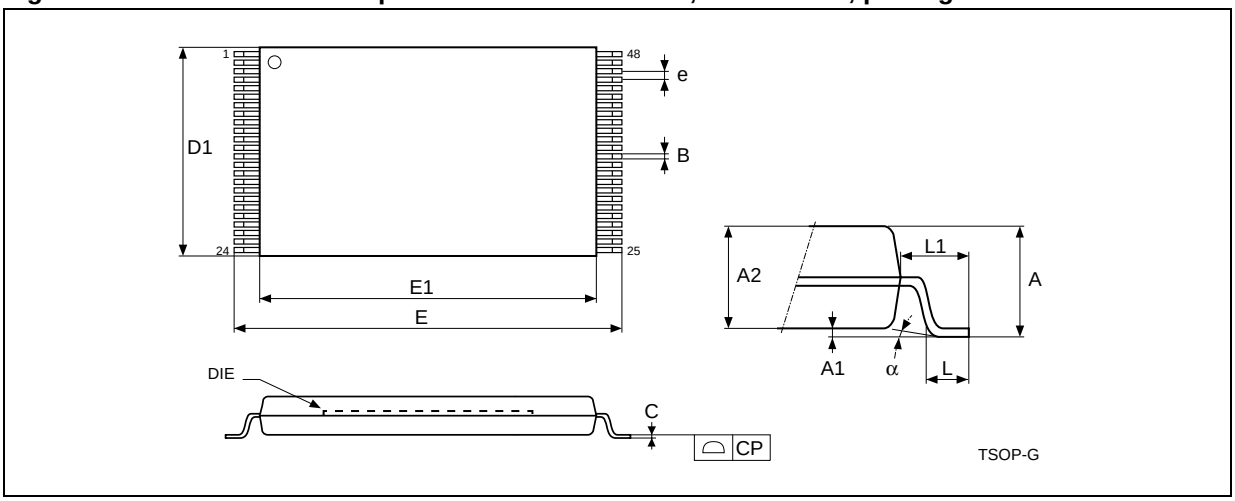
Figure 34. Data protection



12 Package mechanical

In order to meet environmental requirements, Numonyx offers these devices in ECOPACK® packages. ECOPACK® packages are lead-free. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

Figure 35. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline

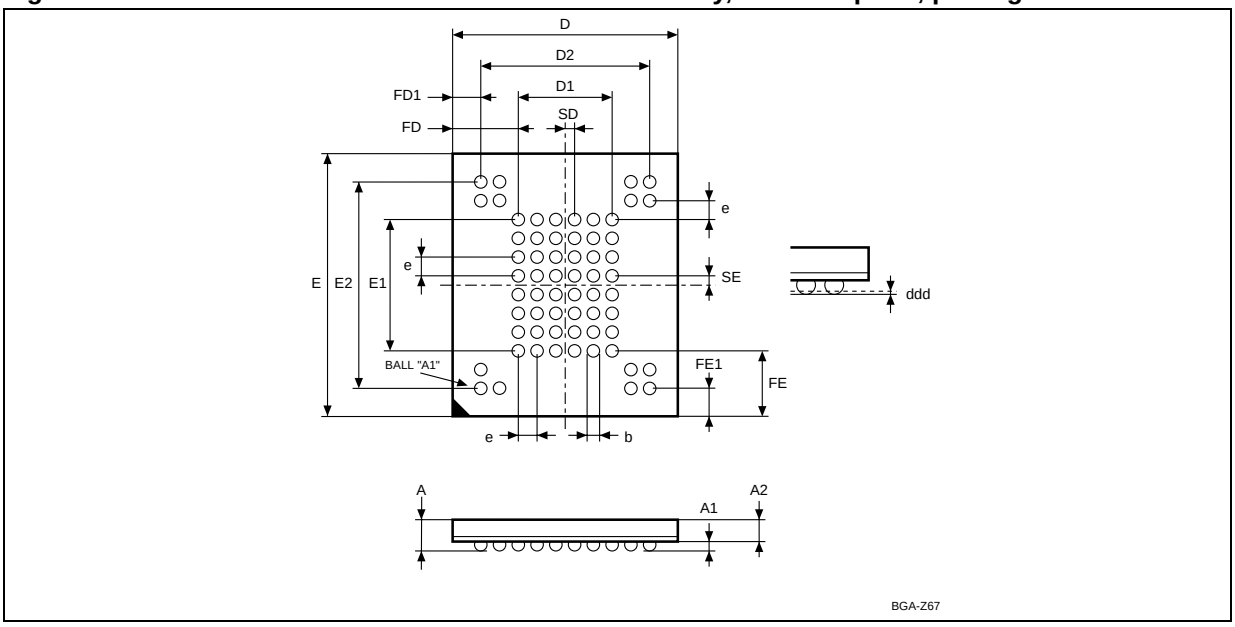


1. Drawing is not to scale.

Table 26. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.17	0.27	0.009	0.007	0.011
C		0.10	0.21		0.004	0.008
CP			0.08			0.003
D1	12.00	11.90	12.10	0.472	0.468	0.476
E	20.00	19.80	20.20	0.787	0.779	0.795
E1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	–	–	0.020	–	
L	0.60	0.50	0.70	0.024	0.020	0.028
L1	0.80			0.031		
α	3°	0°	5°	3°	0°	5°

Figure 36. VFBGA63 9.5 x 12 mm - 6 x 8 active ball array, 0.80 mm pitch, package outline

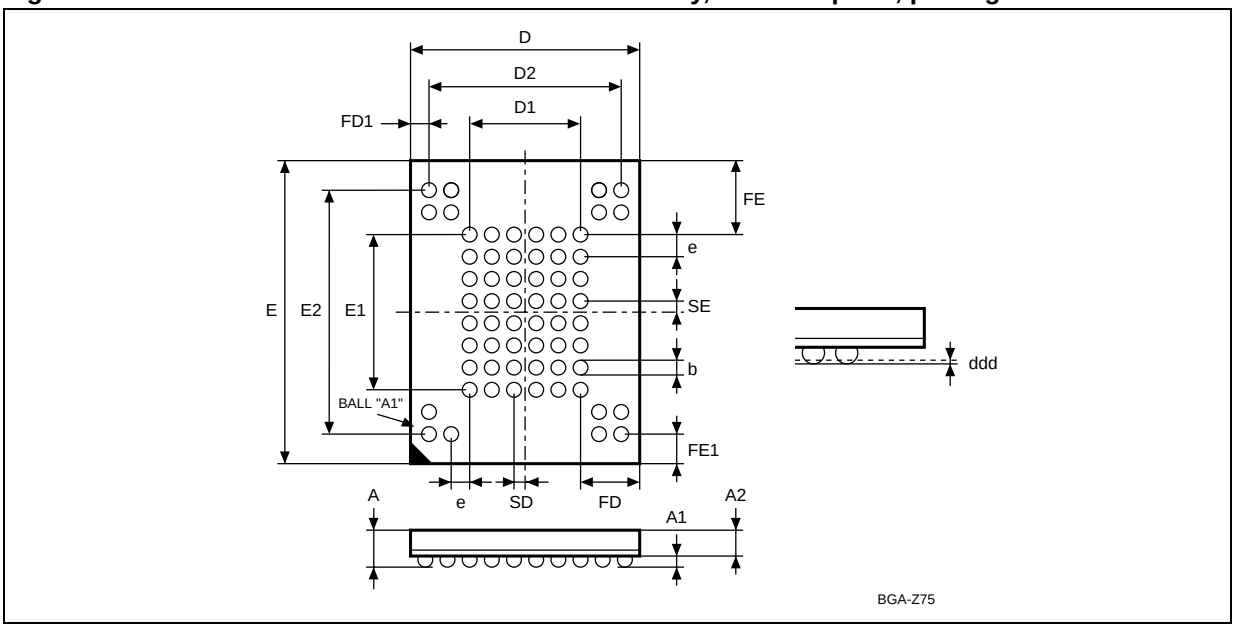


1. Drawing is not to scale

Table 27. VFBGA63 9.5 x 12 mm - 6 x 8 ball array, 0.80 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.05			0.041
A1		0.25			0.010	
A2			0.70			0.028
b	0.45	0.40	0.50	0.018	0.016	0.020
D	9.50	9.40	9.60	0.374	0.370	0.378
D1	4.00			0.157		
D2	7.20			0.283		
ddd			0.10			0.004
E	12.00	11.90	12.10	0.472	0.468	0.476
E1	5.60			0.220		
E2	8.80			0.346		
e	0.80	–	–	0.031	–	–
FD	2.75			0.108		
FD1	1.15			0.045		
FE	3.20			0.126		
FE1	1.60			0.063		
SD	0.40			0.016		
SE	0.40			0.016		

Figure 37. VFBGA63 9 x 11 mm - 6 x 8 active ball array, 0.80 mm pitch, package outline



1. Drawing is not to scale

Table 28. VFBGA63 9 x 11 mm - 6 x 8 active ball array, 0.80 mm pitch, package mechanical data

Symbol	millimeters			inches		
	Typ	Min	Max	Typ	Min	Max
A			1.05			0.041
A1		0.25			0.010	
A2			0.70			0.028
b	0.45	0.40	0.50	0.018	0.016	0.020
D	9.00	8.90	9.10	0.354	0.350	0.358
D1	4.00			0.157		
D2	7.20			0.283		
ddd			0.10			0.004
E	11.00	10.90	11.10	0.433	0.429	0.437
E1	5.60			0.220		
E2	8.80			0.346		
e	0.80	–	–	0.031	–	–
FD	2.50			0.098		
FD1	0.90			0.035		
FE	2.70			0.106		
FE1	1.10			0.043		
SD	0.40	–	–	0.016	–	–
SE	0.40	–	–	0.016	–	–

13 Ordering information

Table 29. Ordering information scheme

Example: NAND02GR3B2C ZA 6 E

Device type
NAND flash memory

Density
01G = 1 Gbit
02G = 2 Gbits

Operating voltage
R = V_{DD} = 1.7 to 1.95 V
W = V_{DD} = 2.7 to 3.6 V

Bus width
3 = x8
4 = x16(1)

Family identifier
B = 2112-byte/ 1056-word page

Device options
2 = chip enable don't care enabled

Product version
B = second version (1-Gbit devices)
C = third version (2-Gbit devices)

Package
N = TSOP48 12 x 20 mm
ZA = VFBGA63 9.5 x 12 x 1 mm, 0.8 mm pitch(2)
ZA= VFBGA63 9 x 11 x 1 mm, 0.8 mm pitch(3)

Temperature range
1 = 0 to 70 °C
6 = –40 to 85 °C

Option
E = ECOPACK® package, standard packing
F = ECOPACK® package, tape & reel packing

1. x16 organization only available for MCP products.
2. For NAND02G-B2C devices only.
3. For NAND01G-B2B devices only.

Note: Devices are shipped from the factory with the memory content bits, in valid blocks, erased to '1'. For further information on any aspect of this device, please contact your nearest Numonyx sales office.

14 Revision history

Table 30. Document revision history

Date	Version	Changes
18-May-2006	0.1	Initial release.
01-Jun-2006	1	Document status changed to preliminary data.
09-Jun-2006	2	VFBGA63 9 x 11 x 1 mm package added for NAND01G-B2B devices and VFBGA63 9.5 x 12 x 1 mm dedicated to NAND02G-B2C devices.
23-Nov-2006	3	Note 2 below *Commands* removed. Overview of *Section 6.1: Read memory array* updated. Paragraph concerning Exit Cache Read command updated in *Section 6.2: Cache read*. Block replacement section replaced by *Section 8.2: NAND flash memory failure modes*. t_{WHALL} added in *Table 24: AC characteristics for command, address, data input*. $R\overline{B}$ waveform updated in *Figure 25: Page read operation AC waveforms*, and CL waveform modified in *Figure 26: Page program AC waveforms*.
20-Apr-2007	4	An error correction code (ECC) is required to obtain a data integrity of 100 000 program/erase cycles per block. *Section 3.9: Ready/Busy (RB)* modified. t_{RHRL2} timing removed from *Figure 9: Page program operation* and *Table 25: AC characteristics for operations*. Note removed below *Figure 11: Copy back program*. t_{WHBH2} replaced by t_{BLBH5}, cash busy time, in *Section 6.5: Cache program*. Alt. symbol for t_{BLBH4} is t_{RST} in *Table 25: AC characteristics for operations*.
14-Apr-2008	5	Applied Numonyx branding.

Please Read Carefully: