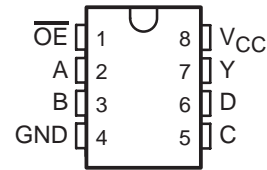


SN74LVC1G99 ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE WITH 3-STATE OUTPUTS

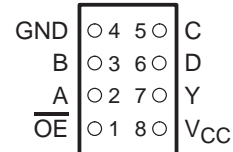
SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

- Available in Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Inputs Accept Voltages to 5.5 V
- Max t_{pd} of 6.7 ns at 3.3 V
- Low Power Consumption, 10- μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- Offers Nine Different Logic Functions in a Single Package
- I_{off} Supports Partial-Power-Down Mode Operation
- Input Hysteresis Allows for Slow Input Transition Time and Better Noise Immunity at Input
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DCT OR DCU PACKAGE
(TOP VIEW)



YEP OR YZP PACKAGE
(BOTTOM VIEW)



description/ordering information

The SN74LVC1G99 is operational from 1.65 V to 5.5 V.

The SN74LVC1G99 features configurable multiple functions with a 3-state output. The output is disabled when the output-enable (\overline{OE}) input is high. When \overline{OE} is low, the output state is determined by 16 patterns of 4-bit input. The user can choose logic functions, such as MUX, AND, OR, NAND, NOR, XOR, XNOR, inverter, and buffer. All inputs can be connected to V_{CC} or GND.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ – WCSP (DSBGA) 0.23-mm Large Bump – YEP	Reel of 3000	SN74LVC1G99YEPR	DE_
	NanoFree™ – WCSP (DSBGA) 0.23-mm Large Bump – YZP (Pb-free)		SN74LVC1G99YZPR	
	SSOP – DCT	Reel of 3000	SN74LVC1G99DCTR	C99_ _ _
		Reel of 250	SN74LVC1G99DCTT	
	VSSOP – DCU	Reel of 3000	SN74LVC1G99DCUR	C99_
		Reel of 250	SN74LVC1G99DCUT	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DCT: The actual top-side marking has three additional characters that designate the year, month, and assembly/test site.

DCU: The actual top-side marking has one additional character that designates the assembly/test site.

YEP/YZP: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site. Pin 1 identifier indicates solder-bump composition (1 = SnPb, • = Pb-free).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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SN74LVC1G99

ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE

WITH 3-STATE OUTPUTS

SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

description/ordering information (continued)

This device functions as an independent inverter, but because of Schmitt action, it has different input threshold levels for positive-going (V_{T+}) and negative-going (V_{T-}) signals.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

FUNCTION TABLE

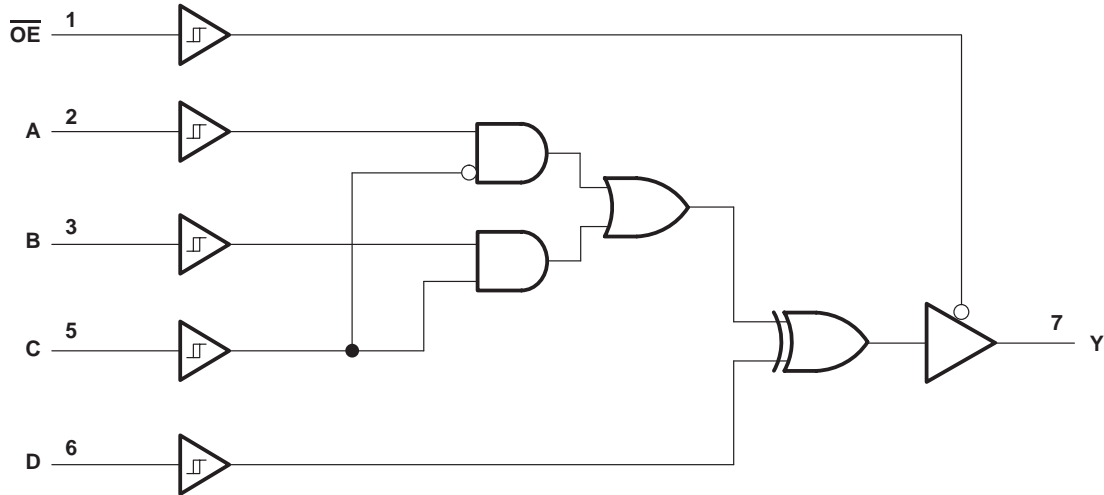
INPUTS					OUTPUT Y
\overline{OE}	D	C	B	A	
L	L	L	L	L	L
L	L	L	L	H	H
L	L	L	H	L	L
L	L	L	H	H	H
L	L	H	L	L	L
L	L	H	L	H	L
L	L	H	H	L	H
L	L	H	H	H	H
L	H	L	L	L	H
L	H	L	L	H	L
L	H	L	H	L	H
L	H	L	H	H	L
L	H	H	L	L	H
L	H	H	L	H	H
L	H	H	H	L	L
L	H	H	H	H	L
H	H or L	H or L	H or L	H or L	Z

SN74LVC1G99

ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE WITH 3-STATE OUTPUTS

SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

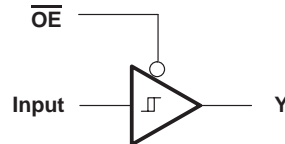
logic diagram (positive logic)



FUNCTION SELECTION TABLE

PRIMARY FUNCTION	COMPLEMENTARY FUNCTION	PAGE
3-state buffer		3
3-state inverter		3
3-state 2-in-1 data selector MUX		4
3-state 2-in-1 data selector MUX, inverted out		4
3-state 2-input AND	3-state 2-input NOR, both inputs inverted	5
3-state 2-input AND, one input inverted	3-state 2-input NOR, one input inverted	5
3-state 2-input AND, both inputs inverted	3-state 2-input NOR	5
3-state 2-input NAND	3-state 2-input OR, both inputs inverted	6
3-state 2-input NAND, one input inverted	3-state 2-input OR, one input inverted	6
3-state 2-input NAND, both inputs inverted	3-state 2-input OR	6
3-state 2-input XOR		7
3-state 2-input XNOR	3-state 2-input XOR, one input inverted	7

3-STATE BUFFER FUNCTIONS AVAILABLE

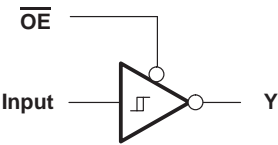


FUNCTION	\overline{OE}	A	B	C	D
3-state buffer	L	Input	H or L	L	L
		H or L	Input	H	L
		L	H	Input	L
		H	L	Input	H
		H	H or L	L	Input
		H or L	L	H	Input
		L	L	H or L	Input

SN74LVC1G99
ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE
WITH 3-STATE OUTPUTS

SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

3-STATE INVERTER FUNCTIONS AVAILABLE



FUNCTION	\overline{OE}	A	B	C	D
3-state inverter	L	Input	H or L	L	H
		X	Input	H	H
		L	H	Input	H
		H	L	Input	L
		H	H or L	L	Input
		H or L	H	H	Input
		H	H	H or L	Input

3-STATE MUX FUNCTIONS AVAILABLE



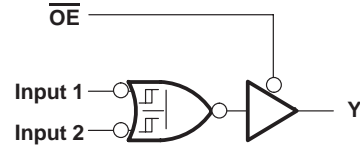
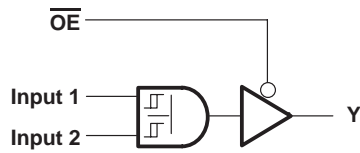
FUNCTION	\overline{OE}	A	B	C	D
3-state 2-to-1	L	Input 1	Input 2	$\overline{\text{Input 1 or Input 2}}$	L
3-state 2-to-1		Input 2	Input 1	$\overline{\text{Input 2 or Input 1}}$	L
3-state 2-to-1		Input 1	Input 2	$\overline{\text{Input 1 or Input 2}}$	H
3-state 2-to-1		Input 2	Input 1	$\overline{\text{Input 2 or Input 1}}$	H

SN74LVC1G99

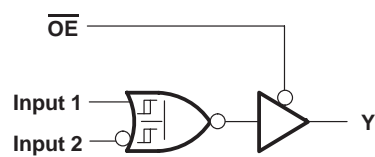
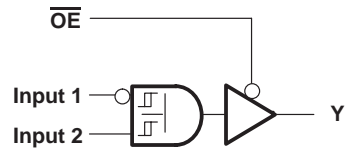
ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE WITH 3-STATE OUTPUTS

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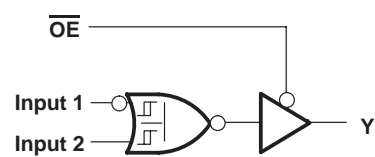
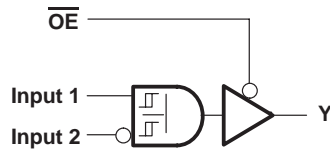
3-STATE AND/NOR FUNCTIONS AVAILABLE



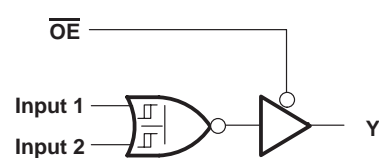
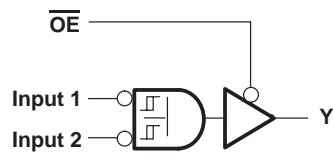
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state AND	3-state NOR	L	L	Input 1	Input 2	L
2	3-state AND	3-state NOR		L	Input 2	Input 1	L



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state AND	3-state NOR	L	Input 2	L	Input 1	L
2	3-state AND	3-state NOR		H	Input 1	Input 2	H



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state AND	3-state NOR	L	Input 1	L	Input 2	L
2	3-state AND	3-state NOR		H	Input 2	Input 1	H



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state AND	3-state NOR	L	Input 1	H	Input 2	L
2	3-state AND	3-state NOR		Input 2	H	Input 1	L

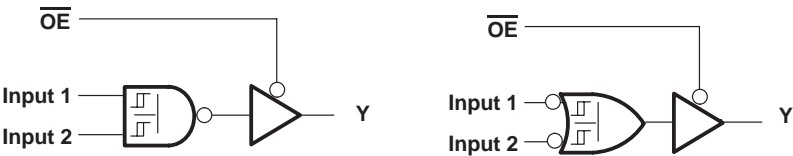
SN74LVC1G99

ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE

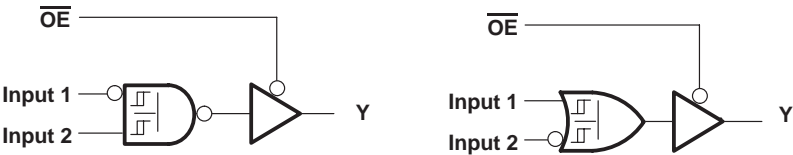
WITH 3-STATE OUTPUTS

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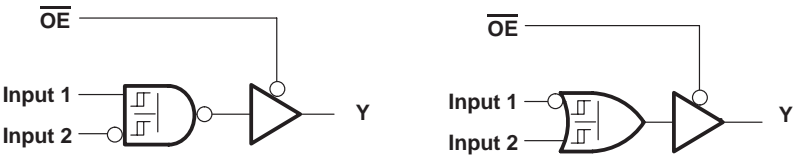
3-STATE NAND/OR FUNCTIONS AVAILABLE



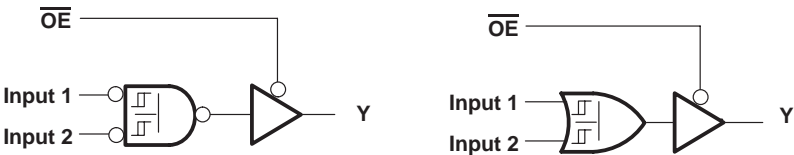
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state NAND	3-state OR	L	L	Input 1	Input 2	H
2	3-state NAND	3-state OR		L	Input 2	Input 1	H



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state NAND	3-state OR	L	Input 2	L	Input 1	H
2	3-state NAND	3-state OR		H	Input 1	Input 2	L



NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state NAND	3-state OR	L	Input 1	L	Input 2	H
2	3-state NAND	3-state OR		H	Input 2	Input 1	L



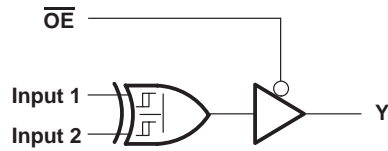
NO. OF INPUTS	AND/NAND FUNCTION	OR/NOR FUNCTION	\overline{OE}	A	B	C	D
2	3-state NAND	3-state OR	L	Input 1	H	Input 2	L
2	3-state NAND	3-state OR		Input 2	H	Input 1	L

SN74LVC1G99

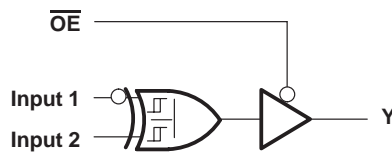
ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE WITH 3-STATE OUTPUTS

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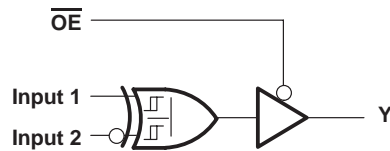
3-STATE XOR/XNOR FUNCTIONS AVAILABLE



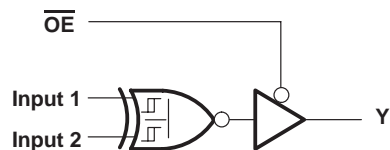
FUNCTION	\overline{OE}	A	B	C	D
3-state XOR	L	Input 1	H or L	L	Input 2
		Input 2	H or L	L	Input 1
		H or L	Input 1	H	Input 2
		H or L	Input 2	H	Input 1
		L	H	Input 1	Input 2
		L	H	Input 2	Input 1



FUNCTION	\overline{OE}	A	B	C	D
3-state XOR	L	H	L	Input 1	Input 2



FUNCTION	\overline{OE}	A	B	C	D
3-state XOR	L	H	L	Input 1	Input 2



FUNCTION	\overline{OE}	A	B	C	D
3-state XNOR	L	H	L	Input 1	Input 2
3-state XNOR		H	L	Input 2	Input 1

SN74LVC1G99

ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE

WITH 3-STATE OUTPUTS

SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DCT package	220°C/W
DCU package	227°C/W
YEP/YZP package	102°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V_{CC} Supply voltage	Operating	1.65	5.5	V
	Data retention only	1.5		
V_I Input voltage		0	5.5	V
V_O Output voltage		0	V_{CC}	V
I_{OH} High-level output current	$V_{CC} = 1.65$ V		–4	mA
	$V_{CC} = 2.3$ V		–8	
	$V_{CC} = 3$ V		–16	
			–24	
	$V_{CC} = 4.5$ V		–32	
I_{OL} Low-level output current	$V_{CC} = 1.65$ V		4	mA
	$V_{CC} = 2.3$ V		8	
	$V_{CC} = 3$ V		16	
			24	
	$V_{CC} = 4.5$ V		32	
$\Delta t/\Delta v$ Input transition rise or fall rate	$V_{CC} = 1.8$ V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
	$V_{CC} = 3.3$ V ± 0.3 V		10	
	$V_{CC} = 5$ V ± 0.5 V		5	

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

SN74LVC1G99

ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE WITH 3-STATE OUTPUTS

SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP†	MAX	UNIT
V _{T+} Positive-going input threshold voltage		1.65 V	0.79		1.26	V
		2.3 V	1.11		1.66	
		3 V	1.5		1.97	
		4.5 V	2.16		2.84	
		5.5 V	2.61		3.43	
V _{T–} Negative-going input threshold voltage		1.65 V	0.39		0.72	V
		2.3 V	0.58		0.97	
		3 V	0.84		1.24	
		4.5 V	1.41		1.89	
		5.5 V	1.87		2.39	
ΔV_T Hysteresis (V _{T+} – V _{T–})		1.65 V	0.37		0.72	V
		2.3 V	0.48		0.87	
		3 V	0.56		0.97	
		4.5 V	0.71		1.14	
		5.5 V	0.71		1.21	
V _{OH}	I _{OH} = –100 μ A	1.65 V to 5.5 V	V _{CC} – 0.1			V
	I _{OH} = –4 mA	1.65 V	1.2			
	I _{OH} = –8 mA	2.3 V	1.9			
	I _{OH} = –16 mA	3 V	2.4			
	I _{OH} = –24 mA		2.3			
	I _{OH} = –32 mA	4.5 V	3.8			
V _{OL}	I _{OL} = 100 μ A	1.65 V to 5.5 V	0.1			V
	I _{OL} = 4 mA	1.65 V	0.45			
	I _{OL} = 8 mA	2.3 V	0.3			
	I _{OL} = 16 mA	3 V	0.4			
	I _{OL} = 24 mA		0.55			
	I _{OL} = 32 mA	4.5 V	0.55			
I _I	V _I = 5.5 V or GND	0 to 5.5 V			±5	μ A
I _{off}	V _I or V _O = 5.5 V	0			±10	μ A
I _{OZ}	V _O = V _{CC} or GND	1.65 V to 5.5 V			±10	μ A
I _{CC}	V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10	μ A
ΔI_{CC}	One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V			500	μ A
C _i	V _I = V _{CC} or GND	3.3 V			3.5	pF
C _O	V _O = V _{CC} or GND	3.3 V			6	pF

† T_A = 25°C

SN74LVC1G99

ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE

WITH 3-STATE OUTPUTS

SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

switching characteristics over recommended operating free-air temperature range, $C_L = 15$ pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.5	30.1	2.5	11.3	1.8	7.5	1.3	4.8	ns
	B		4.4	28.3	2.4	10.8	1.8	7.2	1.3	4.7	
	C		4.4	29.1	2.4	11.7	1.9	7.6	1.3	5	
	D		4.3	25.1	2.4	10.2	1.7	6.7	1.3	4.5	
t_{en}	\overline{OE}	Y	3.4	24.7	2.1	10	1.3	5.8	1	3.8	ns
t_{dis}	\overline{OE}	Y	4	15.5	2.7	7.5	3.5	7	2	5.5	ns

switching characteristics over recommended operating free-air temperature range, $C_L = 30$ pF or 50 pF (unless otherwise noted) (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 1.8\text{ V}$ $\pm 0.15\text{ V}$		$V_{CC} = 2.5\text{ V}$ $\pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$		$V_{CC} = 5\text{ V}$ $\pm 0.5\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd}	A	Y	4.6	30.8	2.6	11.7	2.4	8.4	1.8	5.5	ns
	B		4.6	28.9	2.6	11.3	2.3	8.2	1.8	5.4	
	C		4.4	29.8	2.5	12.3	2.5	8.6	1.8	5.7	
	D		4.3	25.7	2.5	10.7	2.4	7.6	1.6	5.2	
t_{en}	\overline{OE}	Y	4.2	25.2	2.4	11.3	2	7	1.7	4.7	ns
t_{dis}	\overline{OE}	Y	3.7	15	2	5.8	2.1	5.6	1	4.5	ns

operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC} = 1.8\text{ V}$	$V_{CC} = 2.5\text{ V}$	$V_{CC} = 3.3\text{ V}$	$V_{CC} = 5\text{ V}$	UNIT
		TYP	TYP	TYP	TYP	
C_{pd} Power dissipation capacitance	$f = 10\text{ MHz}$	19	20	22	27	pF

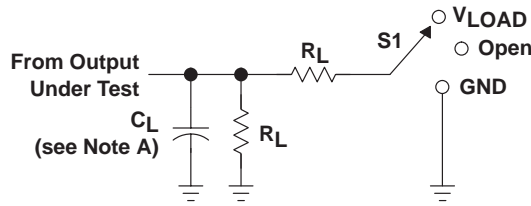
SN74LVC1G99

ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE

WITH 3-STATE OUTPUTS

SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

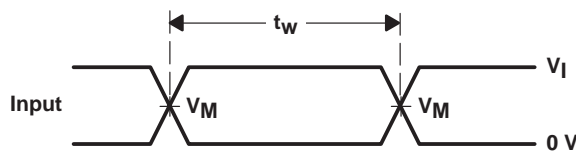
PARAMETER MEASUREMENT INFORMATION



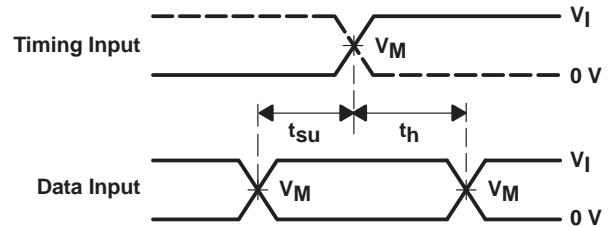
LOAD CIRCUIT

TEST	S_1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

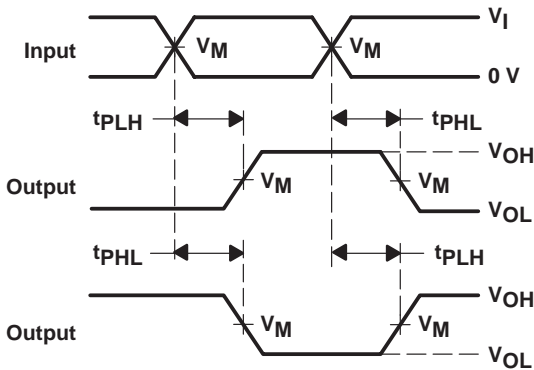
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	15 pF	1 M Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	15 pF	1 M Ω	0.3 V



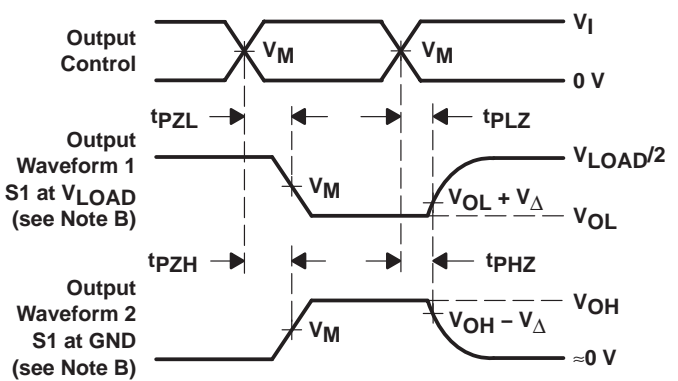
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - D. The outputs are measured one at a time, with one transition per measurement.
 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms



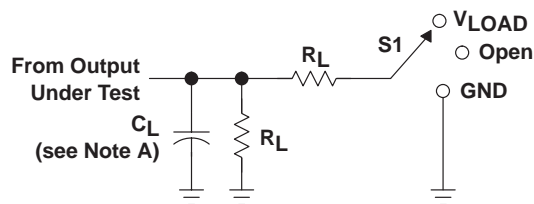
SN74LVC1G99

ULTRA-CONFIGURABLE MULTIPLE-FUNCTION GATE

WITH 3-STATE OUTPUTS

SCES609B – SEPTEMBER 2004 – REVISED JANUARY 2005

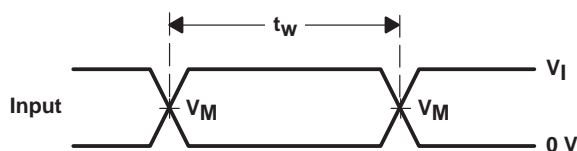
PARAMETER MEASUREMENT INFORMATION



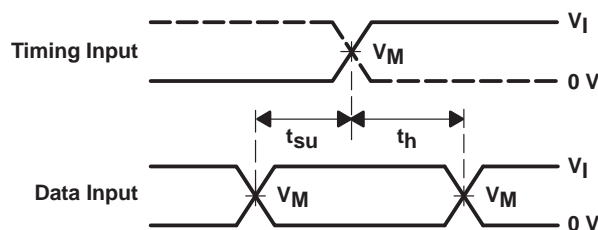
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

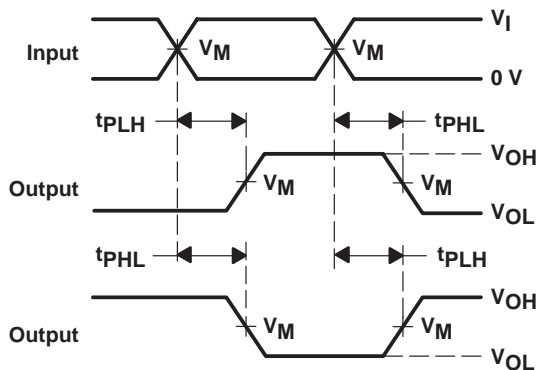
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



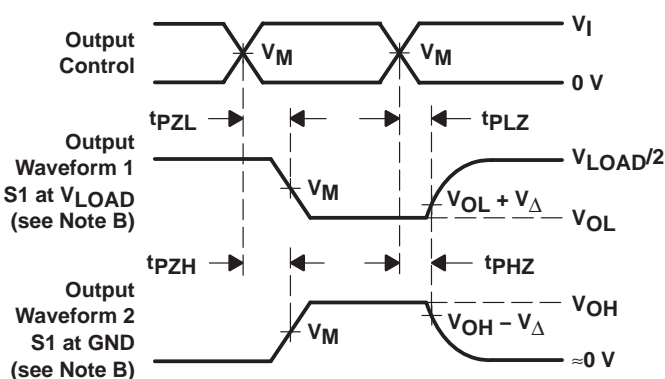
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10\text{ MHz}$, $Z_O = 50\ \Omega$.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 2. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74LVC1G99DCTR	ACTIVE	SM8	DCT	8	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G99DCTT	ACTIVE	SM8	DCT	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G99DCTTE4	ACTIVE	SM8	DCT	8	250	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G99DCUR	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G99DCURE4	ACTIVE	US8	DCU	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G99DCUT	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G99DCUTE4	ACTIVE	US8	DCU	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LVC1G99YEPR	NRND	WCSP	YEP	8	3000	TBD	SNPB	Level-1-260C-UNLIM
SN74LVC1G99YZPR	ACTIVE	WCSP	YZP	8	3000	Pb-Free (RoHS)	SNAGCU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

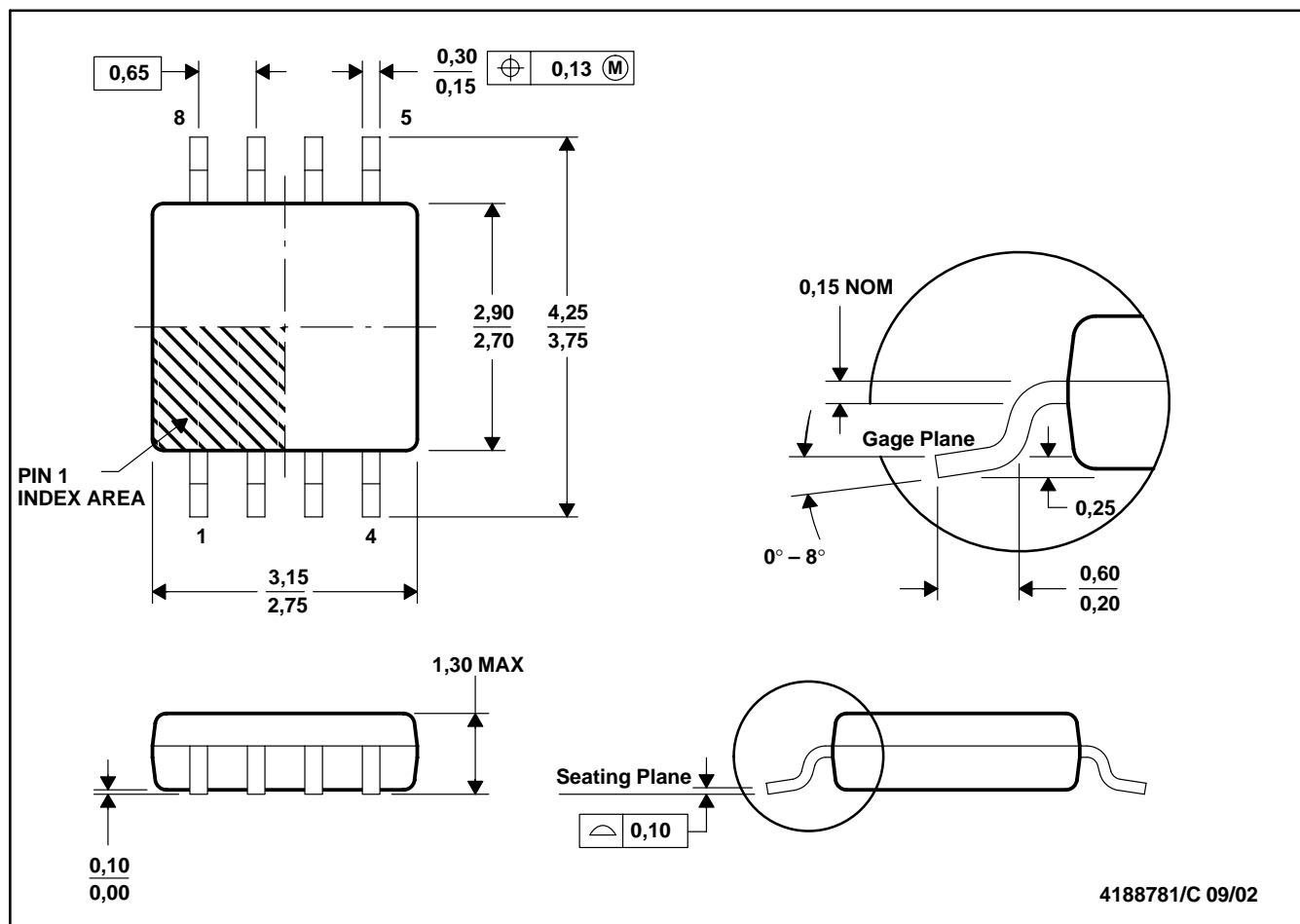
⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DCT (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion.
 - Falls within JEDEC MO-187 variation DA.

DCU (R-PDSO-G8)

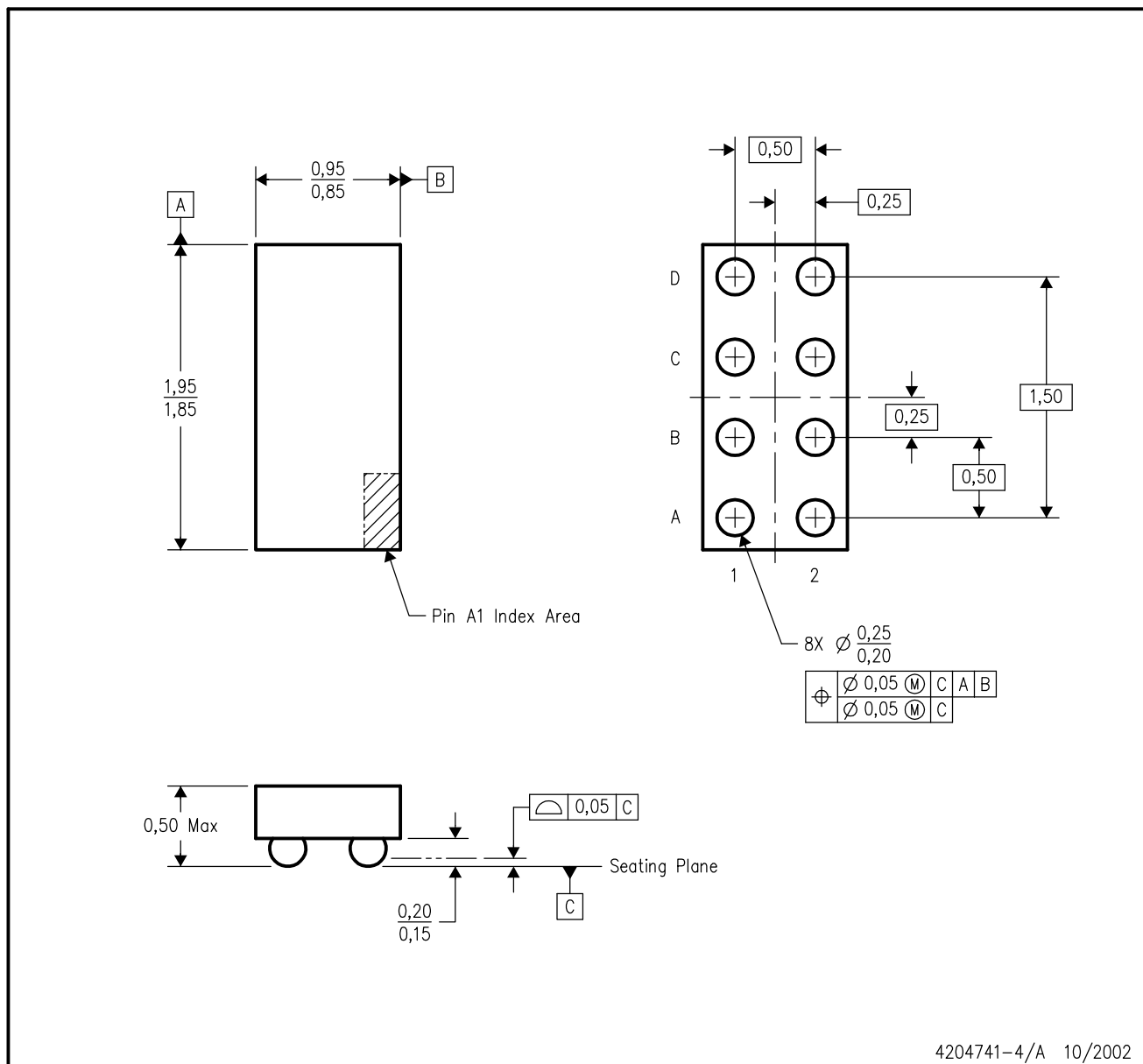
PLASTIC SMALL-OUTLINE PACKAGE (DIE DOWN)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-187 variation CA.

YZP (R-XBGA-N8)

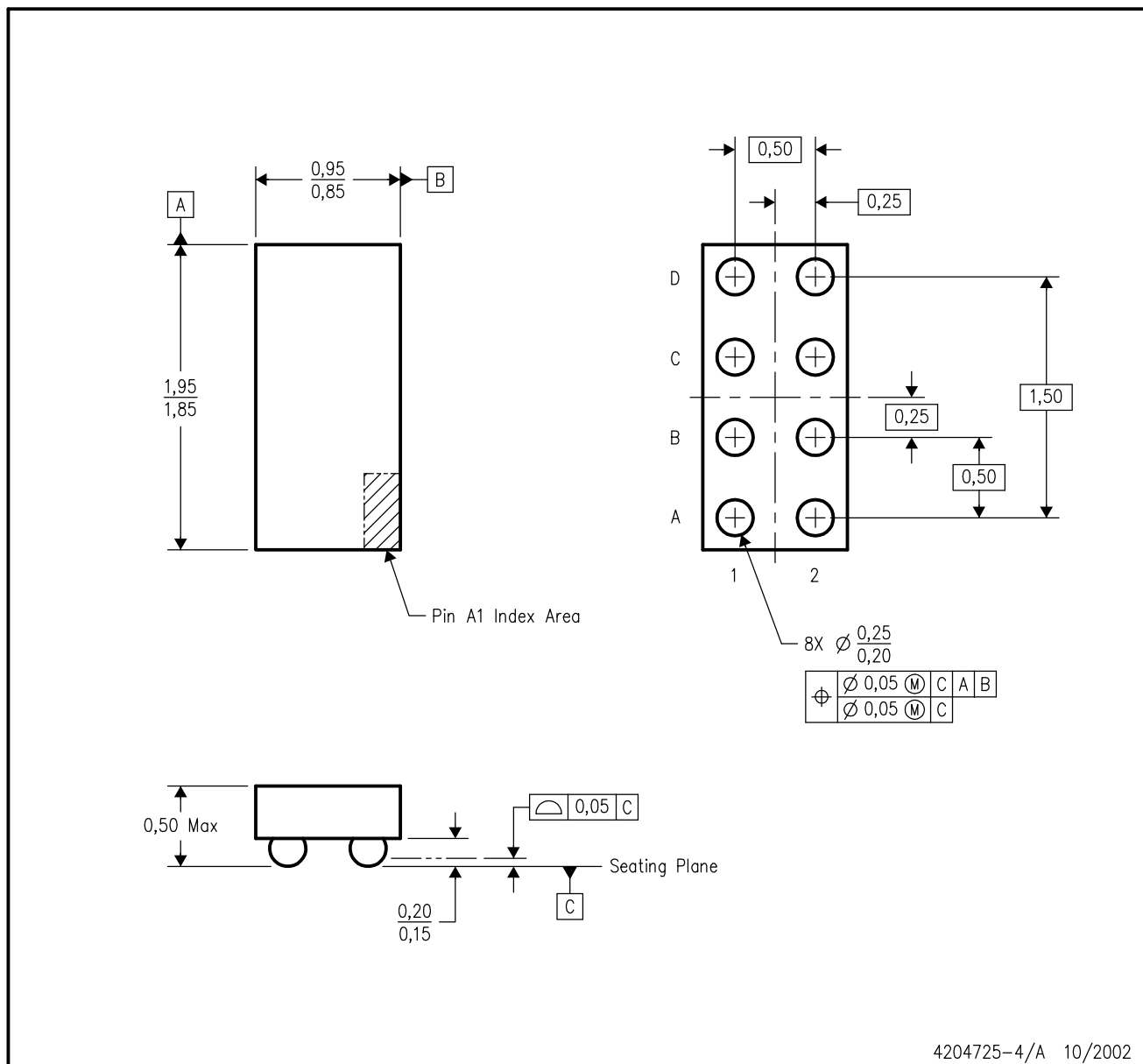
DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoFree™ package configuration.
 - D. This package is lead-free. Refer to the 8 YEP package (drawing 4204725) for tin-lead (SnPb).

YEP (R-XBGA-N8)

DIE-SIZE BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. NanoStar™ package configuration.
 - D. This package is tin-lead (SnPb). Refer to the 8 YZP package (drawing 4204741) for lead-free.

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