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- **Qualification in Accordance With AEC-Q100†**
- **Qualified for Automotive Applications**
- **Customer-Specific Configuration Control** Can Be Supported Along With **Major-Change Approval**
- Operating Range of 4.5 V to 5.5 V
- Max t_{pd} of 9.5 ns at 5 V
- Low Power Consumption, 20-µA Max I_{CC}
- ±8-mA Output Drive at 5 V
- Inputs Are TTL-Voltage Compatible
- **ESD Protection Level Per AEC-Q100** Classification
 - 2000-V (H2) Human-Body Model
 - 200-V (M3) Machine Model
 - 1000-V (C5) Charged-Device Model

DBV OR DCK PACKAGE (TOP VIEW) вΠ GND 3

□ v_{cc}

description/ordering information

The SN74AHCT1G32 is a single 2-input positive-OR gate. The device performs the Boolean function $Y = A + B \text{ or } Y = \overline{A \bullet B} \text{ in positive logic.}$

ORDERING INFORMATION

TA	PACKAGE	‡	ORDERABLE PART NUMBER	TOP-SIDE MARKING§
400C to 4050C	SOT (SOT-23) – DBV	Reel of 3000	CAHCT1G32QDBVRQ1	B32_
-40°C to 125°C	SOT (SC-70) - DCK	Reel of 3000	CAHCT1G32QDCKRQ1	BG_

[‡] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

FUNCTION TABLE

INPU	JTS	OUTPUT
Α	В	Υ
Н	Χ	Н
Х	Н	Н
L	L	L

logic diagram (positive logic)





Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



[†] Contact factory for details. Q100 qualification data available on request.

[§] The actual top-side marking has one additional character that designates the assembly/test site.

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	–0.5 V to 7 V
Input voltage range, V _I (see Note 1)	–0.5 V to 7 V
Output voltage range, V _O (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, $I_{ K }(V_{ } < 0)$	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V _{CC} or GND	±50 mA
Package thermal impedance, θ_{JA} (see Note 2): DBV package	206°C/W
DCK package	252°C/W
Storage temperature range, T _{stg}	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
Vcc	Supply voltage	4.5	5.5	V
VIH	High-level input voltage	2		V
V _{IL}	Low-level input voltage		8.0	V
VI	Input voltage	0	5.5	V
VO	Output voltage	0	VCC	V
lOH	High-level output current		-8	mA
lOL	Low-level output current		8	mA
Δt/Δν	Input transition rise or fall rate		20	ns/V
TA	Operating free-air temperature	-40	125	°C

NOTE 3: All unused inputs of the device must be held at VCC or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

	TEGT CONDITIONS	.,	T _A = 25°C			-40°C TO 85°C		-40°C TO 125°C		
PARAMETER	TEST CONDITIONS	VCC	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT
V	ΙΟΗ = -50 μΑ		4.4	4.5		4.4		4.4		V
VOH	$I_{OH} = -8 \text{ mA}$	4.5 V	3.94			3.8		3.7		٧
V	I _{OL} = 50 μA	45.77			0.1		0.1		0.1	
VOL	I _{OL} = 8 mA	4.5 V			0.36		0.44		0.52	V
lį	$V_I = 5.5 \text{ V or GND}$	0 V to 5.5 V			±0.1		±1		±1	μΑ
ICC	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			1		10		20	μΑ
Δl _{CC} ‡	One input at 3.4 V, Other inputs at V _{CC} or GND	5.5 V			1.35		1.5		1.65	mA
Ci	$V_I = V_{CC}$ or GND	5 V		2	10		10		10	pF

 $[\]ddagger$ This is the increase in supply current for each input at one of the specified TTL voltage levels, rather than 0 V or V_{CC}.



NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

^{2.} The package thermal impedance is calculated in accordance with JESD 51-7.

SN74AHCT1G32-Q1 SINGLE 2-INPUT POSITIVE-OR GATE

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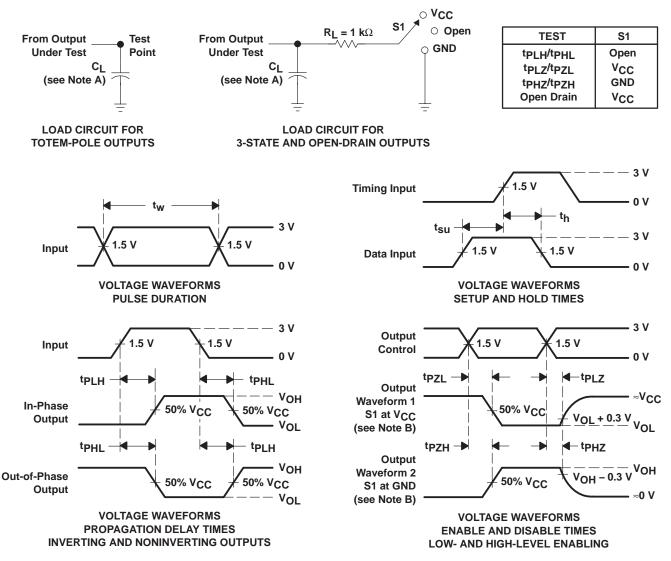
switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	LOAD	T,	ղ = 25°C	;	-40°C TC	0 85°C	-40°C TO	125°C										
PARAMETER	(INPUT)	(OUTPUT)	CAPACITANCE	MIN	TYP	MAX	MIN	MAX	MIN	MAX	UNIT									
t _{PLH}	A == D	V	0. 45 = 5		5	6.9	1	8		9.5										
t _{PHL}	A or B	T	Ť	Y	Y C[= 15]	ĭ	T T	Y	C _L = 15 pF	CL = 15 pr	f CL = 15 pr	CL = 15 pr		5	6.9	1	8		9.5	ns
t _{PLH}	A or B	V	C 50 pF		5.5	7.9	1	9		10.5	no									
t _{PHL}	AOIB	'	C _L = 50 pF		5.5	7.9	1	9		10.5	ns									

operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER	TEST CO	NDITIONS	TYP	UNIT
C _{pd}	Power dissipation capacitance	No load,	f = 1 MHz	11.5	pF

PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_I includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_Q = 50 \Omega$, $t_f \leq 3$ ns, $t_f \leq 3$ ns.
 - D. The outputs are measured one at a time, with one input transition per measurement.
 - E. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms





PACKAGE OPTION ADDENDUM

6-Dec-2006

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
CAHCT1G32QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM
CAHCT1G32QDCKRQ1	ACTIVE	SC70	DCK	5	3000	Pb-Free (RoHS)	CU NIPDAU	Level-1-260C-UNLIM

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DBV (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



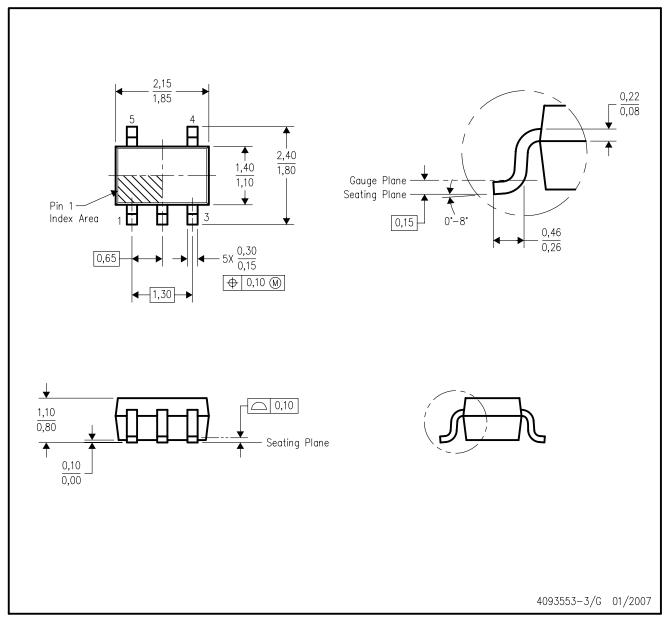
NOTES:

- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Falls within JEDEC MO-178 Variation AA.



DCK (R-PDSO-G5)

PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.

- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
- D. Falls within JEDEC MO-203 variation AA.



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