

PMN55LN

μTrenchMOS™ logic level FET

Rev. 01 — 24 March 2003

Product data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PMN55LN in SOT457 (TSOP6).

1.2 Features

- Low on-state resistance in small surface mount package.

1.3 Applications

- DC-to-DC primary side.

1.4 Quick reference data

- $V_{DS} \leq 20 \text{ V}$
- $I_D \leq 4.1 \text{ A}$
- $P_{tot} \leq 1.75 \text{ W}$
- $R_{DS(on)} \leq 65 \text{ m}\Omega$

2. Pinning information

Table 1: Pinning - SOT457 (TSOP6), simplified outline and symbol

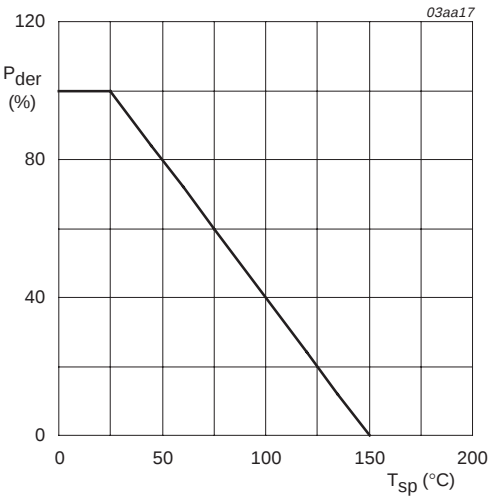
Pin	Description	Simplified outline	Symbol
1,2,5,6	drain (d)	Top view MBK092 SOT457 (TSOP6)	MBB076
3	gate (g)		
4	source (s)		

3. Limiting values

Table 2: Limiting values

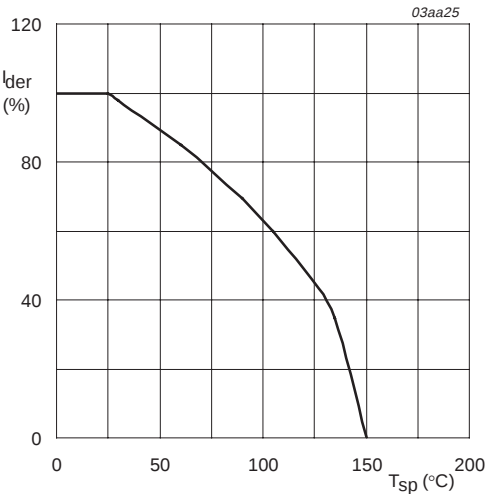
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$	-	20	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ }^{\circ}\text{C} \leq T_j \leq 150\text{ }^{\circ}\text{C}$; $R_{GS} = 20\text{ k}\Omega$	-	20	V
V_{GS}	gate-source voltage (DC)		-	± 15	V
I_D	drain current (DC)	$T_{sp} = 25\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	4.1	A
		$T_{sp} = 100\text{ }^{\circ}\text{C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	2.6	A
I_{DM}	peak drain current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	16.5	A
P_{tot}	total power dissipation	$T_{sp} = 25\text{ }^{\circ}\text{C}$; Figure 1	-	1.75	W
T_{stg}	storage temperature		-55	+150	$^{\circ}\text{C}$
T_j	junction temperature		-55	+150	$^{\circ}\text{C}$
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{sp} = 25\text{ }^{\circ}\text{C}$	-	1.45	A
I_{SM}	peak source (diode forward) current	$T_{sp} = 25\text{ }^{\circ}\text{C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	5.95	A



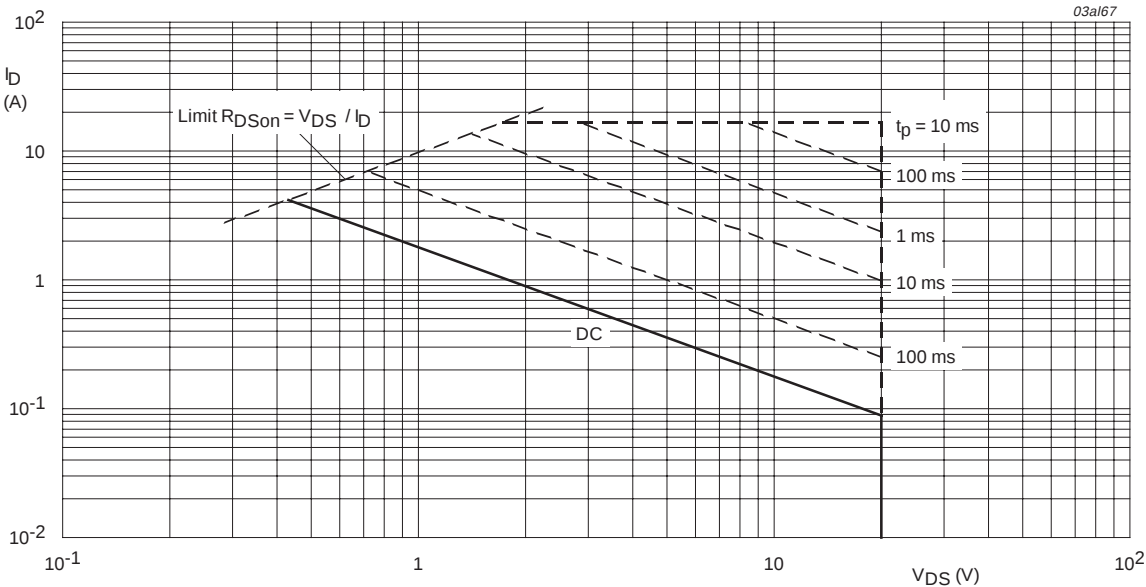
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25$ °C; I_{DM} is single pulse; $V_{GS} = 10$ V

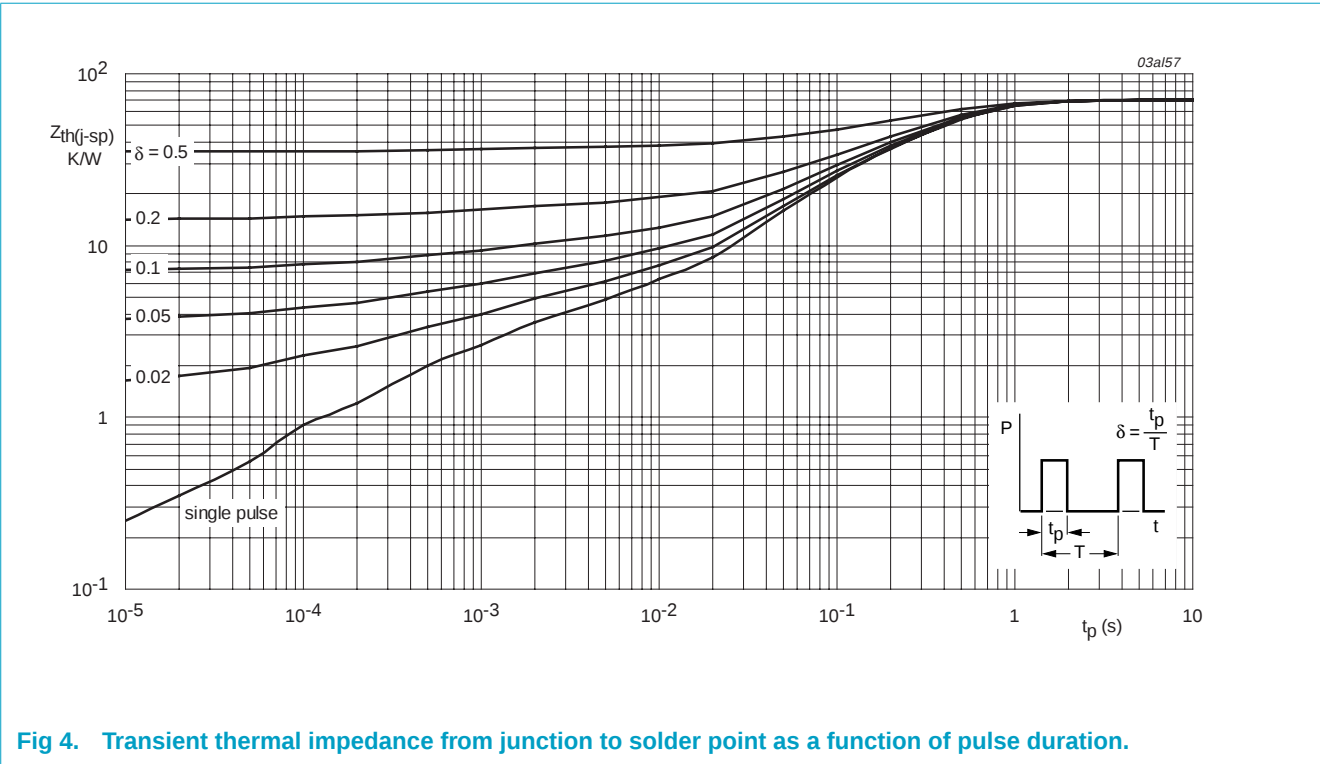
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Figure 4	-	-	70	K/W

4.1 Transient thermal impedance

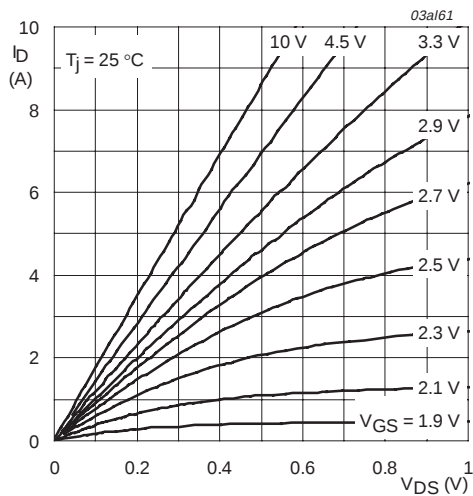


5. Characteristics

Table 4: Characteristics

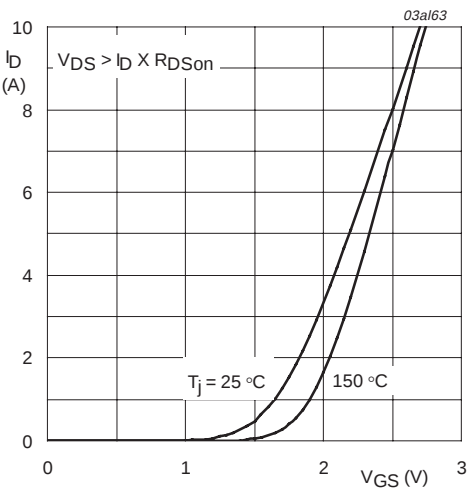
$T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	20	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	18	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$; Figure 9				
		$T_j = 25\text{ }^\circ\text{C}$	1	-	2	V
		$T_j = 150\text{ }^\circ\text{C}$	0.6	-	-	V
		$T_j = -55\text{ }^\circ\text{C}$	-	-	2.3	V
I_{DSS}	drain-source leakage current	$V_{DS} = 16\text{ V}$; $V_{GS} = 0\text{ V}$				
		$T_j = 25\text{ }^\circ\text{C}$	-	-	1	μA
		$T_j = 150\text{ }^\circ\text{C}$	-	-	100	μA
I_{GSS}	gate-source leakage current	$V_{GS} = \pm 15\text{ V}$; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$; $I_D = 2.5\text{ A}$; Figure 7 and 8				
		$T_j = 25\text{ }^\circ\text{C}$	-	55	65	m Ω
		$T_j = 150\text{ }^\circ\text{C}$	-	88	104	m Ω
		$V_{GS} = 4.5\text{ V}$; $I_D = 2\text{ A}$; Figure 7 and 8	-	70	82	m Ω
Dynamic characteristics						
$Q_{g(tot)}$	total gate charge	$I_D = 6\text{ A}$; $V_{DD} = 10\text{ V}$; $V_{GS} = 10\text{ V}$; Figure 13	-	13.1	-	nC
Q_{gs}	gate-source charge		-	1.9	-	nC
Q_{gd}	gate-drain (Miller) charge		-	2.3	-	nC
C_{iss}	input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 20\text{ V}$; $f = 1\text{ MHz}$; Figure 11	-	500	-	pF
C_{oss}	output capacitance		-	170	-	pF
C_{rss}	reverse transfer capacitance		-	110	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 10\text{ V}$; $R_D = 10\text{ }\Omega$; $V_{GS} = 4.5\text{ V}$; $R_G = 6\text{ }\Omega$	-	10	-	ns
t_r	rise time		-	14	-	ns
$t_{d(off)}$	turn-off delay time		-	23	-	ns
t_f	fall time		-	12	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	$I_S = 1.7\text{ A}$; $V_{GS} = 0\text{ V}$; Figure 12	-	0.8	1.2	V



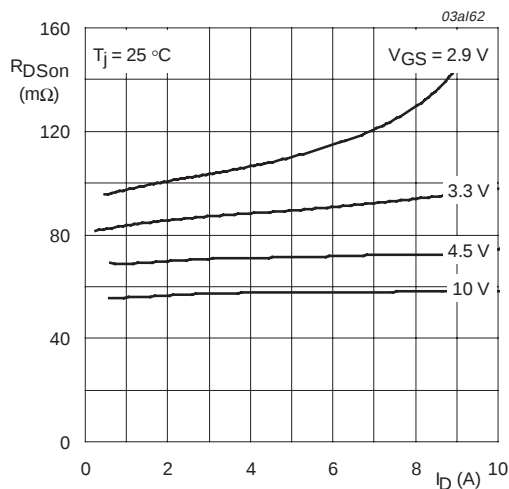
$T_j = 25\text{ °C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



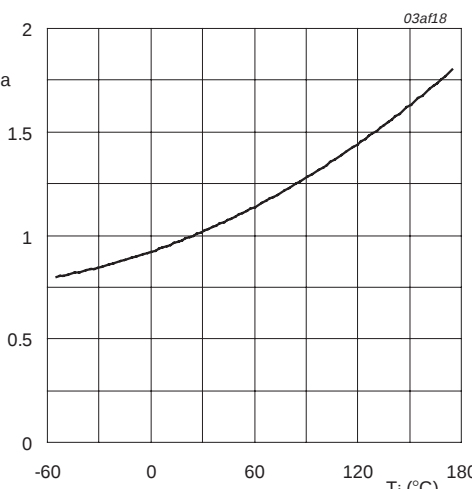
$T_j = 25\text{ °C}$ and 150 °C ; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



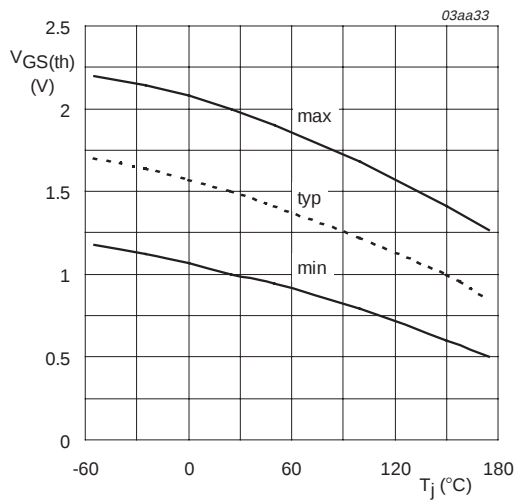
$T_j = 25\text{ °C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



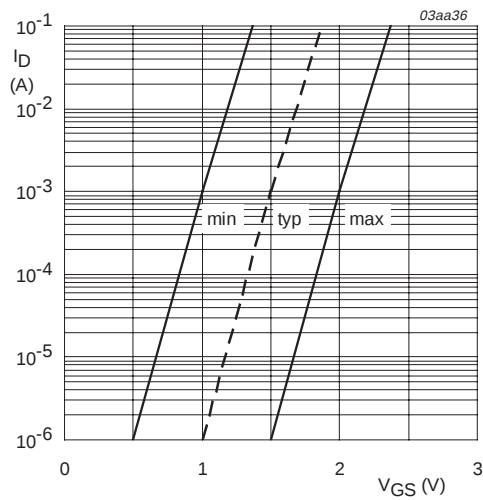
$$a = \frac{R_{DSon}}{R_{DSon(25\text{ °C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



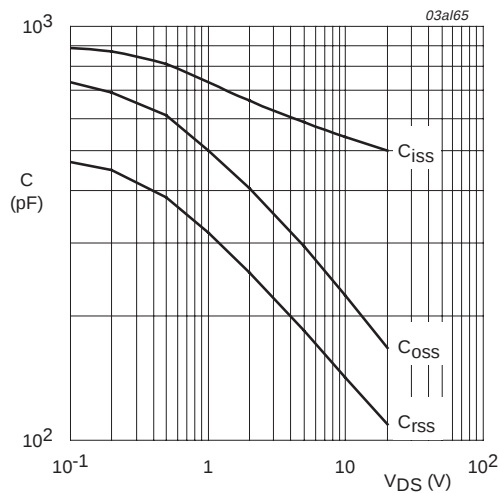
$I_D = 1\text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



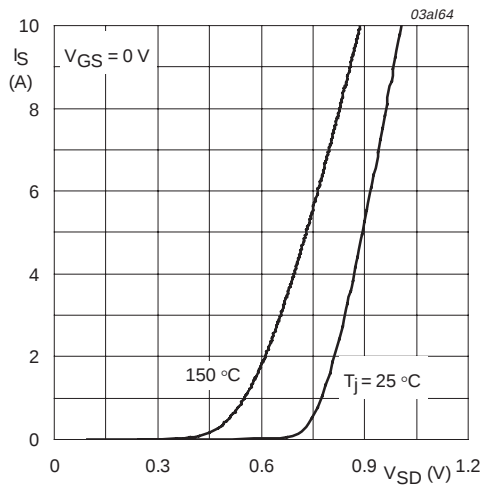
$T_j = 25\text{ °C}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



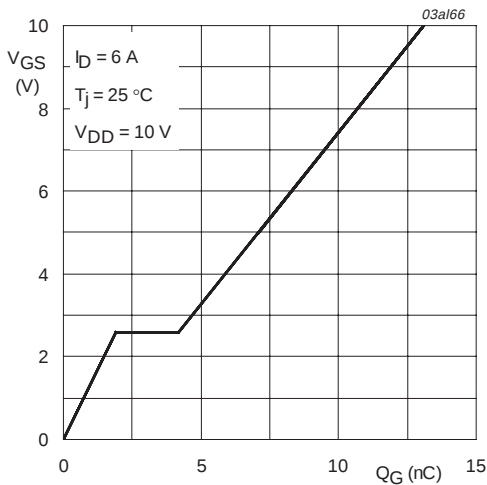
$V_{GS} = 0\text{ V}; f = 1\text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_J = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{GS} = 0\text{ V}$

Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$I_D = 6\text{ A}$; $V_{DD} = 10\text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

Plastic surface mounted package; 6 leads

SOT457

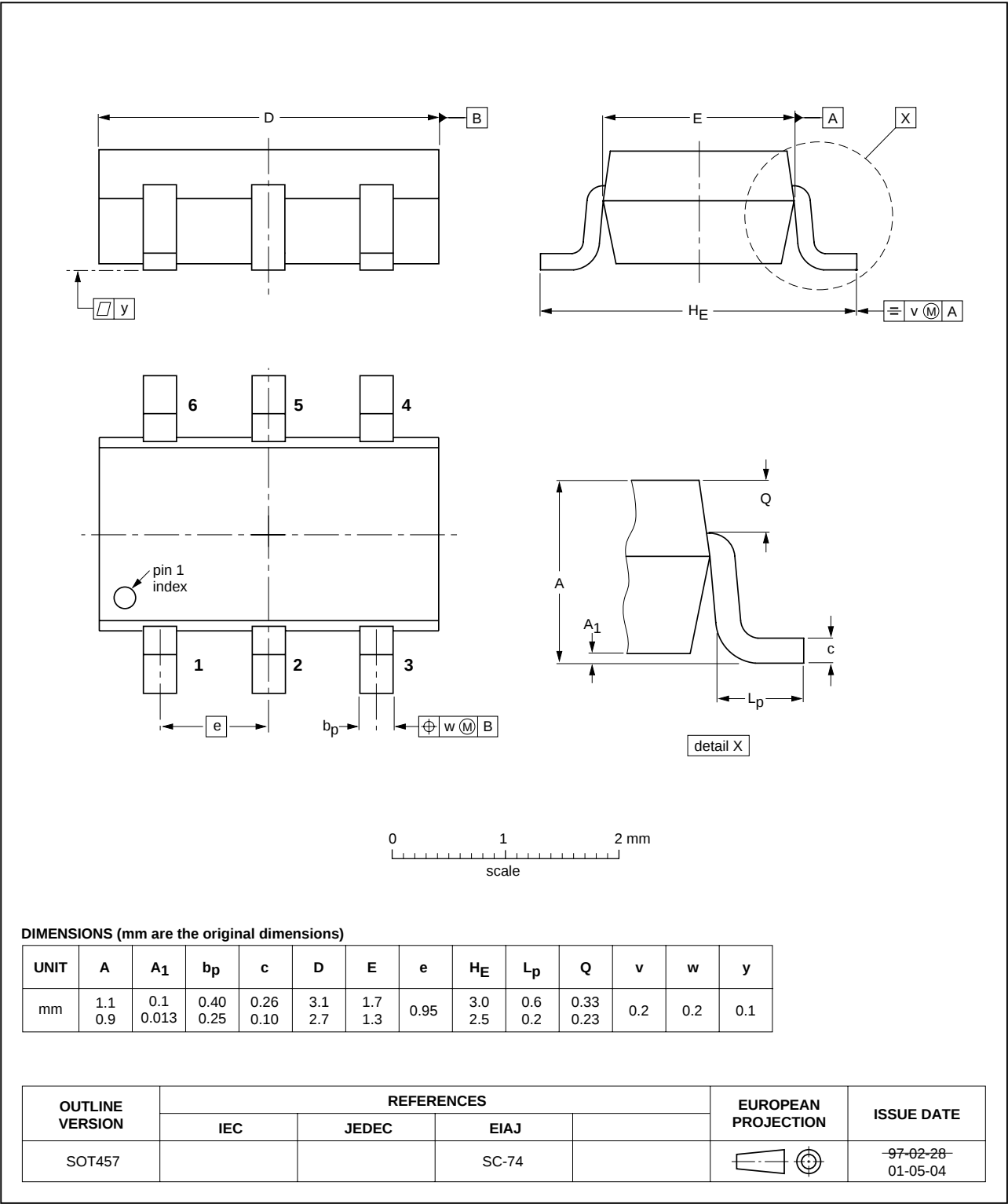


Fig 14. SOT457 (TSOP6).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20030324	-	Product data (9397 750 10937)

8. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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