

HD74ACT161/HD74ACT163

Synchronous Presetable Binary Counter

REJ03D0279-0200Z
(Previous ADE-205-402 (Z))
Rev.2.00
Jul.16.2004

Description

The HD74ACT161 and HD74ACT163 are high-speed synchronous modulo-16 binary counters. They are synchronously presetable for application in programmable dividers and have two types of Count Enable inputs plus a Terminal Count output for versatility in forming synchronous multistage counters. The HD74ACT161 have an asynchronous Master Reset input that overrides all other inputs and forces the outputs Low. The HD74ACT163 has a Synchronous Reset input that overrides counting and parallel loading and allows the outputs to be simultaneously reset on the rising edge of the clock.

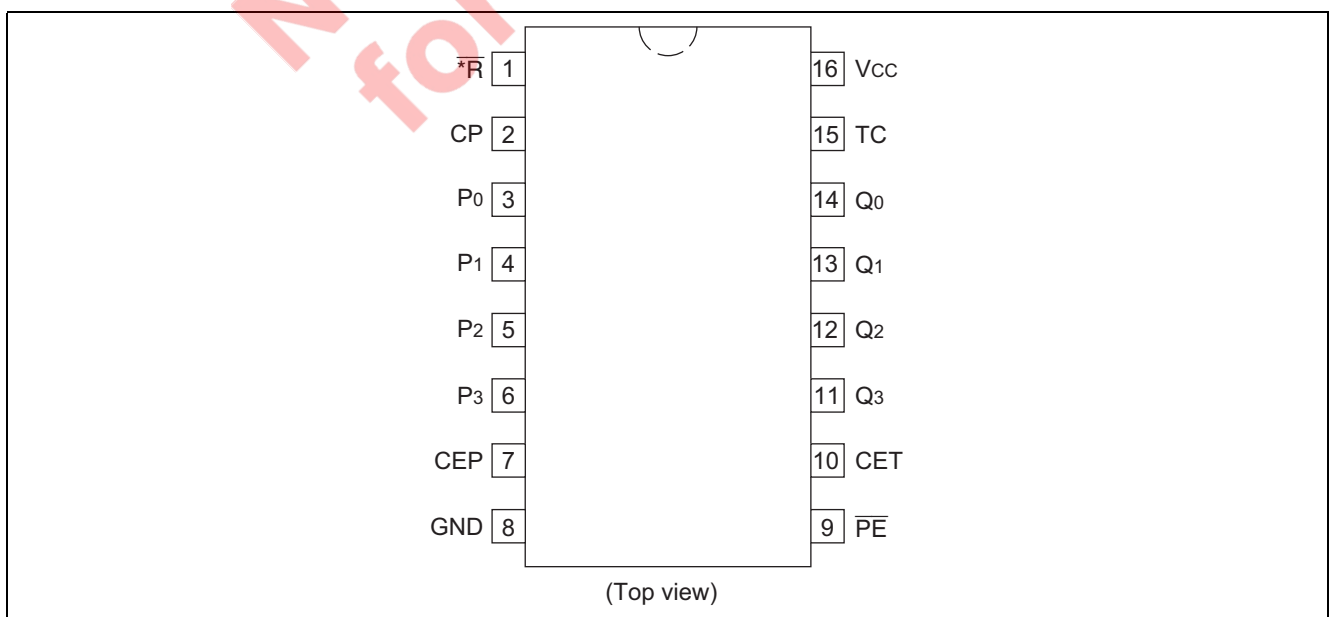
Features

- Synchronous Counting and Loading
- High-Speed Synchronous Expansion
- Typical Count Rate of 125 MHz
- Outputs Source/Sink 24 mA
- HD74ACT161 and HD74ACT163 have TTL-Compatible Inputs
- Ordering Information: Ex. HD74ACT161

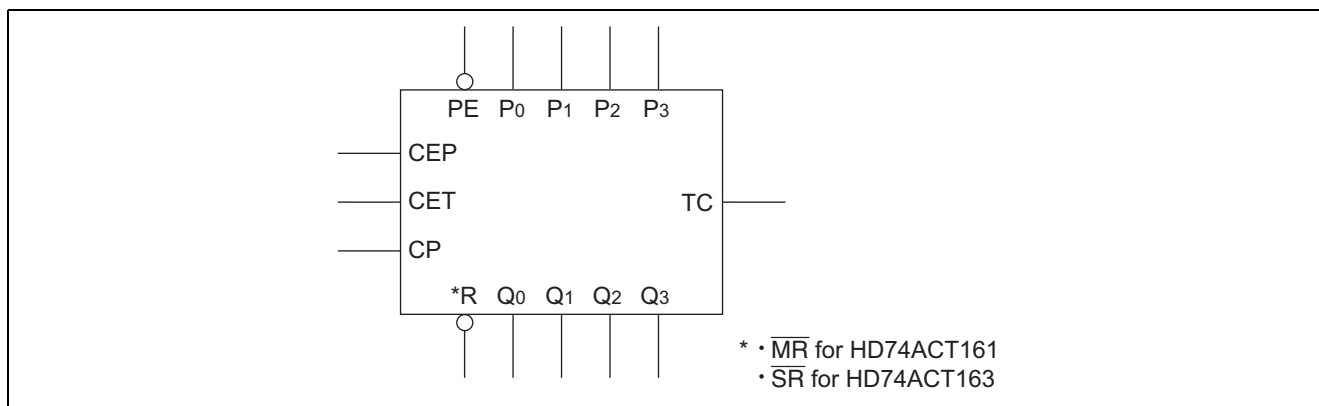
Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)
HD74ACT161FPEL	SOP-16 pin (JEITA)	FP-16DAV	FP	EL (2,000 pcs/reel)
HD74ACT161RPEL	SOP-16 pin (JEDEC)	FP-16DNV	RP	EL (2,500 pcs/reel)

Notes: 1. Please consult the sales office for the above package availability.
2. The packages with lead-free pins are distinguished from the conventional products by adding V at the end of the package code.

Pin Arrangement



Logic Symbol



Pin Names

CEP	Count Enable Parallel Input
CET	Count Enable Trickle Input
CP	Clock Pulse Input
$\overline{MR}$ (HD74ACT161)	Asynchronous Master Reset Input
$\overline{SR}$ (HD74ACT163)	Synchronous Reset Input
P_0 to P_3	Parallel Data Inputs
$\overline{PE}$	Parallel Enable Input
Q_0 to Q_3	Flip-Flop Outputs
TC	Terminal Count Output

Functional Description

The HD74ACT161 and HD74ACT163 count in modulo-16 binary sequence. From state 15 (HHHH) they increment to state 0 (LLLL). The clock inputs of all flip-flops are driven in parallel through a clock buffer. Thus all changes of the Q outputs (except due to Master Reset of the HD74ACT161) occur as a reset of, and synchronous with, the Low-to-High transition of the CP input signal. The circuits have four fundamental modes of operation, in order of precedence: asynchronous reset (HD74ACT161), synchronous reset (HD74ACT163), parallel load, countup and hold. Five control inputs – Master Reset ($\overline{MR}$, HD74ACT161), Synchronous Reset ($\overline{SR}$, HD74ACT163), Parallel Enable ($\overline{PE}$), Count Enable Parallel (CEP) and Count Enable Trickle (CET) – determine the mode of operation, as shown in the Mode Select Table. A Low signal on $\overline{MR}$ overrides all other inputs and asynchronously forces all outputs Low. A Low signal on $\overline{SR}$ overrides counting and parallel loading and allows all outputs to go Low on the next rising edge of CP. A Low signal on $\overline{PE}$ overrides counting and allows information on the Parallel Data (P_n) inputs to be loaded into the flip-flops on the next rising edge of CP. With $\overline{PE}$ and $\overline{MR}$ (HD74ACT161) or $\overline{SR}$ (HD74ACT163) High, CEP and CET permit counting when both are High. Conversely, a Low signal on either CEP or CET inhibits counting.

The HD74ACT161 and HD74ACT163 use D-type edge-triggered flip-flops and changing the $\overline{SR}$, $\overline{PE}$, CEP and CET inputs when the CP is in either state does not cause errors, provided that the recommended setup and hold times, with respect to the rising edge of CP, are observed. The Terminal Count (TC) output is High when CET is High and counter is in state 15. To implement synchronous multistage counters, the TC outputs can be used with the CEP and CET inputs in two different ways. The TC output is subject to decoding spikes due to internal race conditions and is therefore not recommended for use as a clock or asynchronous reset for flip-flops, counters or registers.

Logic Equations: Count Enable = $CEP \cdot CET \cdot \overline{PE}$

$$TC = Q_0 \cdot Q_1 \cdot Q_2 \cdot Q_3 \cdot CET$$

Mode Select Table

$\overline{SR}^{*1}$	$\overline{PE}$	CET	CEP	Action on the Rising Clock Edge ($\uparrow$)
L	X	X	X	Reset (Clear)
H	L	X	X	Load ($P_n \rightarrow Q_n$)
H	H	H	H	Count (Increment)
H	H	L	X	No change (Hold)
H	H	X	L	No change (Hold)

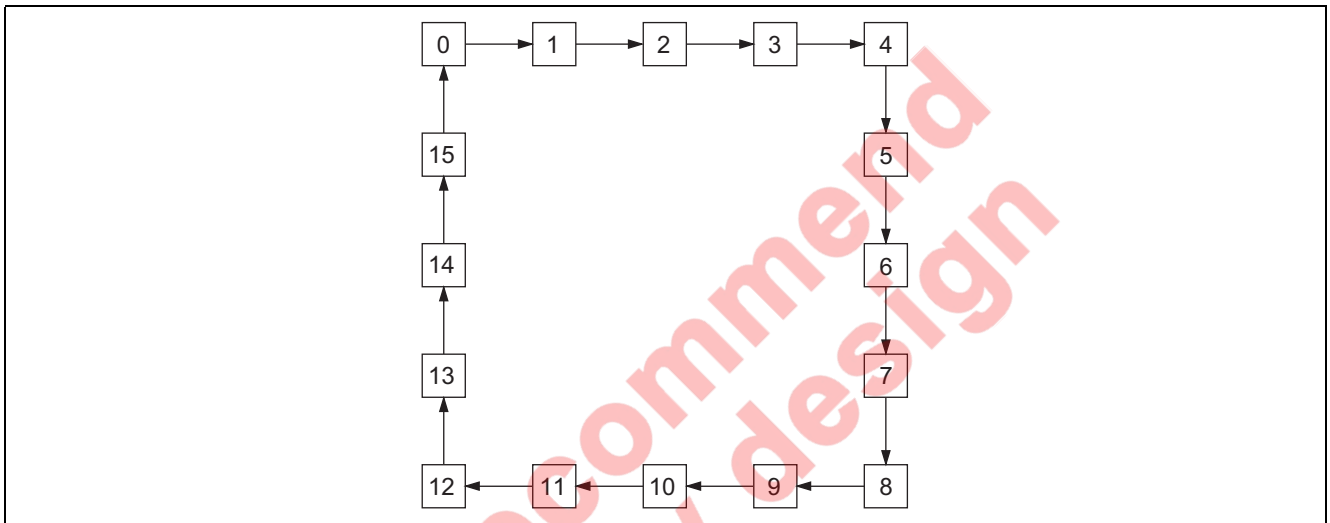
Note: 1. For HD74ACT163

H : High Voltage Level

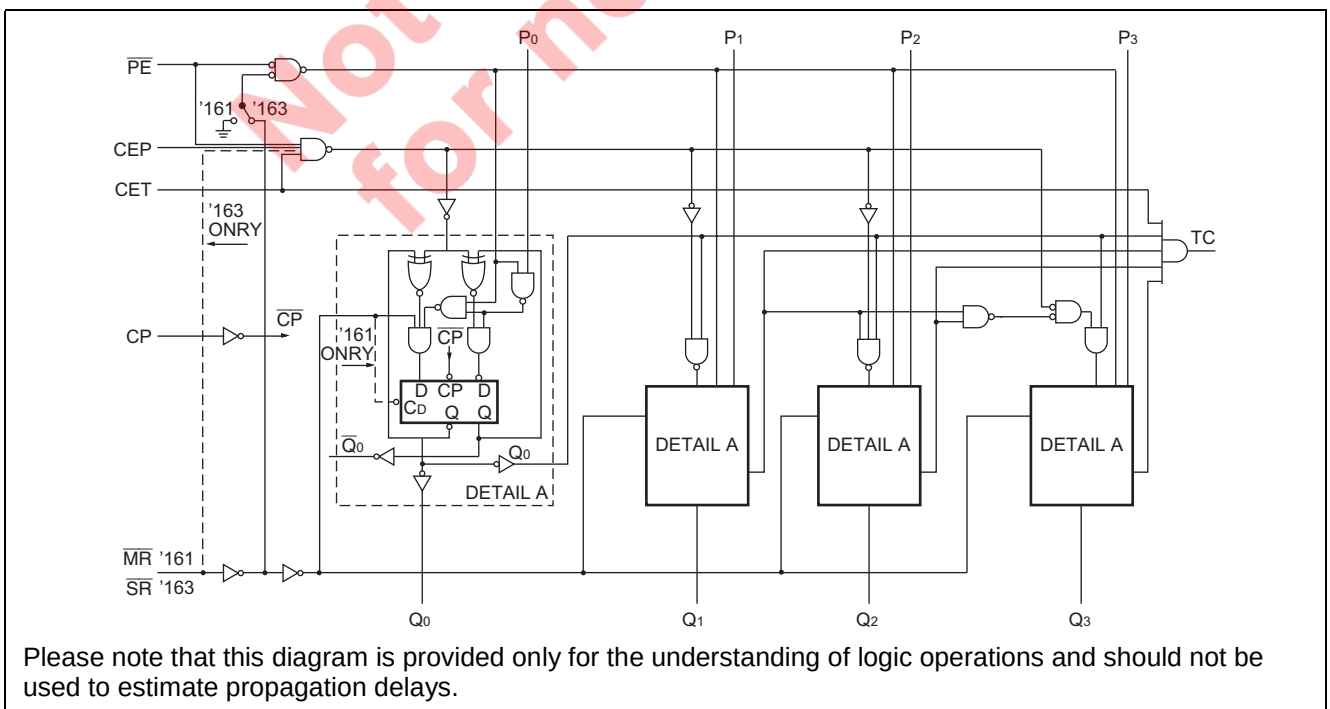
L : Low Voltage Level

X : Immaterial

State Diagram



Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	-0.5 to 7	V	
DC input diode current	I_{IK}	-20	mA	$V_I = -0.5V$
		20	mA	$V_I = V_{CC}+0.5V$
DC input voltage	V_I	-0.5 to $V_{CC}+0.5$	V	
DC output diode current	I_{OK}	-50	mA	$V_O = -0.5V$
		50	mA	$V_O = V_{CC}+0.5V$
DC output voltage	V_O	-0.5 to $V_{CC}+0.5$	V	
DC output source or sink current	I_O	± 50	mA	
DC V_{CC} or ground current per output pin	I_{CC}, I_{GND}	± 50	mA	
Storage temperature	T_{stg}	-65 to +150	°C	

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
Input and output voltage	V_I, V_O	0 to V_{CC}	V	
Operating temperature	T_a	-40 to +85	°C	
Input rise and fall time (except Schmitt inputs) V_{IN} 0.8 to 2.0 V	t_r, t_f	8	ns/V	$V_{CC} = 4.5V$ $V_{CC} = 5.5V$

DC Characteristics

Item	Sym- bol	V_{CC} (V)	$T_a = 25^\circ C$			$T_a = -40 \text{ to } +85^\circ C$		Unit	Condition
			min.	typ.	max.	min.	max.		
Input voltage	V_{IH}	4.5	2.0	1.5	—	2.0	—	V	$V_{OUT} = 0.1 V \text{ or } V_{CC}-0.1 V$
		5.5	2.0	1.5	—	2.0	—		
	V_{IL}	4.5	—	1.5	0.8	—	0.8		$V_{OUT} = 0.1 V \text{ or } V_{CC}-0.1 V$
		5.5	—	1.5	0.8	—	0.8		
Output voltage	V_{OH}	4.5	4.4	4.49	—	4.4	—	V	$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OUT} = -50 \mu A$
		5.5	5.4	5.49	—	5.4	—		
		4.5	3.94	—	—	3.80	—		$V_{IN} = V_{IL}$ $I_{OH} = -24 mA$
		5.5	4.94	—	—	4.80	—		$I_{OH} = -24 mA$
	V_{OL}	4.5	—	0.001	0.1	—	0.1		$V_{IN} = V_{IL} \text{ or } V_{IH}$ $I_{OUT} = 50 \mu A$
		5.5	—	0.001	0.1	—	0.1		
		4.5	—	—	0.32	—	0.37		$V_{IN} = V_{IL}$ $I_{OL} = 24 mA$
		5.5	—	—	0.32	—	0.37		$I_{OL} = 24 mA$
Input current	I_{IN}	5.5	—	—	± 0.1	—	± 1.0	μA	$V_{IN} = V_{CC} \text{ or } GND$
I_{CC} /input current	I_{CCT}	5.5	—	0.6	—	—	1.5	mA	$V_{IN} = V_{CC}-2.1 V$
Dynamic output current*	I_{OLD}	5.5	—	—	—	86	—	mA	$V_{OLD} = 1.1 V$
	I_{OHD}	5.5	—	—	—	-75	—	mA	$V_{OHD} = 3.85 V$
Quiescent supply current	I_{CC}	5.5	—	—	8.0	—	80	μA	$V_{IN} = V_{CC} \text{ or } ground$

*Maximum test duration 2.0 ms, one output loaded at a time.

AC Characteristics: HD74ACT161

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF			Ta = -40°C to +85°C C _L = 50 pF		Unit
			Min	Typ	Max	Min	Max	
Maximum count frequency	f _{max}	5.0	115	125	—	100	—	MHz
Propagation delay CP to Q _n ($\overline{\text{PE}}$ Input HIGH or LOW)	t _{PLH}	5.0	1.0	5.5	9.5	1.0	10.5	ns
Propagation delay CP to Q _n (PE Input HIGH or LOW)	t _{PLH}	5.0	1.0	6.0	10.5	1.0	11.5	ns
Propagation delay CP to TC	t _{PLH}	5.0	1.0	7.0	11.0	1.0	12.5	ns
Propagation delay CP to TC	t _{PHL}	5.0	1.0	8.0	12.5	1.0	13.5	ns
Propagation delay CET to TC	t _{PLH}	5.0	1.0	5.5	8.5	1.0	10.0	ns
Propagation delay CET to TC	t _{PHL}	5.0	1.0	6.0	9.5	1.0	10.5	ns
Propagation delay MR to Q _n	t _{PHL}	5.0	1.0	6.0	10.0	1.0	11.0	ns
Propagation delay MR to TC	t _{PHL}	5.0	1.0	8.0	13.5	1.0	14.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

AC Operating Requirements: HD74ACT161

Item	Symbol	V _{CC} (V)*1	Ta = +25°C C _L = 50 pF		Ta = -40°C to +85°C C _L = 50 pF	Unit
			Typ	Guaranteed Minimum		
Set-up time, HIGH or LOW P _n to CP	t _{su}	5.0	4.0	9.5	11.5	ns
Hold time, HIGH or LOW P _n to CP	t _h	5.0	-5.0	0	0	ns
Setup time, HIGH or LOW MR to CP	t _{su}	5.0	4.0	8.5	9.5	ns
Hold time, HIGH or LOW MR to CP	t _h	5.0	-5.5	-0.5	-0.5	ns
Setup time, HIGH or LOW $\overline{\text{PE}}$ to CP	t _{su}	5.0	4.0	8.5	9.5	ns
Hold time, HIGH or LOW $\overline{\text{PE}}$ to CP	t _h	5.0	-5.5	-0.5	-0.5	ns
Setup time, HIGH or LOW CEP or CET to CP	t _{su}	5.0	2.5	5.5	6.5	ns
Hold time, HIGH or LOW CEP or CET to CP	t _h	5.0	-3.0	0	0	ns
Clock pulse width (Load) HIGH or LOW	t _w	5.0	2.0	3.0	3.5	ns
Clock pulse width (Count) HIGH or LOW	t _w	5.0	2.0	3.0	3.5	ns
MR pulse width, LOW	t _w	5.0	3.0	3.0	7.5	ns
Recovery time MR to CP	t _{rec}	5.0	0	0	0.5	ns

Note: 1. Voltage Range 5.0 is 5.0 V ± 0.5 V

Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	C_{PD}	45.0	pF	$V_{CC} = 5.0 \text{ V}$

AC Characteristics: HD74ACT163

Item	Symbol	$V_{CC} \text{ (V)}^{*1}$	$T_a = +25^\circ\text{C}$ $C_L = 50 \text{ pF}$			$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50 \text{ pF}$		Unit
			Min	Typ	Max	Min	Max	
Maximum count frequency	f_{max}	5.0	120	128	—	105	—	MHz
Propagation delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	t_{PLH}	5.0	1.0	5.5	10.0	1.0	11.0	ns
Propagation delay CP to Q_n ($\overline{PE}$ Input HIGH or LOW)	t_{PHL}	5.0	1.0	6.0	11.0	1.0	12.0	ns
Propagation delay CP to TC	t_{PLH}	5.0	1.0	7.0	11.5	1.0	13.5	ns
Propagation delay CP to TC	t_{PHL}	5.0	1.0	8.0	13.5	1.0	15.0	ns
Propagation delay CET to TC	t_{PLH}	5.0	1.0	5.5	9.0	1.0	10.5	ns
Propagation delay CET to TC	t_{PHL}	5.0	1.0	6.0	10.0	1.0	11.0	ns

Note: 1. Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

AC Operating Requirements: HD74ACT163

Item	Symbol	$V_{CC} \text{ (V)}^{*1}$	$T_a = +25^\circ\text{C}$ $C_L = 50 \text{ pF}$		$T_a = -40^\circ\text{C to } +85^\circ\text{C}$ $C_L = 50 \text{ pF}$	Unit
			Typ	Guaranteed Minimum		
Set-up time, HIGH or LOW P_n to CP	t_{su}	5.0	4.0	10.0	12.0	ns
Hold time, HIGH or LOW P_n to CP	t_h	5.0	−5.0	0.5	0.5	ns
Setup time, HIGH or LOW $\overline{SR}$ to CP	t_{su}	5.0	4.0	10.0	11.5	ns
Hold time, HIGH or LOW $\overline{SR}$ to CP	t_h	5.0	−5.5	−0.5	−0.5	ns
Setup time, HIGH or LOW $\overline{PE}$ to CP	t_{su}	5.0	4.0	8.5	10.5	ns
Hold time, HIGH or LOW $\overline{PE}$ to CP	t_h	5.0	−5.5	−0.5	0	ns
Setup time, HIGH or LOW CEP or CET to CP	t_{su}	5.0	2.5	5.5	6.5	ns
Hold time, HIGH or LOW CEP or CET to CP	t_h	5.0	−3.0	0	0.5	ns
Clock pulse width (Load) HIGH or LOW	t_w	5.0	2.0	3.5	3.5	ns
Clock pulse width (Count) HIGH or LOW	t_w	5.0	2.0	3.5	3.5	ns

Note: 1. Voltage Range 5.0 is $5.0 \text{ V} \pm 0.5 \text{ V}$

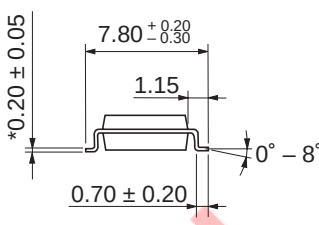
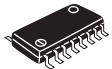
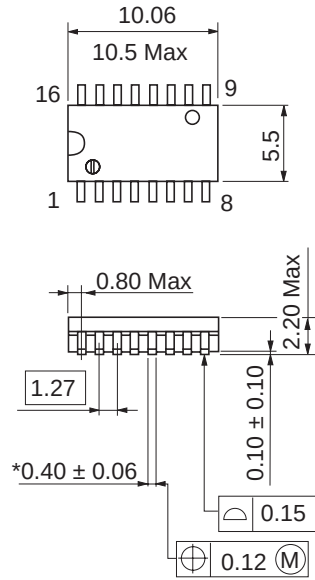
Capacitance

Item	Symbol	Typ	Unit	Condition
Input capacitance	C_{IN}	4.5	pF	$V_{CC} = 5.5 \text{ V}$
Power dissipation capacitance	C_{PD}	45.0	pF	$V_{CC} = 5.0 \text{ V}$

Not recommend
for new design

Package Dimensions

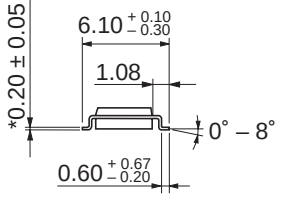
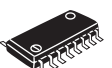
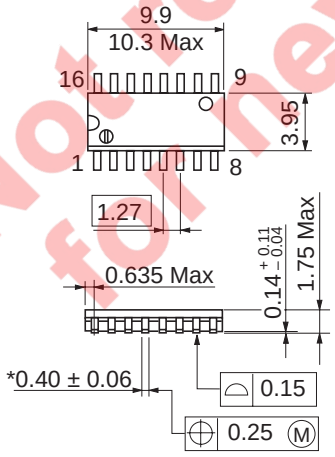
As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DAV
JEDEC	—
JEITA	Conforms
Mass (reference value)	0.24 g

As of January, 2003
Unit: mm



*Ni/Pd/Au plating

Package Code	FP-16DNV
JEDEC	Conforms
JEITA	Conforms
Mass (reference value)	0.15 g

Renesas Technology Corp. Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500 Fax: <1> (408) 382-7501

Renesas Technology Europe Limited.

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, United Kingdom
Tel: <44> (1628) 585 100, Fax: <44> (1628) 585 900

Renesas Technology Europe GmbH

Dornacher Str. 3, D-85622 Feldkirchen, Germany
Tel: <49> (89) 380 70 0, Fax: <49> (89) 929 30 11

Renesas Technology Hong Kong Ltd.

7/F., North Tower, World Finance Centre, Harbour City, Canton Road, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2375-6836

Renesas Technology Taiwan Co., Ltd.

FL 10, #99, Fu-Hsing N. Rd., Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

26/F., Ruijin Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1, Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001