

HD74CBT1G125

Single FET Bus Switch

REJ03D0815-0100
(Previous: ADE-205-645)
Rev.1.00
Apr 07, 2006

Description

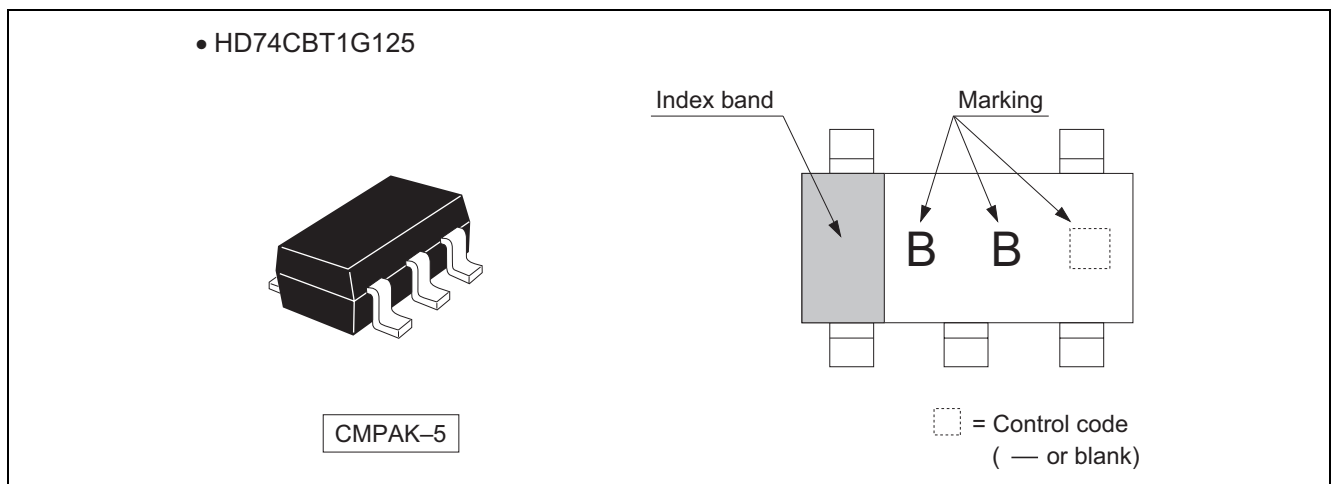
The HD74CBT1G125 features a single high-speed line switch. The switch is disabled when the output enable (\overline{OE}) input is high.

Features

- Minimal propagation delay through the switch.
- $5\ \Omega$ switch connection between two ports.
- TTL-compatible input levels.
- Ultra low quiescent power.
— Ideally suited for notebook applications.
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74CBT1G125CME	CMPAK-5pin	PTSP0005ZC-A (CMPAK-5V)	CM	E (3,000pcs / Reel)

Outline and Article Indication



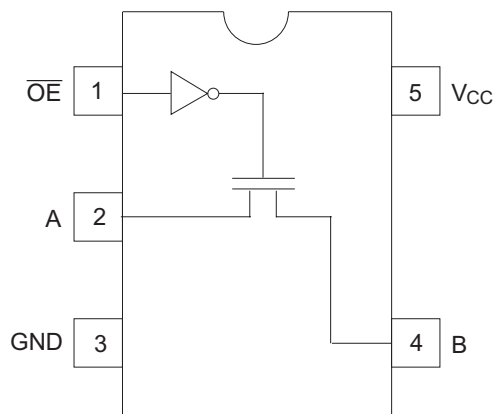
Function Table

Input \overline{OE}	Function
L	A port = B port
H	Disconnect

H: High level

L: Low level

Pin Arrangement



(Top view)

Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage range	V_{CC}	-0.5 to 7.0	V	
Input voltage range ^{*1}	V_I	-0.5 to 7.0	V	
Input clamp current	I_{IK}	-50	mA	$V_I < 0$
Continuous output current	I_O	128	mA	$V_O = 0$ to V_{CC}
Continuous current through V_{CC} or GND	I_{CC} or I_{GND}	± 100	mA	
Maximum power dissipation at $T_a = 25^\circ\text{C}$ (in still air) ^{*2}	P_T	200	mW	
Storage temperature	T_{stg}	-65 to 150	$^\circ\text{C}$	

Notes: The absolute maximum ratings are values which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

1. The input and output voltage ratings may be exceeded even if the input and output clamp-current ratings are observed.
2. The maximum package power dissipation was calculated using a junction temperature of 150°C .

Recommended Operating Conditions

Item	Symbol	Min	Max	Unit	Conditions
Supply voltage range	V_{CC}	4.0	5.5	V	
Input voltage range	V_I	0	5.5	V	
Output voltage range	V_{IO}	0	5.5	V	
Input transition rise or fall rate	$\Delta t / \Delta v$	0	5	ns / V	$V_{CC} = 4.5$ to 5.5 V
Operating free-air temperature	T_a	-40	85	$^\circ\text{C}$	

Note: Unused or floating inputs must be held high or low.

DC Electrical Characteristics

(Ta = -40 to 85°C)

Item	Symbol	V _{CC} (V)	Min	Typ ^{*1}	Max	Unit	Test conditions
Clamp diode voltage	V _{IK}	4.5	—	—	-1.2	V	I _{IN} = -18 mA
Input voltage	V _{IH}	4.0 to 5.5	2.0	—	—	V	
	V _{IL}	4.0 to 5.5	—	—	0.8		
On-state switch resistance ^{*2}	R _{ON}	4.0	—	14	20	Ω	V _{IN} = 2.4 V, I _{IN} = 15 mA Typ at V _{CC} = 4.0 V
		4.5	—	5	7		V _{IN} = 0 V, I _{IN} = 64 mA
		4.5	—	5	7		V _{IN} = 0 V, I _{IN} = 30 mA
		4.5	—	10	15		V _{IN} = 2.4 V, I _{IN} = 15 mA
Input current	I _{IN}	0 to 5.5	—	—	±1.0	μA	V _{IN} = 5.5 V or GND
Off-state leakage current	I _{OZ}	5.5	—	—	±1.0	μA	0 ≤ A, B ≤ V _{CC}
Quiescent supply current	I _{CC}	5.5	—	—	1.0	μA	V _{IN} = V _{CC} or GND, I _O = 0 mA
Increase in I _{CC} per input ^{*3}	ΔI _{CC}	5.5	—	—	2.5	mA	One input at 3.4 V, other inputs at V _{CC} or GND

Notes: For condition shown as Min or Max use the appropriate values under recommended operating conditions.

1. All typical values are at V_{CC} = 5 V (unless otherwise noted), Ta = 25°C.
2. Measured by the voltage drop between the A and B terminals at the indicated current through the switch.
On-state resistance is determined by the lower voltage of the two (A or B) terminals.
3. This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Capacitance

(Ta = 25°C)

Item	Symbol	V _{CC} (V)	Min	Typ	Max	Unit	Test conditions
Control input capacitance	C _{IN}	5.0	—	3	—	pF	V _{IN} = 0 or 3 V
Input / output capacitance	C _{I/O (OFF)}	5.0	—	5	—	pF	V _O = 0 or 3 V, $\overline{\text{OE}} = \text{V}_{\text{CC}}$

Note: This parameter is determined by device characterization is not production tested.

Switching Characteristics

(Ta = -40 to 85°C)

V_{CC} = 4.0 V

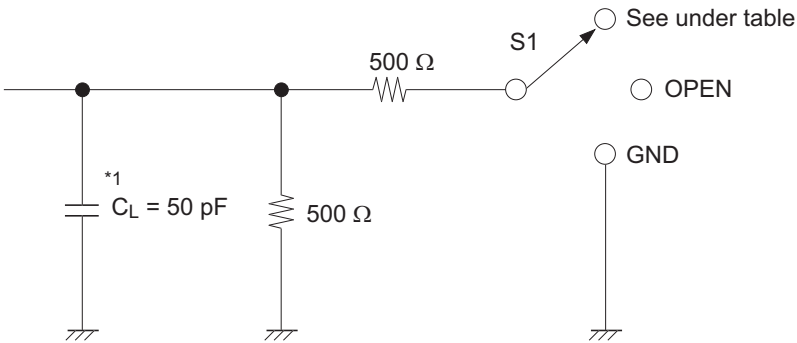
Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time ^{*1}	t _{PLH} t _{PHL}	—	0.35	ns	C _L = 50 pF R _L = 500 Ω	A or B	B or A
Enable time	t _{ZH} t _{ZL}	—	5.5	ns	C _L = 50 pF R _L = 500 Ω	$\overline{\text{OE}}$	A or B
Disable time	t _{HZ}	—	4.5	ns	C _L = 50 pF R _L = 500 Ω	$\overline{\text{OE}}$	A or B
	t _{LZ}	—	4.5				

V_{CC} = 5.0±0.5 V

Item	Symbol	Min	Max	Unit	Test conditions	FROM (Input)	TO (Output)
Propagation delay time ^{*1}	t _{PLH} t _{PHL}	—	0.25	ns	C _L = 50 pF R _L = 500 Ω	A or B	B or A
Enable time	t _{ZH} t _{ZL}	1.6	4.9	ns	C _L = 50 pF R _L = 500 Ω	$\overline{\text{OE}}$	A or B
Disable time	t _{HZ}	1.0	4.2	ns	C _L = 50 pF R _L = 500 Ω	$\overline{\text{OE}}$	A or B
	t _{LZ}	1.0	4.8				

Note: 1. The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

Test Circuit

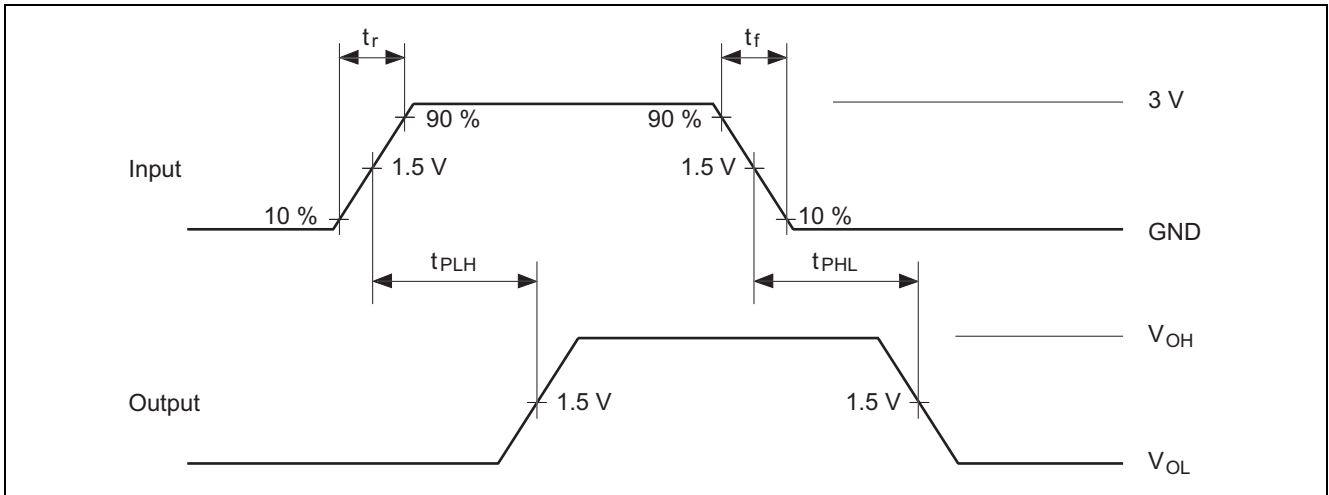


Load circuit for outputs

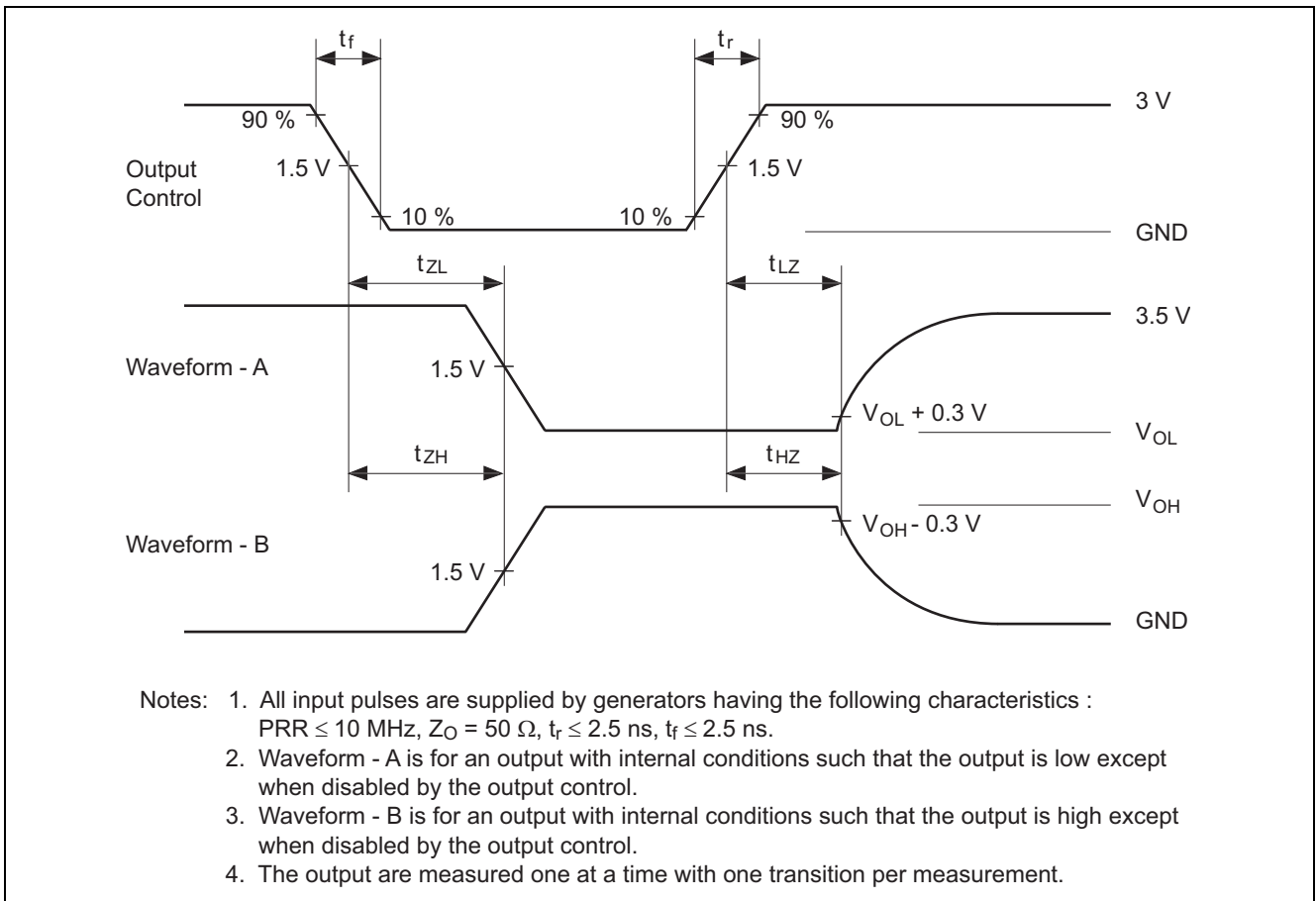
Symbol	S1
t _{PLH} / t _{PHL}	OPEN
t _{ZH} / t _{HZ}	OPEN
t _{ZL} / t _{LZ}	7 V

Note: 1. C_L includes probe and jig capacitance.

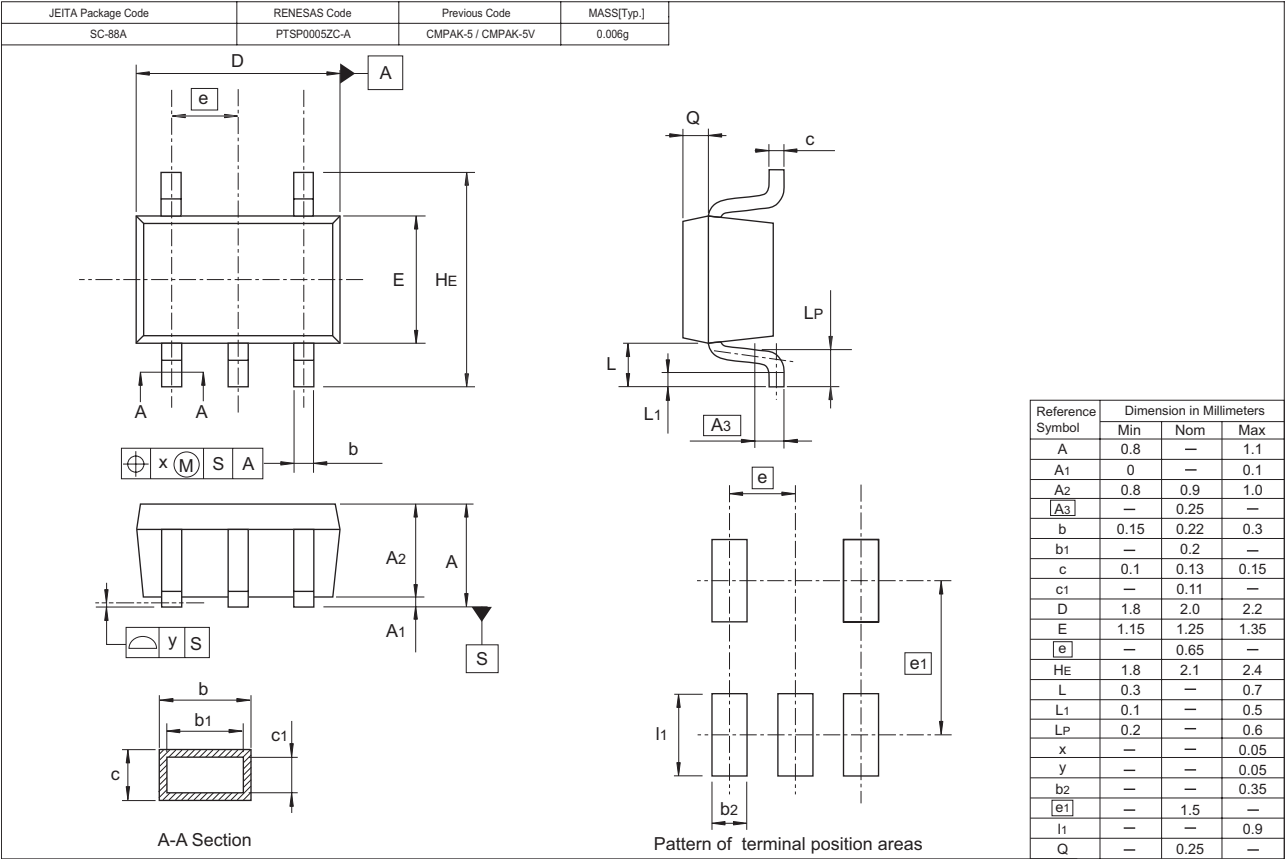
Waveforms – 1



Waveforms – 2



Package Dimensions



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