

HD74CDCF2509B

140 MHz, 0 to 85°C Operation
3.3-V Phase-lock Loop Clock Driver

REJ03D0827-1000
(Previous: ADE-205-224H)
Rev.10.00
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Description

The HD74CDCF2509B is a high-performance, low-skew, low-jitter, phase-lock loop clock driver. It uses a phase-lock loop (PLL) to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The HD74CDCF2509B operates at 3.3 V V_{CC} and is designed to drive up to five clock loads per output.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of the input clock. Output signal duty cycles are adjusted to 50 percent independent of the duty cycle at the input clock. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the HD74CDCF2509B does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, HD74CDCF2509B requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, as well as following any changes to the PLL reference or feedback signals.

Features

- Supports PC133 and meets "PC SDRAM registered DIMM specification, Rev. 1.1"
- Phase-lock loop clock distribution for synchronous DRAM applications
- External feedback (FBIN) pin is used to synchronize the outputs to the clock input
- No external RC network required
- Support spread spectrum clock (SSC) synthesizers
- Supports frequencies up to 140 MHz
- 0 to 85°C operating range
- Ordering Information

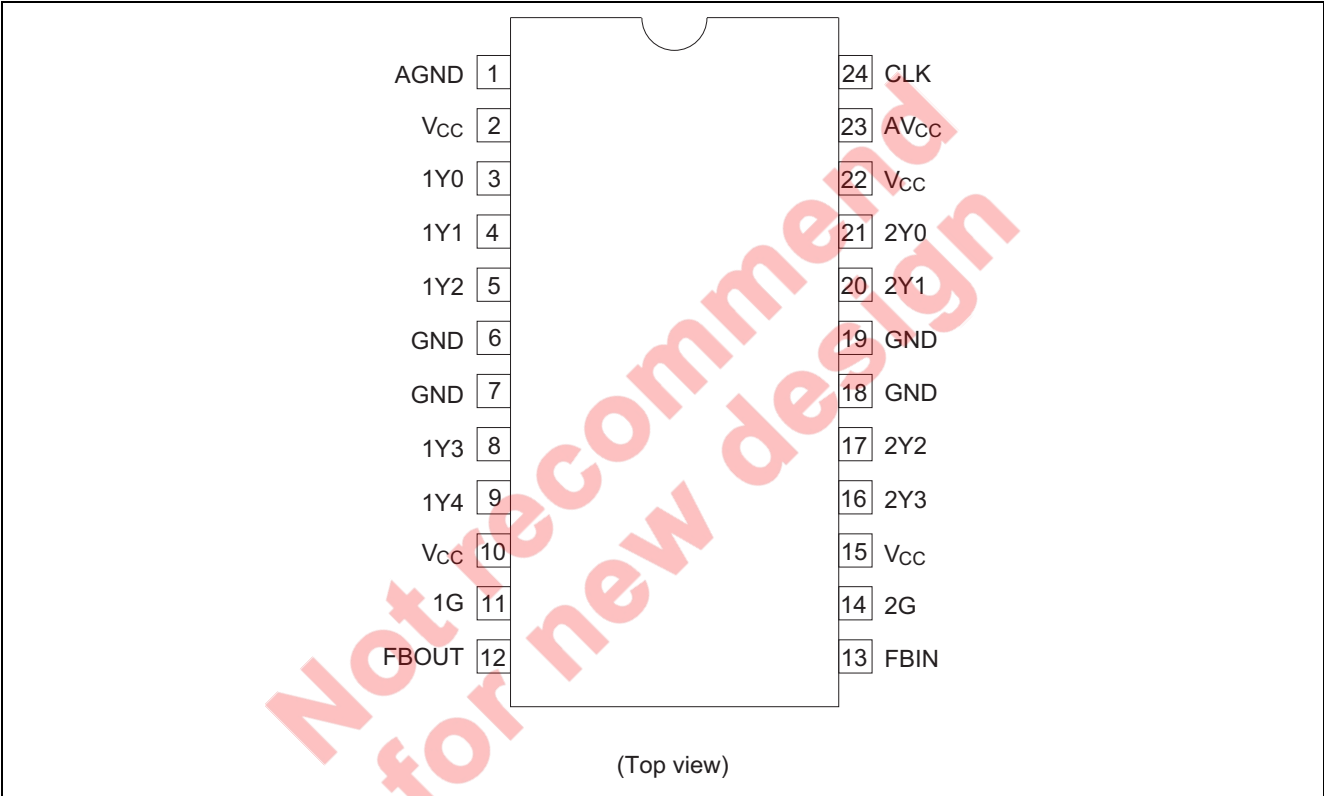
| Part Name | Package Type | Package Code (Previous code) | Package Abbreviation | Taping Abbreviation (Quantity) |
|------------------|--------------|---------------------------------|-------------------------|-----------------------------------|
| HD74CDCF2509BTEL | TSSOP-24 pin | PTSP0024JB-A (TTP-24DBV) | T | EL (1,000 pcs / Reel) |

Function Table

| Inputs | | | Outputs | | |
|--------|----|-----|----------|----------|-------|
| 1G | 2G | CLK | 1Y (0:4) | 2Y (0:3) | FBOUT |
| X | X | L | L | L | L |
| L | L | H | L | L | H |
| L | H | H | L | H | H |
| H | L | H | H | L | H |
| H | H | H | H | H | H |

H : High level
L : Low level
X : Immaterial

Pin Arrangement



Absolute Maximum Ratings

| Item | Symbol | Ratings | Unit | Conditions |
|---|-----------------------|------------------------|------------------|-----------------------------|
| Supply voltage | V_{CC} | −0.5 to 4.6 | V | |
| Input voltage ^{*1} | V_I | −0.5 to 6.5 | V | |
| Output voltage ^{*1, 2} | V_O | −0.5 to $V_{CC} + 0.5$ | V | |
| Input clamp current | I_{IK} | −50 | mA | $V_I < 0$ |
| Output clamp current | I_{OK} | ±50 | mA | $V_O < 0$ or $V_O > V_{CC}$ |
| Continuous output current | I_O | ±50 | mA | $V_O = 0$ to V_{CC} |
| Supply current | I_{CC} or I_{GND} | ±100 | mA | |
| Maximum power dissipation at $T_a = 55^\circ\text{C}$ (in still air) ^{*3} | P_T | 0.7 | W | |
| Storage temperature | T_{stg} | −65 to +150 | $^\circ\text{C}$ | |

Notes: Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

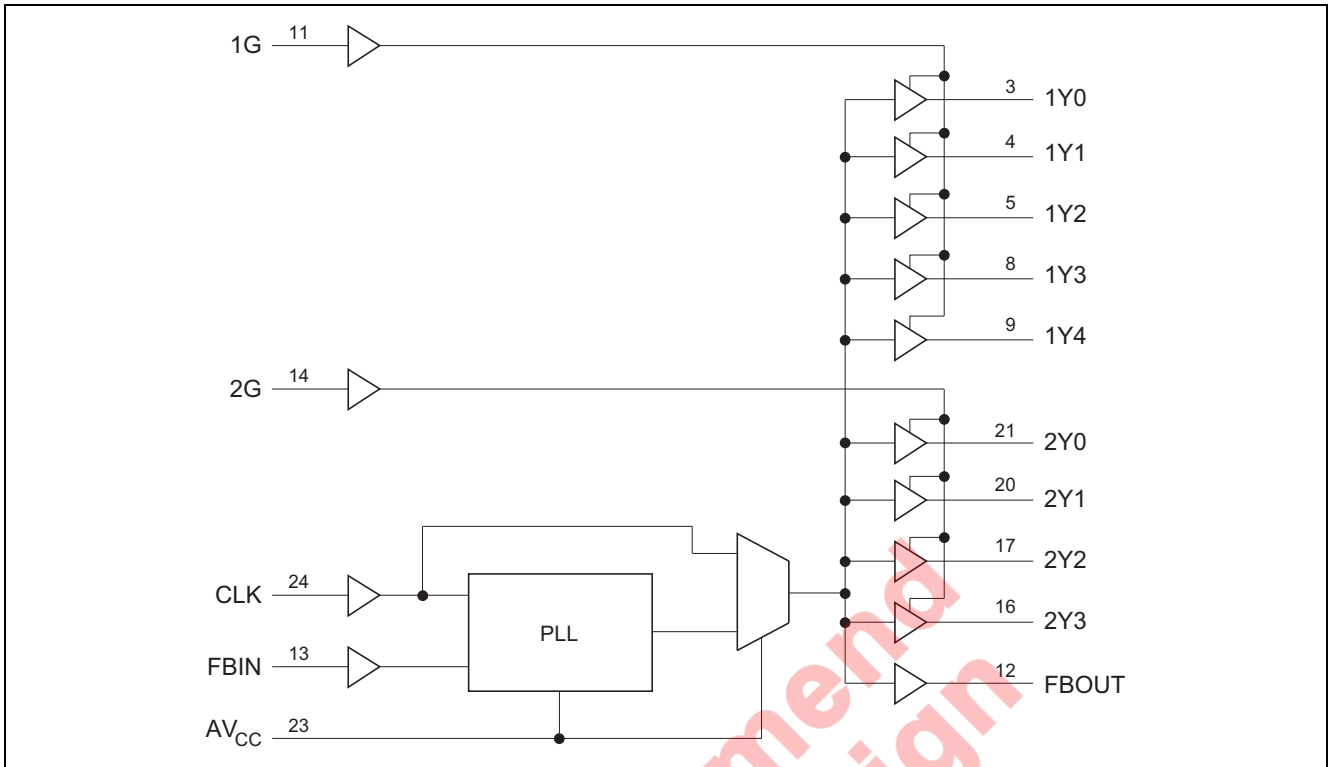
1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
2. This value is limited to 4.6 V maximum.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

Recommended Operating Conditions

| Item | Symbol | Min | Typ | Max | Unit | Conditions |
|-----------------------|----------|-----|-----|----------|------------------|------------|
| Supply voltage | V_{CC} | 3.0 | — | 3.6 | V | |
| Input voltage | V_{IH} | 2.0 | — | — | V | |
| | V_{IL} | — | — | 0.8 | | |
| | V_I | 0 | — | V_{CC} | | |
| Output current | I_{OH} | — | — | −12 | mA | |
| | I_{OL} | — | — | 12 | | |
| Operating temperature | T_a | 0 | — | 85 | $^\circ\text{C}$ | |

Note: Unused inputs must be held high or low to prevent them from floating.

Logic Diagram



Pin Function

| Pin name | No. | Type | Description |
|------------------|----------------|--------|--|
| CLK | 24 | I | Clock input. CLK provides the clock signal to be distributed by the HD74CDCF2509B clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal. |
| FBIN | 13 | I | Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN. |
| 1G | 11 | I | Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK. |
| 2G | 14 | I | Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK. |
| FBOUT | 12 | O | Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. |
| 1Y(0:4) | 3, 4, 5, 8, 9 | O | Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic low state by deasserting the 1G control input. |
| 2Y(0:3) | 16, 17, 20, 21 | O | Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic low state by deasserting the 2G control input. |
| AV _{CC} | 23 | Power | Analog power supply. AV _{CC} provides the power reference for the analog circuitry. In addition, AV _{CC} can be used to bypass the PLL for test purposes. When AV _{CC} is strapped to ground, PLL is bypassed. This bypass mode is used for Hitachi test. |
| AGND | 1 | Ground | Analog ground. AGND provides the ground reference for the analog circuitry. |
| V _{CC} | 2, 10, 15, 22 | Power | Power supply |
| GND | 6, 7, 18, 19 | Ground | Ground |

Electrical Characteristics

| Item | Symbol | Min | Typ ^{*1} | Max | Unit | Test Conditions |
|--------------------------|------------------|----------------------|-------------------|------|------|--|
| Input clamp voltage | V _{IK} | — | — | −1.2 | V | V _{CC} = 3 V, I _I = −18 mA |
| Output voltage | V _{OH} | V _{CC} −0.2 | — | — | V | V _{CC} = Min to Max, I _{OH} = −100 μA |
| | | 2.1 | — | — | | V _{CC} = 3 V, I _{OH} = −12 mA |
| | | 2.4 | — | — | | V _{CC} = 3 V, I _{OH} = −6 mA |
| | V _{OL} | — | — | 0.2 | | V _{CC} = Min to Max, I _{OL} = 100 μA |
| | | — | — | 0.8 | | V _{CC} = 3 V, I _{OL} = 12 mA |
| | | — | — | 0.55 | | V _{CC} = 3 V, I _{OL} = 6 mA |
| Input current | I _{IN} | — | — | ±5 | μA | V _{CC} = 3.6 V, V _{IN} = V _{CC} or GND |
| Quiescent supply current | I _{CC} | — | — | 10 | μA | AV _{CC} = GND, V _{CC} = 3.6 V, V _I = V _{CC} or GND, I _O = 0 |
| | ΔI _{CC} | — | — | 500 | μA | AV _{CC} = GND, V _{CC} = 3.3 to 3.6 V One input at V _{CC} −0.6 V, Other inputs at V _{CC} or GND |
| Input capacitance | C _{IN} | — | 4 | — | pF | V _{CC} = 3.3 V, V _I = V _{CC} or GND |
| Output capacitance | C _O | — | 6 | — | pF | V _{CC} = 3.3 V, V _O = V _{CC} or GND |

Note: 1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

Switching Characteristics

(C_L = 25 pF, T_a = 0 to 85°C)

| Item | Symbol | V _{CC} = 3.3 V±0.3 V | | | Unit | From (Input) | To (Output) |
|---|---------------------------------|-------------------------------|-----|-----|-------------------|---|------------------|
| | | Min | Typ | Max | | | |
| Phase error time | t _{pe} | -125 | — | 125 | ps | CLKIN↑ = 133 MHz | FBIN↑ |
| Between output pins skew ^{*1} | t _{sk(O)} | — | — | 150 | ps | Any Y or FBOUT, F (clkin = 133 MHz) | Any Y or FBOUT |
| Cycle to cycle jitter | | -75 | — | 75 | ps | F (clkin = 133 MHz) | Any Y or FBOUT |
| Duty cycle | | 45 | — | 55 | % | F (clkin = 133 MHz) | Any Y or FBOUT |
| Slew rate | | 5.0 | — | 1.0 | volts/ns | | Any Y or FBOUT |
| Analog power supply rejection (DC to 10 MHz) | V _{apsr} ^{*2} | 100 | — | — | mV _{P-P} | | AV _{CC} |

Notes: The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.

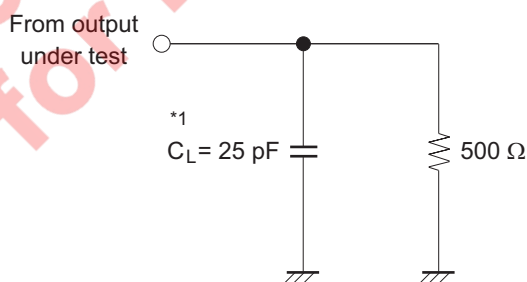
1. The t_{sk(O)} specification is only valid for equal loading of all outputs.
2. This parameter is characterized but not tested.

Timing Requirements

| Item | Symbol | Min | Max | Unit | Test Conditions |
|----------------------------------|--------------------|-----|-----|------|-----------------|
| Input clock frequency | f _{clock} | 50 | 140 | MHz | |
| Input clock duty cycle | | 40 | 60 | % | |
| Stabilization time ^{*1} | | — | 1 | ms | After power up |

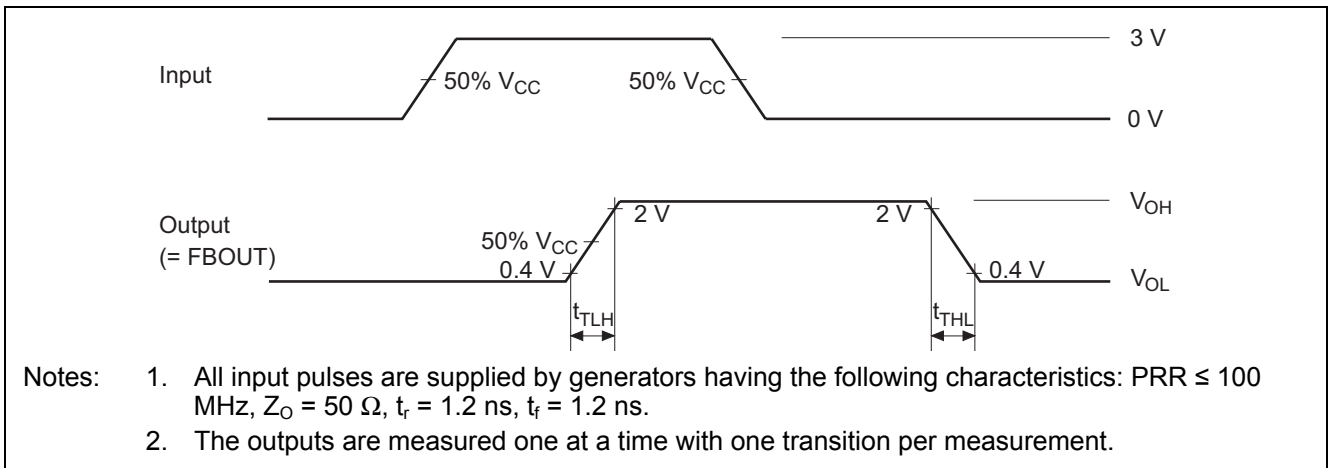
Note: 1. Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics table are not applicable.

Test Circuit

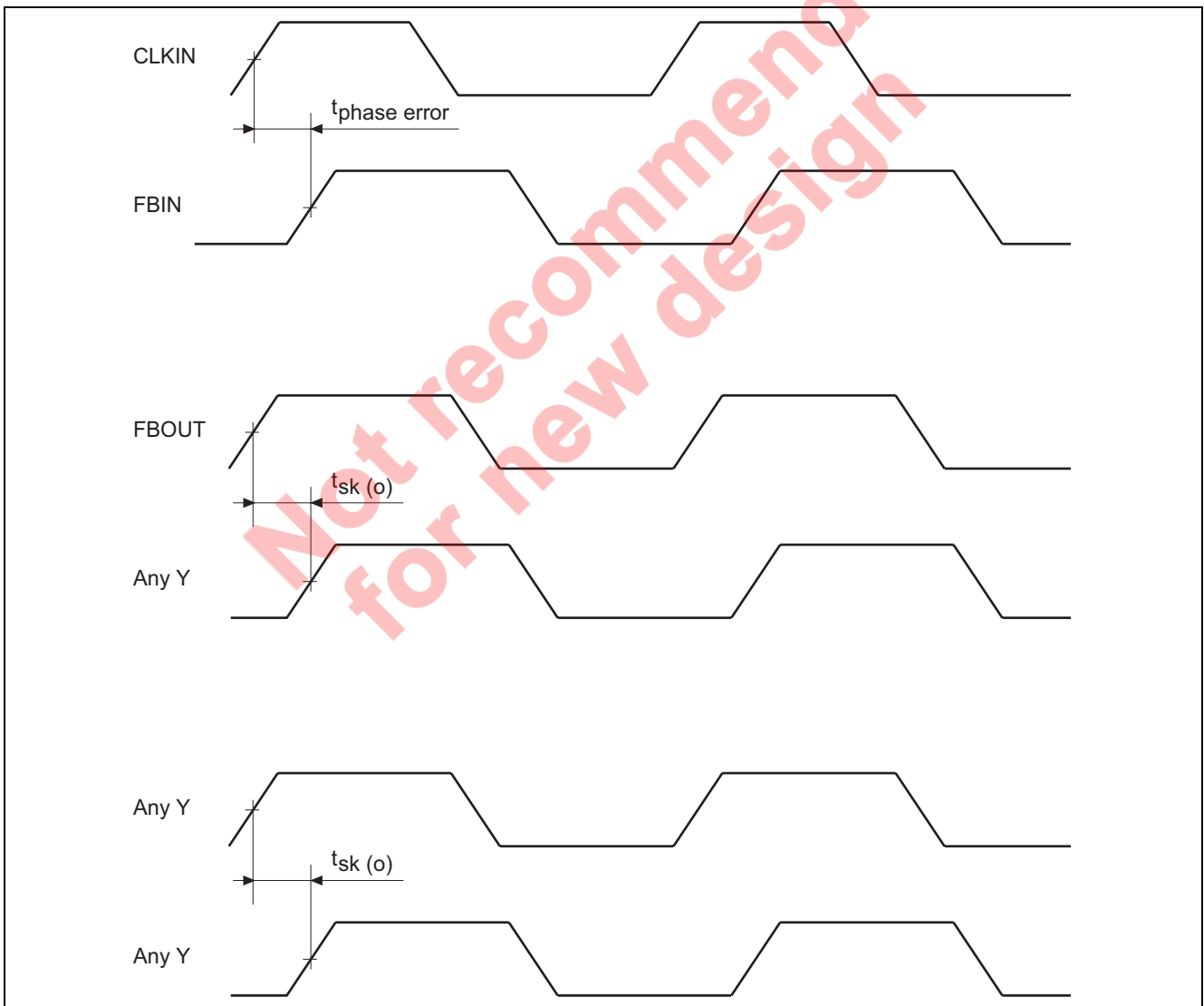


Note: 1. C_L includes probe and jig capacitance.

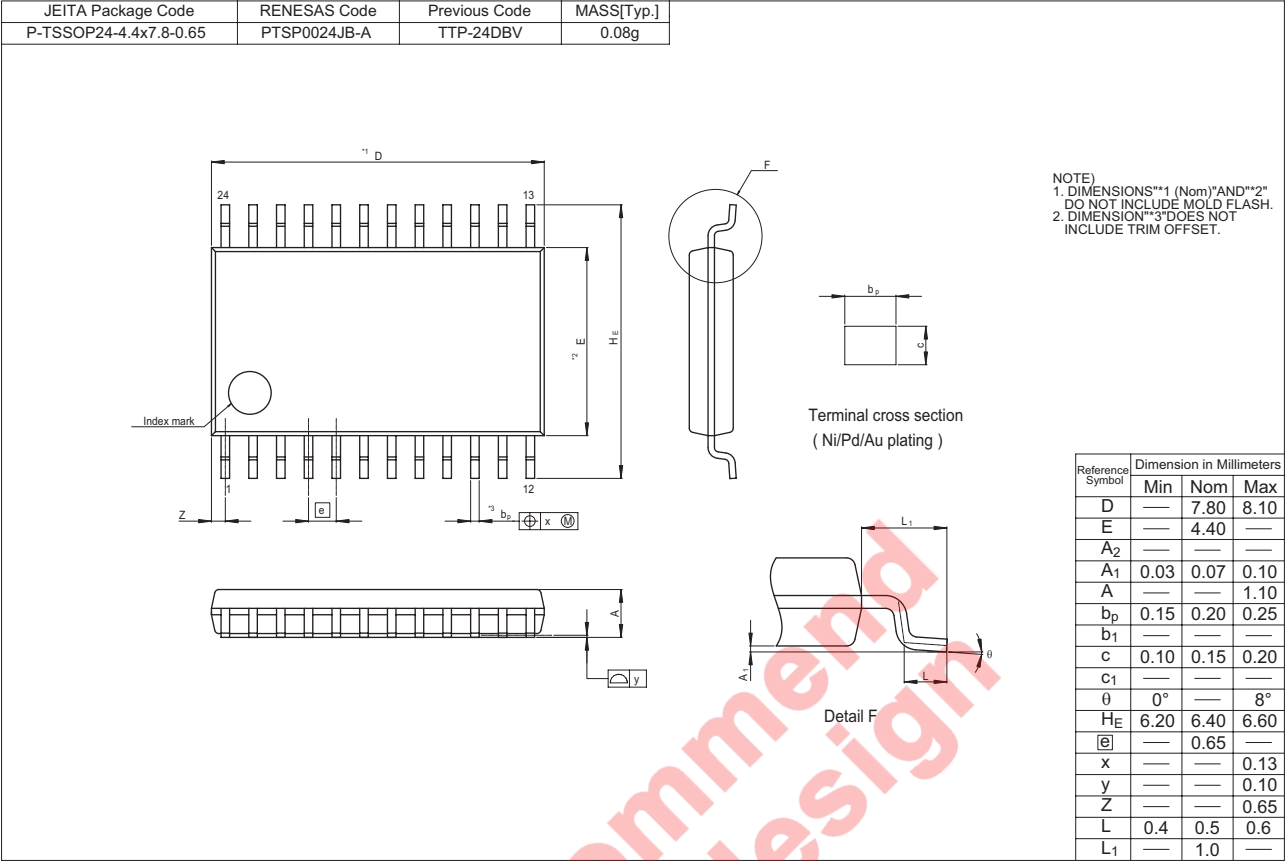
Waveforms – 1



Waveforms – 2



Package Dimensions



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Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd, Pudong District, Shanghai, China 200120
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510