

HD74HC195

4-bit Parallel-Access Shift Register

REJ03D0590-0200
(Previous ADE-205-467)
Rev.2.00
Jan 31, 2006

Description

This shift register features parallel inputs, parallel outputs, J- \bar{K} serial inputs, Shift/Load control input, and a direct overriding clear. This shift register can operate in two modes: Parallel load; shift from Q_A towards Q_D .

Parallel loading is accomplished by applying the four bits of data, and taking the Shift/Load control Input low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock input. During parallel loading, serial data flow is inhibited. Serial shifting occurs synchronously when the Shift/Load control input is high. Serial data for this mode is entered at the J- \bar{K} inputs. These inputs allow the first stage to perform as a J- \bar{K} or toggle flip-flop as shown in the function table.

Features

- High Speed Operation: t_{pd} (Clock to Q) = 13 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 10 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μ A max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μ A max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC195P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—

Function Table

Inputs									Outputs				
Clear	Shift/ Load	Clock	Serial		Parallel								
			J	\bar{K}	A	B	C	D	Q_A	Q_B	Q_C	Q_D	\bar{Q}_D
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	\square	X	X	a	b	c	d	a	b	c	d	\bar{d}
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	\bar{Q}_{D0}
H	H	\square	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\square	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\square	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}
H	H	\square	H	L	X	X	X	X	Q_{An}	Q_{An}	Q_{Bn}	Q_{Cn}	\bar{Q}_{Cn}

H : high level (steady state)

L : low level (steady state)

X : don't care

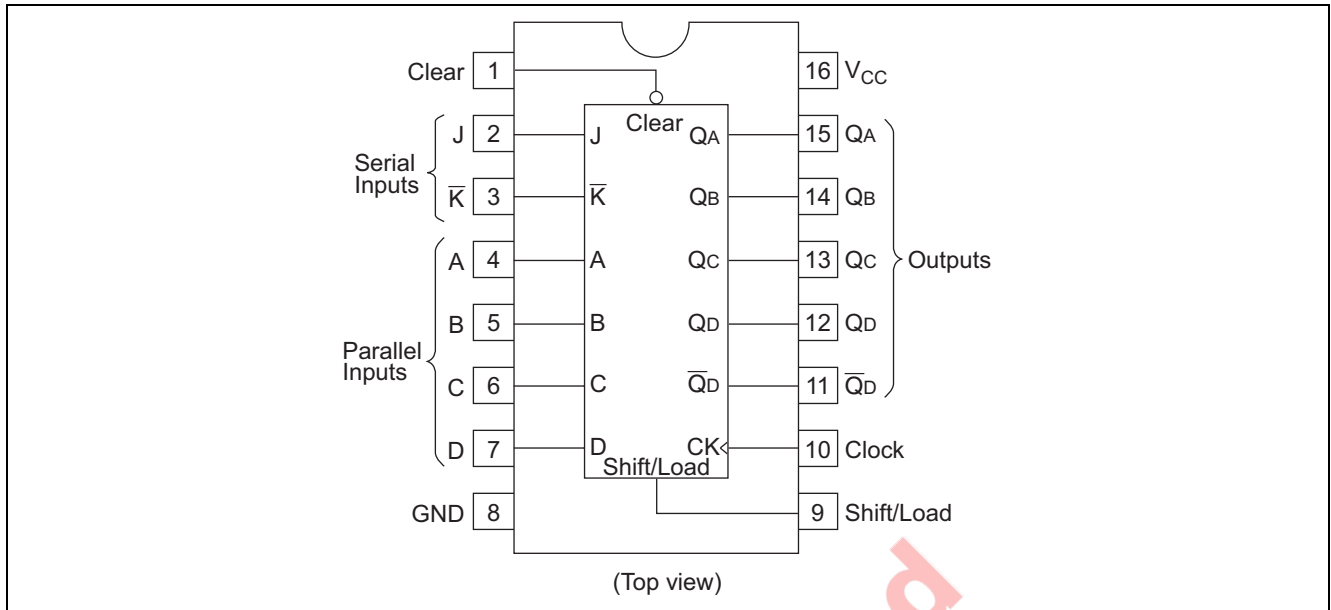
\square : transition from low to high level.

a, b, c, d : the level of steady-state input at inputs A, B, C or D respectively.

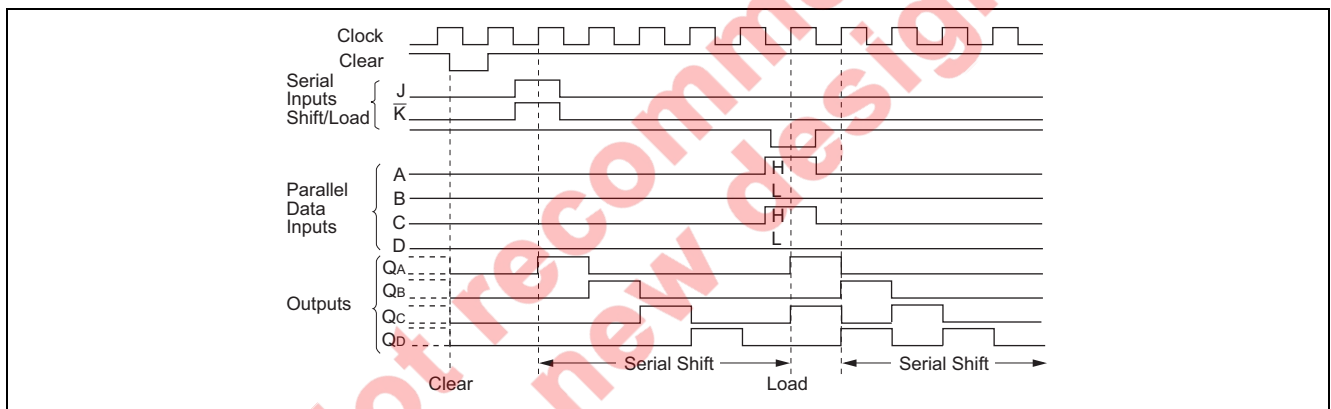
Q_{A0} , Q_{B0} , Q_{C0} , Q_{D0} : the level of Q_A , Q_B , Q_C or Q_D respectively, before the indicated steady-state input conditions were established.

Q_{An} , Q_{Bn} , Q_{Cn} , Q_{Dn} : the level of Q_A , Q_B , Q_C or Q_D respectively before the most recent \square transition of the clock.

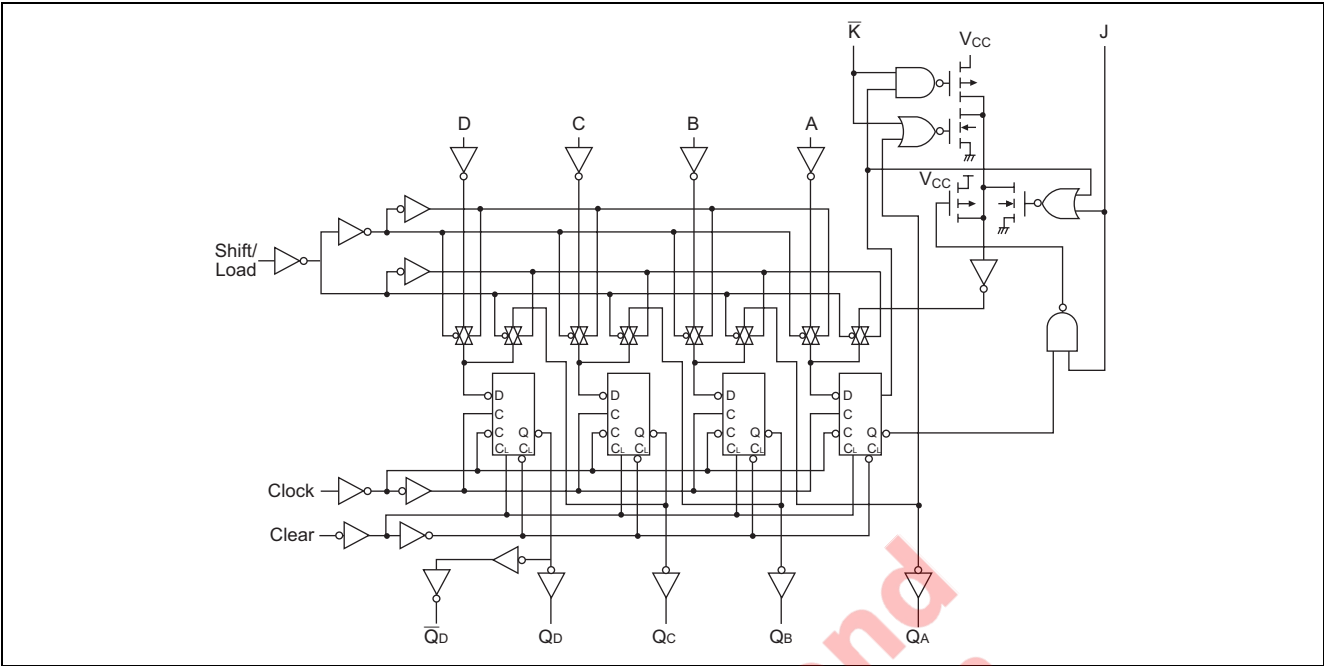
Pin Arrangement



Timing Diagram



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_O	± 25	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 50	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Notes: 1. This item guarantees maximum limit when one input switches.
Waveform: Refer to test circuit of switching characteristics.

Electrical Characteristics

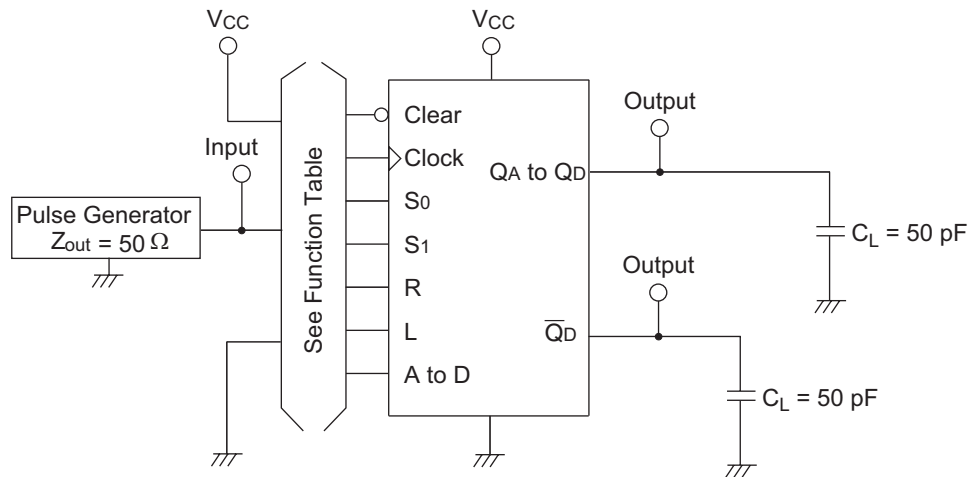
Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V _{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V _{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V _{OH}	2.0	1.9	2.0	—	1.9	—	V	Vin = V _{IH} or V _{IL}	I _{OH} = -20 µA
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			I _{OH} = -4 mA
		6.0	5.68	—	—	5.63	—			I _{OH} = -5.2 mA
	V _{OL}	2.0	—	0.0	0.1	—	0.1	V	Vin = V _{IH} or V _{IL}	I _{OL} = 20 µA
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			I _{OL} = 4 mA
		6.0	—	—	0.26	—	0.33			I _{OL} = 5.2 mA
Input current	I _{in}	6.0	—	—	±0.1	—	±1.0	µA	Vin = V _{CC} or GND	
Quiescent supply current	I _{CC}	6.0	—	—	4.0	—	40	µA	Vin = V _{CC} or GND, I _{out} = 0 µA	

Switching Characteristics

(C_L = 50 pF, Input t_r = t_f = 6 ns)

Item	Symbol	V _{CC} (V)	Ta = 25°C			Ta = -40 to +85°C		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	f _{max}	2.0	—	—	6	—	5	MHz	
		4.5	—	—	30	—	24		
		6.0	—	—	35	—	28		
Propagation delay time	t _{PHL}	2.0	—	—	140	—	175	ns	Clock to Q
		4.5	—	13	28	—	35		
		6.0	—	—	24	—	30		
	t _{PLH}	2.0	—	—	140	—	175	ns	
		4.5	—	13	28	—	35		
		6.0	—	—	24	—	30		
	t _{PHL}	2.0	—	—	150	—	190	ns	Clear to Q
		4.5	—	15	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t _w	2.0	80	—	—	100	—	ns	Clock to Clear
		4.5	16	7	—	20	—		
		6.0	14	—	—	17	—		
Setup time	t _{su}	2.0	100	—	—	125	—	ns	A, B, C, D, J, \bar{K} to Clock
		4.5	20	6	—	25	—		
		6.0	17	—	—	21	—		
	t _{su}	2.0	100	—	—	125	—	ns	Shift/Load to Clock
		4.5	20	13	—	25	—		
		6.0	17	—	—	21	—		
Hold time	t _h	2.0	0	—	—	0	—	ns	Any input except Shift/Load
		4.5	0	-3	—	0	—		
		6.0	0	—	—	0	—		
Removal time	t _{rem}	2.0	75	—	—	95	—	ns	Shift/Load to Clock
		4.5	15	8	—	19	—		
		6.0	13	—	—	16	—		
	t _{rem}	2.0	25	—	—	31	—	ns	Clear inactive to Clock
		4.5	5	0	—	6	—		
		6.0	4	—	—	5	—		
Output rise/fall time	t _{TLH}	2.0	—	—	75	—	95	ns	
	t _{THL}	4.5	—	5	15	—	19		
	t _{THL}	6.0	—	—	13	—	16		
Input capacitance	C _{in}	—	—	5	10	—	10	pF	

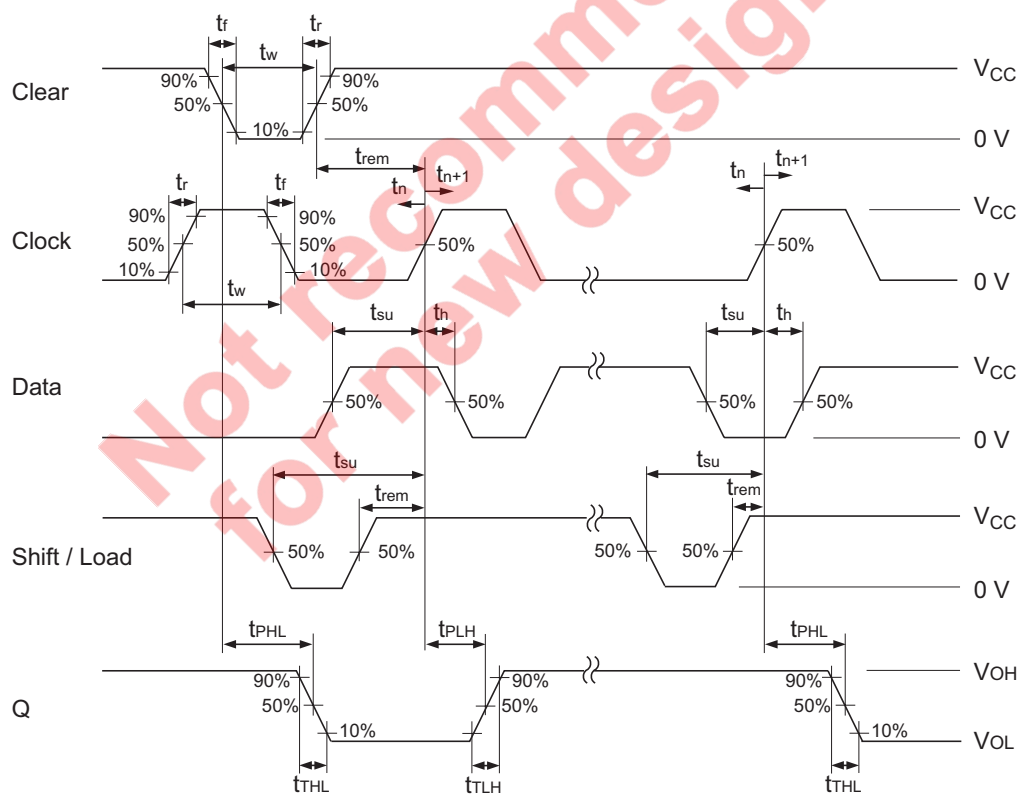
Test Circuit



Note : 1. C_L includes probe and jig capacitance.

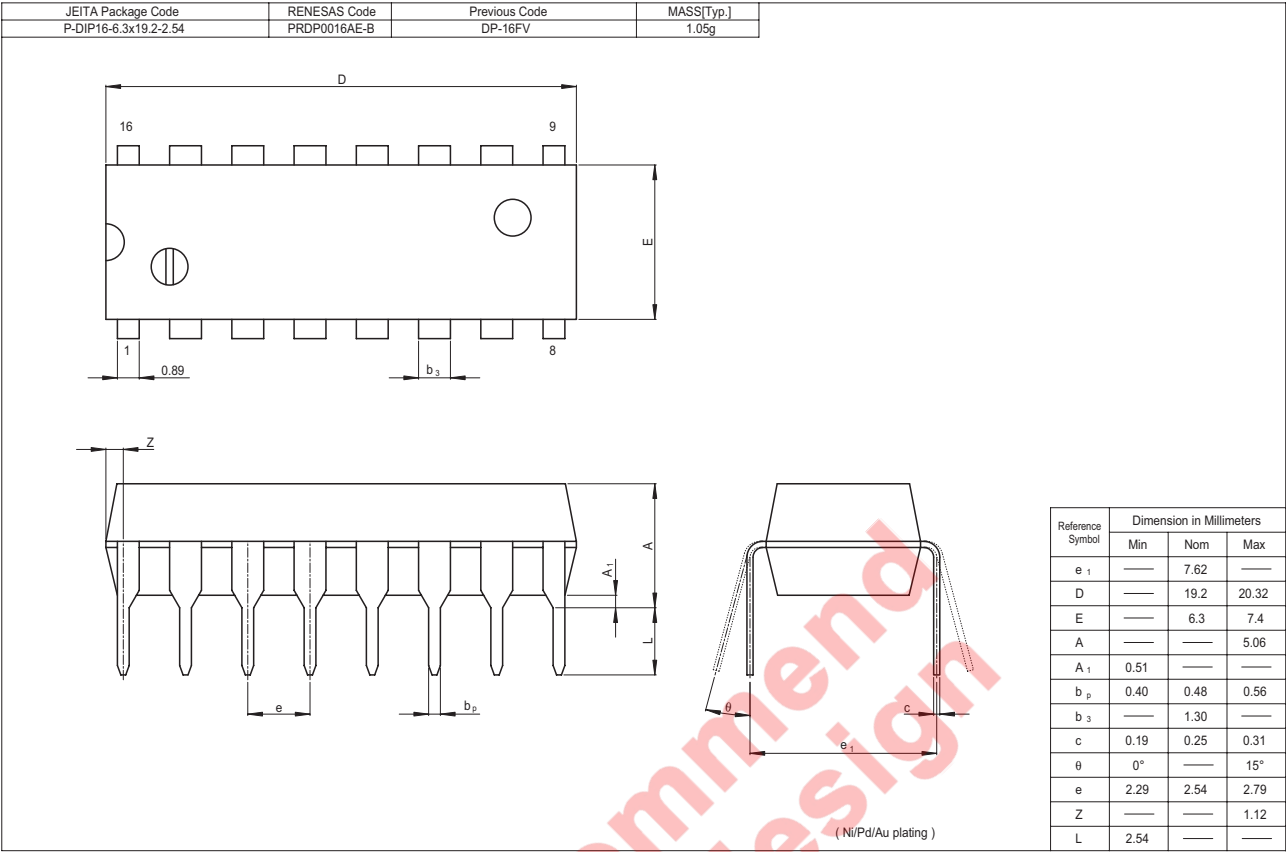
Waveforms

• Waveform



- Notes :
1. Input pulse : $PRR \leq 1 \text{ MHz}$, $Z_o = 50 \Omega$, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. A clear pulse is applied prior to each test.
 3. Propagation delay times (t_{PLH} and t_{PHL}) are measured at t_{n+1} .
Proper shifting of data is verified at t_{n+4} with a functional test.
 4. J and \bar{K} inputs are tested the same as data A, B, C and D inputs except that Shift / Load input remains high.
 5. t_n : bit time before clocking transition.
 6. t_{n+1} : bit time after one clocking transition.
 7. t_{n+4} : bit time after four clocking transition.

Package Dimensions



Keep safety first in your circuit designs!

1. Renesas Technology Corp. puts the maximum effort into making semiconductor products better and more reliable, but there is always the possibility that trouble may occur with them. Trouble with semiconductors may lead to personal injury, fire or property damage. Remember to give due consideration to safety when making your circuit designs, with appropriate measures such as (i) placement of substitutive, auxiliary circuits, (ii) use of nonflammable material or (iii) prevention against any malfunction or mishap.

Notes regarding these materials

1. These materials are intended as a reference to assist our customers in the selection of the Renesas Technology Corp. product best suited to the customer's application; they do not convey any license under any intellectual property rights, or any other rights, belonging to Renesas Technology Corp. or a third party.
2. Renesas Technology Corp. assumes no responsibility for any damage, or infringement of any third-party's rights, originating in the use of any product data, diagrams, charts, programs, algorithms, or circuit application examples contained in these materials.
3. All information contained in these materials, including product data, diagrams, charts, programs and algorithms represents information on products at the time of publication of these materials, and are subject to change by Renesas Technology Corp. without notice due to product improvements or other reasons. It is therefore recommended that customers contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor for the latest product information before purchasing a product listed herein.
The information described here may contain technical inaccuracies or typographical errors.
Renesas Technology Corp. assumes no responsibility for any damage, liability, or other loss rising from these inaccuracies or errors.
Please also pay attention to information published by Renesas Technology Corp. by various means, including the Renesas Technology Corp. Semiconductor home page (<http://www.renesas.com>).
4. When using any or all of the information contained in these materials, including product data, diagrams, charts, programs, and algorithms, please be sure to evaluate all information as a total system before making a final decision on the applicability of the information and products. Renesas Technology Corp. assumes no responsibility for any damage, liability or other loss resulting from the information contained herein.
5. Renesas Technology Corp. semiconductors are not designed or manufactured for use in a device or system that is used under circumstances in which human life is potentially at stake. Please contact Renesas Technology Corp. or an authorized Renesas Technology Corp. product distributor when considering the use of a product contained herein for any specific purposes, such as apparatus or systems for transportation, vehicular, medical, aerospace, nuclear, or undersea repeater use.
6. The prior written approval of Renesas Technology Corp. is necessary to reprint or reproduce in whole or in part these materials.
7. If these products or technologies are subject to the Japanese export control restrictions, they must be exported under a license from the Japanese government and cannot be imported into a country other than the approved destination.
Any diversion or reexport contrary to the export control laws and regulations of Japan and/or the country of destination is prohibited.
8. Please contact Renesas Technology Corp. for further details on these materials or the products contained therein.



RENESAS SALES OFFICES

<http://www.renesas.com>

Refer to "<http://www.renesas.com/en/network>" for the latest and detailed information.

Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

Renesas Technology Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: <44> (1628) 585-100, Fax: <44> (1628) 585-900

Renesas Technology (Shanghai) Co., Ltd.

Unit 205, AZIA Center, No.133 Yincheng Rd (n), Pudong District, Shanghai 200120, China
Tel: <86> (21) 5877-1818, Fax: <86> (21) 6887-7898

Renesas Technology Hong Kong Ltd.

7th Floor, North Tower, World Finance Centre, Harbour City, 1 Canton Road, Tsimshatsui, Kowloon, Hong Kong
Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

Renesas Technology Korea Co., Ltd.

Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> (2) 796-3115, Fax: <82> (2) 796-2145

Renesas Technology Malaysia Sdn. Bhd

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510