

HD74HC590

8-bit Binary Counter/Register (with 3-state outputs)

REJ03D0632-0200
(Previous ADE-205-512)
Rev.2.00
Mar 30, 2006

Description

This device each contains an 8-bit binary counter that feeds an 8-bit storage register. The storage register has parallel outputs. Separate clocks are provided for both the binary counter and storage register. The binary counter features a direct clear input $\overline{\text{CCLR}}$ and a count enable input $\overline{\text{CCKEN}}$. For cascading a ripple carry output $\overline{\text{RCO}}$ is provided. Expansion is easily accomplished by tying $\overline{\text{RCO}}$ of the first stage to $\overline{\text{CCKEN}}$ of the second stage, etc.

Both the counter and register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the counter state will always be one count ahead of the register, Internal circuitry prevents clocking from the clock enable.

Features

- High Speed Operation: t_{pd} (RCK to Q) = 18.5 ns typ ($C_L = 50$ pF)
- High Output Current: Fanout of 15 LSTTL Loads
- Wide Operating Voltage: $V_{CC} = 2$ to 6 V
- Low Input Current: 1 μA max
- Low Quiescent Supply Current: I_{CC} (static) = 4 μA max ($T_a = 25^\circ\text{C}$)
- Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74HC590P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	P	—
HD74HC590FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)

Note: Please consult the sales office for the above package availability.

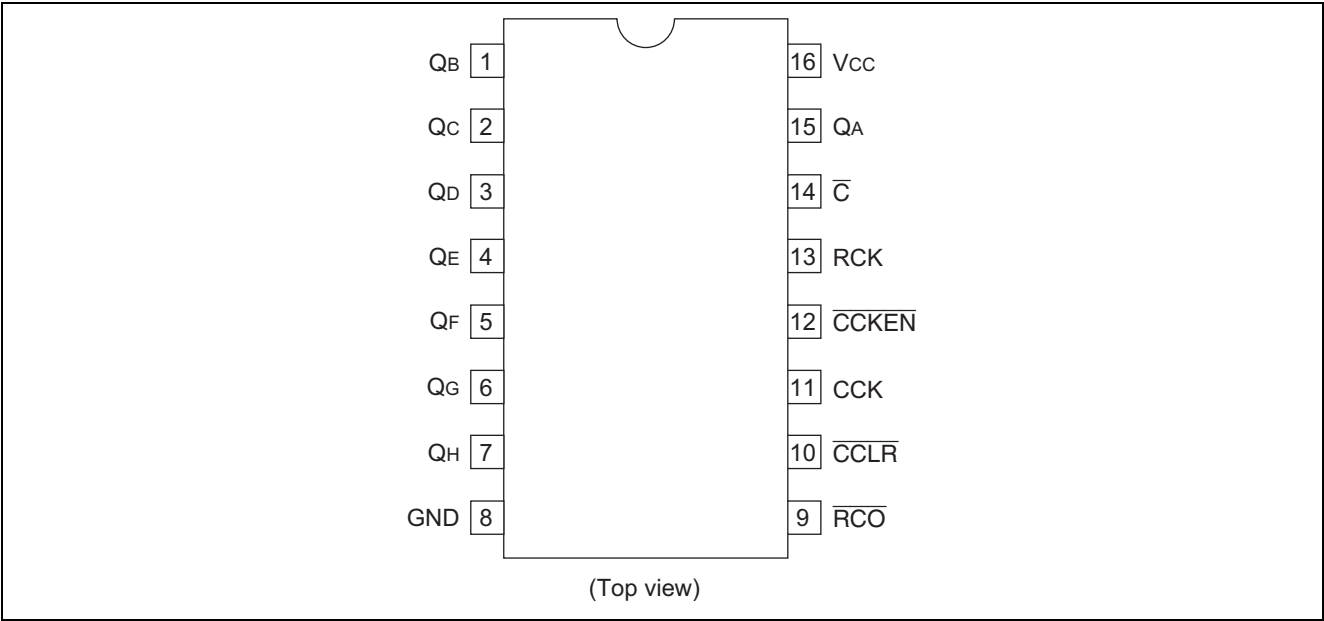
Function Table

Inputs					Function
$\overline{\text{G}}$	RCK	$\overline{\text{CCLR}}$	$\overline{\text{CCKEN}}$	CCK	
H	X	X	X	X	Q output disabled
L	X	X	X	X	Q output enabled
X		X	X	X	Contents of counter stored to register
X		X	X	X	No change in register
X	X	L	X	X	Counter clear
X	X	H	L		Count up
X	X	H	L		No count
X	X	H	H	X	No count

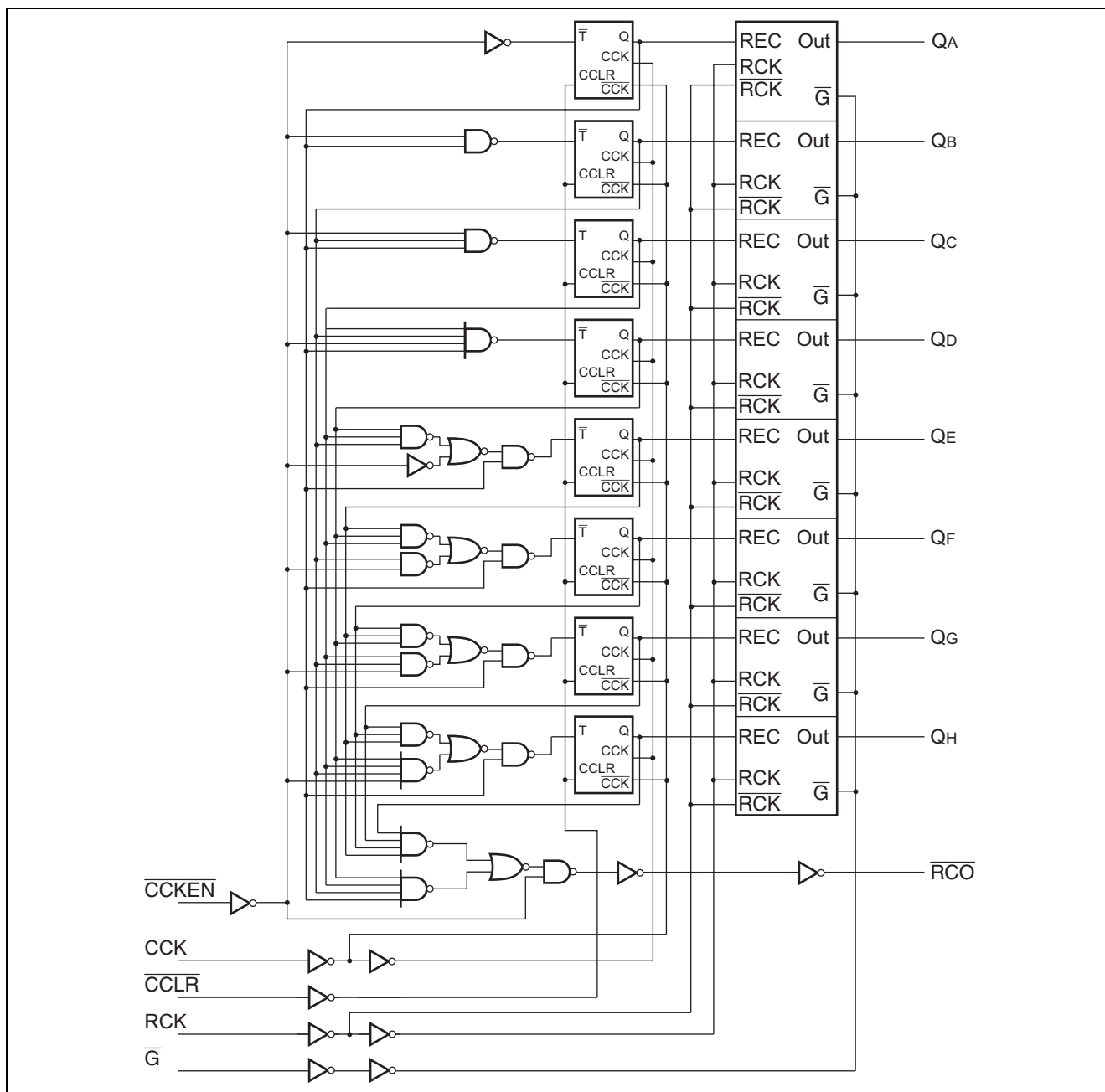
$$\overline{\text{RCO}} = \text{QA}' \cdot \text{QB}' \cdot \text{QC}' \cdot \text{QD}' \cdot \text{QE}' \cdot \text{QF}' \cdot \text{QG}' \cdot \text{QH}' \cdot (\overline{\text{CCKEN}})$$

(QA' to QH': Output of Internal Counter)

Pin Arrangement



Logic Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage range	V_{CC}	-0.5 to 7.0	V
Input / Output voltage	V_{IN}, V_{OUT}	-0.5 to $V_{CC} + 0.5$	V
Input / Output diode current	I_{IK}, I_{OK}	± 20	mA
Output current	I_{OUT}	± 35	mA
V_{CC} , GND current	I_{CC} or I_{GND}	± 75	mA
Power dissipation	P_T	500	mW
Storage temperature	T_{stg}	-65 to +150	°C

Note: The absolute maximum ratings are values, which must not individually be exceeded, and furthermore, no two of which may be realized at the same time.

Recommended Operating Conditions

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V_{CC}	2 to 6	V	
Input / Output voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	T_a	-40 to 85	°C	
Input rise / fall time ^{*1}	t_r, t_f	0 to 1000	ns	$V_{CC} = 2.0\text{ V}$
		0 to 500		$V_{CC} = 4.5\text{ V}$
		0 to 400		$V_{CC} = 6.0\text{ V}$

Note: 1. This item guarantees maximum limit when one input switches.

Waveform: Refer to test circuit of switching characteristics.

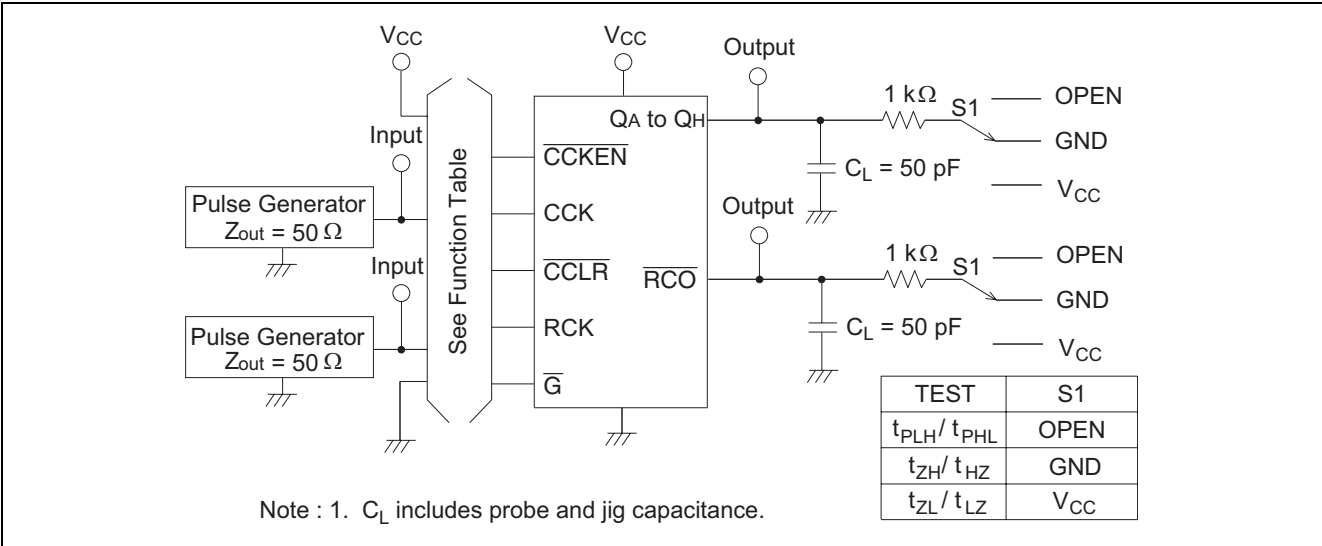
Electrical Characteristics

Item	Symbol	V_{CC} (V)	$T_a = 25^\circ\text{C}$			$T_a = -40\text{ to }+85^\circ\text{C}$		Unit	Test Conditions	
			Min	Typ	Max	Min	Max			
Input voltage	V_{IH}	2.0	1.5	—	—	1.5	—	V		
		4.5	3.15	—	—	3.15	—			
		6.0	4.2	—	—	4.2	—			
	V_{IL}	2.0	—	—	0.5	—	0.5	V		
		4.5	—	—	1.35	—	1.35			
		6.0	—	—	1.8	—	1.8			
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	Q_A to Q_H $V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20\text{ }\mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			$I_{OH} = -6\text{ mA}$
		6.0	5.68	—	—	5.63	—			$I_{OH} = -7.8\text{ mA}$
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	Q_A to Q_H $V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20\text{ }\mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 6\text{ mA}$
		6.0	—	—	0.26	—	0.33			$I_{OL} = 7.8\text{ mA}$
Output voltage	V_{OH}	2.0	1.9	2.0	—	1.9	—	V	$\overline{RCO}$ $V_{in} = V_{IH}$ or V_{IL}	$I_{OH} = -20\text{ }\mu\text{A}$
		4.5	4.4	4.5	—	4.4	—			
		6.0	5.9	6.0	—	5.9	—			
		4.5	4.18	—	—	4.13	—			$I_{OH} = -4\text{ mA}$
		6.0	5.68	—	—	5.63	—			$I_{OH} = -5.2\text{ mA}$
	V_{OL}	2.0	—	0.0	0.1	—	0.1	V	$\overline{RCO}$ $V_{in} = V_{IH}$ or V_{IL}	$I_{OL} = 20\text{ }\mu\text{A}$
		4.5	—	0.0	0.1	—	0.1			
		6.0	—	0.0	0.1	—	0.1			
		4.5	—	—	0.26	—	0.33			$I_{OL} = 4\text{ mA}$
		6.0	—	—	0.26	—	0.33			$I_{OL} = 5.2\text{ mA}$
Off-state output current	I_{OZ}	6.0	—	—	± 0.5	—	± 5.0	μA	$V_{in} = V_{IH}$ or V_{IL} , $V_{out} = V_{CC}$ or GND	
Input current	I_{in}	6.0	—	—	± 0.1	—	± 1.0	μA	$V_{in} = V_{CC}$ or GND	
Quiescent supply current	I_{CC}	6.0	—	—	4.0	—	40	μA	$V_{in} = V_{CC}$ or GND, $I_{out} = 0\text{ }\mu\text{A}$	

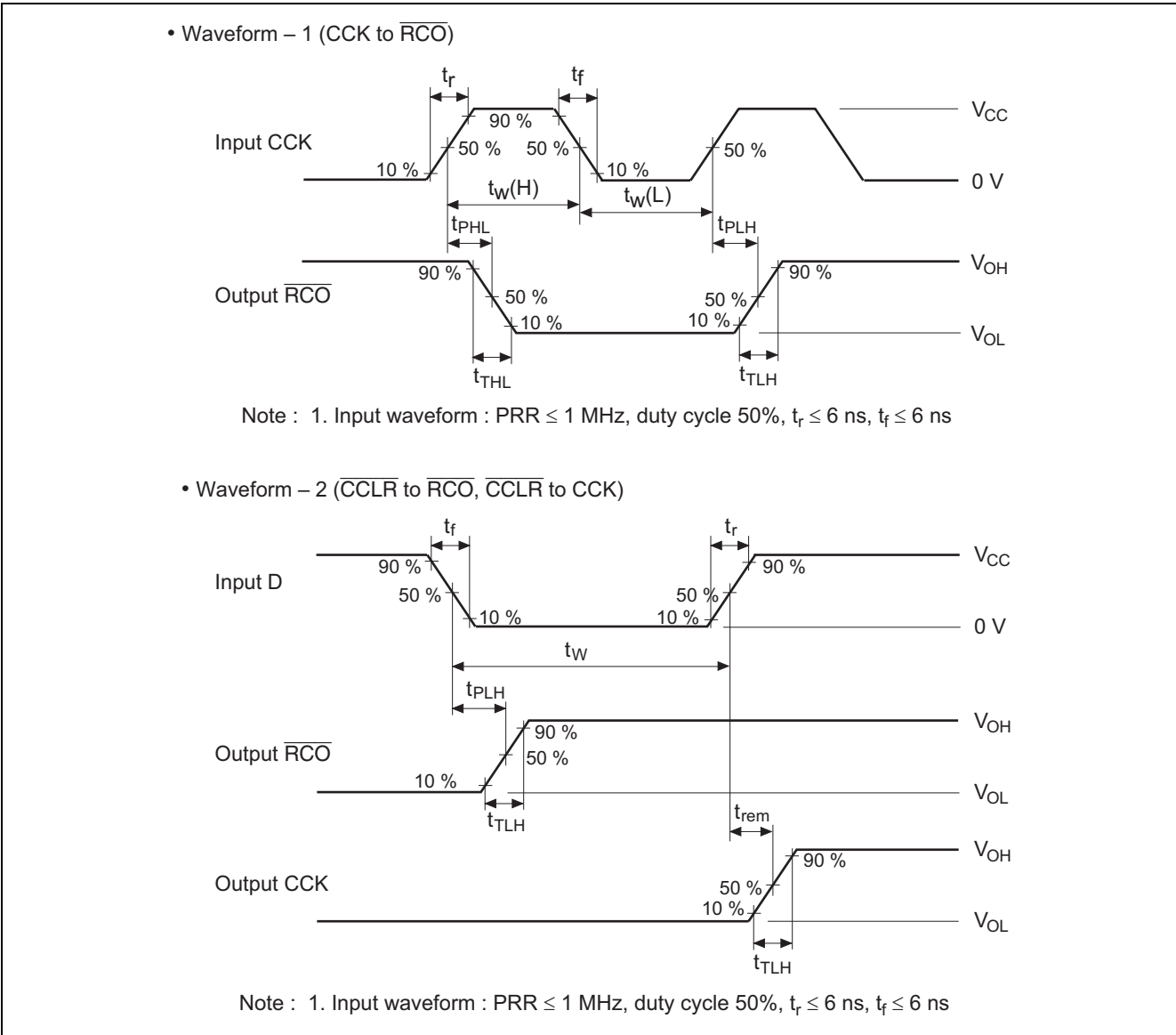
Switching Characteristics ($C_L = 50 \text{ pF}$, Input $t_r = t_f = 6 \text{ ns}$)

Item	Symbol	$V_{CC} \text{ (V)}$	$T_a = 25^\circ\text{C}$			$T_a = -40 \text{ to } +85^\circ\text{C}$		Unit	Test Conditions
			Min	Typ	Max	Min	Max		
Maximum clock frequency	$f_{\max}$	2.0	—	—	5	—	4	MHz	
		4.5	—	—	25	—	20		
		6.0	—	—	29	—	24		
Propagation delay time	t_{PLH}	2.0	—	—	200	—	250	ns	CCK to $\overline{\text{RCO}}$
		4.5	—	18	40	—	50		
		6.0	—	—	34	—	43		
	t_{PLH}	2.0	—	—	250	—	315	ns	CCLR to $\overline{\text{RCO}}$
		4.5	—	17	50	—	63		
		6.0	—	—	43	—	54		
	t_{PLH} t_{PHL}	2.0	—	—	200	—	250	ns	RCK to Q
		4.5	—	18	40	—	50		
		6.0	—	—	34	—	43		
Output enable time	t_{ZL} t_{ZH}	2.0	—	—	150	—	190	ns	
		4.5	—	16	30	—	39		
		6.0	—	—	26	—	33		
Output disable time	t_{LZ} t_{HZ}	2.0	—	—	150	—	190	ns	
		4.5	—	17	30	—	38		
		6.0	—	—	26	—	33		
Pulse width	t_w	2.0	80	—	—	100	—	ns	
		4.5	16	6	—	20	—		
		6.0	14	—	—	17	—		
Removal time	t_{rem}	2.0	5	—	—	5	—	ns	$\overline{\text{CCLR}}$ to CCK
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Setup time	t_{su}	2.0	100	—	—	125	—	ns	$\overline{\text{CCKEN}}$ to CCK
		4.5	20	−3	—	25	—		
		6.0	17	—	—	21	—		
		2.0	200	—	—	250	—	ns	CCK to RCK
		4.5	40	10	—	50	—		
		6.0	34	—	—	43	—		
Hold time	t_h	2.0	5	—	—	5	—	ns	$\overline{\text{CCKEN}}$ to CCK CCK to RCK
		4.5	5	—	—	5	—		
		6.0	5	—	—	5	—		
Output rise/fall time	t_{TLH} t_{THL}	2.0	—	—	60	—	75	ns	Q
		4.5	—	4	12	—	15		
		6.0	—	—	10	—	13		
	t_{TLH} t_{THL}	2.0	—	—	75	—	95	ns	$\overline{\text{RCO}}$
		4.5	—	5	15	—	19		
		6.0	—	—	13	—	16		
Input capacitance	C_{in}	—	—	5	10	—	10	pF	

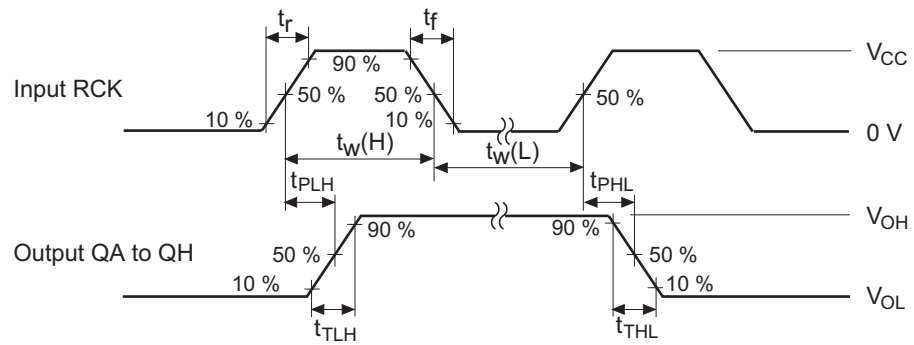
Test Circuit



Waveforms

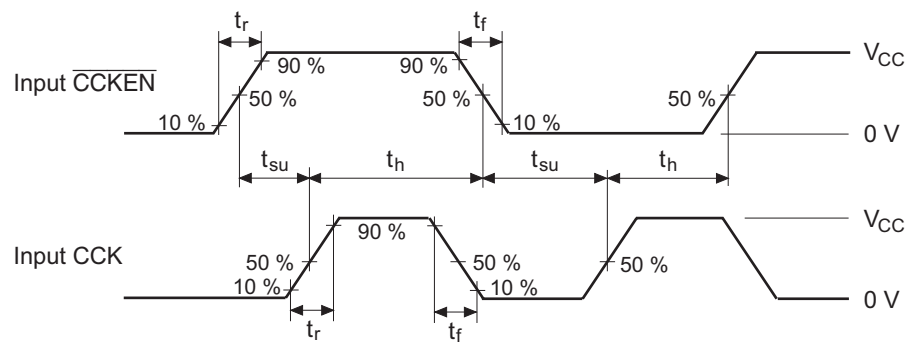


• Waveform – 3 (RCK to Q)



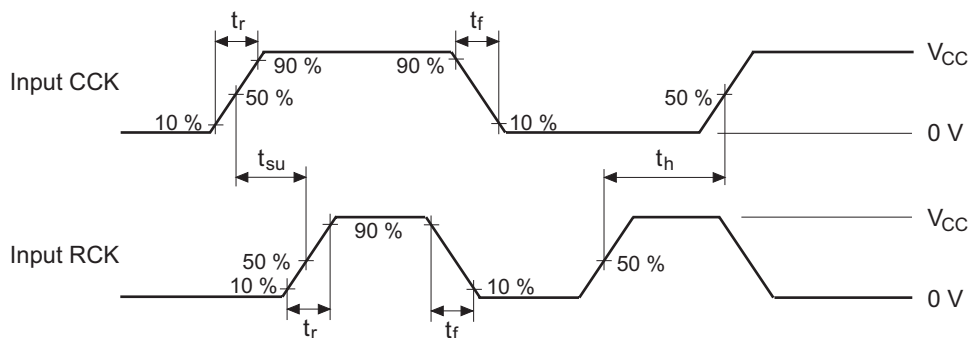
Note : 1. Input waveform : $PRR \leq 1 \text{ MHz}$, duty cycle 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$

• Waveform – 4 ($\overline{CCKEN}$ to CCK)



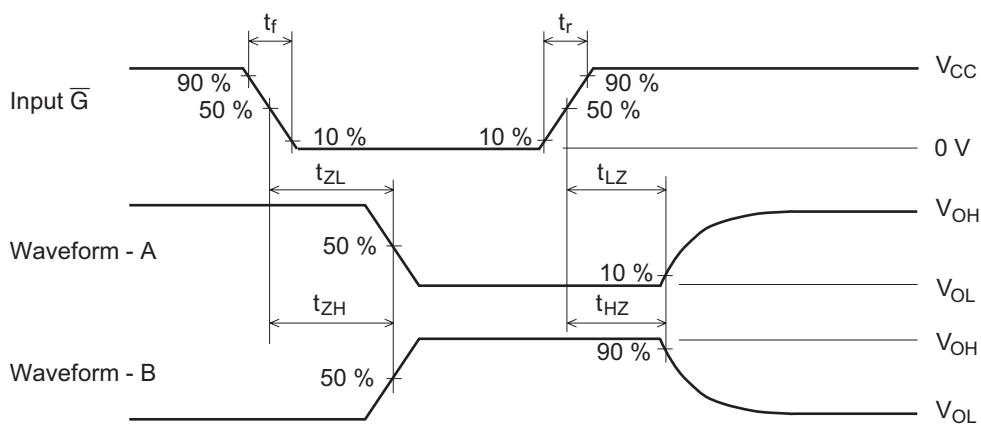
Note : 1. Input waveform : $PRR \leq 1 \text{ MHz}$, duty cycle 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$

• Waveform – 5 (CCK to RCK)



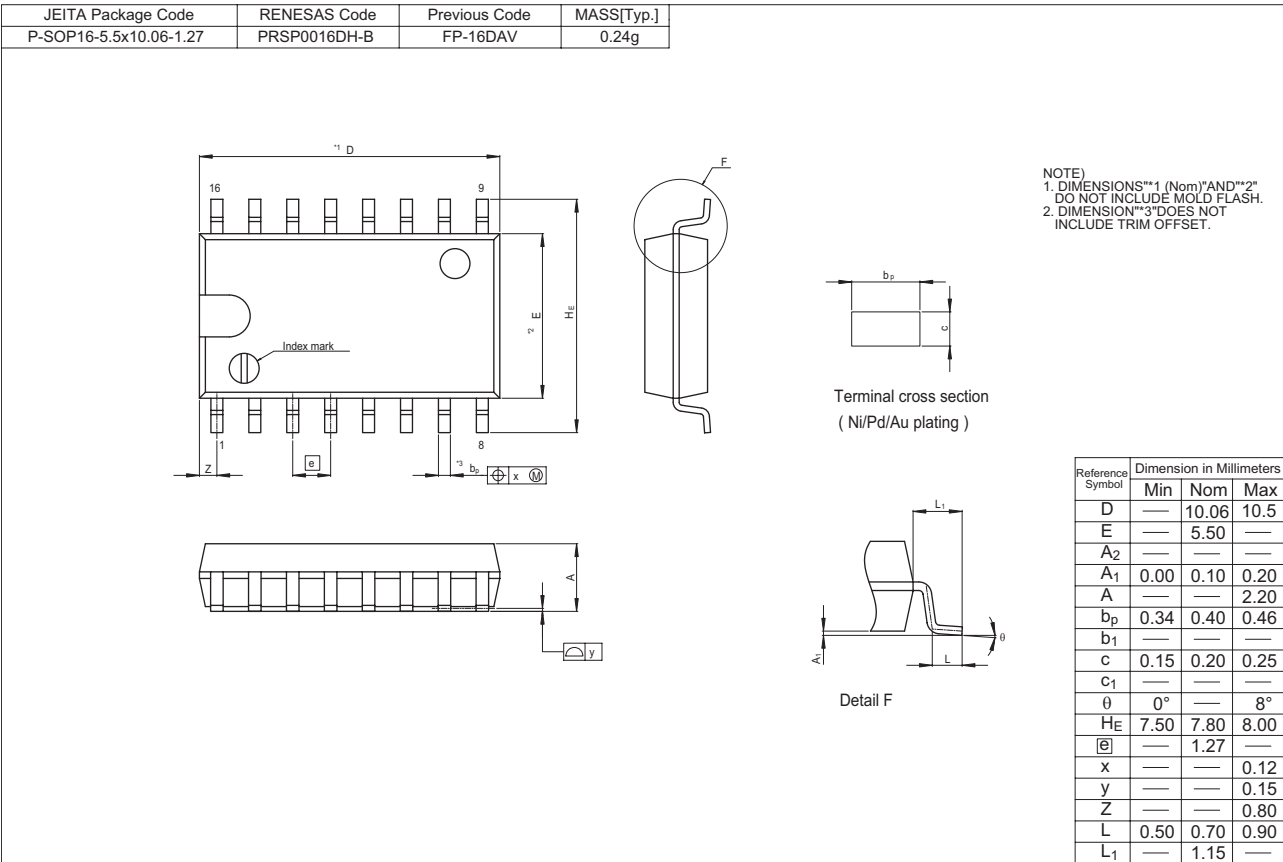
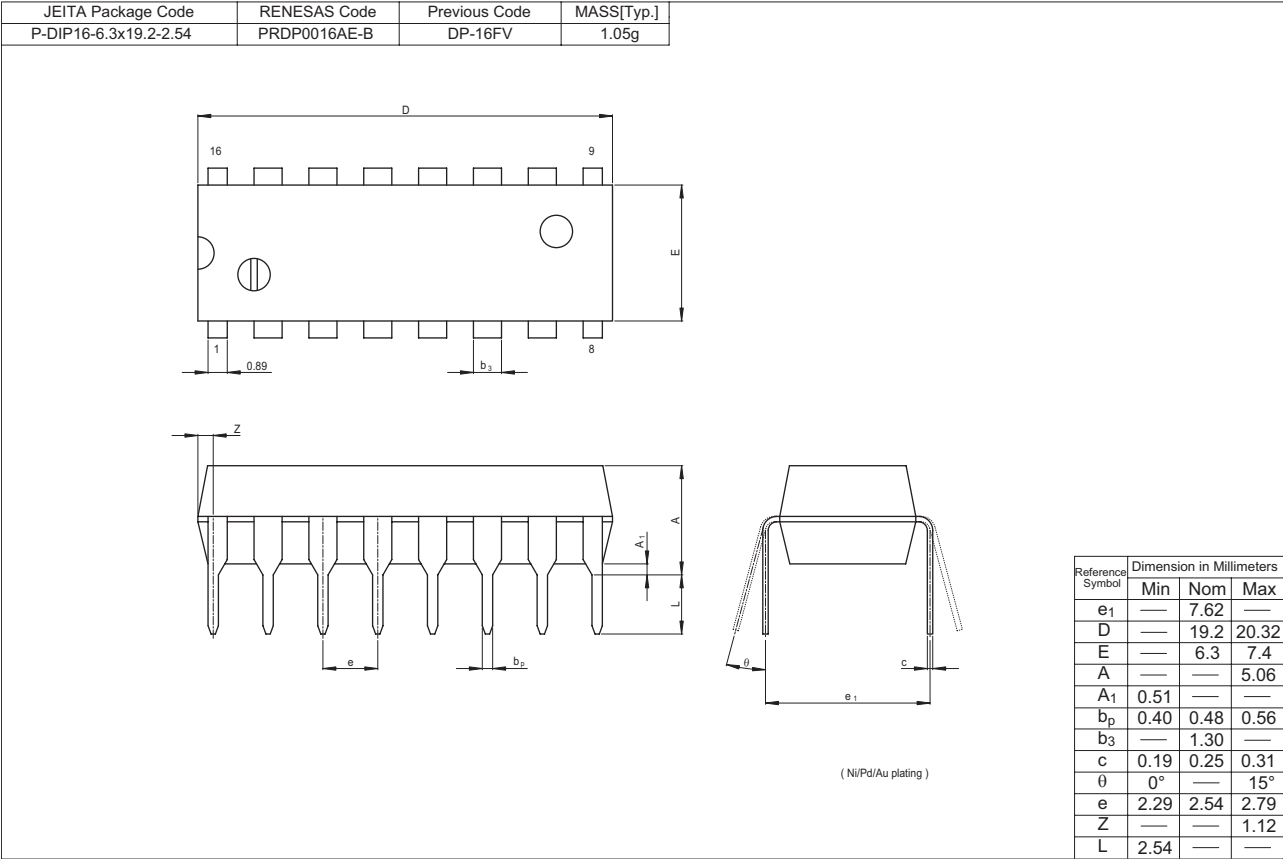
Note : 1. Input waveform : $PRR \leq 1 \text{ MHz}$, duty cycle 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$

• Waveform – 6 (t_{ZL} , t_{ZH} , t_{LZ} , t_{HZ})



- Notes :
1. Input waveform : $PRR \leq 1 \text{ MHz}$, duty cycle 50%, $t_r \leq 6 \text{ ns}$, $t_f \leq 6 \text{ ns}$
 2. Waveform - A is for an output with internal conditions such that the output is low except when disabled by the output control.
 3. Waveform - B is for an output with internal conditions such that the output is high except when disabled by the output control.
 4. The output are measured one at a time with one transition per measurement.

Package Dimensions



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