

HD74LS283

4-bit Binary Full Adder

REJ03D0476-0300 Rev.3.00 Jul.15.2005

The HD74LS283 adder is electrically and functionally identical to the HD74LS83A, respectively; only the arrangement of the terminals has been changed.

This improved full adder performs the addition of two 4-bit binary words.

The sum (Σ) outputs are provided for each bit and the resultant carry (C_4) is obtained from the fourth bits generating the carry term in then nanoseconds.

The adder logic, including the carry, is implemented in its true form.

End around carry can be accomplished without the need for logic or level inversion.

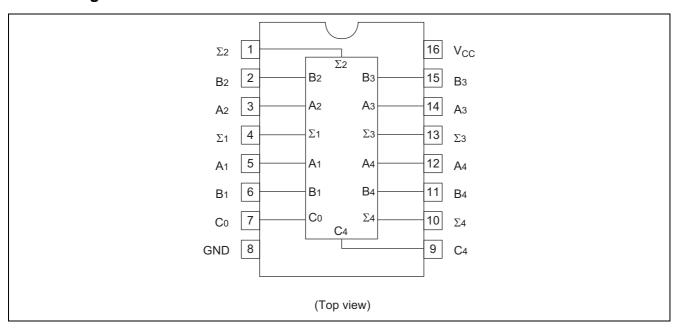
Features

• Ordering Information

Part Name	Package Type	Package Code (Previous Code)	Package Abbreviation	Taping Abbreviation (Quantity)	
HD74LS283P	DILP-16 pin	PRDP0016AE-B (DP-16FV)	Р	_	
HD74LS283FPEL	SOP-16 pin (JEITA)	PRSP0016DH-B (FP-16DAV)	FP	EL (2,000 pcs/reel)	

Note: Please consult the sales office for the above package availability.

Pin Arrangement



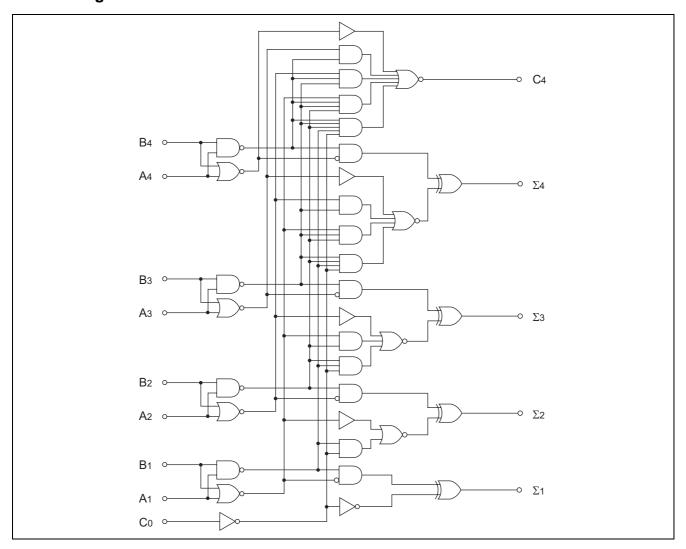
Function Table

				Outputs							
	Inp	uts		When C ₀	=L		When C ₀ = H				
					Wh	en C ₂ = L		When $C_2 = H$			
A ₁	B ₁	A ₂	B ₂	Σ ₁	Σ ₂	C ₂	Σ_1	Σ_2	C ₂		
A ₃	B ₃	A ₄	B ₄	Σ_3	Σ_4	C ₄	Σ_3	Σ_4	C ₄		
L	L	L	L	L	L	L	Н	L	L		
Н	L	L	L	Н	L	L	L	Н	L		
L	Н	L	L	Н	L	L	L	Н	L		
Н	Н	L	L	L	Н	L	Н	Н	L		
L	L	Н	L	L	Н	L	Н	Н	L		
Н	L	Н	L	Н	Н	L	L	L	Н		
L	Н	Н	L	Н	Н	L	L	L	Н		
Н	Н	Н	L	L	L	Н	Н	L	Н		
L	L	L	Н	L	Н	L	Н	Н	L		
Н	L	L	Н	Н	Н	L	L	L	Н		
L	Н	L	Н	Н	Н	L	L	L	Н		
Н	Н	L	Н	L	L	Н	Н	L	Н		
L	L	Н	Н	L	L	Н	Н	L	Н		
Н	L	Н	Н	Н	L	Н	L	Н	Н		
L	Н	Н	Н	Н	L	Н	L	Н	Н		
Н	Н	Н	Н	L	Н	Н	Н	Н	Н		

H; high level, L; low level

Note: Input conditions at A_1 , B_1 , A_2 , B_2 , and C_0 are use to determine outputs Σ_1 and Σ_2 and the value of the internal carry C_2 . The values at C_2 , A_3 , A_4 , and A_4 are then used to determine outputs A_4 , and A_5 , and A_6 .

Block Diagram



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit
Supply voltage	V _{CC}	7	V
Input voltage	V _{IN}	7	V
Power dissipation	P _T	400	mW
Storage temperature	Tstg	-65 to +150	°C

Note: Voltage value, unless otherwise noted, are with respect to network ground terminal.

Recommended Operating Conditions

Item	Symbol	Min	Тур	Max	Unit
Supply voltage	Vcc	4.75	5.00	5.25	V
Output current	I _{OH}	_	_	-400	μΑ
Output current	I _{OL}	_	_	8	mA
Operating temperature	Topr	-20	25	75	°C

Electrical Characteristics

 $(Ta = -20 \text{ to } +75 \text{ }^{\circ}\text{C})$

Item		Symbol	min.	typ.*	max.	Unit	Conditio	n	
Input voltage		V _{IH}	2.0	_	_	V			
		V _{IL}	_	_	0.8	V			
Output valta		V _{OH}	2.7	_	_	V	$V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V}$ $I_{OH} = -400 \mu\text{A}$	$V_{IL} = 0.8 V$	
Output volta	ge	\/	_	_	0.4	V	$I_{OL} = 4 \text{ mA}$ $V_{CC} = 4.75 \text{ V}, V_{IH} = 2 \text{ V},$ $I_{OL} = 8 \text{ mA}$ $V_{IL} = 0.8 \text{ V}$		
		V _{OL}	_	_	0.5	V			
	except C ₀	1	_	_	40	^	V - 5 25 V V - 2 7 V		
	C ₀	I _{IH}	_	_	20	μΑ	$V_{CC} = 5.25 \text{ V}, V_I = 2.7 \text{ V}$		
Input	except C ₀	I	_	_	-0.8	mA	V _{CC} = 5.25 V, V _I = 0.4 \	/	
current	C ₀	- I _{IL}	_	_	-0.4	IIIA	VCC = 3.23 V, VI = 0.4 V		
	except C ₀	l ₁	_	_	0.2	mA	V _{CC} = 5.25 V, V _I = 7 V		
	C ₀	"	_	_	0.1	IIIA	V _{CC} = 5.25 V, V _I = 7 V		
Short-circuit	output current	los	-20	_	-100	mA	V _{CC} = 5.25 V		
				22	39		All inputs grounded		
Supply current		laa		19	34	mA	All B low	V _{CC} = 5.25 V	
		I _{CC}		19	34	111/4	other inputs at 4.5V	v _{CC} = 0.20 V	
				19	34		All inputs at 4.5V		
Input clamp voltage		V_{IK}		_	-1.5	V	$V_{CC} = 4.75 \text{ V}, I_{IN} = -18$	mA	

Note: ${}^*V_{CC} = 5 \text{ V}, \text{ Ta} = 25 {}^{\circ}\text{C}$

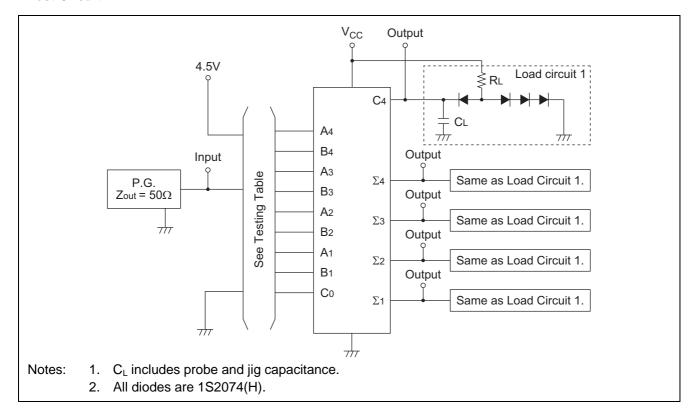
Switching Characteristics

 $(V_{CC} = 5 \text{ V}, \text{Ta} = 25^{\circ}\text{C})$

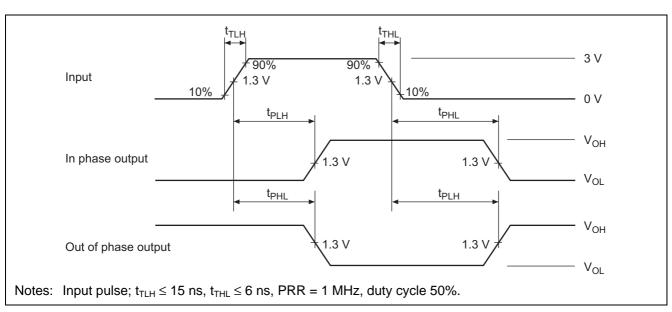
Item	Symbol	Inputs	Outputs	min.	typ.	max.	Unit	Condition
	t _{PLH}	C ₀	Σί	_	16	24	ns	
	t _{PHL}			_	15	24	ns	
	t _{PLH}	Ai, Bi	Σί	_	15	24	ns	
Propagation delay	t _{PHL}			_	15	24	ns	$C_L = 15 \text{ pF},$ $R_L = 2 \text{ k}\Omega$
time	t _{PLH}	C ₀	C ₄	_	11	17	ns	$R_L = 2 k\Omega$
	t _{PHL}			_	11	22	ns	
	t _{PLH}	Ai, Bi	C ₄	_	11	17	ns	
	t _{PHL}			_	12	17	ns	

Testing Method

Test Circuit



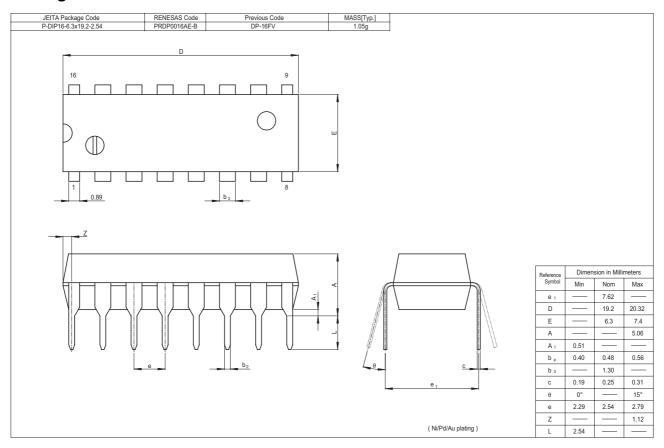
Waveform

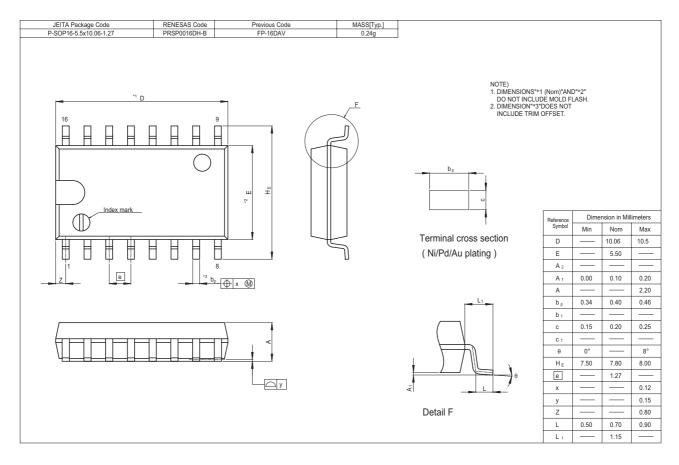


Testing Table

Ite	From input		Inputs						Outputs						
m	to output	\mathbf{B}_4	\mathbf{A}_4	B_3	\mathbf{A}_3	\mathbf{B}_2	\mathbf{A}_2	B ₁	\mathbf{A}_1	Co	C ₄	Σ_4	Σ_3	Σ_2	Σ_1
	0 5: 0	GND	GND	GND	GND	GND	GND	GND	GND	IN	_	_	_	_	OUT
	$C_0 \rightarrow \Sigma i$ or C_4	GND	4.5V	GND	4.5V	GND	4.5V	GND	4.5V	IN	OUT	OUT	OUT	OUT	OUT
		GND	GND	GND	GND	GND	GND	GND	IN	GND					OUT
		GIND	GIND	GIND	GIVD	GIND	GIND	IN	GND	GIND					001
		GND	GND	GND	GND	GND	IN	GND	GND	GND				OUT	
	iрLH	GND	GND	GIND	GND	IN	GND	GIND	GND GND	GIND	_			001	_
		GND C	GND	GND IN IN GND	GND GND	GND	GND	GND	_		OUT		_		
					GND	GIVD	SIND GIVE	OND	OND C	GIND			001		
t_{PLH}		GND	IN	GND	IND GND	GND GND	GND	GND	GND GND	D GND		OUT			
t_{PHL}	Ai or Bi	IN	GND					GIND				001			
	${ ightarrow}\Sigma i$ or C_4	GND	GND GND GND GN	GND	GND GND	GND	4.5V	IN	GND				OUT	OUT	
		GIND	GIND	GIND	GIVD	GIND	GIND	IN	4.5V	GIND				001	001
		GND	GND	GND	GND	4.5V	IN	GND	GND	GND	_		OUT	OUT	
		GIVD	GIVD	GIND	GIVD	IN	4.5V	GIND	GIND	GIND			001	0	
		GND	GND	4.5V	IN	GND	GND	GND	GND	GND		OUT	OUT		
		GIND	GIND	IN	4.5V	GIND	GIND	GIND	GIND	GND		001	001		
		4.5V	IN	GND	GND	GND	GND	GND	GND	GND	OUT	OUT			
		IN	4.5V	טאט	GIND	GIND	GIND	GIND	GIND	GIND	OUT	OUT	_	_	

Package Dimensions





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