

HD74SSTV16857A

1:1 14-bit SSTL_2 Registered Buffer

REJ03D0831-0100 (Previous: ADE-205-695)

Rev.1.00

Apr 07, 2006

Description

The HD74SSTV16857A is a 14-bit registered buffer designed for 2.3 V to 2.7 V Vcc operation and LVCMOS reset (RESET) input / SSTL_2 data (D) inputs and CLK input.

Data flow from D to Q is controlled by differential clock pins (CLK, $\overline{\text{CLK}}$) and the $\overline{\text{RESET}}$. Data is triggered on the positive edge of the positive clock (CLK), and the negative clock ($\overline{\text{CLK}}$) must be used to maintain noise margins. When $\overline{\text{RESET}}$ is low, all registers are reset and all outputs are low.

To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up.

Features

- Supports LVCMOS reset (RESET) input / SSTL_2 data (D) inputs and CLK input
- Differential SSTL_2 (Stub series terminated logic) CLK signal
- Flow through architecture optimizes PCB layout
- Ordering Information

Part Name	Package Type	Package Code (Previous code)	Package Abbreviation	Taping Abbreviation (Quantity)
HD74SSTV16857ATEL	TSSOP-48 pin	PTSP0048KA-A (TTP-48DBV)	T	EL (1,000 pcs / Reel)
HD74SSTV16857ANEL		PTSP0048LA-A (TTP-48DEV)	N	EL (1,000 pcs / Reel)

Note: Please consult the sales office for the above package availability.

Function Table

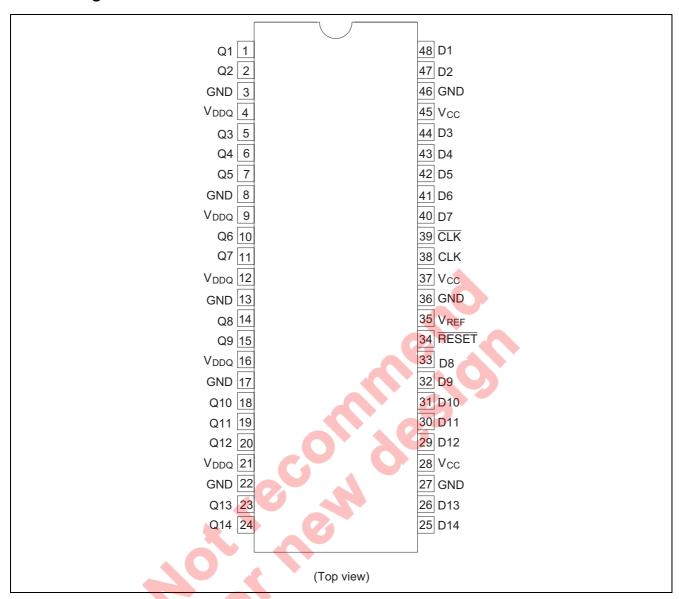
	Output O			
RESET	CLK	CLK	D	Output Q
L	X	X	X	L
Н	\	↑	Н	Н
Н	\	↑	L	L
Н	L or H	H or L	Х	Q_0^{*1}

H: High levelL: Low levelX: Immaterial

↑: Low to high transition ↓: High to low transition

Note: 1. Output level before the indicated steady state input conditions were established.

Pin Arrangement



Absolute Maximum Ratings

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V _{CC} or V _{DDQ}	-0.5 to 3.6	V	
Input voltage *1	VI	-0.5 to V _{DDQ} +0.5	V	
Output voltage *1, 2	Vo	-0.5 to V _{DDQ} +0.5	V	
Input clamp current	I _{IK}	±50	mA	$V_1 < 0$ or $V_1 > V_{CC}$
Output clamp current	I _{OK}	±50	mA	$V_O < 0$ or $V_O > V_{DDQ}$
Continuous output current	I _O	±50	mA	$V_O = 0$ to V_{DDQ}
V _{CC} , V _{DDQ} or GND current / pin	I _{CC} , I _{DDQ} or I _{GND}	±100	mA	
Maximum power dissipation	P _T	115	°C / W	TSSOP
at Ta = 55°C (in still air)				
Storage temperature	Tstg	-65 to +150	°C	

Notes: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device.

These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

- 1. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.
- 2. This current will flow only when the output is in the high state and $V_0 > V_{DDQ}$.

Recommended Operating Conditions

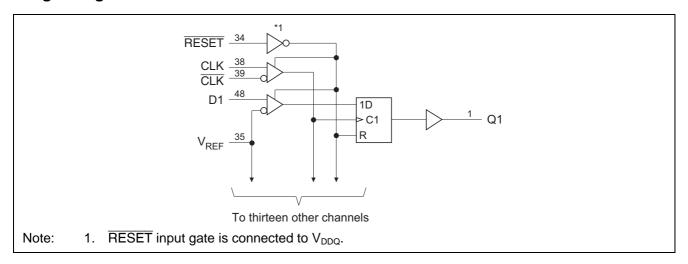
	Item	Symbol	Min	Тур	Max	Unit	Conditions
Supply voltag	e	V_{CC}	V _{DDQ}	2.5	2.7	V	
Output supply	/ voltage	V_{DDQ}	2.3	2.5	2.7	V	
Reference vo	ltage	V_{REF}	1.15	1.25	1.35	V	$V_{REF} = 0.5 \times V_{DDQ}$
Termination v	oltage	V _{TT}	V _{REF} -40 mV	V_{REF}	V _{REF} +40 mV	V	
Input voltage		Vı	0		V _{CC}	V	
AC high level	input voltage	V _{IH}	V _{REF} +310 mV	_	_	V	D
AC low level input voltage		VIL		_	V _{REF} –310 mV	V	D
DC high level	input voltage	V _{IH}	V _{REF} +150 mV	_	_	V	D
DC low level	input voltage	V_{IL}		_	V _{REF} -150 mV	V	D
High level inp	ut voltage	V _{IH}	1.7	_	V _{DDQ} +0.3	V	RESET
Low level inpu	ut voltage	V_{IL}	-0.3	_	0.7	V	RESET
Differential	(Common mode range)	V _{CMR}	0.97	_	1.53	V	CLK, CLK
	(Minimum peak to peak input)	V_{PP}	360	_	_	mV	CLK, CLK
High level out	ligh level output current		_	_	-20	mA	
Low level out	put current	I _{OL}	_	_	20	mA	
Operating ten	nperature	Ta	0	_	70	°C	

Note: The $\overline{\text{RESET}}$ input of the device must be held at V_{DDQ} or GND to ensure proper device operation. The differential inputs must not be floating, unless $\overline{\text{RESET}}$ is low.

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Logic Diagram



Electrical Characteristics

Item	Symbol	V _{CC} (V)	Min	Тур	Max	Unit	Test Conditions
Input diode voltage	Vıĸ	2.3	_	_	-1.2	V	I _{IN} = −18 mA
Output voltage	V _{OH}	2.3 to 2.7	V _{CC} -0.2	_		V	I _{OH} = -100 μA
		2.3	1.95		V _{DDQ}	07.	I _{OH} = −16 mA
	V _{OL}	2.3 to 2.7	_	4	0.2		I _{OL} = 100 μA
		2.3	0		0.35		I _{OL} = 16 mA
Input current (All inp		2.7	_	7 - (±5	μΑ	V _{IN} = 2.7 V or 0
Quiescent supply currer	nt Icc *2	2.7	(e)	25	45	mA	$V_{IN} = V_{IH(AC)}$ or $V_{IL(AC)}$, $I_O = 0$
Standby current	I _{CC (stdy)}	2.7	7 – , 1	\ <u> </u>	10	μΑ	RESET = GND
Dynamic operating clock	k only I _{CCD} *2	2.7	-1	38	45	μΑ/	RESET = V _{CC} ,
						clock	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$,
	1					MHz	CLK and CLK switching 50%
							duty cycle
Dynamic operating per	each I _{CCD} *2	2.7	· —	11	15	μΑ/	$\overline{RESET} = V_{CC}$
data input						clock	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$,
						MHz/	CLK and CLK switching 50%
						data input	duty cycle. One data input
							switching at half clock
*0	Ť				+4		frequency, 50% duty cycle.
Output high *3	r _{OH}	2.3 to 2.7	7	_	20 *4	Ω	$I_{OH} = -20 \text{ mA}$
Output low *3	r _{OL}	2.3 to 2.7	7	_	20 *4	Ω	$I_{OL} = 20 \text{ mA}$
r _{OH} - r _{OL} each	$r_{O(\Delta)}$	2.5	_	_	4	Ω	$I_O = 20 \text{ mA}, Ta = 25^{\circ}\text{C}$
separate bit *3							
Input Data in	puts C _{IN}	2.5 *1	2.5	_	3.5	pF	$V_I = V_{REF} \pm 310 \text{ mV}$
capacitance CLK an	d CLK		2.5	_	3.5		$V_{CMR} = 1.25 \text{ V}, V_{PP} = 360 \text{ mV}$
RESET	Ī			3.0	_		$V_I = V_{CC}$ or GND

Notes: 1. All typical values are at $V_{CC} = 2.5 \text{ V}$, $Ta = 25^{\circ}\text{C}$.

- 2. Total I_{CC} (max) = I_{CC} + { I_{CCD} (clock)×f(clock)} + { I_{CCD} (Data)×1/2f(clock)×14}
- 3. This is effective in the case that it did terminate by resistance.
- 4. See figure. 1, 2.

Switching Characteristics

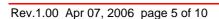
ltem		Symbol	V _{CC} = 2.	5 ± 0.2 V	Unit	Test Condition
		Symbol	Min	Max	Ullit	rest Condition
Clock frequen	cy *1	f _{clock}	_	200	MHz	
Setup time	Fast slew rate *4, 6	t _{su}	0.75	_	ns	Data before CLK↑, CLK↓
	Slow slew rate *5, 6		0.9	_		
Hold time	Fast slew rate *4, 6	t _h	0.75	_	ns	Data after CLK↑, CLK↓
	Slow slew rate *5, 6		0.9	_		
Differential inputs active time		t _{act}	22	_	ns	Data inputs must be low after RESET high.
Differential inputs inactive time		t _{inact}	22	_	ns	Data and clock inputs must be held at valid levels (not floating) after RESET low.
Pulse width Output slew *3		t _w	2.5	_	ns	CLK, CLK "H" or "L"
		t _{SL}	1	4	volt/ns	

 $(C_L = 30 \text{ pF}, R_L = 50 \Omega, V_{REF} = V_{TT} = V_{DDQ} \times 0.5)$

Item	Symbol	$V_{CC} = 2.5 \pm 0.2 \text{ V}$		Unit	FROM	ТО	
item	Symbol	Min	Тур	Max	Oille	(Input)	(Output)
Maximum clock frequency	f _{max}	200	_	70	MHz		
Propagation delay time *2	t _{PLH} , t _{PHL}	1.1	_	2.8	ns	CLK, CLK	Q
	t _{PHL}	_		5.0	3. ON	RESET	Q

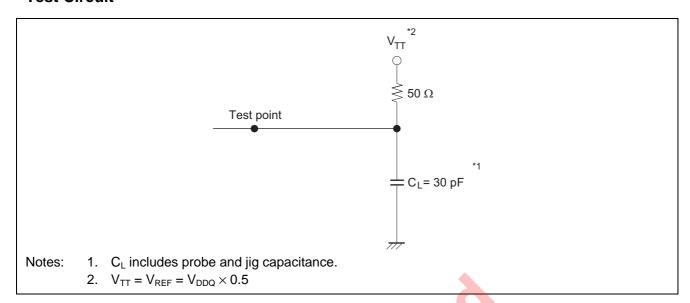
Notes: 1. Although the clock is differential, all timing is relative to CLK going high and CLK going low.

- 2. This timing relationship is specified into test load (see waveforms 3, 4) with all of the outputs switching.
- 3. Assumes into an equivalent, distributed load to the address net structure defined in the application information provided in this specification.
- 4. For data signal input slew rate ≥ 1 V/ns.
- 5. For data signal input slew rate ≥ 0.5 V/ns and < 1 V/ns.
- 6. CLK, CLK signals input slew rates are ≥ 1 V/ns.

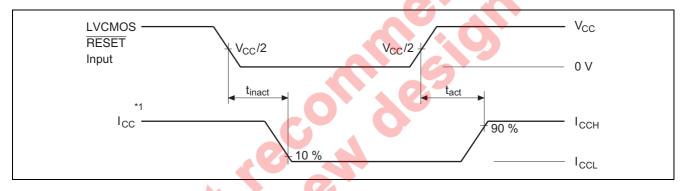




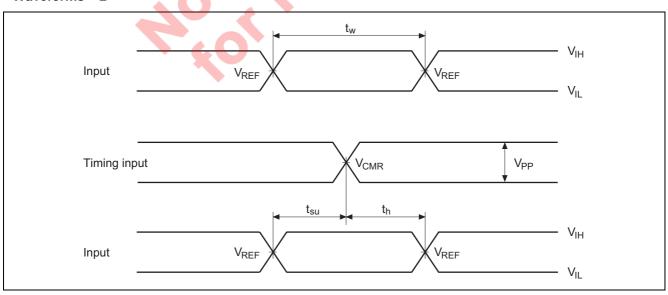
Test Circuit



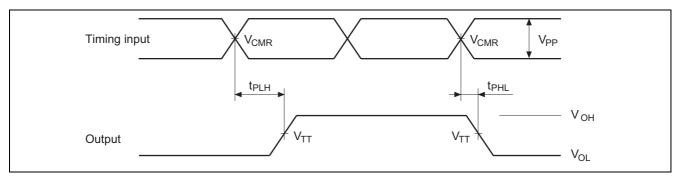
Waveforms - 1



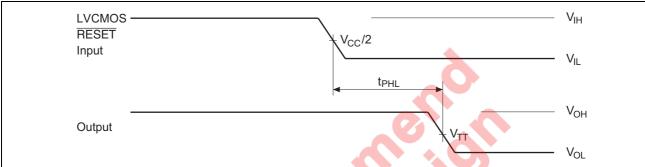
Waveforms - 2



Waveforms - 3



Waveforms - 4



Notes:

- 1. I_{CC} tested with clock and data inputs held at V_{CC} or GND, and $I_0 = 0$ mA.
- 2. All input pulses are supplied by generators having the following characteristics : PRR \leq 10 MHz, Zo = 50 Ω , input slew rate = 1 V/ns \pm 20% (unless otherwise specified).
- 3. The outputs are measured one at a time with one transition per measurement.
- 4. $V_{TT} = V_{REF} = V_{DDQ}/2$
- 5. V_{IH} = V_{REF}+310 mV (AC voltage levels) for differential inputs. V_{IH} = V_{CC} for LVCMOS input.
 6. V_{IL} = V_{REF}-310 mV (AC voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
- 7. t_{PLH} and t_{PHL} are the same as t_{pd}

Application Data

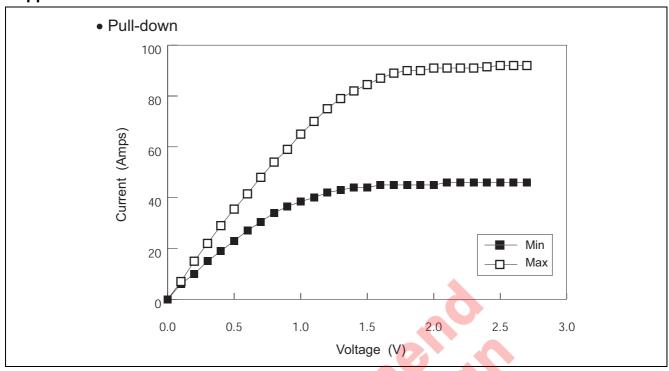


Figure 1

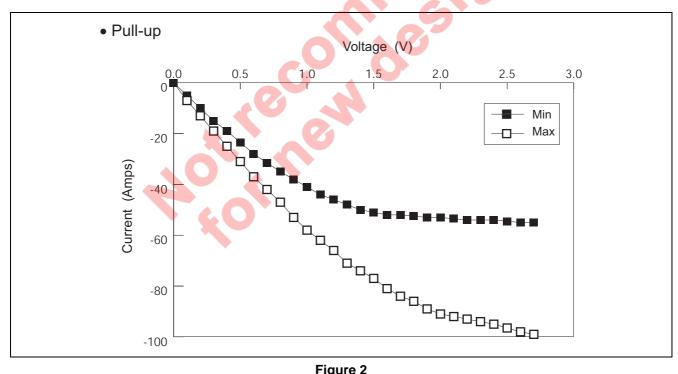
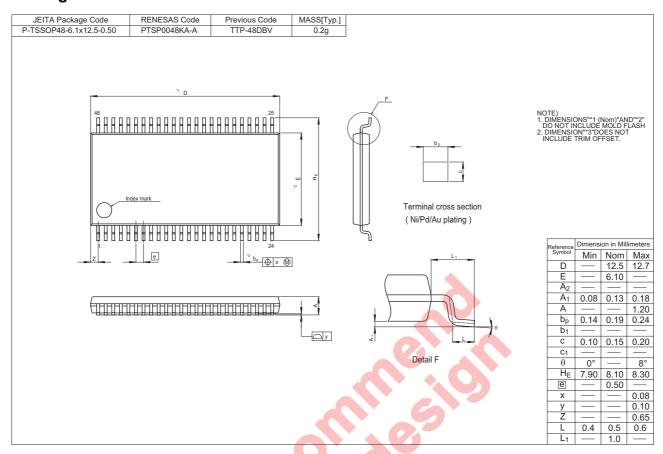


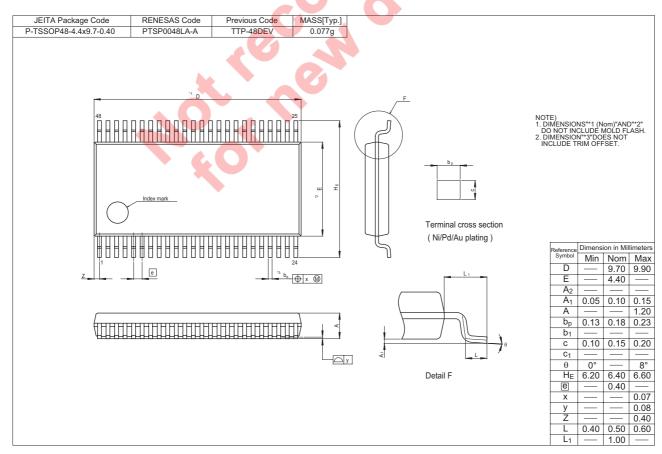
Figure 2

Curve Data

	Pull-c	down	Pull-up		
Voltage (V)	I (mA)	I (mA)	I (mA)	I (mA)	
	Min	Max	Min	Max	
0.0	0	0	0	0	
0.1	6	7	-6	– 7	
0.2	11.5	15	-11.5	-13	
0.3	16	22	-16	-19	
0.4	20	29	-20	-25	
0.5	23	35.5	-23.5	-31	
0.6	27	41.5	-28	-37	
0.7	30.5	48	-31.5	-42	
0.8	34	54	-35	-47	
0.9	36.5	59	-38	-53	
1.0	38.5	65	-41	-58	
1.1	40	70	-4 4	-62	
1.2	42	75	-46	-66	
1.3	43	79	-48	-71	
1.4	44	82	-50	-74	
1.5	44	84.5	-51	–77	
1.6	45	87	-52	-81	
1.7	45	89	-52	-84	
1.8	45	90	-52.5	-86	
1.9	45	90	-53	-89	
2.0	45	91	-53	– 91	
2.1	46	91	-53.5	-92	
2.2	46	91	– 54	-93	
2.3	46	91	-54	-94	
2.4	46	91.5	-54	– 95	
2.5	46	92	-54.5	-96.5	
2.6	46	92	– 55	-98	
2.7	46	92	-55	-99	

Package Dimensions





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