

To all our customers

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Customer Support Dept.  
April 1, 2003

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# HM628512CI Series

Wide Temperature Range Version  
4 M SRAM (512-kword  $\times$  8-bit)



ADE-203-1211C (Z)  
Rev. 3.0  
Dec. 18, 2002

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## Description

The Hitachi HM628512CI is a 4-Mbit static RAM organized 512-kword  $\times$  8-bit. HM628512CI Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). The HM628512CI Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has packaged in 32-pin SOP, 32-pin TSOP II and 32-pin DIP.

## Features

- Single 5 V supply
- Access time: 55/70 ns (max)
- Power dissipation
  - Active: 10 mW/MHz (typ)
  - Standby: 4  $\mu$ W (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly TTL compatible: All inputs and outputs
- Battery backup operation
- Operating temperature:  $-40$  to  $+85^{\circ}\text{C}$

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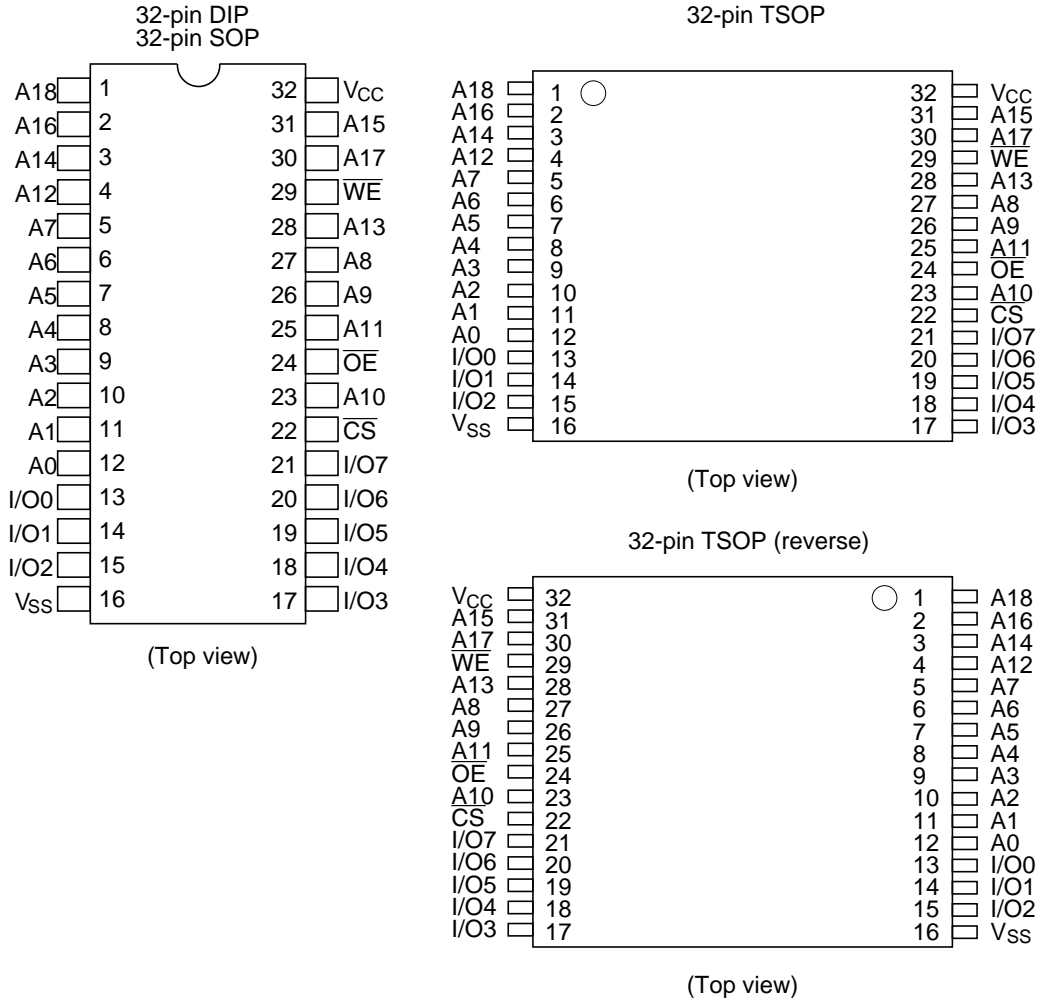
## HM628512CI Series

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### Ordering Information

Type No.	Access time	Package
HM628512CLPI-7	70 ns	600-mil 32-pin plastic DIP (DP-32)
HM628512CLFPI-5	55 ns	525-mil 32-pin plastic SOP (FP-32D)
HM628512CLFPI-7	70 ns	
HM628512CLTTI-5	55 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM628512CLTTI-7	70 ns	
HM628512CLRRI-7	70 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)

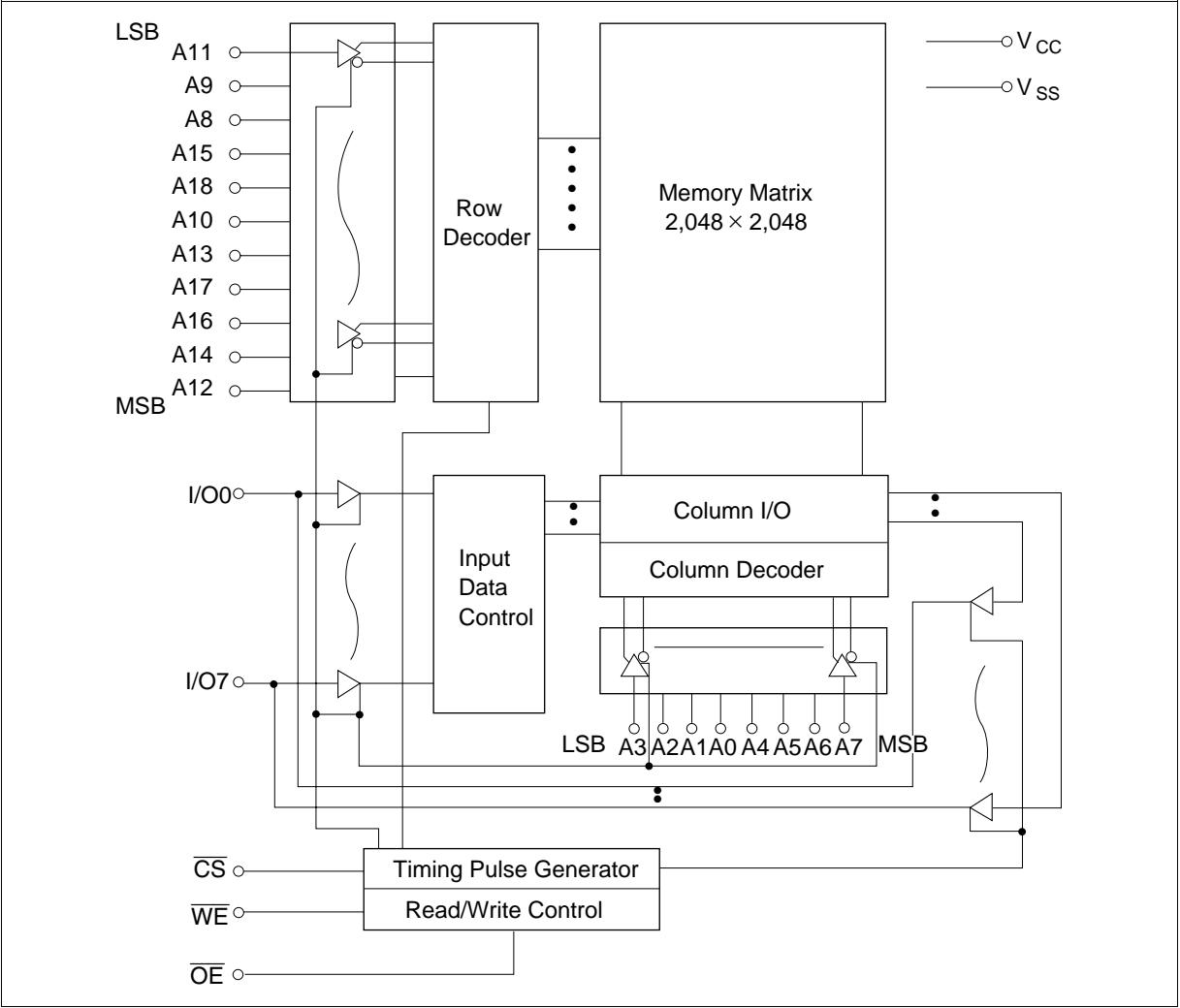
## Pin Arrangement



## Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
$\overline{CS}$	Chip select
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
$V_{CC}$	Power supply
$V_{SS}$	Ground

Block Diagram



## Function Table

$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	Mode	$V_{CC}$ current	Dout pin	Ref. cycle
×	H	×	Not selected	$I_{SB}, I_{SB1}$	High-Z	—
H	L	H	Output disable	$I_{CC}$	High-Z	—
H	L	L	Read	$I_{CC}$	Dout	Read cycle
L	L	H	Write	$I_{CC}$	Din	Write cycle (1)
L	L	L	Write	$I_{CC}$	Din	Write cycle (2)

Note: ×: H or L

## Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	$V_{CC}$	−0.5 to +7.0	V
Voltage on any pin relative to $V_{SS}$	$V_T$	−0.5* <sup>1</sup> to $V_{CC} + 0.3$ * <sup>2</sup>	V
Power dissipation	$P_T$	1.0	W
Operating temperature	$T_{opr}$	−40 to +85	°C
Storage temperature	$T_{stg}$	−55 to +125	°C
Storage temperature under bias	$T_{bias}$	−40 to +85	°C

Notes: 1.  $V_T$  min: −3.0 V for pulse half-width ≤ 30 ns.

2. Maximum voltage is 7.0 V.

## Recommended DC Operating Conditions ( $T_a = -40$ to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	$V_{CC}$	4.5	5.0	5.5	V
	$V_{SS}$	0	0	0	V
Input high voltage	$V_{IH}$	2.4	—	$V_{CC} + 0.3$	V
Input low voltage	$V_{IL}$	−0.3* <sup>1</sup>	—	0.6	V

Note: 1.  $V_{IL}$  min: −3.0 V for pulse half-width ≤ 30 ns.

## DC Characteristics

Parameter		Symbol	Min	Typ* <sup>1</sup>	Max	Unit	Test conditions
Input leakage current		$ I_{LI} $	—	—	1	$\mu\text{A}$	$V_{in} = V_{SS}$ to $V_{CC}$
Output leakage current		$ I_{LO} $	—	—	1	$\mu\text{A}$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ , $V_{I/O} = V_{SS}$ to $V_{CC}$
Operating power supply current: DC		$I_{CC}$	—	1.5	3	mA	$\overline{CS} = V_{IL}$ , others = $V_{IH}/V_{IL}$ , $I_{I/O} = 0$ mA
Operating power supply current	HM628512CI-5	$I_{CC1}$	—	8	25	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$ , others = $V_{IH}/V_{IL}$ $I_{I/O} = 0$ mA
	HM628512CI-7	$I_{CC1}$	—	7	25	mA	
Operating power supply current		$I_{CC2}$	—	2	5	mA	Cycle time = 1 $\mu\text{s}$ , duty = 100% $I_{I/O} = 0$ mA, $\overline{CS} \leq 0.2$ V $V_{IH} \geq V_{CC} - 0.2$ V, $V_{IL} \leq 0.2$ V
Standby power supply current: DC		$I_{SB}$	—	0.1	0.5	mA	$\overline{CS} = V_{IH}$
Standby power supply current (1): DC		$I_{SB1}$	—	0.8* <sup>2</sup>	20* <sup>2</sup>	$\mu\text{A}$	$V_{in} \geq 0$ V, $\overline{CS} \geq V_{CC} - 0.2$ V
Output low voltage		$V_{OL}$	—	—	0.4	V	$I_{OL} = 2.1$ mA
Output high voltage		$V_{OH}$	2.4	—	—	V	$I_{OH} = -1.0$ mA

Notes: 1. Typical values are at  $V_{CC} = 5.0$  V,  $T_a = +25^\circ\text{C}$  and specified loading, and not guaranteed.

## Capacitance ( $T_a = +25^\circ\text{C}$ , $f = 1$ MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance* <sup>1</sup>	$C_{in}$	—	8	pF	$V_{in} = 0$ V
Input/output capacitance* <sup>1</sup>	$C_{I/O}$	—	10* <sup>2</sup>	pF	$V_{I/O} = 0$ V

Note: 1. This parameter is sampled and not 100% tested.

2.  $C_{I/O}$  max = 12 pF only for HM628512CLPI Series.



**AC Characteristics** ( $T_a = -40$  to  $+85^{\circ}\text{C}$ ,  $V_{CC} = 5\text{ V} \pm 10\%$ , unless otherwise noted.)

**Test Conditions**

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input and output timing reference levels: 1.5 V
- Output load: 1 TTL Gate +  $C_L$  (50 pF) (HM628512CI-5)  
1 TTL Gate +  $C_L$  (100 pF) (HM628512CI-7)  
(Including scope and jig)

**Read Cycle**

		HM628512CI					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Read cycle time	t <sub>RC</sub>	55	—	70	—	ns	
Address access time	t <sub>AA</sub>	—	55	—	70	ns	
Chip select access time	t <sub>CO</sub>	—	55	—	70	ns	
Output enable to output valid	t <sub>OE</sub>	—	25	—	35	ns	
Chip selection to output in low-Z	t <sub>LZ</sub>	10	—	10	—	ns	2
Output enable to output in low-Z	t <sub>OLZ</sub>	5	—	5	—	ns	2
Chip deselection to output in high-Z	t <sub>HZ</sub>	0	20	0	25	ns	1, 2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	ns	1, 2
Output hold from address change	t <sub>OH</sub>	10	—	10	—	ns	

## Write Cycle

		HM628512CI					
		-5		-7			
Parameter	Symbol	Min	Max	Min	Max	Unit	Notes
Write cycle time	t <sub>WC</sub>	55	—	70	—	ns	
Chip selection to end of write	t <sub>CW</sub>	50	—	60	—	ns	4
Address setup time	t <sub>AS</sub>	0	—	0	—	ns	5
Address valid to end of write	t <sub>AW</sub>	50	—	60	—	ns	
Write pulse width	t <sub>WP</sub>	40	—	50	—	ns	3, 12
Write recovery time	t <sub>WR</sub>	0	—	0	—	ns	6
$\overline{WE}$ to output in high-Z	t <sub>WHZ</sub>	0	20	0	25	ns	1, 2, 7
Data to write time overlap	t <sub>DW</sub>	25	—	30	—	ns	
Data hold from write time	t <sub>DH</sub>	0	—	0	—	ns	
Output active from output in high-Z	t <sub>OW</sub>	5	—	5	—	ns	2
Output disable to output in high-Z	t <sub>OHZ</sub>	0	20	0	25	ns	1, 2, 7

Notes: 1.  $t_{HZ}$ ,  $t_{OHZ}$  and  $t_{WHZ}$  are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and a low  $\overline{WE}$ . A write begins at the later transition of  $\overline{CS}$  going low or  $\overline{WE}$  going low. A write ends at the earlier transition of  $\overline{CS}$  going high or  $\overline{WE}$  going high.  $t_{WP}$  is measured from the beginning of write to the end of write.

4.  $t_{CW}$  is measured from  $\overline{CS}$  going low to the end of write.

5.  $t_{AS}$  is measured from the address valid to the beginning of write.

6.  $t_{WR}$  is measured from the earlier of  $\overline{WE}$  or  $\overline{CS}$  going high to the end of write cycle.

7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

8. If the  $\overline{CS}$  low transition occurs simultaneously with the  $\overline{WE}$  low transition or after the  $\overline{WE}$  transition, the output remain in a high impedance state.

9. Dout is the same phase of the write data of this write cycle.

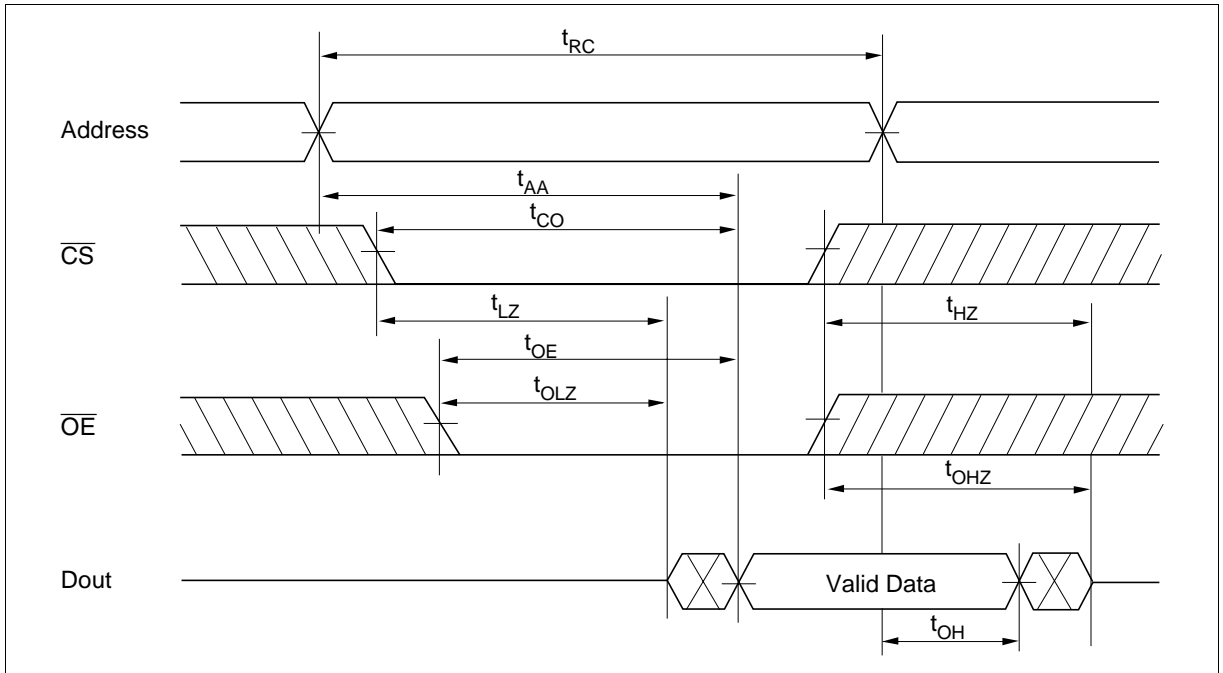
10. Dout is the read data of next address.

11. If  $\overline{CS}$  is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

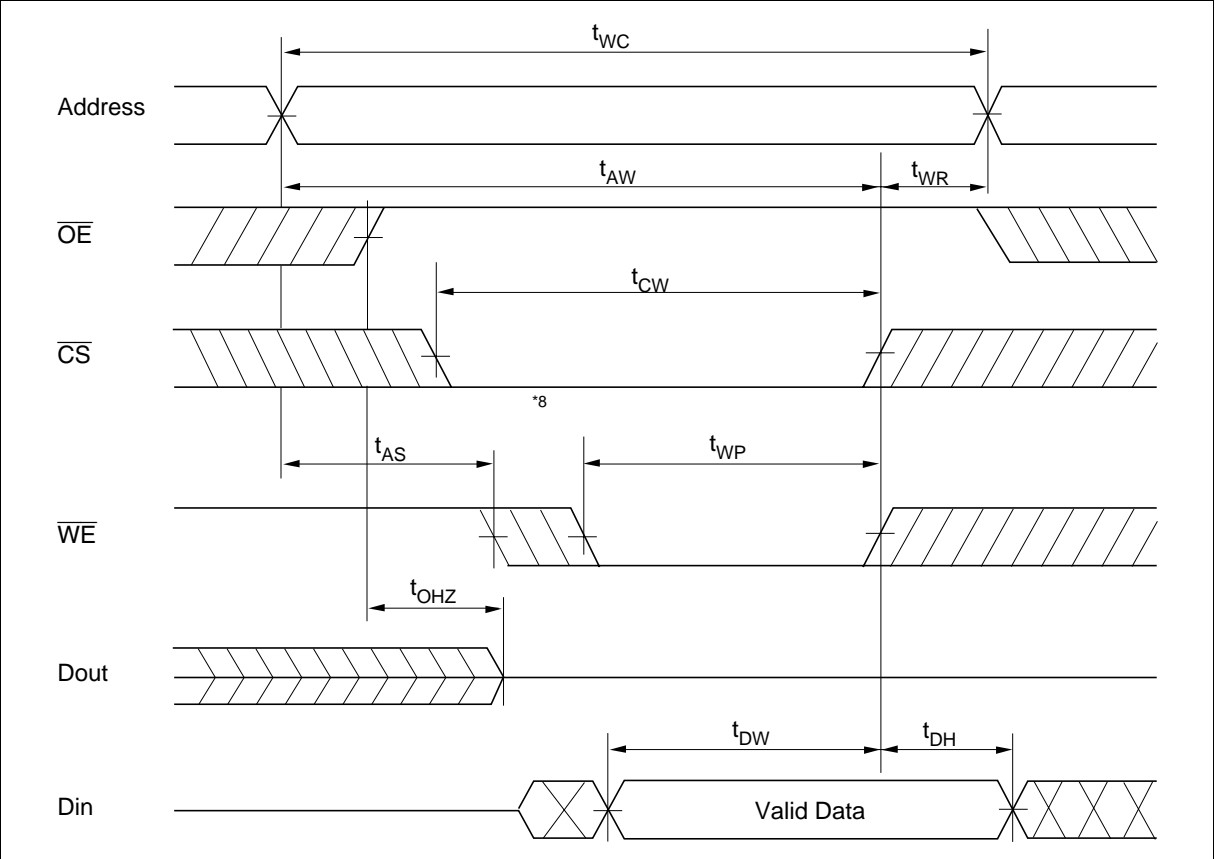
12. In the write cycle with  $\overline{OE}$  low fixed,  $t_{WP}$  must satisfy the following equation to avoid a problem of data bus contention.  $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

## Timing Waveforms

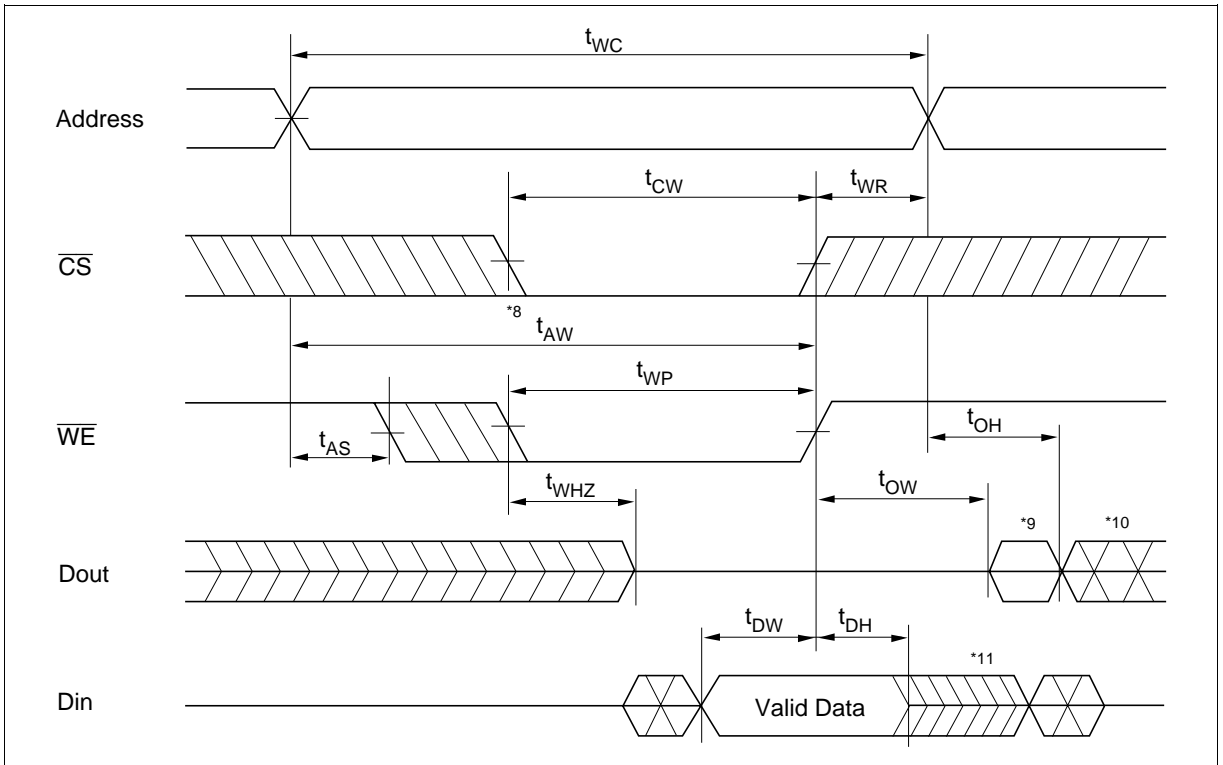
### Read Timing Waveform ( $\overline{WE} = V_{IH}$ )



Write Timing Waveform (1) ( $\overline{\text{OE}}$  Clock)



Write Timing Waveform (2) ( $\overline{\text{OE}}$  Low Fixed)

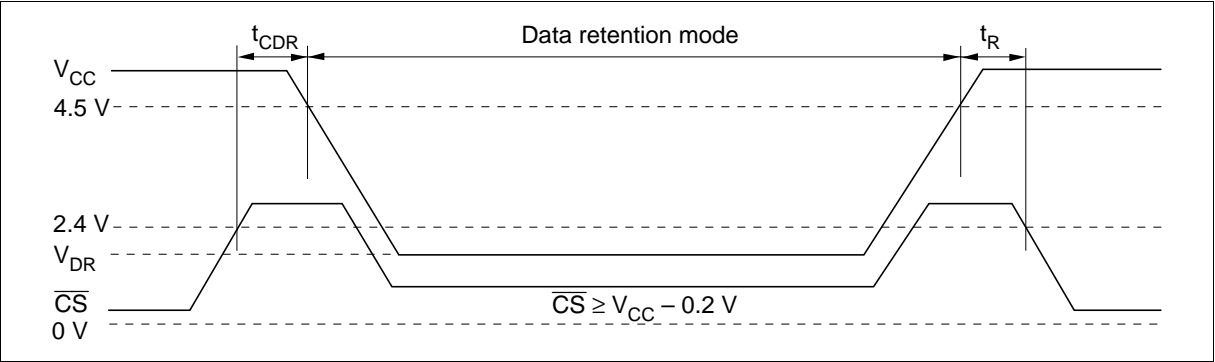


Low V<sub>CC</sub> Data Retention Characteristics (Ta = -40 to +85°C)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions*2
V <sub>CC</sub> for data retention	V <sub>DR</sub>	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$ , Vin ≥ 0 V
Data retention current	I <sub>CDDR</sub>	—	0.8*3	20*1	μA	V <sub>CC</sub> = 3.0 V, Vin ≥ 0 V $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
Chip deselect to data retention time	t <sub>CDR</sub>	0	—	—	ns	See retention waveform
Operation recovery time	t <sub>R</sub>	t <sub>RC</sub> *4	—	—	ns	

- Notes:
- 1. 10 μA (max) at Ta = -40 to +40°C.
  - 2.  $\overline{CS}$  controls address buffer,  $\overline{WE}$  buffer,  $\overline{OE}$  buffer, and Din buffer. In data retention mode, Vin levels (address,  $\overline{WE}$ ,  $\overline{OE}$ , I/O) can be in the high impedance state.
  - 3. Typical values are at V<sub>CC</sub> = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.
  - 4. t<sub>RC</sub> = read cycle time.

Low V<sub>CC</sub> Data Retention Timing Waveform ( $\overline{CS}$  Controlled)

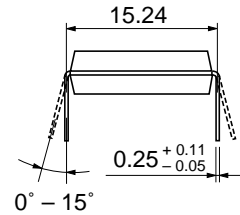
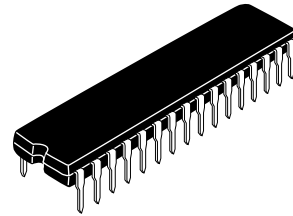
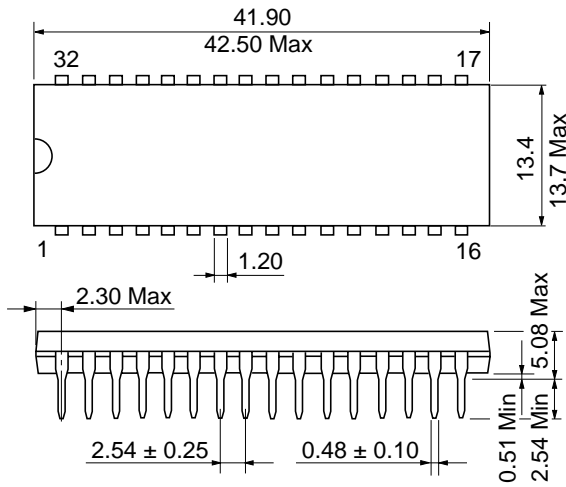


# Package Dimensions

## HM628512CLPI Series (DP-32)

As of July, 2002

Unit: mm



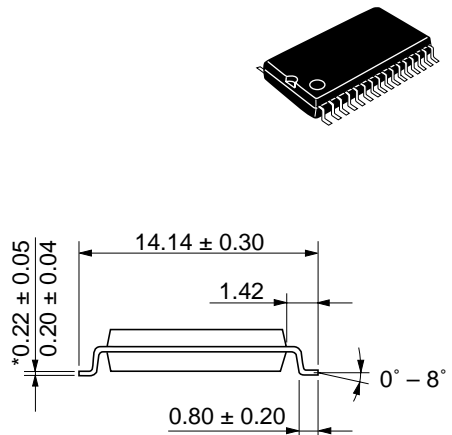
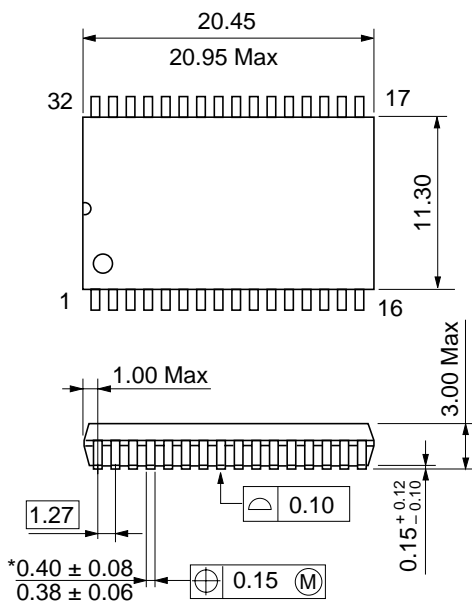
Hitachi Code	DP-32
JEDEC	—
JEITA	Conforms
Mass (reference value)	5.1 g

# HM628512CI Series

## Package Dimensions (cont.)

### HM628512CLFPI Series (FP-32D)

As of July, 2002  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	FP-32D
JEDEC	Conforms
JEITA	—
Mass (reference value)	1.3 g

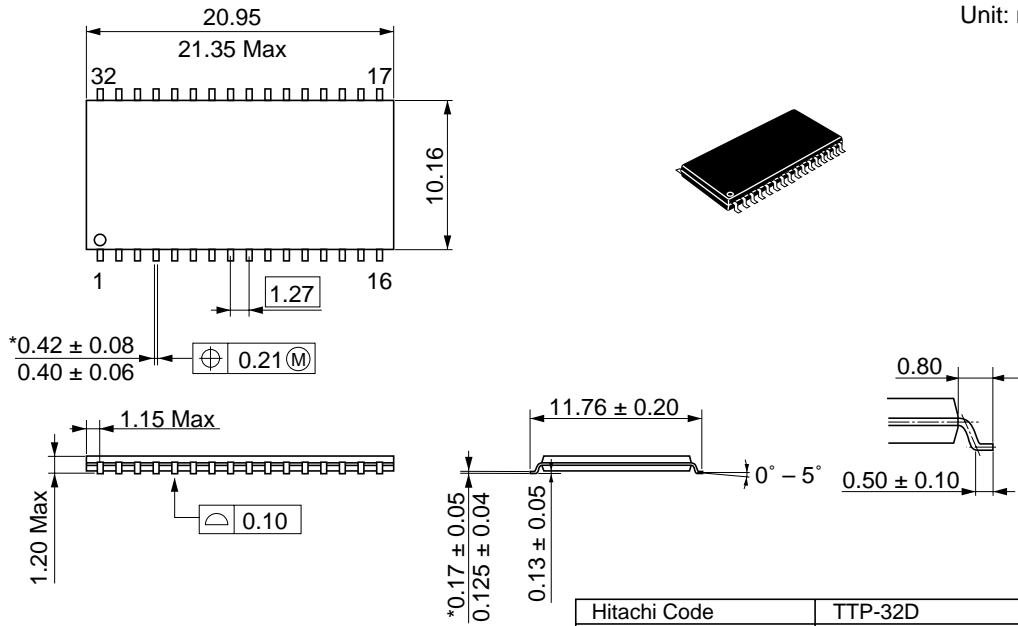


## Package Dimensions (cont.)

## HM628512CLTTI Series (TTP-32D)

As of July, 2002

Unit: mm

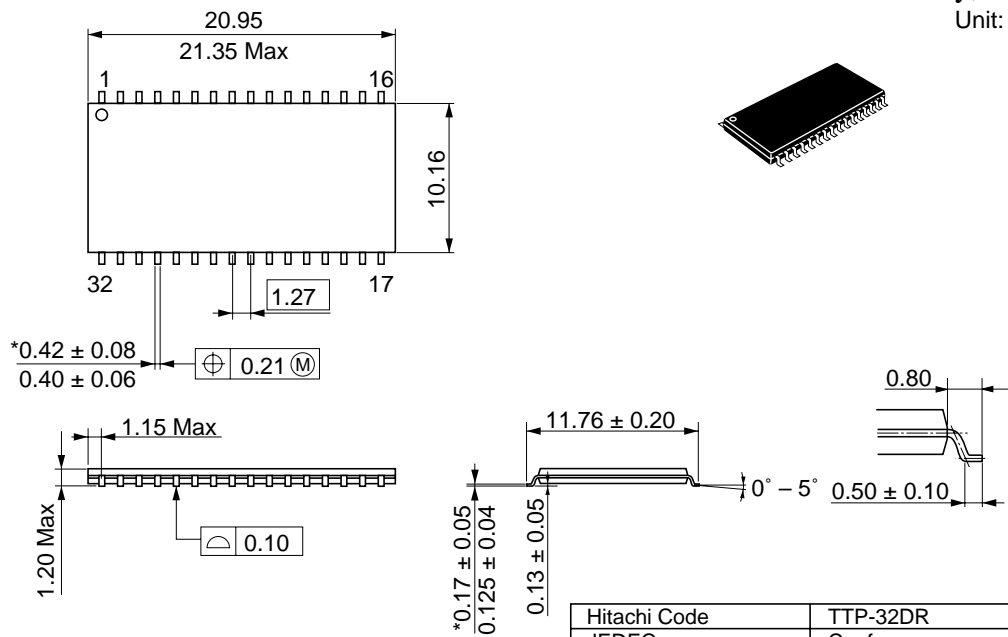

$$\frac{\text{*Dimension including the plating thickness}}{\text{Base material dimension}}$$

Hitachi Code	TTP-32D
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.51 g

Package Dimensions (cont.)

HM628512CLRRI Series (TTP-32DR)

As of July, 2002  
Unit: mm



\*Dimension including the plating thickness  
Base material dimension

Hitachi Code	TTP-32DR
JEDEC	Conforms
JEITA	—
Mass (reference value)	0.51 g

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