
HM62A16100I Series

Wide Temperature Range Version
16 M SRAM (1-Mword \times 16-bit)

REJ03C0053-0001Z
Preliminary
Rev. 0.01
Jun.02.2003

Description

The Renesas HM62A16100I Series is 16-Mbit static RAM organized 1-Mword \times 16-bit. HM62A16100I Series has realized higher density, higher performance and low power consumption by employing CMOS process technology (6-transistor memory cell). It offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It has the package variations of 48-bump chip size package with 0.75 mm bump pitch for high density surface mounting.

Features

- Single 1.8 V supply: 1.65 V to 2.2 V
- Fast access time: 70 ns (max)
- Power dissipation:
 - Active: 3.6 mW/MHz (typ)
 - Standby: 0.9 μ W (typ)
- Completely static memory.
 - No clock or timing strobe required
- Equal access and cycle times
- Common data input and output.
 - Three state output
- Battery backup operation.
 - 2 chip selection for battery backup
- Temperature range: -40 to $+85^{\circ}\text{C}$

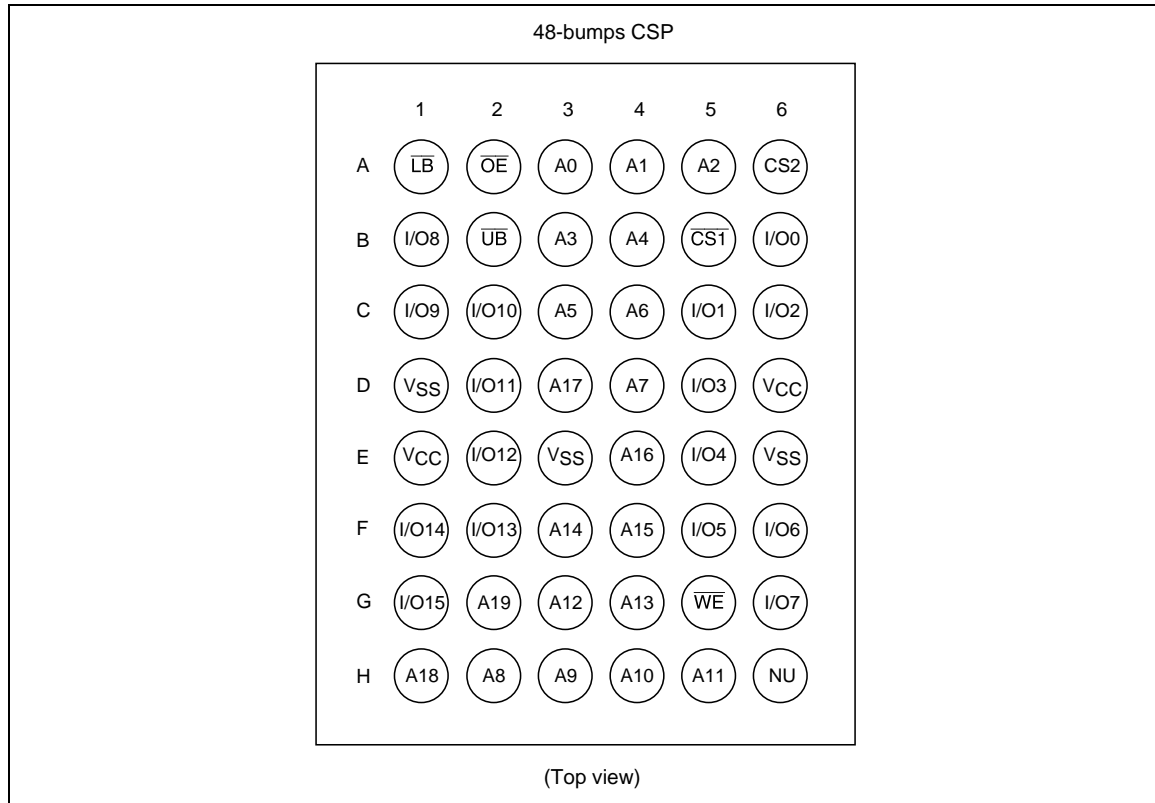
Preliminary: The specification of this device are subject to change without notice. Please contact your nearest Renesas Technology's Sales Dept. regarding specification.

HM62A16100I Series

Ordering Information

| Type No. | Access time | Package |
|--------------------|--------------------|---|
| HM62A16100LBPI-7 | 70 ns | 48-bump CSP with 0.75 mm bump pitch (TBP-48F) |
| HM62A16100LBPI-7SL | 70 ns | |

Pin Arrangement

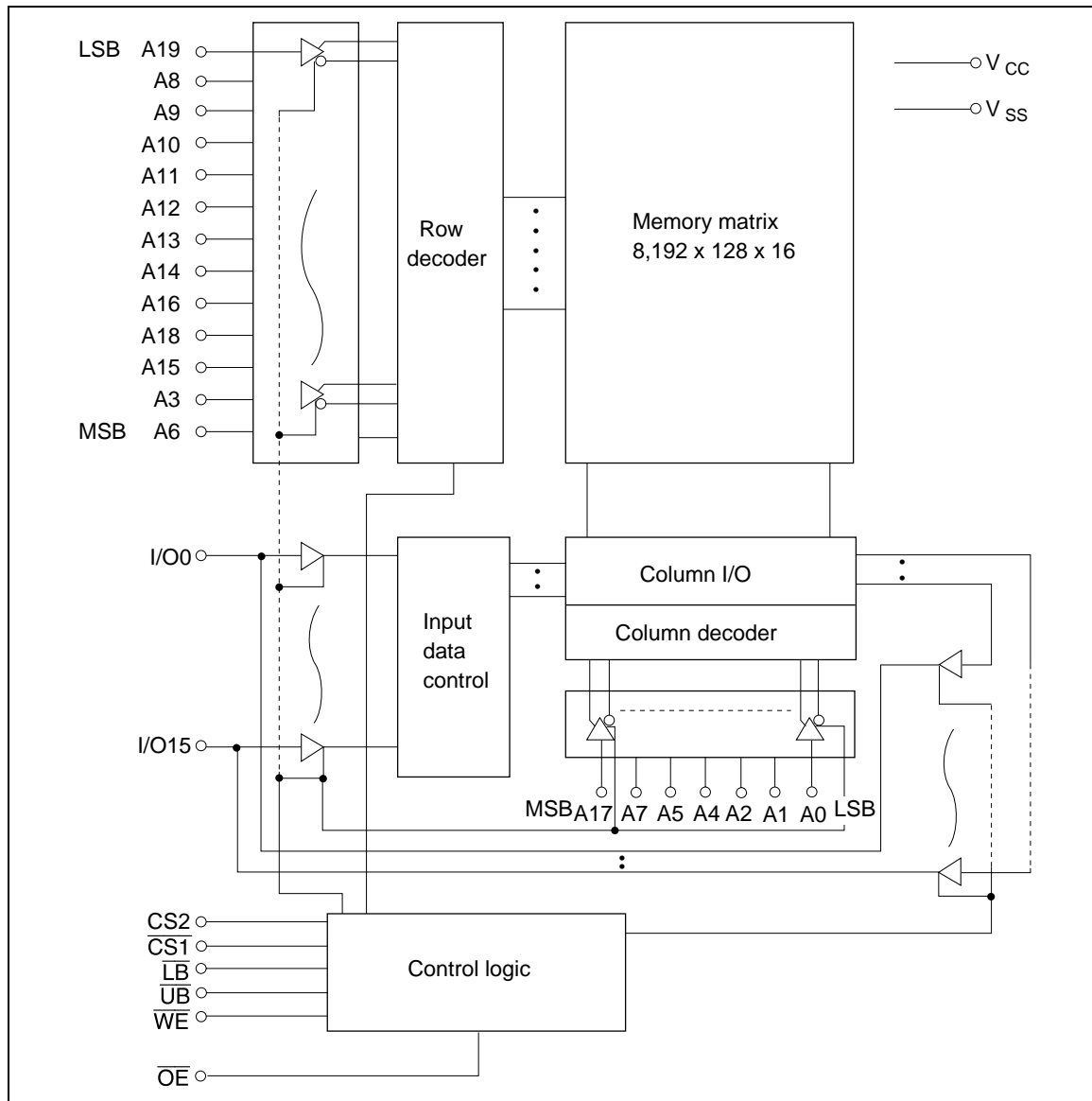


Pin Description

| Pin name | Function |
|------------------|--------------------------|
| A0 to A19 | Address input |
| I/O0 to I/O15 | Data input/output |
| CS1 | Chip select 1 |
| CS2 | Chip select 2 |
| WE | Write enable |
| OE | Output enable |
| LB | Lower byte select |
| UB | Upper byte select |
| V _{cc} | Power supply |
| V _{ss} | Ground |
| NU ^{*1} | Not used (test mode pin) |

Note: 1. This pin should be connected to a ground (V_{ss}), or not be connected (open).

Block Diagram



HM62A16100I Series

Operation Table

| CS1 | CS2 | WE | OE | UB | LB | I/O0 to I/O7 | I/O8 to I/O15 | Operation |
|-----|-----|----|----|----|----|--------------|---------------|------------------|
| H | × | × | × | × | × | High-Z | High-Z | Standby |
| × | L | × | × | × | × | High-Z | High-Z | Standby |
| × | × | × | × | H | H | High-Z | High-Z | Standby |
| L | H | H | L | L | L | Dout | Dout | Read |
| L | H | H | L | H | L | Dout | High-Z | Lower byte read |
| L | H | H | L | L | H | High-Z | Dout | Upper byte read |
| L | H | L | × | L | L | Din | Din | Write |
| L | H | L | × | H | L | Din | High-Z | Lower byte write |
| L | H | L | × | L | H | High-Z | Din | Upper byte write |
| L | H | H | H | × | × | High-Z | High-Z | Output disable |

Note: H: V_{IH} , L: V_{IL} , ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

| Parameter | Symbol | Value | Unit |
|--|----------|---|------|
| Power supply voltage relative to V_{SS} | V_{CC} | -0.3 to +2.6 | V |
| Terminal voltage on any pin relative to V_{SS} | V_T | -0.3* ¹ to $V_{CC} + 0.3$ * ² | V |
| Power dissipation | P_T | 1.0 | W |
| Storage temperature range | Tstg | -55 to +125 | °C |
| Storage temperature range under bias | Tbias | -40 to +85 | °C |

Notes: 1. V_T min: -2.0 V for pulse half-width ≤ 10 ns.

2. Maximum voltage is +2.6 V.

DC Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit | Note |
|---------------------------|----------|----------------------|-----|----------------------|------|------|
| Supply voltage | V_{CC} | 1.65 | 1.8 | 2.2 | V | |
| | V_{SS} | 0 | 0 | 0 | V | |
| Input high voltage | V_{IH} | $0.75 \times V_{CC}$ | — | $V_{CC} + 0.3$ | V | |
| Input low voltage | V_{IL} | -0.3 | — | $0.25 \times V_{CC}$ | V | 1 |
| Ambient temperature range | Ta | -40 | — | 85 | °C | |

Note: 1. V_{IL} min: -2.0 V for pulse half-width ≤ 10 ns.

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DC Characteristics

| Parameter | Symbol | Min | Typ* ¹ | Max | Unit | Test conditions |
|---------------------------|--------------------------|----------------|-------------------|-----|---------------|---|
| Input leakage current | $ I_{UI} $ | — | — | 1 | μA | $V_{in} = V_{SS} \text{ to } V_{CC}$ |
| Output leakage current | $ I_{LO} $ | — | — | 1 | μA | CS1 = V_{IH} or CS2 = V_{IL} or OE = V_{IH} or WE = V_{IL} or LB = UB = V_{IH} , $V_{IO} = V_{SS} \text{ to } V_{CC}$ |
| Operating current | I_{CC} | — | — | 8 | mA | CS1 = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL} , $I_{IO} = 0 \text{ mA}$ |
| Average operating current | I_{CC1} | — | 20 | 30 | mA | Min. cycle, duty = 100%, $I_{IO} = 0 \text{ mA}$, CS1 = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL} |
| | I_{CC2} | — | 2 | 5 | mA | Cycle time = 1 μs , duty = 100%, $I_{IO} = 0 \text{ mA}$, CS1 $\leq 0.2 \text{ V}$, CS2 $\geq V_{CC} - 0.2 \text{ V}$, $V_{IH} \geq V_{CC} - 0.2 \text{ V}$, $V_{IL} \leq 0.2 \text{ V}$ |
| Standby current | I_{SB} | — | 0.1 | 0.5 | mA | CS2 = V_{IL} |
| Standby current | I_{SB1} * ² | — | 0.5 | 25 | μA | 0 V $\leq V_{in}$ (1) 0 V \leq CS2 $\leq 0.2 \text{ V}$ or (2) CS1 $\geq V_{CC} - 0.2 \text{ V}$, CS2 $\geq V_{CC} - 0.2 \text{ V}$ or (3) LB = UB $\geq V_{CC} - 0.2 \text{ V}$, CS2 $\geq V_{CC} - 0.2 \text{ V}$, CS1 $\leq 0.2 \text{ V}$ Average value |
| | I_{SB1} * ³ | — | 0.5 | 8 | μA | |
| Output high voltage | V_{OH} | $V_{CC} - 0.2$ | — | — | V | $I_{OH} = -100 \mu\text{A}$ |
| Output low voltage | V_{OL} | — | — | 0.2 | V | $I_{OL} = 100 \mu\text{A}$ |

Notes: 1. Typical values are at $V_{CC} = 1.8 \text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

2. This characteristic is guaranteed only for L-version.

3. This characteristic is guaranteed only for L-SL version.

Capacitance

($T_a = +25^\circ\text{C}$, $f = 1.0 \text{ MHz}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Test conditions | Note |
|--------------------------|----------|-----|-----|-----|------|------------------------|------|
| Input capacitance | C_{in} | — | — | 8 | pF | $V_{in} = 0 \text{ V}$ | 1 |
| Input/output capacitance | C_{IO} | — | — | 10 | pF | $V_{IO} = 0 \text{ V}$ | 1 |

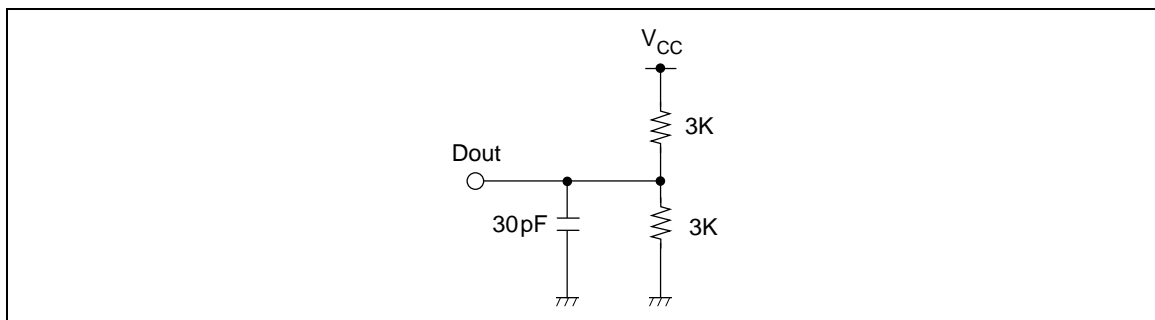
Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics

($T_a = -40$ to $+85^\circ\text{C}$, $V_{CC} = 1.65\text{ V}$ to 2.2 V , unless otherwise noted.)

Test Conditions

- Input pulse levels: $V_{IL} = 0.2\text{ V}$, $V_{IH} = V_{CC} - 0.2\text{ V}$
- Input rise and fall time: 3 ns
- Input and output timing reference levels: $0.5 \times V_{CC}$
- Output load: See figures (Including scope and jig)



HM62A16100I Series

Read Cycle

| HM62A16100I | | | | | |
|------------------------------------|------------|-----|-----|------|---------|
| -7 | | | | | |
| Parameter | Symbol | Min | Max | Unit | Notes |
| Read cycle time | t_{RC} | 70 | — | ns | |
| Address access time | t_{AA} | — | 70 | ns | |
| Chip select access time | t_{ACS1} | — | 70 | ns | |
| | t_{ACS2} | — | 70 | ns | |
| Output enable to output valid | t_{OE} | — | 35 | ns | |
| Output hold from address change | t_{OH} | 10 | — | ns | |
| LB, UB access time | t_{BA} | — | 70 | ns | |
| Chip select to output in low-Z | t_{CLZ1} | 10 | — | ns | 2, 3 |
| | t_{CLZ2} | 10 | — | ns | 2, 3 |
| LB, UB enable to low-Z | t_{BLZ} | 5 | — | ns | 2, 3 |
| Output enable to output in low-Z | t_{OLZ} | 5 | — | ns | 2, 3 |
| Chip deselect to output in high-Z | t_{CHZ1} | 0 | 25 | ns | 1, 2, 3 |
| | t_{CHZ2} | 0 | 25 | ns | 1, 2, 3 |
| LB, UB disable to high-Z | t_{BHZ} | 0 | 25 | ns | 1, 2, 3 |
| Output disable to output in high-Z | t_{OHZ} | 0 | 25 | ns | 1, 2, 3 |

Write Cycle

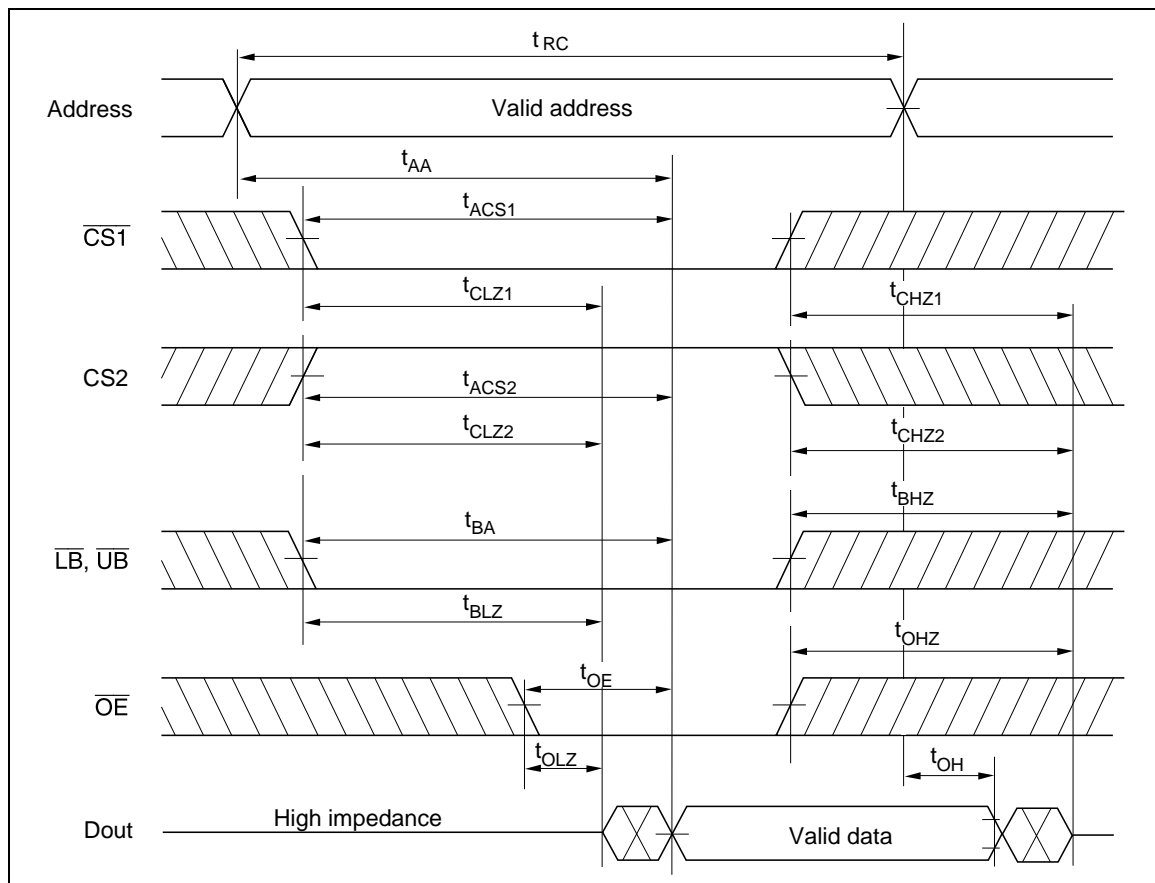
| HM62A16100I | | | | | |
|------------------------------------|-----------|-----|-----|------|-------|
| -7 | | | | | |
| Parameter | Symbol | Min | Max | Unit | Notes |
| Write cycle time | t_{WC} | 70 | — | ns | |
| Address valid to end of write | t_{AW} | 60 | — | ns | |
| Chip selection to end of write | t_{CW} | 60 | — | ns | 5 |
| Write pulse width | t_{WP} | 50 | — | ns | 4 |
| LB, UB valid to end of write | t_{BW} | 60 | — | ns | |
| Address setup time | t_{AS} | 0 | — | ns | 6 |
| Write recovery time | t_{WR} | 0 | — | ns | 7 |
| Data to write time overlap | t_{DW} | 30 | — | ns | |
| Data hold from write time | t_{DH} | 0 | — | ns | |
| Output active from end of write | t_{OW} | 5 | — | ns | 2 |
| Output disable to output in high-Z | t_{OHZ} | 0 | 25 | ns | 1, 2 |
| Write to output in high-Z | t_{WHZ} | 0 | 25 | ns | 1, 2 |

HM62A16100I Series

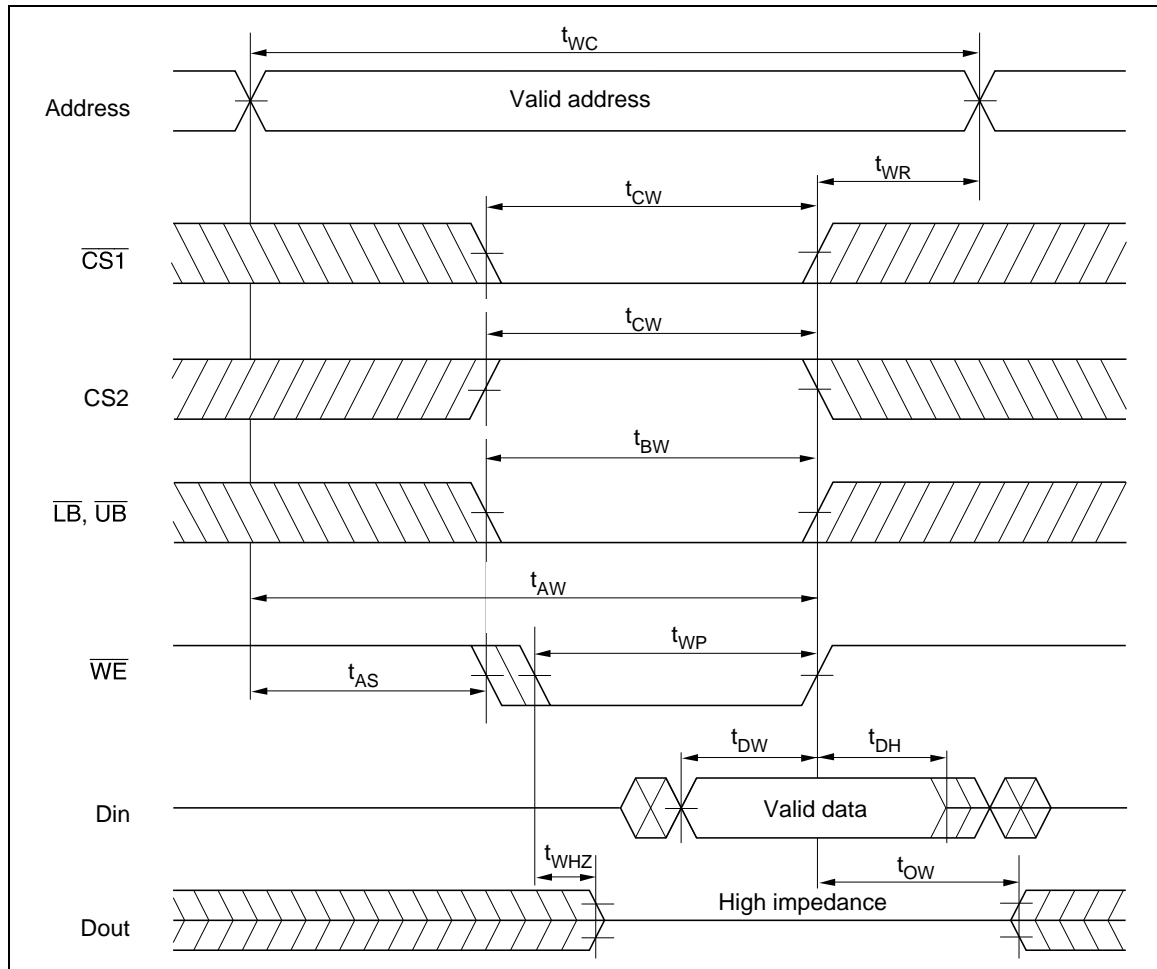
- Notes:
1. t_{CHZ} , t_{OHZ} , t_{WHZ} and t_{BHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
 2. This parameter is sampled and not 100% tested.
 3. At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.
 4. A write occurs during the overlap of a low CS1, a high CS2, a low WE and a low LB or a low UB. A write begins at the latest transition among CS1 going low, CS2 going high, WE going low and LB going low or UB going low. A write ends at the earliest transition among CS1 going high, CS2 going low, WE going high and LB going high or UB going high. t_{WP} is measured from the beginning of write to the end of write.
 5. t_{CW} is measured from the later of CS1 going low or CS2 going high to the end of write.
 6. t_{AS} is measured from the address valid to the beginning of write.
 7. t_{WR} is measured from the earliest of CS1 or WE going high or CS2 going low to the end of write cycle.

Timing Waveform

Read Cycle

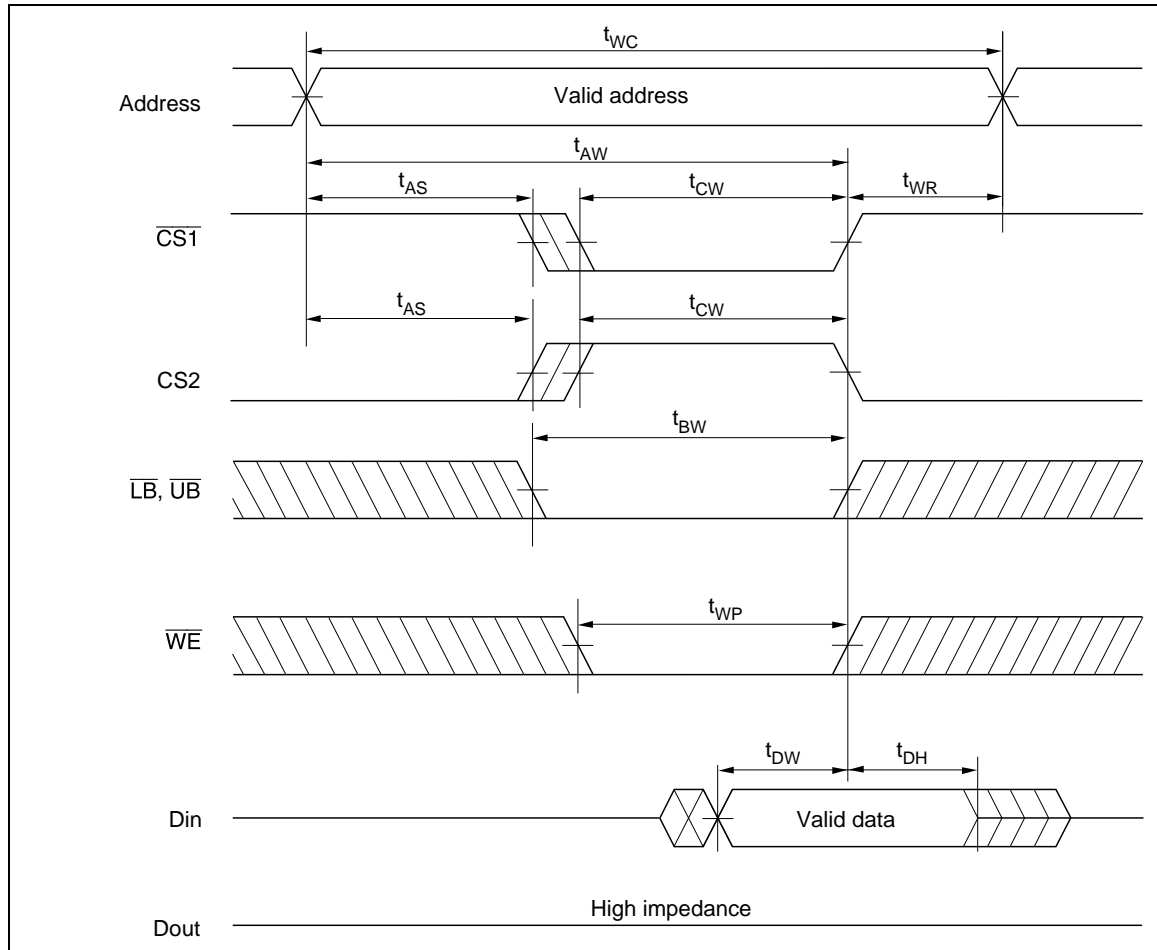


Write Cycle (1) (WE Clock)



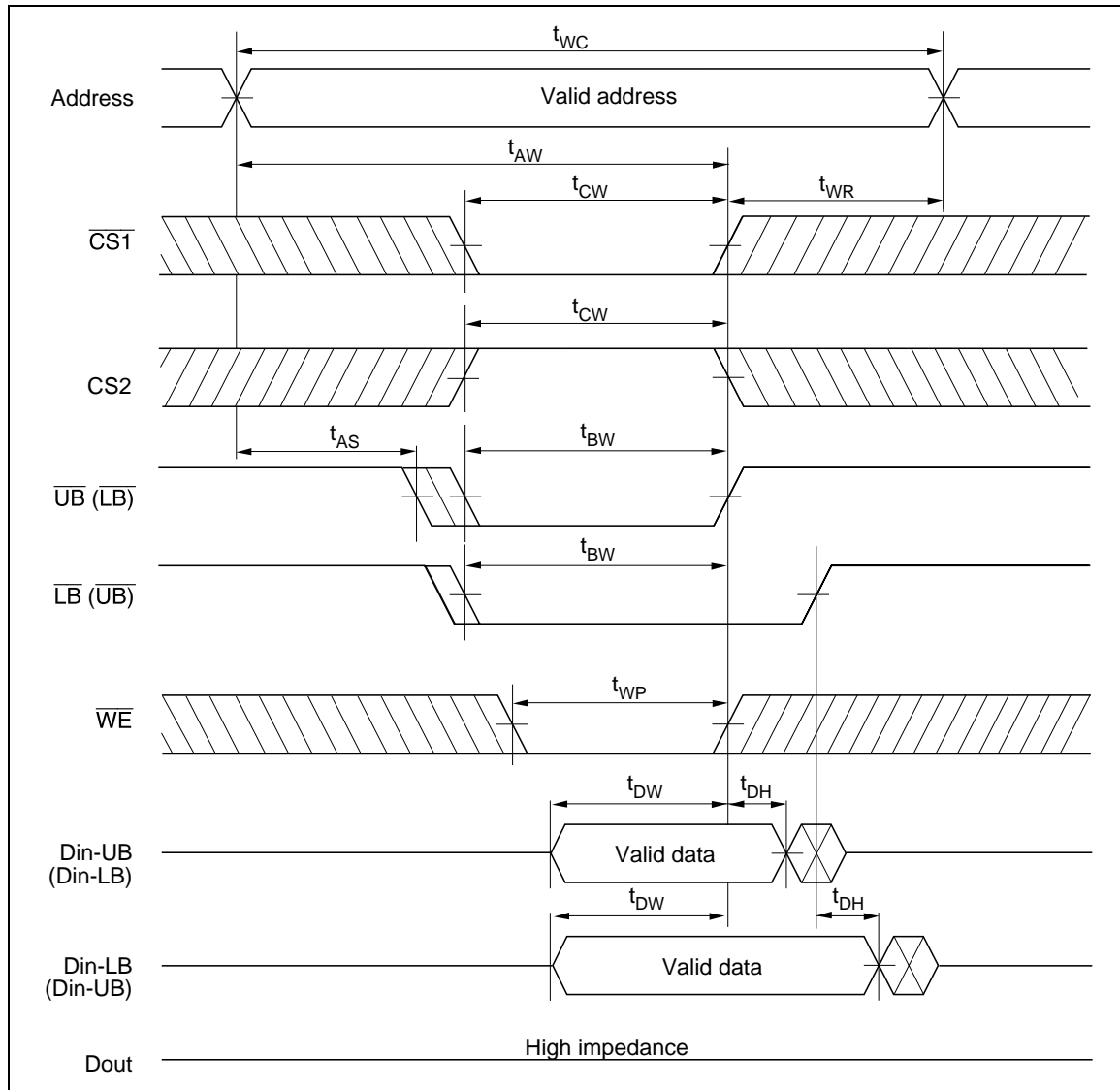
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Write Cycle (2) (CS1, CS2 Clock, OE = V_{IH})



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Write Cycle (3) (LB, UB Clock, OE = V_{IH})



Low V_{CC} Data Retention Characteristics

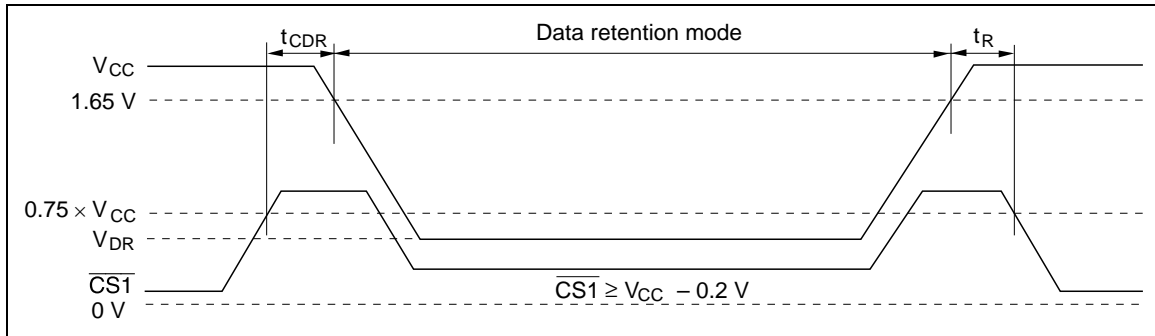
($T_a = -40$ to $+85^\circ\text{C}$)

| Parameter | Symbol | Min | Typ ^{*4} | Max | Unit | Test conditions ^{*3} |
|--------------------------------------|-----------------|-----|-------------------|-----|---------------|---|
| V_{CC} for data retention | V_{DR} | 1.0 | — | 2.2 | V | $V_{in} \geq 0$ V (1) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$ or (2) $CS2 \geq V_{CC} - 0.2\text{ V}$, $CS1 \geq V_{CC} - 0.2\text{ V}$ or (3) $LB = UB \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$, $CS1 \leq 0.2\text{ V}$ |
| Data retention current | I_{CCDR}^{*1} | — | 0.5 | 25 | μA | $V_{CC} = 1.5\text{ V}$, $V_{in} \geq 0\text{ V}$ (1) $0\text{ V} \leq CS2 \leq 0.2\text{ V}$ or (2) $CS2 \geq V_{CC} - 0.2\text{ V}$, $CS1 \geq V_{CC} - 0.2\text{ V}$ or (3) $LB = UB \geq V_{CC} - 0.2\text{ V}$, $CS2 \geq V_{CC} - 0.2\text{ V}$, $CS1 \leq 0.2\text{ V}$ Average value |
| | I_{CCDR}^{*2} | — | 0.5 | 8 | μA | |
| Chip deselect to data retention time | t_{CDR} | 0 | — | — | ns | See retention waveforms |
| Operation recovery time | t_R | 5 | — | — | ms | |

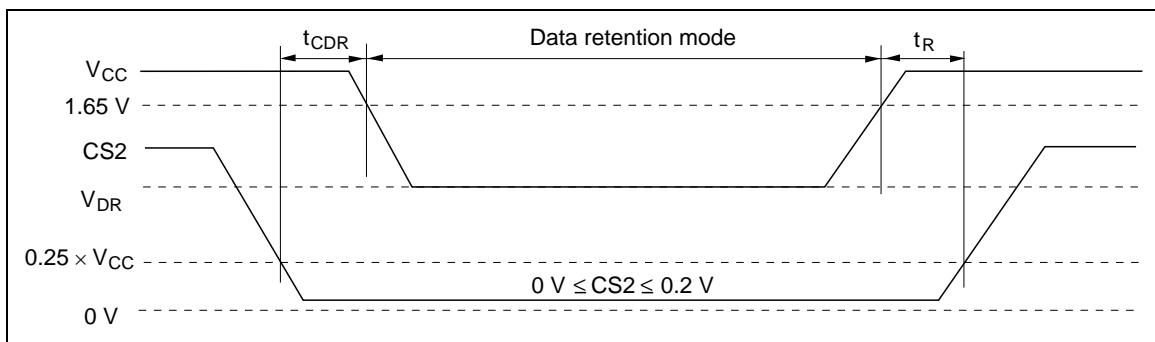
- Notes: 1. This characteristic is guaranteed only for L-version.
 2. This characteristic is guaranteed only for L-SL version.
 3. CS2 controls address buffer, WE buffer, CS1 buffer, OE buffer, LB, UB buffer and Din buffer. If CS2 controls data retention mode, V_{in} levels (address, WE, OE, CS1, LB, UB, I/O) can be in the high impedance state. If CS1 controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2\text{ V}$ or $0\text{ V} \leq CS2 \leq 0.2\text{ V}$. The other input levels (address, WE, OE, LB, UB, I/O) can be in the high impedance state.
 4. Typical values are at $V_{CC} = 1.5\text{ V}$, $T_a = +25^\circ\text{C}$ and not guaranteed.

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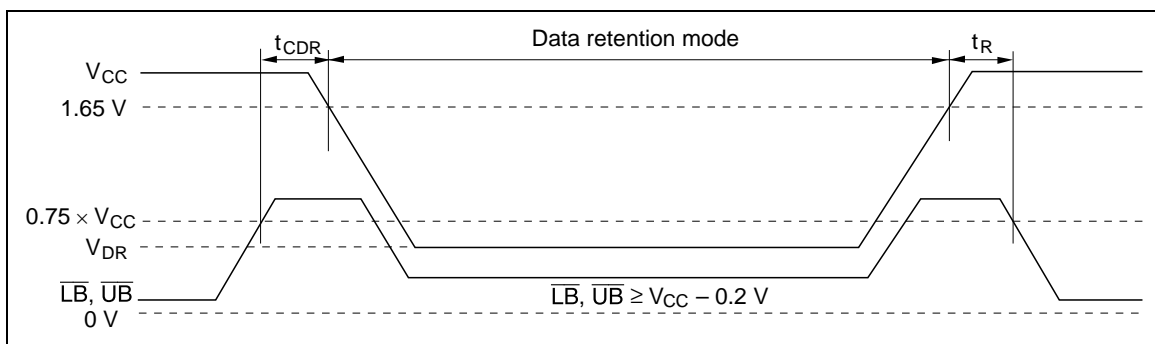
Low V_{CC} Data Retention Timing Waveform (1) (CS1 Controlled)



Low V_{CC} Data Retention Timing Waveform (2) (CS2 Controlled)



Low V_{CC} Data Retention Timing Waveform (3) (LB, UB Controlled)

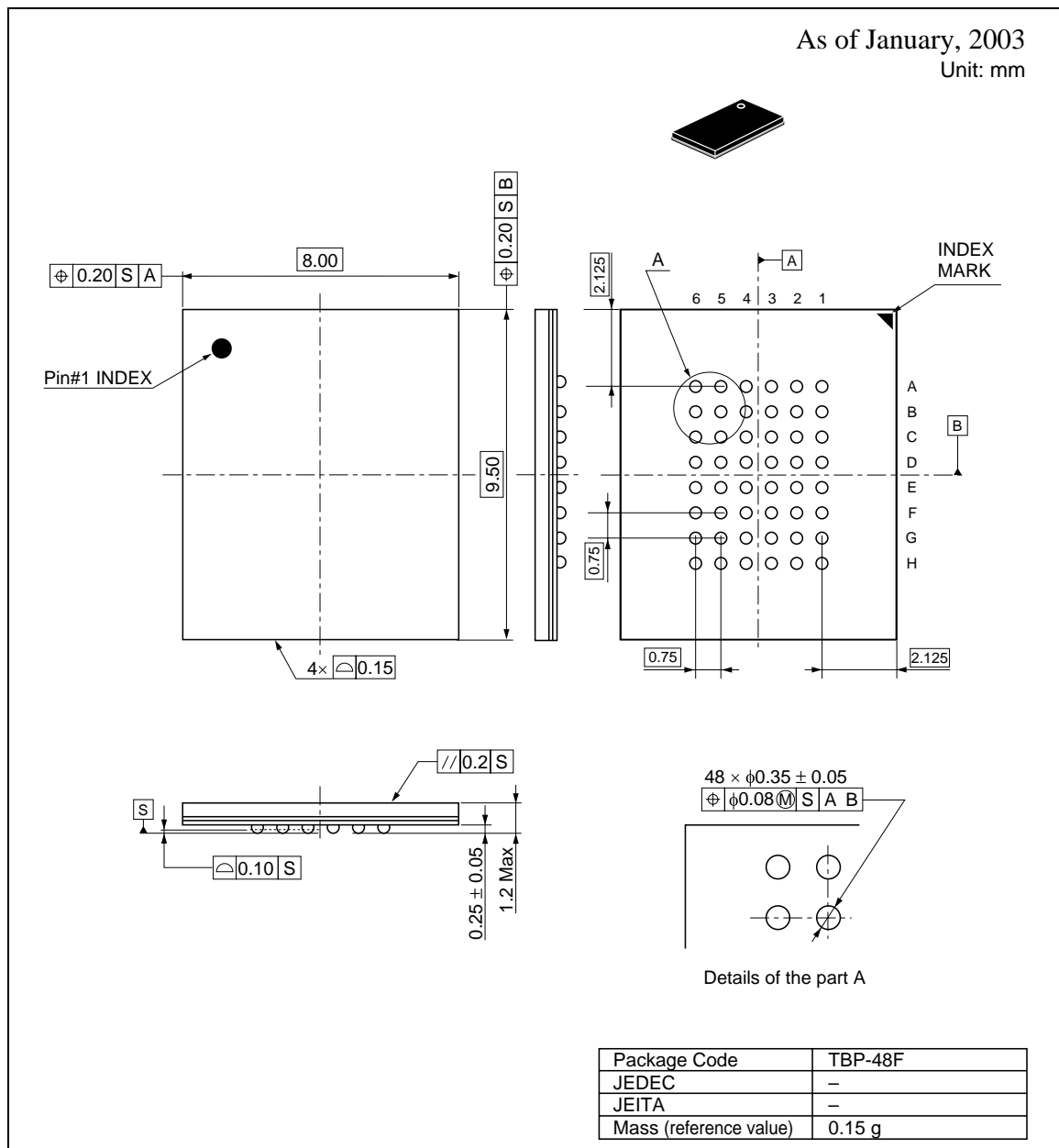


HM62A16100I Series

Package Dimensions

HM62A16100LBPI Series (TBP-48F)

As of January, 2003
Unit: mm



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