EM65570

68COM / 98SEG 65K Color STN LCD Driver

Product Specification

DOC. VERSION 1.0

ELAN MICROELECTRONICS CORP.

September 2005

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Specification Revision History

Doc. Version	Revision Description	Date
0.1	Initial version	2004/12/ 6
0.2	1. Modify Pad define: GND→VSS 2. Add VBA application circuit	2005/02/21
0.3	1. Remove all graphic function & graphic control registers descriptions. 2. Modify system block diagram on page 11. 3. Modify VBA and VREF pin descriptions on page 12. 4. Modify power circuit diagram on page 37~38. 5. Modify scroll function sample code on page 48~49. 6. Modify description and diagram about 'SWAP' on page 63~65. 7. Add scrolling mode diagram on page 84. 8. Modify VREF recommended value on page 85. 9. Remove CSL pin, VPP pin, VPP_EXT control bit and its descriptions. 10. Modify DV value table and add description of DV limitation on page 75. 11. Remove all external power mode descriptions, diagrams. 12. Modify Alignment Mark coordinate	2005/04/21
1.0	Add tray information	2005/09/05

1 General Description

EM65570 is one of the industry's most advanced wide-screen STN-LCD drivers for 65K-color display. It also has a built-in display RAM, a power supply circuit for LCD drive, an LCD controller circuit, and supports EEPROM function for programming information to tune the V_{LCD} offset voltage to get the best contrast which helps in compacting system design. EM65570 contributes to compact system design and with its partial display function, low power consumption is achieved.

Its "partial display"[1] function realizes results in low power consumption.

2 Feature

- 65K-color display
- LCD output**:** Segment 98RGB (294 outputs); Common 68 outputs
- Display RAM capacity**:** 98x68x16=106624 bits
- Built-in display RAM and power supply circuit
- Partial display functions
- Bus connection with 80-family/68-family MPU
- Logic power supply voltage range**:** 2.2 to 3.3 V
- Analog power supply voltage range**:** 2.4 to 3.3 V
- LCD driving voltage range**:** 4.5 to 16 V
- Booster**:** 2 to 6 times
- Fast burst-RAM write function
- Screen scroll function
- EEPROM function for setting the LCD operating voltage Vop
- Write system cycle: 200 ns
- Package**:**

Part Number	Package
EM65570AGH	Gold bumped chip

NOTE

The EM65570 series has the following sub-codes depending on their shapes.

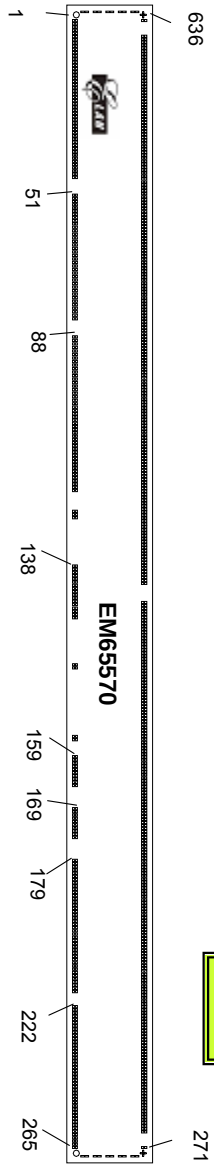
***H:** Bare chip (Aluminum pad with no bump);*
***GH:** Gold bumped chip; **F:** COF package; **T:** TAB (TCP) package*
*Example: **EM65570AGH → EM65570:** Elan product number*
***A:** Package Version*
***GH:** Gold bump chip*

[1] A function that utilizes only part of the screen, thus reducing power consumption.

3 Applications

- Mobile phone
- Small PDA

4 Pin Configurations



NOTE
The Elan logo at the left end (as shown in the figure) and Pin 1 is at the bottom-left corner.

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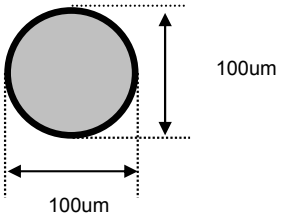
Figure 4-1 Pin Configuration

4.1 Alignment Key

Mark	Coordinates (X,Y)	Mark	Coordinates (X,Y)
U-Left	-8899,534	U-Right	8899,534
D-Left	-8898.95,-534.05	D-Right	8898.95,-534.05

Coordinates Origin**:** Chip center

D-Left and D-Right:



U-Left and U-Right:

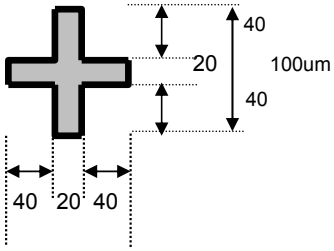


Figure. 4-2 Pin Alignment Key

4.2 Pin Dimensions

Item	Pad No.	Size		Unit
		X	Y	
Chip size	-	18100	1370	μm
Bump Size	1 ~ 265	35	76	
	266 ~ 270, 637 ~ 641	22	127	
	271 ~ 636	31.5	84	
Pad Pitch	1 ~ 265	50		
	266 ~ 270, 637 ~ 641	55		
	271 ~ 636	46.5		
	Min pitch	46.5		
Die thickness (excluding bumps)	20 ± 1 mil (500 ± 25 um)			
Bump Height	17 ± 3 μm			
Minimum Bump Gap	15			
Coordinate Origin	Chip center			

4.3 Recommended Cog Ito Traces Resistor

Interface	ITO Traces Resistances
V0~V4 CAP1+,CAP1-,CAP2+,CAP2-,CAP3+, CAP4+,CAP5+,Vout VDD,VEE VSS	Max=50Ω
WRB,RDB,CSB,…,D0~D7	Max=3KΩ
RESB	Max=5~10KΩ

4.4 PAD Coordinates Table

Pin No.	Pad Name	Coordinates (X, Y)	Pin No.	Pad Name	Coordinates (X, Y)
1	NC1	-8807.65, -554.0	51	WRB	-6079.75, -554.0
2	VSS	-8757.65, -554.0	52	WRB	-6029.75, -554.0
3	VSS	-8707.65, -554.0	53	WRB	-5979.75, -554.0
4	VSS	-8657.65, -554.0	54	RDB	-5929.75, -554.0
5	VSS	-8607.65, -554.0	55	RDB	-5879.75, -554.0
6	VSS	-8557.65, -554.0	56	RDB	-5829.75, -554.0
7	VSS	-8507.65, -554.0	57	VDD	-5779.75, -554.0
8	VSS	-8457.65, -554.0	58	VDD	-5729.75, -554.0
9	VSS	-8407.65, -554.0	59	VDD	-5679.75, -554.0
10	VSS	-8357.65, -554.0	60	VDD	-5629.75, -554.0
11	VSS	-8307.65, -554.0	61	D0	-5577.25, -554.0
12	VSS	-8257.65, -554.0	62	D0	-5522.25, -554.0
13	VSS	-8207.65, -554.0	63	D0	-5467.25, -554.0
14	VSS	-8157.65, -554.0	64	D1	-5412.25, -554.0
15	VSS	-8107.65, -554.0	65	D1	-5357.25, -554.0
16	VSS	-8057.65, -554.0	66	D1	-5302.25, -554.0
17	VSS	-8007.65, -554.0	67	D2	-5247.25, -554.0
18	TEST	-7957.65, -554.0	68	D2	-5192.25, -554.0
19	TEST	-7907.65, -554.0	69	D2	-5137.25, -554.0
20	TEST	-7857.65, -554.0	70	D3	-5082.25, -554.0
21	PS	-7807.65, -554.0	71	D3	-5027.25, -554.0
22	PS	-7757.65, -554.0	72	D3	-4972.25, -554.0
23	PS	-7707.65, -554.0	73	D4	-4917.25, -554.0
24	M86	-7657.65, -554.0	74	D4	-4862.25, -554.0
25	M86	-7607.65, -554.0	75	D4	-4807.25, -554.0
26	M86	-7557.65, -554.0	76	D5	-4752.25, -554.0
27	CSB	-7507.65, -554.0	77	D5	-4697.25, -554.0
28	CSB	-7457.65, -554.0	78	D5	-4642.25, -554.0
29	CSB	-7407.65, -554.0	79	D6	-4587.25, -554.0
30	VSS	-7357.65, -554.0	80	D6	-4532.25, -554.0
31	VSS	-7307.65, -554.0	81	D6	-4477.25, -554.0
32	VSS	-7257.65, -554.0	82	D7	-4422.25, -554.0
33	VSS	-7207.65, -554.0	83	D7	-4367.25, -554.0
34	VDD	-7157.65, -554.0	84	D7	-4312.25, -554.0
35	VDD	-7107.65, -554.0	85	D8	-4257.25, -554.0
36	VDD	-7057.65, -554.0	86	D8	-4202.25, -554.0
37	VDD	-7007.65, -554.0	87	D8	-4147.25, -554.0
38	RESB	-6957.65, -554.0	88	D9	-3864.35, -554.0
39	RESB	-6907.65, -554.0	89	D9	-3809.35, -554.0
40	RESB	-6857.65, -554.0	90	D9	-3754.35, -554.0
41	RS	-6807.65, -554.0	91	D10	-3699.35, -554.0
42	RS	-6757.65, -554.0	92	D10	-3644.35, -554.0
43	RS	-6707.65, -554.0	93	D10	-3589.35, -554.0
44	CK	-6657.65, -554.0	94	D11	-3534.35, -554.0
45	CK	-6607.65, -554.0	95	D11	-3479.35, -554.0
46	CK	-6557.65, -554.0	96	D11	-3424.35, -554.0
47	VSS	-6507.65, -554.0	97	D12	-3369.35, -554.0
48	VSS	-6457.65, -554.0	98	D12	-3314.35, -554.0
49	VSS	-6407.65, -554.0	99	D12	-3259.35, -554.0
50	VSS	-6357.65, -554.0	100	D13	-3204.35, -554.0

Pin No.	Pad Name	Coordinates (X, Y)	Pin No.	Pad Name	Coordinates (X, Y)
101	D13	-3149.35, -554.0	151	CAP5P	377.7, -554.0
102	D13	-3094.35, -554.0	152	CAP5P	427.7, -554.0
103	D14	-3039.35, -554.0	153	CAP5P	477.7, -554.0
104	D14	-2984.35, -554.0	154	CAP5P	527.7, -554.0
105	D14	-2929.35, -554.0	155	CAP3P	1261.65, -554.0
106	D15	-2874.35, -554.0	156	CAP3P	1311.65, -554.0
107	D15	-2819.35, -554.0	157	CAP1P	2384.35, -554.0
108	D15	-2764.35, -554.0	158	CAP1P	2434.35, -554.0
109	VSS	-2711.85, -554.0	159	CAP1N	2698.15, -554.0
110	VSS	-2661.85, -554.0	160	CAP1N	2748.15, -554.0
111	VSS	-2611.85, -554.0	161	CAP1N	2798.15, -554.0
112	VSS	-2561.85, -554.0	162	CAP1N	2848.15, -554.0
113	TEST1	-2511.85, -554.0	163	CAP1N	2898.15, -554.0
114	TEST1	-2461.85, -554.0	164	CAP1N	2948.15, -554.0
115	TEST1	-2411.85, -554.0	165	CAP1N	2998.15, -554.0
116	CKS	-2361.85, -554.0	166	CAP1N	3048.15, -554.0
117	CKS	-2311.85, -554.0	167	CAP1N	3098.15, -554.0
118	CKS	-2261.85, -554.0	168	CAP1N	3148.15, -554.0
119	VDD	-2211.85, -554.0	169	VEE	3511.15, -554.0
120	VDD	-2161.85, -554.0	170	VEE	3561.15, -554.0
121	VDD	-2111.85, -554.0	171	VEE	3611.15, -554.0
122	VDD	-2061.85, -554.0	172	VEE	3661.15, -554.0
123	VDD	-2011.85, -554.0	173	VEE	3711.15, -554.0
124	VDD	-1961.85, -554.0	174	VEE	3761.15, -554.0
125	VDD	-1911.85, -554.0	175	VEE	3811.15, -554.0
126	VDD	-1861.85, -554.0	176	VEE	3861.15, -554.0
127	VDD	-1811.85, -554.0	177	VEE	3911.15, -554.0
128	VDD	-1761.85, -554.0	178	VEE	3961.15, -554.0
129	VDD	-1711.85, -554.0	179	CAP2N	4320.7, -554.0
130	VDD	-1661.85, -554.0	180	CAP2N	4370.7, -554.0
131	VDD	-1611.85, -554.0	181	CAP2N	4420.7, -554.0
132	VDD	-1561.85, -554.0	182	CAP2N	4470.7, -554.0
133	VDD	-1511.85, -554.0	183	CAP2N	4520.7, -554.0
134	VDD	-1461.85, -554.0	184	CAP2N	4570.7, -554.0
135	NC2	-1137.05, -554.0	185	CAP2N	4620.7, -554.0
136	NC3	-1087.05, -554.0	186	CAP2N	4670.7, -554.0
137	NC4	-1037.05, -554.0	187	CAP2P	4720.7, -554.0
138	VBA	-281.0, -554.0	188	CAP2P	4770.7, -554.0
139	VREF	-231.0, -554.0	189	CAP2P	4820.7, -554.0
140	VOUT	-181.0, -554.0	190	CAP2P	4870.7, -554.0
141	VOUT	-131.0, -554.0	191	CAP2P	4920.7, -554.0
142	VOUT	-81.0, -554.0	192	CAP2P	4970.7, -554.0
143	VOUT	-31.0, -554.0	193	CAP2P	5020.7, -554.0
144	VOUT	19.0, -554.0	194	CAP2P	5070.7, -554.0
145	VOUT	69.0, -554.0	195	CAP2P	5120.7, -554.0
146	VOUT	119.0, -554.0	196	CAP2P	5170.7, -554.0
147	VOUT	169.0, -554.0	197	CAP2P	5220.7, -554.0
148	VOUT	219.0, -554.0	198	CAP2P	5270.7, -554.0
149	VOUT	269.0, -554.0	199	CAP4P	5320.7, -554.0
150	VOUT	319.0, -554.0	200	CAP4P	5370.7, -554.0

Pin No.	Pad Name	Coordinates (X, Y)	Pin No.	Pad Name	Coordinates (X, Y)
201	CAP4P	5420.7, -554.0	251	V1	8107.6, -554.0
202	CAP4P	5470.7, -554.0	252	V1	8157.6, -554.0
203	CAP4P	5520.7, -554.0	253	V1	8207.6, -554.0
204	CAP4P	5570.7, -554.0	254	V1	8257.6, -554.0
205	CAP4P	5620.7, -554.0	255	V1	8307.6, -554.0
206	CAP4P	5670.7, -554.0	256	V0	8357.6, -554.0
207	CAP4P	5720.7, -554.0	257	V0	8407.6, -554.0
208	CAP4P	5770.7, -554.0	258	V0	8457.6, -554.0
209	CAP4P	5820.7, -554.0	259	V0	8507.6, -554.0
210	CAP4P	5870.7, -554.0	260	V0	8557.6, -554.0
211	VSS	5920.7, -554.0	261	V0	8607.6, -554.0
212	VSS	5970.7, -554.0	262	V0	8657.6, -554.0
213	VSS	6020.7, -554.0	263	V0	8707.6, -554.0
214	VSS	6070.7, -554.0	264	V0	8757.6, -554.0
215	VSS	6120.7, -554.0	265	NC5	8807.6, -554.0
216	VSS	6170.7, -554.0	266	NC6	8945.0, -400.5
217	VSS	6220.7, -554.0	267	NC7	8945.0, -200.25
218	VSS	6270.7, -554.0	268	NC8	8945.0, 0.0
219	VSS	6320.7, -554.0	269	NC9	8945.0, 200.25
220	VSS	6370.7, -554.0	270	NC10	8945.0, 400.5
221	VSS	6607.6, -554.0	271	NC11	8809.4, 550.0
222	VSS	6657.6, -554.0	272	COM66	8564.75, 550.0
223	VSS	6707.6, -554.0	273	COM64	8518.25, 550.0
224	VSS	6757.6, -554.0	274	COM62	8471.75, 550.0
225	VSS	6807.6, -554.0	275	COM60	8425.25, 550.0
226	V4	6857.6, -554.0	276	COM58	8378.75, 550.0
227	V4	6907.6, -554.0	277	COM56	8332.25, 550.0
228	V4	6957.6, -554.0	278	COM54	8285.75, 550.0
229	V4	7007.6, -554.0	279	COM52	8239.25, 550.0
230	V4	7057.6, -554.0	280	COM50	8192.75, 550.0
231	V4	7107.6, -554.0	281	COM48	8146.25, 550.0
232	V4	7157.6, -554.0	282	COM46	8099.75, 550.0
233	V4	7207.6, -554.0	283	COM44	8053.25, 550.0
234	V3	7257.6, -554.0	284	COM42	8006.75, 550.0
235	V3	7307.6, -554.0	285	COM40	7960.25, 550.0
236	V3	7357.6, -554.0	286	COM38	7913.75, 550.0
237	V3	7407.6, -554.0	287	COM36	7867.25, 550.0
238	V3	7457.6, -554.0	288	COM34	7820.75, 550.0
239	V3	7507.6, -554.0	289	COM32	7774.25, 550.0
240	V3	7557.6, -554.0	290	COM30	7727.75, 550.0
241	V2	7607.6, -554.0	291	COM28	7681.25, 550.0
242	V2	7657.6, -554.0	292	COM26	7634.75, 550.0
243	V2	7707.6, -554.0	293	COM24	7588.25, 550.0
244	V2	7757.6, -554.0	294	COM22	7541.75, 550.0
245	V2	7807.6, -554.0	295	COM20	7495.25, 550.0
246	V2	7857.6, -554.0	296	COM18	7448.75, 550.0
247	V2	7907.6, -554.0	297	COM16	7402.25, 550.0
248	V1	7957.6, -554.0	298	COM14	7355.75, 550.0
249	V1	8007.6, -554.0	299	COM12	7309.25, 550.0
250	V1	8057.6, -554.0	300	COM10	7262.75, 550.0

Pin No.	Pad Name	Coordinates (X, Y)	Pin No.	Pad Name	Coordinates (X, Y)
301	COM8	7216.25, 550.0	351	SEGC14	4891.25, 550.0
302	COM6	7169.75, 550.0	352	SEGA15	4844.75, 550.0
303	COM4	7123.25, 550.0	353	SEGB15	4798.25, 550.0
304	COM2	7076.75, 550.0	354	SEGC15	4751.75, 550.0
305	COM0	7030.25, 550.0	355	SEGA16	4705.25, 550.0
306	NC12	6983.75, 550.0	356	SEGB16	4658.75, 550.0
307	SEGA0	6937.25, 550.0	357	SEGC16	4612.25, 550.0
308	SEGB0	6890.75, 550.0	358	SEGA17	4565.75, 550.0
309	SEGC0	6844.25, 550.0	359	SEGB17	4519.25, 550.0
310	SEGA1	6797.75, 550.0	360	SEGC17	4472.75, 550.0
311	SEGB1	6751.25, 550.0	361	SEGA18	4426.25, 550.0
312	SEGC1	6704.75, 550.0	362	SEGB18	4379.75, 550.0
313	SEGA2	6658.25, 550.0	363	SEGC18	4333.25, 550.0
314	SEGB2	6611.75, 550.0	364	SEGA19	4286.75, 550.0
315	SEGC2	6565.25, 550.0	365	SEGB19	4240.25, 550.0
316	SEGA3	6518.75, 550.0	366	SEGC19	4193.75, 550.0
317	SEGB3	6472.25, 550.0	367	SEGA20	4147.25, 550.0
318	SEGC3	6425.75, 550.0	368	SEGB20	4100.75, 550.0
319	SEGA4	6379.25, 550.0	369	SEGC20	4054.25, 550.0
320	SEGB4	6332.75, 550.0	370	SEGA21	4007.75, 550.0
321	SEGC4	6286.25, 550.0	371	SEGB21	3961.25, 550.0
322	SEGA5	6239.75, 550.0	372	SEGC21	3914.75, 550.0
323	SEGB5	6193.25, 550.0	373	SEGA22	3868.25, 550.0
324	SEGC5	6146.75, 550.0	374	SEGB22	3821.75, 550.0
325	SEGA6	6100.25, 550.0	375	SEGC22	3775.25, 550.0
326	SEGB6	6053.75, 550.0	376	SEGA23	3728.75, 550.0
327	SEGC6	6007.25, 550.0	377	SEGB23	3682.25, 550.0
328	SEGA7	5960.75, 550.0	378	SEGC23	3635.75, 550.0
329	SEGB7	5914.25, 550.0	379	SEGA24	3589.25, 550.0
330	SEGC7	5867.75, 550.0	380	SEGB24	3542.75, 550.0
331	SEGA8	5821.25, 550.0	381	SEGC24	3496.25, 550.0
332	SEGB8	5774.75, 550.0	382	SEGA25	3449.75, 550.0
333	SEGC8	5728.25, 550.0	383	SEGB25	3403.25, 550.0
334	SEGA9	5681.75, 550.0	384	SEGC25	3356.75, 550.0
335	SEGB9	5635.25, 550.0	385	SEGA26	3310.25, 550.0
336	SEGC9	5588.75, 550.0	386	SEGB26	3263.75, 550.0
337	SEGA10	5542.25, 550.0	387	SEGC26	3217.25, 550.0
338	SEGB10	5495.75, 550.0	388	SEGA27	3170.75, 550.0
339	SEGC10	5449.25, 550.0	389	SEGB27	3124.25, 550.0
340	SEGA11	5402.75, 550.0	390	SEGC27	3077.75, 550.0
341	SEGB11	5356.25, 550.0	391	SEGA28	3031.25, 550.0
342	SEGC11	5309.75, 550.0	392	SEGB28	2984.75, 550.0
343	SEGA12	5263.25, 550.0	393	SEGC28	2938.25, 550.0
344	SEGB12	5216.75, 550.0	394	SEGA29	2891.75, 550.0
345	SEGC12	5170.25, 550.0	395	SEGB29	2845.25, 550.0
346	SEGA13	5123.75, 550.0	396	SEGC29	2798.75, 550.0
347	SEGB13	5077.25, 550.0	397	SEGA30	2752.25, 550.0
348	SEGC13	5030.75, 550.0	398	SEGB30	2705.75, 550.0
349	SEGA14	4984.25, 550.0	399	SEGC30	2659.25, 550.0
350	SEGB14	4937.75, 550.0	400	SEGA31	2612.75, 550.0

Pin No.	Pad Name	Coordinates (X, Y)	Pin NO	Pad Name	Coordinates (X, Y)
401	SEGB31	2566.25, 550.0	451	SEGA48	-8.75, 550.0
402	SEGC31	2519.75, 550.0	452	SEGB48	-55.25, 550.0
403	SEGA32	2473.25, 550.0	453	SEGC48	-101.75, 550.0
404	SEGB32	2426.75, 550.0	454	SEGA49	-148.25, 550.0
405	SEGC32	2380.25, 550.0	455	SEGB49	-194.75, 550.0
406	SEGA33	2333.75, 550.0	456	SEGC49	-241.25, 550.0
407	SEGB33	2287.25, 550.0	457	SEGA50	-287.75, 550.0
408	SEGC33	2240.75, 550.0	458	SEGB50	-334.25, 550.0
409	SEGA34	2194.25, 550.0	459	SEGC50	-380.75, 550.0
410	SEGB34	2147.75, 550.0	460	SEGA51	-427.25, 550.0
411	SEGC34	2101.25, 550.0	461	SEGB51	-473.75, 550.0
412	SEGA35	2054.75, 550.0	462	SEGC51	-520.25, 550.0
413	SEGB35	2008.25, 550.0	463	SEGA52	-566.75, 550.0
414	SEGC35	1961.75, 550.0	464	SEGB52	-613.25, 550.0
415	SEGA36	1915.25, 550.0	465	SEGC52	-659.75, 550.0
416	SEGB36	1868.75, 550.0	466	SEGA53	-706.25, 550.0
417	SEGC36	1822.25, 550.0	467	SEGB53	-752.75, 550.0
418	SEGA37	1775.75, 550.0	468	SEGC53	-799.25, 550.0
419	SEGB37	1729.25, 550.0	469	SEGA54	-845.75, 550.0
420	SEGC37	1682.75, 550.0	470	SEGB54	-892.25, 550.0
421	SEGA38	1636.25, 550.0	471	SEGC54	-938.75, 550.0
422	SEGB38	1589.75, 550.0	472	SEGA55	-985.25, 550.0
423	SEGC38	1543.25, 550.0	473	SEGB55	-1031.75, 550.0
424	SEGA39	1496.75, 550.0	474	SEGC55	-1078.25, 550.0
425	SEGB39	1450.25, 550.0	475	SEGA56	-1124.75, 550.0
426	SEGC39	1403.75, 550.0	476	SEGB56	-1171.25, 550.0
427	SEGA40	1357.25, 550.0	477	SEGC56	-1217.75, 550.0
428	SEGB40	1310.75, 550.0	478	SEGA57	-1264.25, 550.0
429	SEGC40	1264.25, 550.0	479	SEGB57	-1310.75, 550.0
430	SEGA41	1217.75, 550.0	480	SEGC57	-1357.25, 550.0
431	SEGB41	1171.25, 550.0	481	SEGA58	-1403.75, 550.0
432	SEGC41	1124.75, 550.0	482	SEGB58	-1450.25, 550.0
433	SEGA42	1078.25, 550.0	483	SEGC58	-1496.75, 550.0
434	SEGB42	1031.75, 550.0	484	SEGA59	-1543.25, 550.0
435	SEGC42	985.25, 550.0	485	SEGB59	-1589.75, 550.0
436	SEGA43	938.75, 550.0	486	SEGC59	-1636.25, 550.0
437	SEGB43	892.25, 550.0	487	SEGA60	-1682.75, 550.0
438	SEGC43	845.75, 550.0	488	SEGB60	-1729.25, 550.0
439	SEGA44	799.25, 550.0	489	SEGC60	-1775.75, 550.0
440	SEGB44	752.75, 550.0	490	SEGA61	-1822.25, 550.0
441	SEGC44	706.25, 550.0	491	SEGB61	-1868.75, 550.0
442	SEGA45	659.75, 550.0	492	SEGC61	-1915.25, 550.0
443	SEGB45	613.25, 550.0	493	SEGA62	-1961.75, 550.0
444	SEGC45	566.75, 550.0	494	SEGB62	-2008.25, 550.0
445	SEGA46	520.25, 550.0	495	SEGC62	-2054.75, 550.0
446	SEGB46	473.75, 550.0	496	SEGA63	-2101.25, 550.0
447	SEGC46	427.25, 550.0	497	SEGB63	-2147.75, 550.0
448	SEGA47	380.75, 550.0	498	SEGC63	-2194.25, 550.0
449	SEGB47	334.25, 550.0	499	SEGA64	-2240.75, 550.0
450	SEGC47	287.75, 550.0	500	SEGB64	-2287.25, 550.0

Pin No.	Pad Name	Coordinates (X, Y)	Pin No.	Pad Name	Coordinates (X, Y)
501	SEGC64	-2333.75, 550.0	551	SEGB81	-4658.75, 550.0
502	SEGA65	-2380.25, 550.0	552	SEGC81	-4705.25, 550.0
503	SEGB65	-2426.75, 550.0	553	SEGA82	-4751.75, 550.0
504	SEGC65	-2473.25, 550.0	554	SEGB82	-4798.25, 550.0
505	SEGA66	-2519.75, 550.0	555	SEGC82	-4844.75, 550.0
506	SEGB66	-2566.25, 550.0	556	SEGA83	-4891.25, 550.0
507	SEGC66	-2612.75, 550.0	557	SEGB83	-4937.75, 550.0
508	SEGA67	-2659.25, 550.0	558	SEGC83	-4984.25, 550.0
509	SEGB67	-2705.75, 550.0	559	SEGA84	-5030.75, 550.0
510	SEGC67	-2752.25, 550.0	560	SEGB84	-5077.25, 550.0
511	SEGA68	-2798.75, 550.0	561	SEGC84	-5123.75, 550.0
512	SEGB68	-2845.25, 550.0	562	SEGA85	-5170.25, 550.0
513	SEGC68	-2891.75, 550.0	563	SEGB85	-5216.75, 550.0
514	SEGA69	-2938.25, 550.0	564	SEGC85	-5263.25, 550.0
515	SEGB69	-2984.75, 550.0	565	SEGA86	-5309.75, 550.0
516	SEGC69	-3031.25, 550.0	566	SEGB86	-5356.25, 550.0
517	SEGA70	-3077.75, 550.0	567	SEGC86	-5402.75, 550.0
518	SEGB70	-3124.25, 550.0	568	SEGA87	-5449.25, 550.0
519	SEGC70	-3170.75, 550.0	569	SEGB87	-5495.75, 550.0
520	SEGA71	-3217.25, 550.0	570	SEGC87	-5542.25, 550.0
521	SEGB71	-3263.75, 550.0	571	SEGA88	-5588.75, 550.0
522	SEGC71	-3310.25, 550.0	572	SEGB88	-5635.25, 550.0
523	SEGA72	-3356.75, 550.0	573	SEGC88	-5681.75, 550.0
524	SEGB72	-3403.25, 550.0	574	SEGA89	-5728.25, 550.0
525	SEGC72	-3449.75, 550.0	575	SEGB89	-5774.75, 550.0
526	SEGA73	-3496.25, 550.0	576	SEGC89	-5821.25, 550.0
527	SEGB73	-3542.75, 550.0	577	SEGA90	-5867.75, 550.0
528	SEGC73	-3589.25, 550.0	578	SEGB90	-5914.25, 550.0
529	SEGA74	-3635.75, 550.0	579	SEGC90	-5960.75, 550.0
530	SEGB74	-3682.25, 550.0	580	SEGA91	-6007.25, 550.0
531	SEGC74	-3728.75, 550.0	581	SEGB91	-6053.75, 550.0
532	SEGA75	-3775.25, 550.0	582	SEGC91	-6100.25, 550.0
533	SEGB75	-3821.75, 550.0	583	SEGA92	-6146.75, 550.0
534	SEGC75	-3868.25, 550.0	584	SEGB92	-6193.25, 550.0
535	SEGA76	-3914.75, 550.0	585	SEGC92	-6239.75, 550.0
536	SEGB76	-3961.25, 550.0	586	SEGA93	-6286.25, 550.0
537	SEGC76	-4007.75, 550.0	587	SEGB93	-6332.75, 550.0
538	SEGA77	-4054.25, 550.0	588	SEGC93	-6379.25, 550.0
539	SEGB77	-4100.75, 550.0	589	SEGA94	-6425.75, 550.0
540	SEGC77	-4147.25, 550.0	590	SEGB94	-6472.25, 550.0
541	SEGA78	-4193.75, 550.0	591	SEGC94	-6518.75, 550.0
542	SEGB78	-4240.25, 550.0	592	SEGA95	-6565.25, 550.0
543	SEGC78	-4286.75, 550.0	593	SEGB95	-6611.75, 550.0
544	SEGA79	-4333.25, 550.0	594	SEGC95	-6658.25, 550.0
545	SEGB79	-4379.75, 550.0	595	SEGA96	-6704.75, 550.0
546	SEGC79	-4426.25, 550.0	596	SEGB96	-6751.25, 550.0
547	SEGA80	-4472.75, 550.0	597	SEGC96	-6797.75, 550.0
548	SEGB80	-4519.25, 550.0	598	SEGA97	-6844.25, 550.0
549	SEGC80	-4565.75, 550.0	599	SEGB97	-6890.75, 550.0
550	SEGA81	-4612.25, 550.0	600	SEGC97	-6937.25, 550.0

Pin No.	Pad Name	Coordinates (X, Y)
601	NC13	-6983.75, 550.0
602	COM1	-7030.25, 550.0
603	COM3	-7076.75, 550.0
604	COM5	-7123.25, 550.0
605	COM7	-7169.75, 550.0
606	COM9	-7216.25, 550.0
607	COM11	-7262.75, 550.0
608	COM13	-7309.25, 550.0
609	COM15	-7355.75, 550.0
610	COM17	-7402.25, 550.0
611	COM19	-7448.75, 550.0
612	COM21	-7495.25, 550.0
613	COM23	-7541.75, 550.0
614	COM25	-7588.25, 550.0
615	COM27	-7634.75, 550.0
616	COM29	-7681.25, 550.0
617	COM31	-7727.75, 550.0
618	COM33	-7774.25, 550.0
619	COM35	-7820.75, 550.0
620	COM37	-7867.25, 550.0
621	COM39	-7913.75, 550.0
622	COM41	-7960.25, 550.0
623	COM43	-8006.75, 550.0
624	COM45	-8053.25, 550.0
625	COM47	-8099.75, 550.0
626	COM49	-8146.25, 550.0
627	COM51	-8192.75, 550.0
628	COM53	-8239.25, 550.0
629	COM55	-8285.75, 550.0
630	COM57	-8332.25, 550.0
631	COM59	-8378.75, 550.0
632	COM61	-8425.25, 550.0
633	COM63	-8471.75, 550.0
634	COM65	-8518.25, 550.0
635	COM67	-8564.75, 550.0
636	NC14	-8809.4, 550.0
637	NC15	-8945.0, 400.5
638	NC16	-8945.0, 200.25
639	NC17	-8945.0, 0.0
640	NC18	-8945.0, -200.25
641	NC19	-8945.0, -400.5

5 Functional Block Diagram

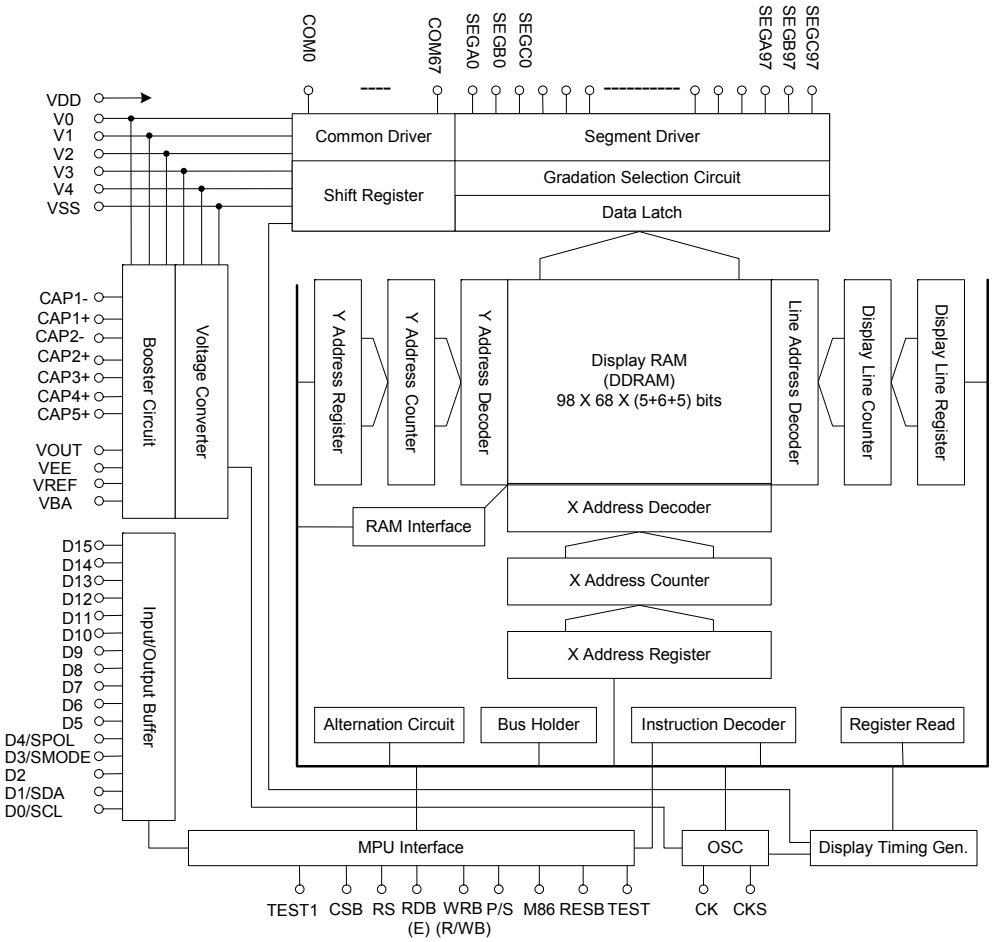


Figure 5-1 System Block Diagram

6 Pin Descriptions

6.1 Power Supply Pins

Symbol	I/O	Description
VDD	Power Supply	Power supply pin for logic circuit to +2.2 to 3.3V
VSS	Power Supply	Ground pin for internal circuit, connect to 0V
V0 V1 V2 V3 V4	Power Supply	Bias power supply pin for the LCD drive voltage These voltages should have the following correlation: VSS<V4<V3<V2<V1<V0 When the internal power supply circuit is active, these voltages are generated by the built-in booster and voltage converter. You must connect each VSS to a capacitor.

6.2 LCD Power Supply Circuit Pins

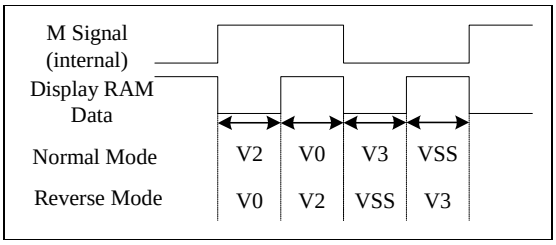
Symbol	I/O	Description
CAP1+	O	Connecting pin for the built-in booster capacitor + side. The capacitor is connected between CAP1– and CAP1+.
CAP1–	O	Connecting pin for the built-in booster capacitor - side. The capacitor is connected between CAP1– and CAP1+.
CAP2+	O	Connecting pin for the built-in booster capacitor + side. The capacitor is connected between CAP2– and CAP2+.
CAP2–	O	Connecting pin for the built-in booster capacitor - side. The capacitor is connected between CAP2– and CAP2+.
CAP3+	O	Connecting pin for the built-in booster capacitor + side. The capacitor is connected between CAP1– and CAP3+.
CAP4+	O	Connecting pin for the built-in booster capacitor + side. The capacitor is connected between CAP2– and CAP4+.
CAP5+	O	Connecting pin for the built-in booster capacitor + side. The capacitor is connected between CAP1– and CAP5+.
VEE	Power Supply	Voltage supply pin for the booster circuit. Usually the same voltage level as VDD.
VOUT	O	Output pin of the boosted voltage in the built-in booster. The capacitor must be connected between this pin and VSS.
VBA	O	Output pin for the regulator voltage of VBA AMP. This pin should not be layed out on LCM ITO circuit.
VREF	O	Output pin for the temperature compensation output voltage. This pin should not be layed out on LCM ITO circuit.

6.3 System Bus Pins

Symbol	I/O	Description
RESB	I	Reset input pin. When RESB is “L”, initialization is executed.
D0/SCL D1/SDA D2 D3/SMODE D4.SPOL D5-D7	I/O	Data bus / Signal interface related pins. When the parallel interface is selected (P/S = “H”), D7-D0 are 8-bit bi-directional data buses connecting to the MPU data bus. When the serial interface is selected (P/S = “L”), D0 and D1 (SCL, SDA) are used as serial interface pins. SCL**:** Input pin for the data transfer clock SDA**:** Serial data input pin SMODE**:** Serial transfer mode select pin SPOL**:** RS pole select pin when the 3-wire serial interface is selected. SDA data is latched at the rising edge of SCL. Internal serial/parallel conversion into 8-bit data occurs at the rising edge of the 8th clock of SCL after the data conversion is completed or when making no access, be sure to set SCL to “L”.
D8-D15	I/O	8-bit bi-directional bus. Connected to the MPU data bus. Used as a data bus for the upper 8 pins in 16-bit access mode.
CSB	I	Chip Select input pin. CSB = “L”**:** accepts access from MPU CSB = “H”**:** denies access from MPU
RS	I	RAM/Register select input pin. RS = “0”**:** D7-D0 are display RAM data RS = “1”**:** D7-D0 are control register data
RDB (E)	I	Read/Write control pin Select 80-family MPU type (M86 = “L”) RDB is a data read signal. When RDB is “L”, D7-D0 are in output state. Select 68-family MPU type (M86 = “H”) R/WB = “H”**:** when E is “H”, D7-D0 are in output state. R/WB = “L”**:** data on D7-D0 is latched at the falling edge of the E signal.
WRB (R/WB)	I	Read/Write control pin Select 80-family MPU type (M86 = “L”) WRB is a data write signal. Data on D7-D0 is latched at the rising edge of the WRB signal. Select 68-family MPU type (M86 = “H”) Read/Write control input pin. R/W = “H”**:** Read R/W = “L”**:** Write
M86	I	MPU interface type selecting input pin. M86 = “H”**:** 68-family interface M86 = “L”**:** 80-family interface Fixed at either “H” or “L”

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>P/S</td><td>I</td><td>Parallel/Serial interface select pin.
<table>
<tr><th>P/S</th><th>Chip Select</th><th>Data Identification</th><th>Data</th><th>Read/Write</th><th>Serial Clock</th></tr>
<tr><td>H</td><td>CSB</td><td>RS</td><td>D0-D7</td><td>RDB, WRB</td><td>-</td></tr>
<tr><td>L</td><td>CSB</td><td>RS</td><td>SDA</td><td>Write only</td><td>SCL</td></tr>
</table>
P/S = “H”: For parallel interface.
P/S = “L”: For serial interface. Fixed D15-D5 pins are Hi-Z, RDB and WRB pins at either “H” or “L”.</td></tr>
<tr><td>TEST</td><td>I</td><td>For testing. Fixed at “L”.</td></tr>
<tr><td>TEST1</td><td>I</td><td>For testing. Fixed at “L”.</td></tr>
</table>

6.4 LCD Drive Circuit Signals

<table>
<tr><th>Symbol</th><th>I/O</th><th>Description</th></tr>
<tr><td>SEGA0-A97
SEGB0-B97
SEGC0-C97</td><td>O</td><td>Segment output pins for LCD drives.
According to the Display RAM data, non-lighted at “0”, lighted at “1” (Normal Mode); non-lighted at “1”, lighted at “0” (Reverse Mode). Furthermore, with a combination of the M signal and display data, one signal level (among V0, V2, V3, and VSS signal levels) is selected.

</td></tr>
<tr><td>COM0-
COM67</td><td>O</td><td>Common output pins for LCD drivers. With a combination of the scanning data and M signal, one signal level (among V0, V1, V4 and VSS signal levels) is selected.
<table>
<tr><th>Data</th><th>M</th><th>Output Level</th></tr>
<tr><td>H</td><td>H</td><td>VSS</td></tr>
<tr><td>L</td><td>H</td><td>V1</td></tr>
<tr><td>H</td><td>L</td><td>V0</td></tr>
<tr><td>L</td><td>L</td><td>V4</td></tr>
</table></td></tr>
</table>

6.5 Oscillating Circuit Pin

Symbol	I/O	Description
CKS	I	Display timing clock source select input pin. CKS = "H": Use external clock from the CK pin CKS = "L": Use the internal oscillated clock
CK	I/O	The external clock input pin for display timing (CKS=1) or the internal clock output pin for display timing (CKS=0). When using the internal oscillator clock, CK must be floating (CKS=0)

7 Function Description

7.1 MPU Interface

7.1.1 Reset Pin Description (RESB)

Hold the RESB at low for at least 80μs, after which the EM65101 accepts this reset command.

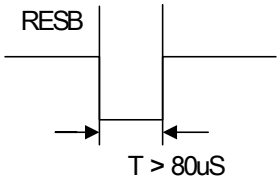


Figure.7-1 RESB Timing

7.1.2 Selection of Interface Type

The EM65570 transfers data through the 8-bit parallel I/O (D7-D0), 16-bit parallel I/O (D15-D0), or serial data input (SDA, SCL). You can use the P/S pin to select the parallel or serial interface. When the serial interface is selected, you are allowed to write only as data reading is prohibited.

P/S	I/F Type	CSB	RS	RDB	WRB	M86	SDA	SCL	Data
H	Parallel	CSB	RS	RDB	WRB	M86	-	-	D7~D0 (D15~D0)
L	Serial	CSB	RS	-	-	-	SDA	SCL	-

7.1.3 Parallel Input

When the parallel interface is selected with the P/S pin, the EM65570 allows data to be transferred in parallel to an 8-bit/16-bit MPU through the data bus. For the 8-bit/16-bit MPU, you can use the M86 pin to select either the 80-family or the 68-family MPU interface.

M86	MPU Type	CSB	RS	RDB	WRB	Data
H	68-family MPU	CSB	RS	E	R/WB	D7~D0 (D15~D0)
L	80-family MPU	CSB	RS	RDB	WRB	D0~D7 (D15~D0)

7.1.4 Read/Write Functions of Register and Display RAM

The EM65570 have four read/write functions in parallel interface mode. Each read/write function is selected with the combinations of RS, RDB, and WRB signals.

RS	68-Family R/WB	80-Family		Function
		RDB	RDB	
1	1	0	1	Read internal Register
1	0	1	0	Write internal Register
0	1	0	1	Read display data
0	0	1	0	Write display data

7.1.5 Serial Interface

The EM65570 has two types of serial interfaces, i.e, 3-wire and 4-wire serial interfaces. Use the SMODE pin to select the serial interface type.

- SMODE = “L”**:** 4-wire serial interface
- SMODE = “H”**:** 3-wire serial interface

7.1.5.1 4-Wire Type Serial Interface

When the chip select is active (CSB = “L”), the 4-wire type serial interface works through the SDA and SCL input pins. When chip select is inactive (CSB = “H”), the internal shift register and counter are reset to the initial condition. Serial data SDA are input sequentially in the order of D7 to D0 at the rising edge of the serial clock (SCL). The RS pin determines whether serial data input (SDA) is used as display RAM data or as control register data.

- RS = “L”**:** display RAM data
- RS = “H”**:** control register data

After completing the 8-bit data transfer or when making no access, be sure to set the serial clock input (SCL) to “L”. Care should be taken during board wiring to avoid external noise from contaminating the SDA and SCL signals. To prevent transfer error due to external noise, release chip select (CSB = “H”) after every complete 8-bit data transfer.

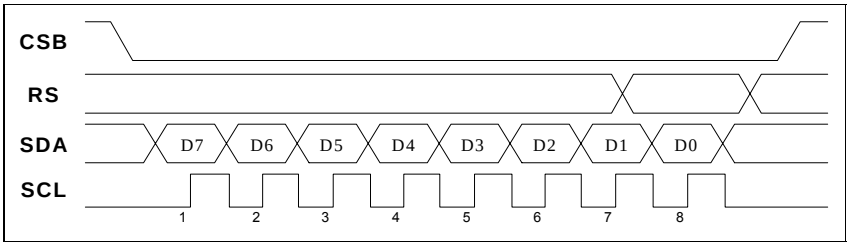


Figure 7-2 4-Wire Type Serial Interface

7.1.5.2 3-Wire Type Serial Interface

When the chip select is active (CSB = “L”), the 3-wire serial interface works through the SDA and SCL input pins. When chip select is inactive (CSB = “H”), the internal shift register and counter are reset to the initial condition. Serial data SDA are input sequentially in the order of RS, D7 to D0 at the rising edge of the serial clock (SCL). The first serial input data (RS) and the SPOL pin determine whether serial data input (SDA) is used as display RAM data or as control register data.

SPOL = “0”		SPOL = “1”	
RS	Display RAM/Register	RS	Display RAM/Register
0	Display RAM Data	0	Control Register Data
1	Control Register Data	1	Display RAM Data

After completing the 9-bit data transfer or when making no access, be sure to set the serial clock input (SCL) to “L”. Care should be taken during board wiring to avoid external noise from contaminating the SDA and SCL signals To prevent transfer error due to external noise, release chip select (CSB = “H”) after every complete 9-bit data transfer.

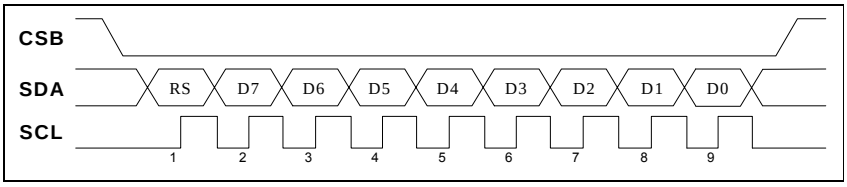


Figure 7-3 3-Wire Type Serial Interface

7.2 Writing Data to Display RAM and Control Register

The procedure of writing data to the display RAM and Control Register is similar except for the RS selection which selects the accessed object.

- RS = "L": Display RAM data
- RS = "H": Control register data

In the case of the 80-family MPU, data is written at the rising edge of WRB. In the case of the 68-family MPU, data is written at the falling edge of signal E.

7.2.1 Writing Data Operation

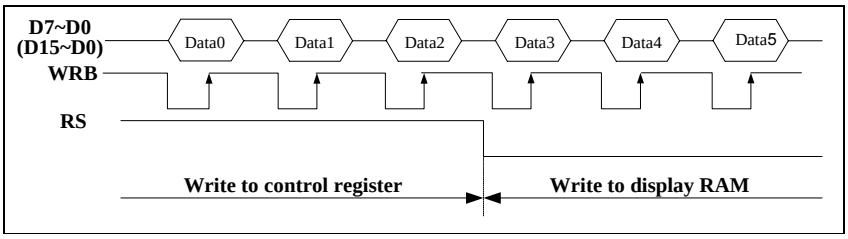


Figure 7-4 Writing Data to Display RAM & Control Register Operation

7.3 Internal Display RAM and Register Read

7.3.1 Read Display RAM Operation

A one-time dummy read operation is required to perform the display RAM read operation. The designated address data are not output to read operation immediately after the address is set to AX or AY register, but are output when the second data read is performed. Dummy read is always required once after the address is set and the write cycle begins.

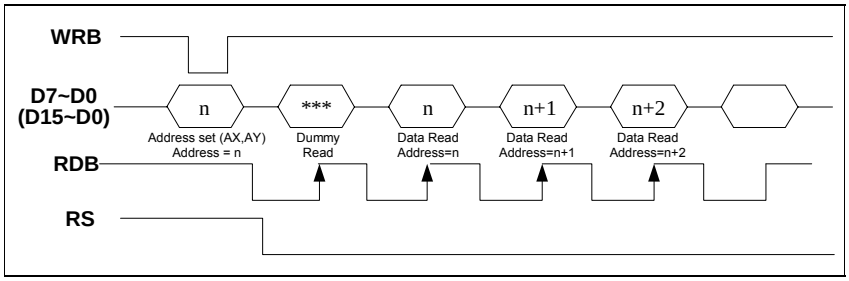


Figure 7-5 Read Display RAM Operation

7.3.2 Register Read Operation

The EM65570 can read the control registers. When issuing a control register read operation, the upper data bus nibble (D7-D4) is used for the register address (0 to FH). Up to 16 registers can be accessed directly. However, more than 16 registers are provided. To solve this over supply problem, the EM65570 uses the register bank control to access the RE register with a bank number. You can access the RE register through any bank. The following lists the steps to be taken when accessing the specific register using the bank access control.

1. Set 01H to RE register for access to the RA register.
2. Set the specific register address to the RA register.
3. Set the specific register bank to the RE register.
4. Read the contents at the specific register.

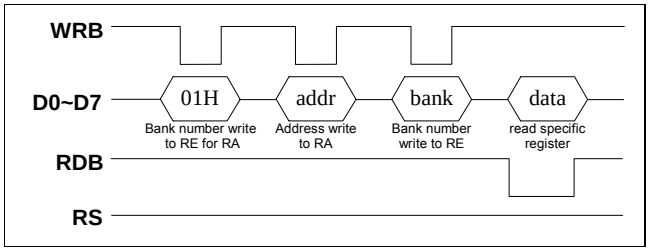


Figure 7-6 Register Read Operation

7.4 16-Bit Data Access to Display RAM

The EM65570 has both 8-bit and 16-bit data bus sizes. The data bus size can be selected by the WLS register.

- WLS = "0"**:** 8-bits bus size
- WLS = "1"**:** 16-bits bus size

In 16-bit access mode, the Control Register Access uses the low-byte data bus (D7~D0) in the internal circuit and does not use the high-byte data bus (D15~D8). When reading control register using 16-bit bus, data exist at D3~D0 while D15~D4 is always 1 or "H".

7.5 Fast Burst RAM Write Function

The EM65570 has a built-in fast burst RAM write function. This function allows data transfer of 32 bits thus requiring only half of the access time needed for common standard RAM write function (16-bit data bus). The burst RAM write function is suitable for frequent data rewriting such as color animation display.

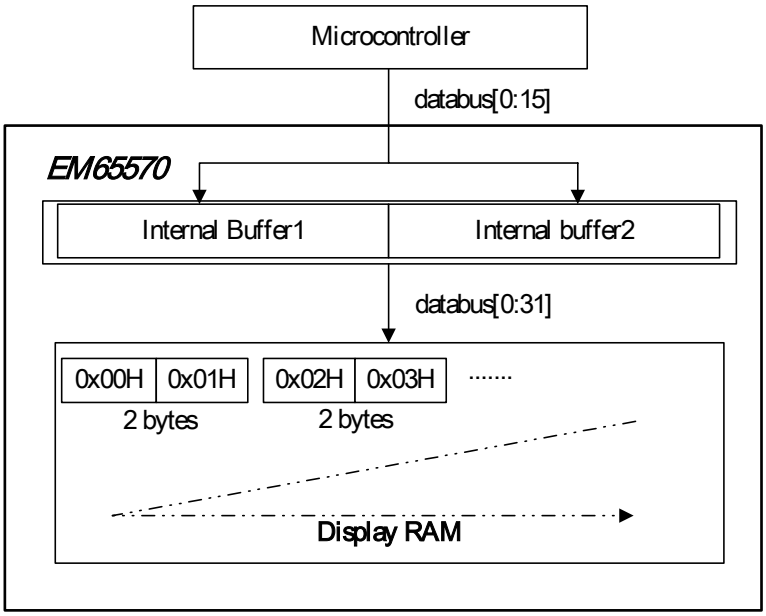


Figure 7-7 Fast Burst RAM Write Operation

NOTE

Fast Burst RAM Write Function works more efficiently in horizontal RAM data writing mode, that is, RDWS[2]=0

7.6 Display RAM Access Using the Windows Function

The EM65570 has a window area setting command for accessing a specified display RAM area. To use the window function, you need to set up the X & Y address positions. In addition, you also need to enable the auto-increment mode (AXI="1", AYI="1"). These two positions represent the window start position and window end position. Set the X address (AX) and Y address (AY) registers to specify the window start position of X and Y respectively. Set the Window X End address (EX) and Window Y End address (AY) to specify the window end positions of X and Y respectively. When accessing the window function, you can set AIM to "1" to modify write access. You should set the following registers before accessing RAM when you use the window function.

WIN = "1", AXI="1", AYI="1"

X Address, Y Address, Window X End Address, Window Y End Address

Moreover, the following address condition must be met:

- Window end X address (EX) ≧ Window start X address (AX)
- Window end Y address (EY) ≧ Window start Y address (AY)

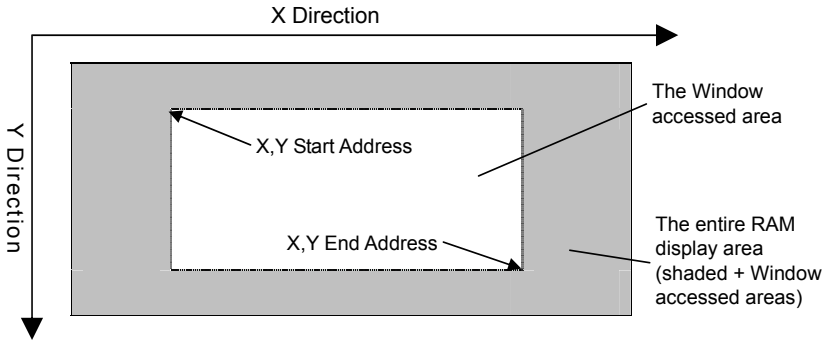


Figure 7-8 Window XY Address Location within RAM Display

7.7 Display RAM Data and LCD

One bit of display RAM data corresponds to one dot of LCD. Normal display and reverse display by the REV register are set up as follows:

- Normal display (REV=0): RAM data = "0," light OFF
  RAM data = "1," light ON
- Reverse display (REV=1): RAM data = "0," light ON
  RAM data = "1" light OFF

7.8 Correlation between Display RAM and Address

The EM65570 executes the address conversion depending on the control register setting. In auto increment mode, usually the AX register is increased by one. For example, when REF and AXI are both "1", AX register is incremented by one, but effective X address seems to decrement because of address conversion. The effective Y address uses AY register values as it is.

7.8.1 Gradation Mode (65K Colors), (C256=0, 65K=1)

■ **8-Bit Mode (WLS=0)**

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment			
*	0	0	X=00H	X=01H	X=C2H	X=C3H
			D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7
			SEG A0	SEG B0	SEG C0	SEG A97	SEG B97	SEG C97

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment			
*	1	0	X=01H	X=00H	X=C3H	X=C2H
			D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7
			SEG A0	SEG B0	SEG C0	SEG A97	SEG B97	SEG C97

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment			
*	0	1	X=00H	X=01H	X=C2H	X=C3H
			D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7
			SEG C0	SEG B0	SEG A0	SEG C97	SEG B97	SEG A97

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment			
*	1	1	X=01H	X=00H	X=C3H	X=C2H
			D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7	D0 D1 D2 D3 D4 D5 D6 D7
			SEG C0	SEG B0	SEG A0	SEG C97	SEG B97	SEG A97

■ **16-Bit Mode (WLS=1)**

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment		
*	*	0	X=00H	X=61H	
			D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	
			SEG A0	SEG B0	SEG C0	SEG A97	SEG B97	SEG C97

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment		
*	*	1	X=00H	X=61H	
			D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	D0 D1 D2 D3 D4 D5 D6 D7 D8 D9 D10 D11 D12 D13 D14 D15	
			SEG C0	SEG B0	SEG A0	SEG C97	SEG B97	SEG A97

7.8.2 Gradation Mode (4096 Colors), (C256=0, 65K=0)

■ **8-Bit Mode (WLS="0")**

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																									
*	0	0	X=00H				X=01H									X=C2H				X=C3H								
			D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	
			SEG A0				SEG B0				SEG C0					SEG A97				SEG B97				SEG C97				

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																									
*	0	1	X=00H				X=01H									X=C2H				X=C3H								
			D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	
			SEG C0				SEG B0				SEG A0					SEG C97				SEG B97				SEG A97				

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																									
*	1	0	X=01H				X=00H									X=C3H				X=C2H								
			D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	
			SEG A0				SEG B0				SEG C0					SEG A97				SEG B97				SEG C97				

ABS	WBS	SWAP	X Address / Data Bus/ Segment Assignment																									
*	1	1	X=01H				X=00H									X=C3H				X=C2H								
			D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D0	D1	D2	D3	D4	D5	D6	D7	
			SEG C0				SEG B0				SEG A0					SEG C97				SEG B97				SEG A97				

■ **16-Bit Mode (WLS="1")**

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																									
0	*	0	X=00H													X=61H												
			D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15		D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15	
			SEG A0				SEG B0				SEG C0					SEG A97				SEG B97				SEG C97				

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																									
0	*	1	X=00H													X=61H												
			D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15		D1	D2	D3	D4	D7	D8	D9	D10	D12	D13	D14	D15	
			SEG C0				SEG B0				SEG A0					SEG C97				SEG B97				SEG A97				

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																									
1	*	0	X=00H													X=61H												
			D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11		D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	
			SEG A0				SEG B0				SEG C0					SEG A97				SEG B97				SEG C97				

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																					
1	*	1	X=00H												X=61H									
			D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11
			SEG C0			SEG B0			SEG A0						SEG C97			SEG B97			SEG A97				

7.8.3 Gradation Mode (256 Colors), (C256=1, 65K=0)

■ **8-Bit Mode (WLS=0)**

ABS	WBS	SWAP	X Address/ Data Bus / Segment Assignment																	
*	*	0	X=00H									X=61H								
			D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D4	D5	D6	D7	
			SEG A0		SEG B0			SEG C0				SEG A97		SEG B97			SEG C97			

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																	
*	*	1	X=00H									X=61H								
			D0	D1	D2	D3	D4	D5	D6	D7		D0	D1	D2	D3	D4	D5	D6	D7	
			SEG C0		SEG B0			SEG A0				SEG C97		SEG B97			SEG A97			

■ **16-Bit Mode (WLS=1)**

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																													
*	*	0	X=00H														X=30H															
			D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
			SEG A0		SEG B0		SEG C0		SEG A1				SEG A1			SEG C1			SEG A96		SEG B96		SEG C96			SEG A97			SEG B97			SEG C97	

ABS	WBS	SWAP	X Address / Data Bus / Segment Assignment																													
*	*	1	X=00H														X=30H															
			D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15
			SEG A1		SEG B1		SEG C1		SEG A0				SEG B0			SEGC0			SEG A97		SEG B97		SEG C97			SEG A96			SEG B96			SEG C96	

7.8.4 Data Read and Write Bit Assignment

■ **16-Bit Data Bus Mode**

ABS=0	65K=1	C256=0	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

ABS=0	65K=0	C256=0	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D15	D14	D13	D12	1	D10	D9	D8	D7	1	1	D4	D3	D2	D1	1

ABS=1	65K=0	C256=0	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			Read	1	1	1	1	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

ABS=*	65K=0	C256=1	Write	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

■ **8-Bit Data Bus Mode**

ABS=*	65K=1	C256=0	Address	00,02,04……..C0,C2H								01,03,05……..C1,C3H							
			Write	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

ABS=*	65K=0	C256=0	Address	00,02,04……..C0,C2H								01,03,05……..C1,C3H							
			Write	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
			Read	1	1	1	1	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0

ABS=*	65K=0	C256=0	Address	00,02,04……..C0,C2H								01,03,05……..C1,C3H							
			Write	D7	D6	D5	D4	D3	D2	D1	D0	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D7	D6	D5	D4	D3	D2	D1	D0	1	1	1	1	D3	D2	D1	D0

ABS=*	65K=0	C256=1	Address	00,01,02……..C1,C2,C3H							
			Write	D7	D6	D5	D4	D3	D2	D1	D0
			Read	D7	D6	D5	D4	D3	D2	D1	D0

7.9 Display Data Structure and Gradation Control

For the purpose of the gradation control, one pixel requires multiple bits of display RAM. The EM65570 has 5-bit data per output to achieve gradation display.

The three outputs of the segment driver are used for one pixel of RGB, and the EM65570 is connected to a color STN LCD panel. It can display 98*68 pixels with 65K colors (5 bits * 6 bits * 5 bits). In this case, since the gradation display data is processed by a single access to the memory, data can be rewritten fast and efficiently.

The weighting for each data bit is dependent on the status of the SWAP bit that is selected when data is written to the display RAM.

7.9.1 Gradation Mode (65K Color)

7.9.1.1 8-Bit Mode

■ **SWAP=0**

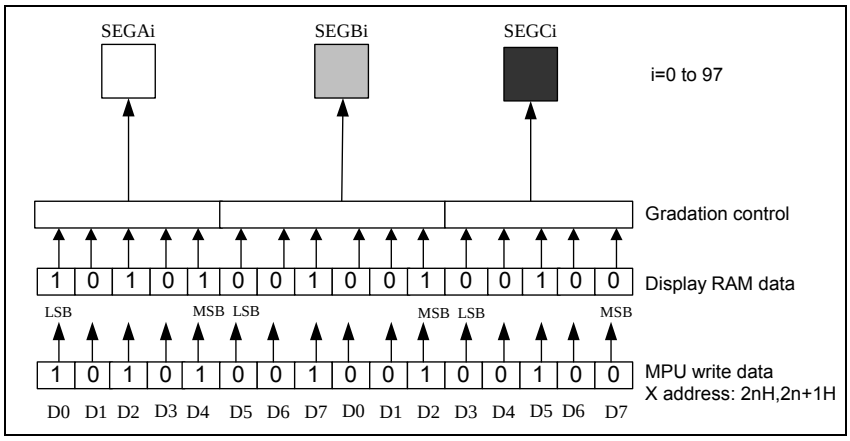


Figure 7-9a Writing Data to Display RAM with SWAP=0 Selected under 8-Bit (65K Color) Mode

■ **SWAP=1**

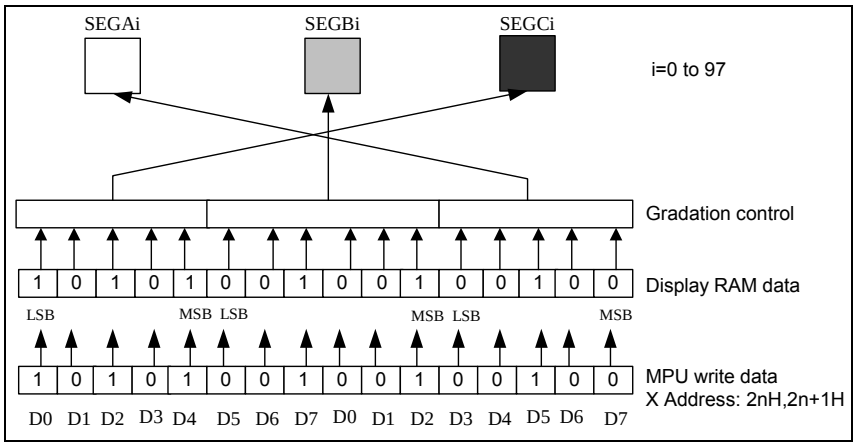


Figure 7-9b Writing Data to Display RAM with SWAP=1 Selected under 8-Bit (65K Color) Mode

7.9.1.2 16-Bit Mode

In 16-bit access mode, the weighting for each data bit is dependent on the status of the SWAP bit that is selected when data is written to the display RAM, as in the case with the 8-bit access mode.

■ **SWAP=0**

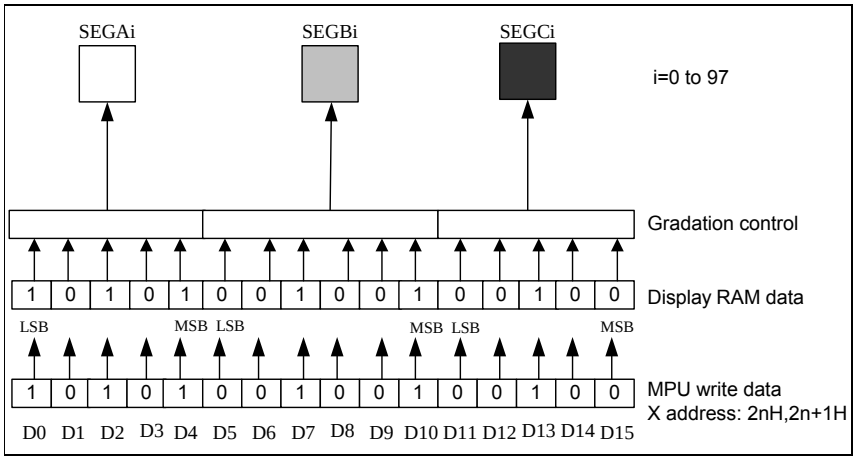


Figure 7-10a Writing Data to Display RAM with SWAP=0 Selected under 16-Bit (65K Color) Mode

■ **SWAP=1**

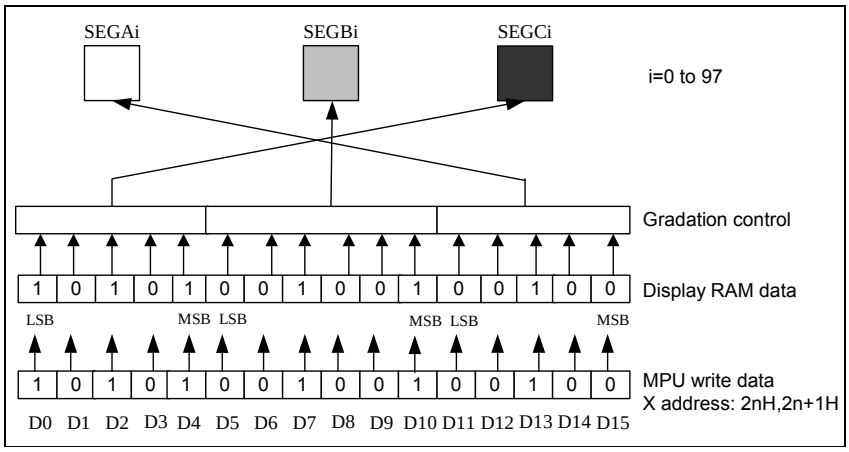


Figure 7-10b Writing Data to Display RAM with SWAP=1 Selected under 16-Bit (65K Color) Mode

7.9.2 Gradation Mode (4096 Color)

7.9.2.1 8-Bit Mode

■ **SWAP=0**

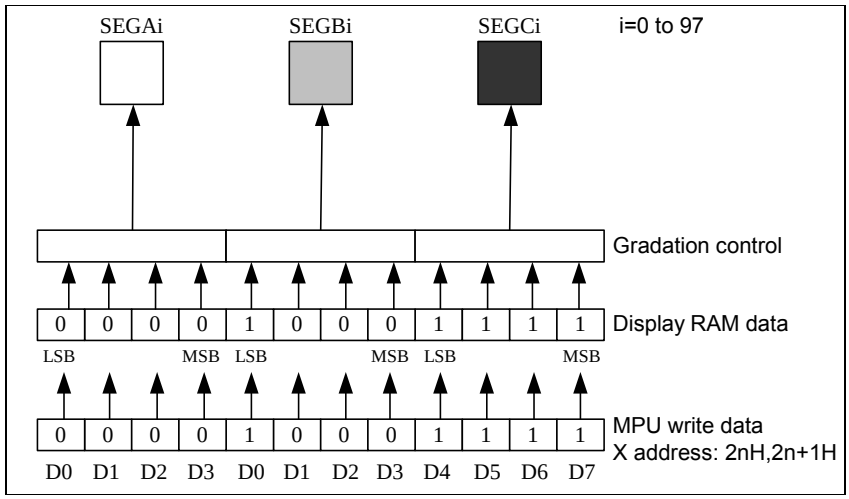


Figure 7-11a Writing Data to Display RAM with SWAP=0 Selected under 8-Bit (4096 Color) Mode

■ **SWAP=1**

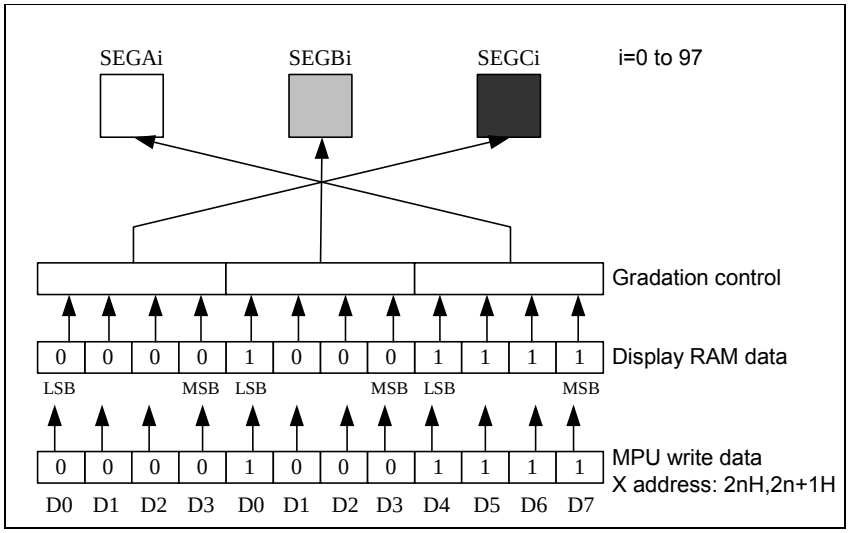


Figure 7-11b Writing Data to Display RAM with SWAP=1 Selected under 8-Bit (4096 Color) Mode

7.9.2.2 16-Bit Mode

In 16-bit access mode, the weighting for each data bit is dependent on the status of the SWAP bit that is selected when data is written to the display RAM, as in the case with the 8-bit access mode.

■ **SWAP=0**

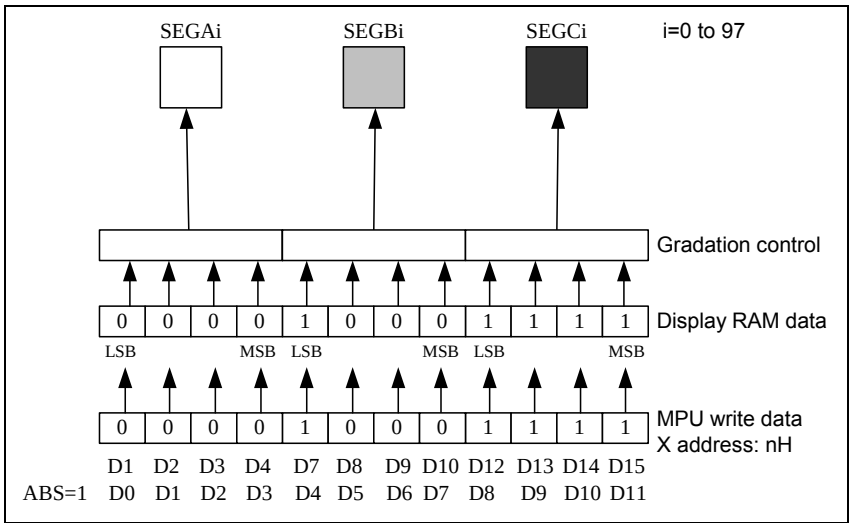


Figure 7-12a Writing Data to Display RAM with SWAP=0 Selected under 16-Bit (4096 Color) Mode

■ **SWAP=1**

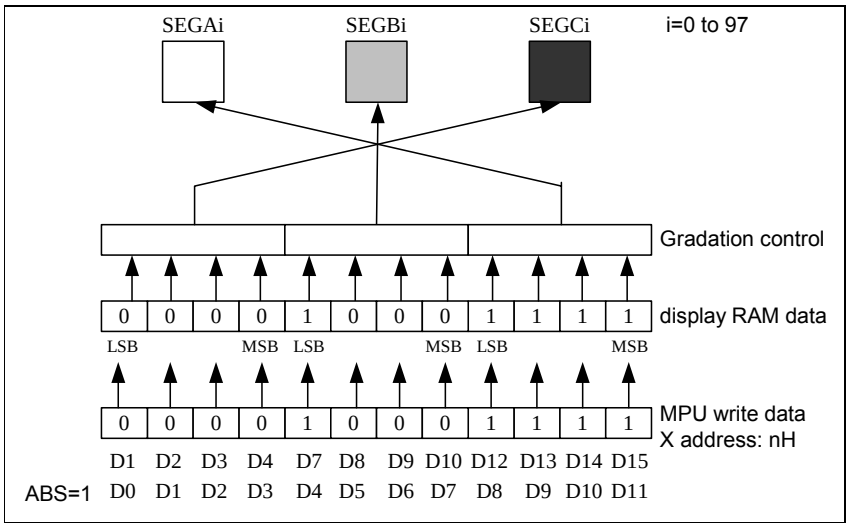


Figure 7-12b Writing Data to Display RAM with SWAP=1 Selected under 16-Bit (4096 Color) Mode

7.9.3 Gradation Mode (256 Color)

7.9.3.1 8-Bit Mode

■ **SWAP=0**

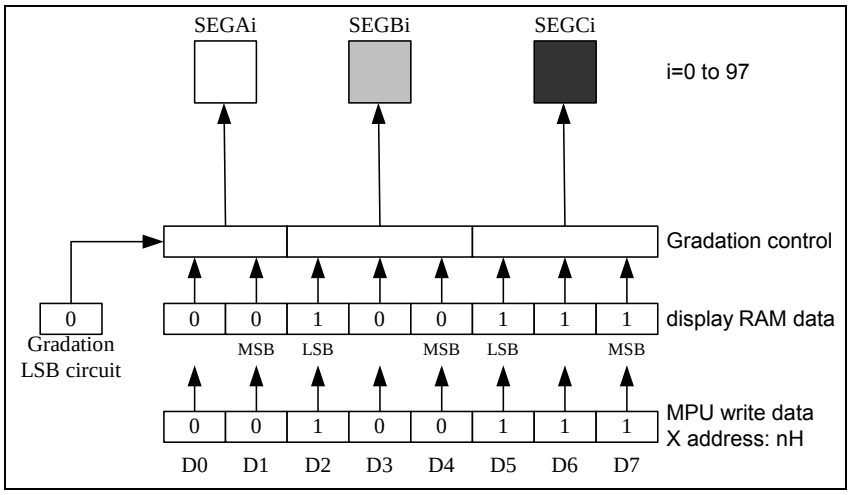


Figure 7-13a Writing Data to Display RAM with SWAP=0 Selected under 8-Bit (256 Color) Mode

■ **SWAP=1**

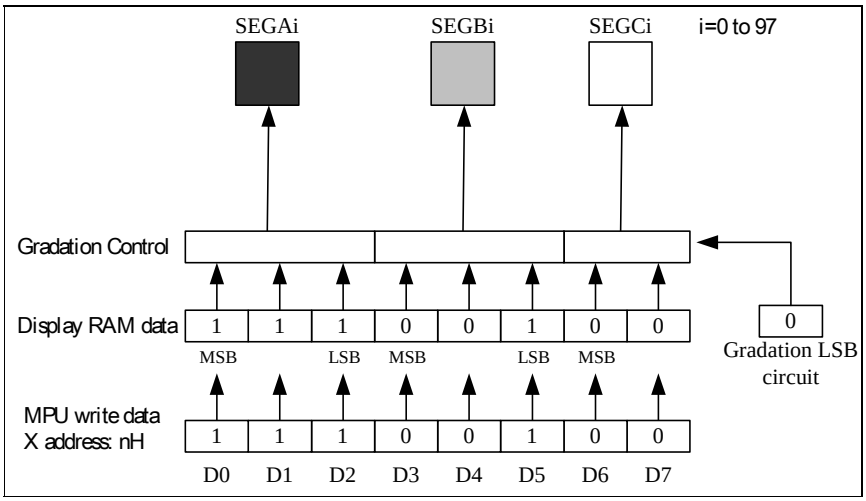


Figure 7-13b Writing Data to Display RAM with SWAP=1 Selected under 8-Bit (256 Color) Mode

7.9.3.2 16-Bit Mode (WLS=1)

■ **SWAP=0**

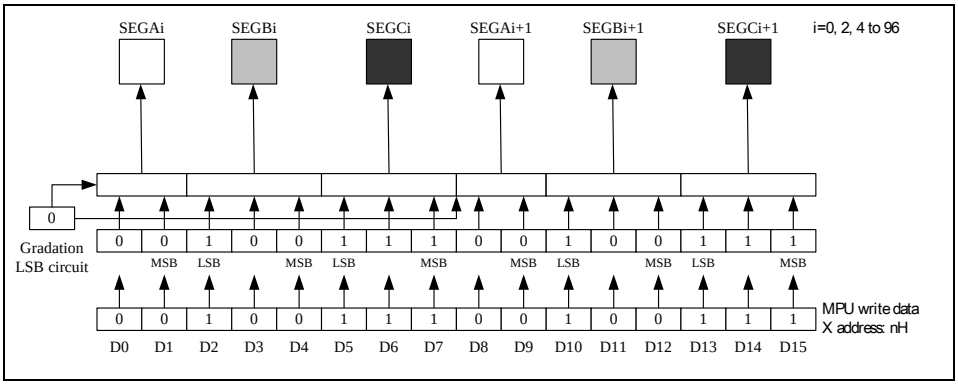


Figure 7-14a Writing Data to Display RAM with SWAP=0 Selected under 16-Bit (256 Color) Mode

■ **SWAP=1**

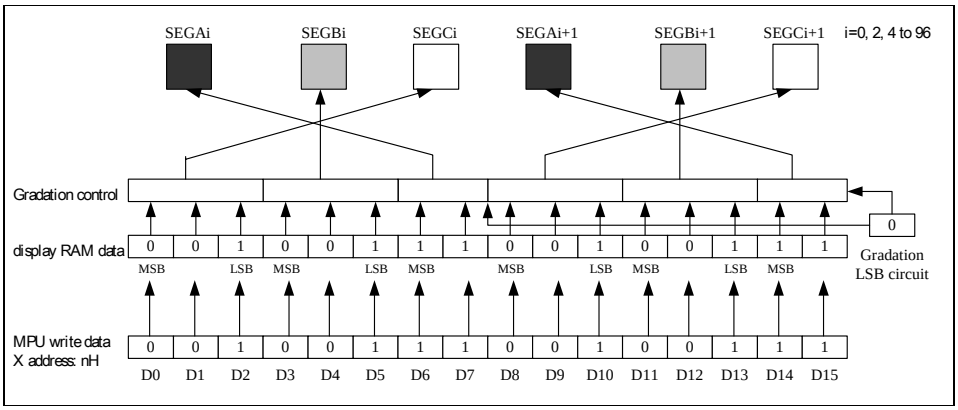


Figure 7-14b Writing Data to Display RAM with SWAP=1 Selected under 16-Bit (256 Color) Mode

7.10 Gradation LSB Control

In 256-color mode (C256=1), the EM65570 provides segment driver output for 8-gradation display using 3 bits. For 4-gradation display, 2 bits are used.

The segment driver output for the 4-gradation display uses 2 bits to write to the corresponding RAM area and additional 1 bit supplemented by the gradation LSB circuit, and then it selects 4-gradation from the 8-gradation.

In 256-color mode (C256=1), the segment driver output for the 4-gradation display will result in a gradation level of "0" regardless of the gradation LSB when 2 bits of data on the display RAM are "00". When 2 bits of data on the display RAM is "11," a gradation level of 7/7 is selected regardless of the bit information of the gradation LSB. The other gradation levels are selected depending on 2 bits of data on the display RAM and the gradation LSB bits.

One bit of data is supplemented by setting the gradation LSB register (GLSB).

The Gradation LSB control bit applies to all 4-gradation segment drivers.

Gradation LSB = "0": Selects 0 as the LSB information on the RAM for 4-gradation segment drivers.

Gradation LSB = "1": Selects 1 as the LSB information on the RAM for 4-gradation segment drivers.

7.11 Display Timing Circuit

The display timing circuit generates internal signals and timing pulses (internal LP, FLM, M) by clock.

Symbol	Description
LP (internal)	The LP is latch clock signal. At the raising edge, count the display line counter. At the falling edge output the LCD drive signal.
FLM (internal)	The signal for the LCD display synchronous signals (first line maker). When FLM is set to "H," the display start-line address is present.
M (internal)	The signal for alternated signals of LCD drive output.

7.11.1 Signal Generation to Display Line Counter and Data Latching Circuit

Clocks to the line counter and display data latching circuit from the display clock (internal LP) are generated. Synchronized with the display clock (internal LP), the line addresses of Display RAM are generated and the 384-bit display data is latched to the display data latching circuit to output to the LCD drive circuit (Segment outputs). Read-out of the display data to the LCD drive circuit is completely independent of MPU. Therefore, MPU has no relationship with the read-out operation that accesses the display data.

7.11.2 Generation of the Alternated Signal (internal M) and the Synchronous Signal (internal FLM)

LCD alternated signal (internal M) and synchronous signal (internal FLM) are generated by the display clock (internal LP). The FLM generates alternated drive waveform to the LCD drive circuit. Normally, the FLM generates alternated drive waveform every frame (M-signal level is reversed every one frame). However, when setting up data (n-1) in an n-line reverse register and n-line alternated control bit (NLIN) at “1,” the n-line reverse waveform is generated.

7.11.3 Display Data Latching Circuit

Display data latching circuit temporally latches the display data that is output to the LCD driver circuit from display RAM every one common period. Normal display/reverse display, display ON/OFF, and display ALL-ON functions are operated by controlling data in display data latch. Therefore, there is no change of data within the display RAM.

7.12 Output Timing of LCD Driver

Display timing at Normal mode (not Reverse mode), 1/68 DUTY.

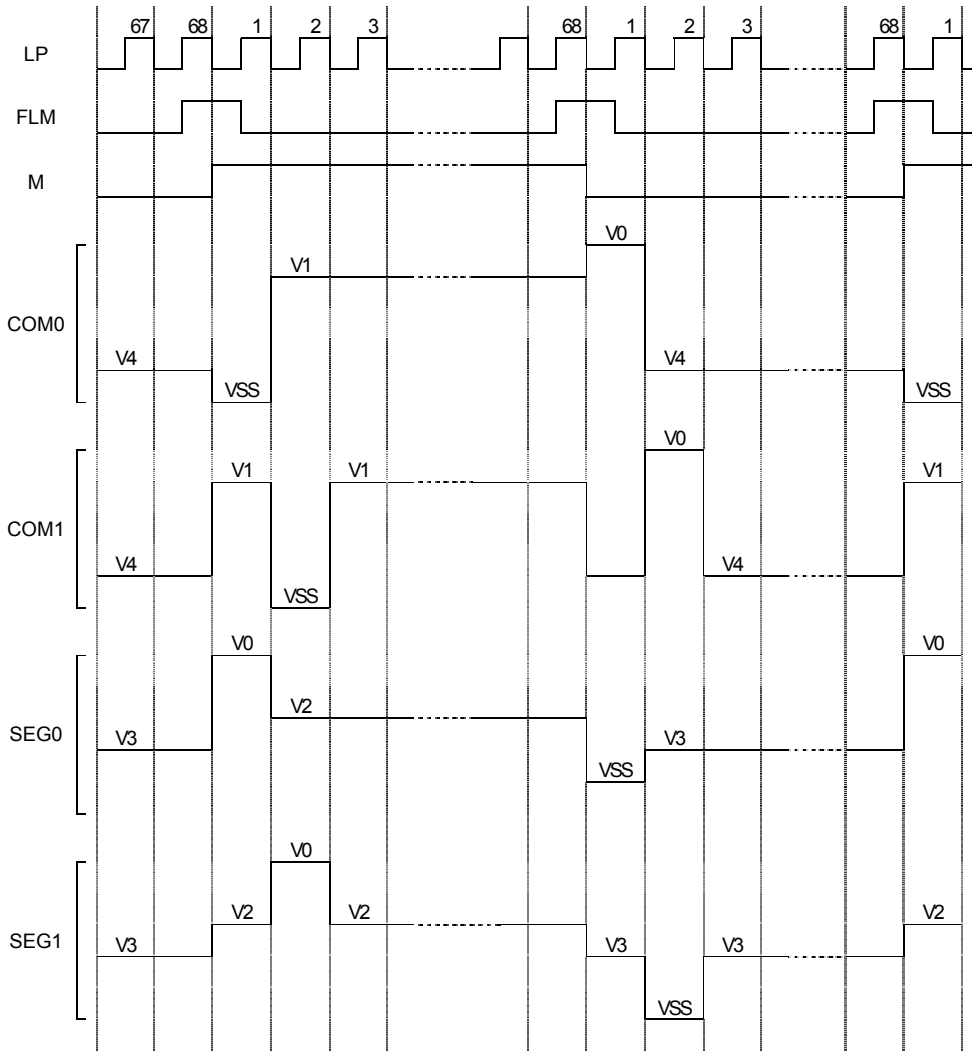


Figure 7-15 LCD Driver Normal Mode Output Timing Diagram

7.13 LCD Drive Circuit

This drive circuit generates four levels of LCD drive voltage. The circuit has 294 segment outputs and 68 common outputs; and outputs combined display data and internal signal M. The common drive circuit shifts register and sequentially outputs common scan signals.

7.14 Oscillator Circuit

The EM65570 has a CR oscillator. The output from this oscillator is used as the signal timing source of the display and the boosting clock to the booster.

When the external clock is used, feed the clock source to the CK pin.

The duty cycle of the external clock must be 50%.

The resistance ratio of the CR oscillator is programmable. When you change this ratio, you must also change the display frame frequency.

7.15 Power Supply Circuit

This circuit supplies voltages necessary to drive a LCD. The circuit consists of booster and voltage converter.

Boosted voltage from the booster is fed to the voltage converter that converts this input voltage into V0, V1, V2, V3, and V4 which are in turn used to drive the LCD. This internal power supply should not be used to drive a large LCD panel containing many pixels. Otherwise, display quality will degrade considerably.

DCON	AMPON	Booster Circuit	Voltage Conversion Circuit
1	1	ENABLE	ENABLE
1	0	ENABLE	DISABLE
0	0	DISABLE	DISABLE

7.16 Booster Circuit

Placing capacitor C1 across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-, across CAP4+ and CAP2-, across CAP5+ and CAP1-, and across VOUT and VSS will boost the voltage coming from VEE and VSS n times and outputs the boosted voltage to the VOUT pin. Voltages that are boosted twice, three, four and five times respectively are output to the VOUT pin by the boost step register set.

(1) To use the voltage that is boosted two times, place C1 only across CAP1+ and CAP1-; and open CAP2+, CAP2-, CAP3+, CAP1-, CAP4+, CAP2-, CAP5+, & CAP1-

(2) To use the voltage that is boosted three times, place C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-; and open CAP3+, CAP1-, CAP4+, CAP2-, CAP5+, & CAP1-

(3) To use the voltage that is boosted four times, place C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-; and open CAP4+, CAP2-, CAP5+, & CAP1-

(4) To use the voltage that is boosted five times, place C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1- across CAP4+ and CAP2-; and open CAP5+ & CAP1-

(5) To use the voltage that is boosted six times, place C1 only across CAP1+ and CAP1-, across CAP2+ and CAP2-, across CAP3+ and CAP1-, across CAP4+ and CAP2-, across CAP5+ and CAP1-

When using the built-in booster circuit, output voltage (VOUT) must be less than the recommended operating voltage (20.0 Volt). If the output voltage (VOUT) is greater than the recommended operating voltage, normal operation of the chip cannot be guaranteed.

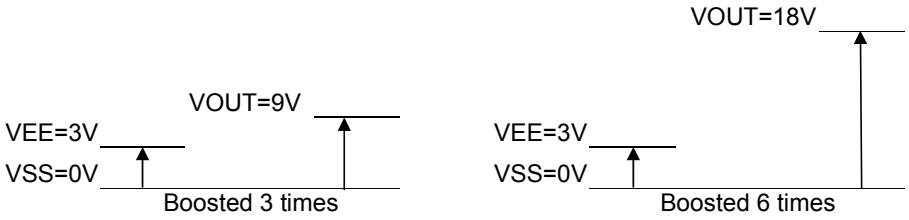


Figure 7-16 Correlation between VEE and VOUT Boost-up Voltages

NOTE

The maximum voltage VOUT of 20V is automatically limited by hardware to avoid damage to the IC.

7.17 Electronic Volume

The voltage conversion circuit has a built-in electronic volume, which allows VBA to be controlled with the DV register setting. The relationship between VBA and DV is given in the following equation**:**

$$VBA = (1+ (M+offset)/381) * VREF$$

Where: ***M:*** *DV register value*
offset: *CV register value*
VREF: *temperature compensation output voltage*

The VBA range is from 1.5V to 2V at 25°C.

7.18 Voltage Regulator

The EM65570 has a built-in reference voltage regulator, which generates the voltage amplified by the input voltage from the internal temperature compensation output voltage VREF pin. The generated voltage is output at the V0 pin. Even if the boosted voltage level fluctuates, V0 will remain stable as long as VOUT is higher than V0. A stable power supply can be obtained using this constant voltage, even if the load fluctuates. The EM65570 uses the generated V0 level as the reference level of the electronic volume to generate the LCD drive voltage.

7.19 Voltage Generation Circuit

The voltage converter contains the voltage generation circuit. The LCD drive voltages other than V0 (that is, V1, V2, V3 and V4) are obtained by dividing V0 through a resistor network. The LCD drive voltage from the EM65570 is biased at 1/4, 1/5, 1/6, 1/7, 1/8 , 1/9. When using the internal power supply, connect a stabilizing capacitor C2 to each of pins V0 to V4. The capacitance of C2 should be determined while selecting the LCD panel to be used.

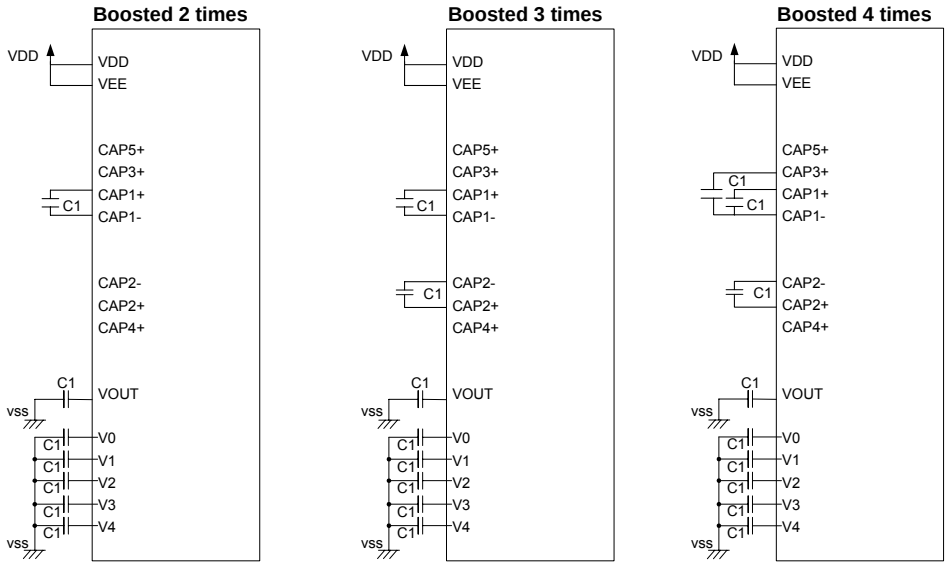


Figure 7-17a Internal Power Capacitor Connections Application Circuits (Voltage Boosted 2, 3, and 4 Times)

Recommended value**:**

C1	1.0 to 1.5 uF

NOTE

The X5R type external capacitor must be used.

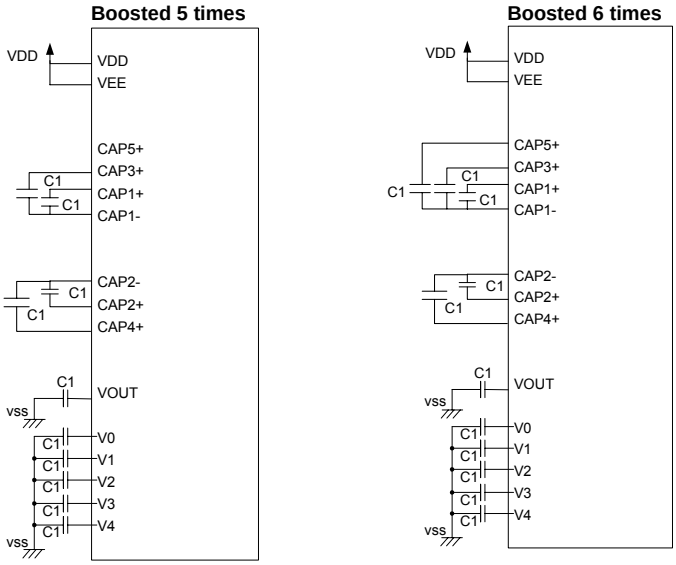


Figure 7-17b Internal Power Capacitor Connections Application Circuits (Voltage Boosted 5 and 6 Times)

Recommended value:

C1	1.0 to 1.5 uF

NOTE

The X5R type external capacitor must be used.

7.20 EEPROM Function

The EM65570 provides EEPROM function to set the LCD operating voltage Vop. It can also select the EEPROM operating mode. In EEPROM select register (Bank 5[AH]), use (M1, M0) to select the operating mode for EEPROM.

(M1, M0)	EEPROM operating mode	Delay time	Needing VDD voltage
00	Read	≧ 10 uS	≧ 2.4V
01	Program	≧ 4 mS	≧ 2.8V
10	Erase	≧ 4 mS	≧ 2.8V
11	Reserve	-	-

NOTE

When using EEPROM function, different operating modes need different VDD voltage levels.

You can get the Vop calibration offset voltage by setting Vop calibration offset register (Bank 5[BH &EH]).

CV5~CV0	Calibration Offset
011111	+31
011110	+30
…	…
000001	+1
000000	0
100000	-32
100001	-31
…	…
111111	-1

7.20.1 EEPROM Program, Read, and Erase Flow Charts

The following are the EEPROM Program, Read and Erase flow charts for achieving correct Vop offset voltage.

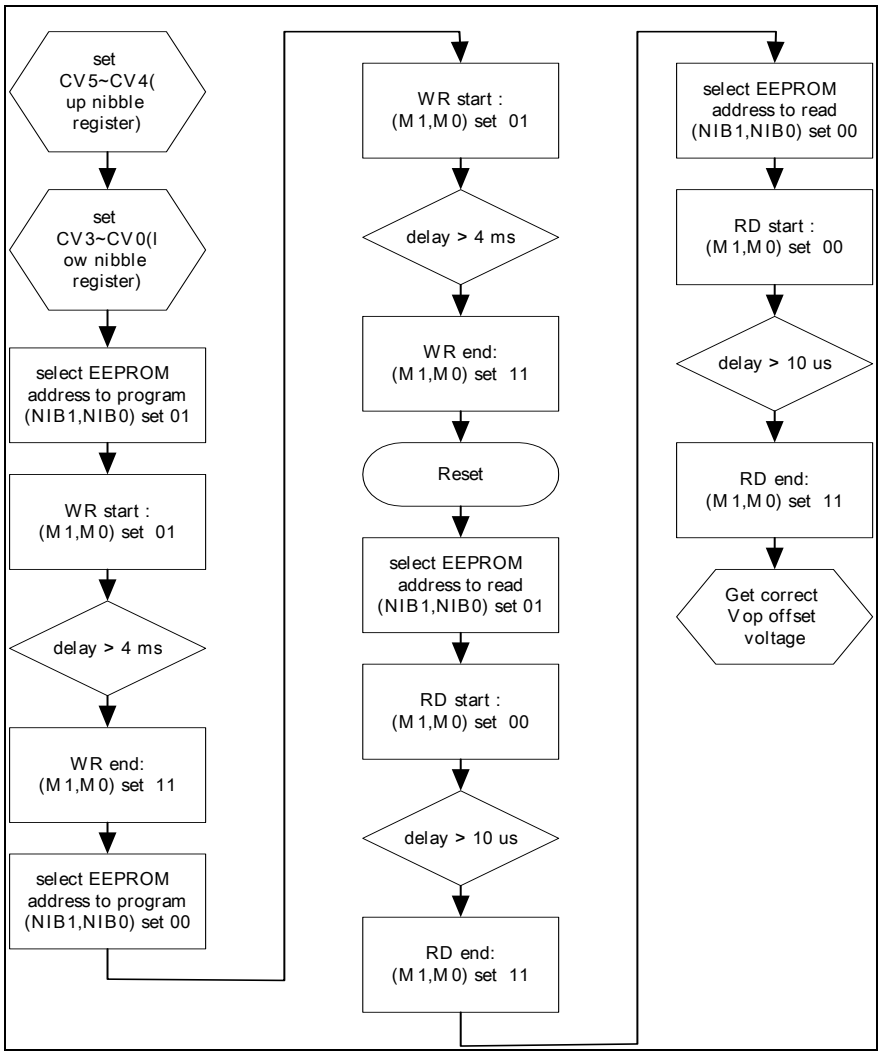
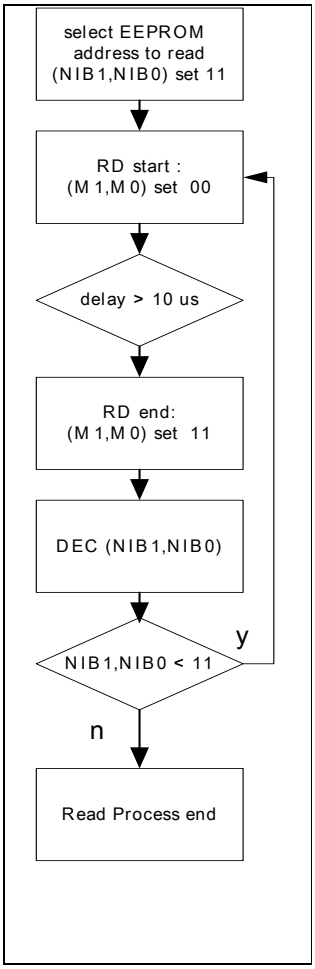
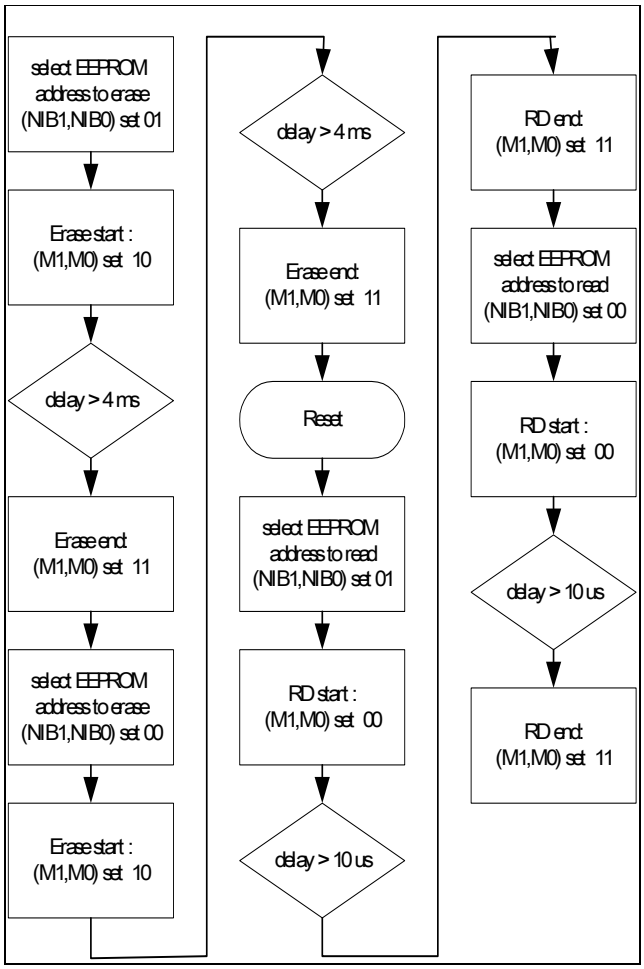


Figure 7-18a EEPROM Program Flow Chart



7-18b EEPROM Read Flow Chart



7-18c EEPROM Erase Flow Chart

7.20.2 Vop Calibration Offset Examples

■ **Program**

If the desired Vop calibration offset is +30, CV5~CV0 is set to 011110. The example code is shown below:

```
WRITE  #F4H      // set RE FLAG 100 → INSTRUCTION Bank 4
WRITE  #71H      // set CV5~CV4=01
WRITE  #6EH      // set CV3~CV0=1110
WRITE  #A1H      // set NIB1~NIB0=01 → program CV5~CV4
WRITE  #52H      // set EEPROM operating mode → programming;
                    ROM power is from internal V0
DELAY > 4 MS     // wait > 4 ms to finish programming
WRITE  #56H      // set EEPROM mode → reserve (finish programming)
WRITE  #A0H      // set NIB1~NIB0=00 → program CV3~CV0
WRITE  #52H      // set EEPROM operating mode → programming;
                    EEPROM power is from internal V0
DELAY > 4 MS     // wait > 4 ms to finish programming
WRITE  #56H      // set EEPROM mode → reserve (finish programming)
WRITE  #F0H      // set RE FLAG 000 → INSTRUCTION Bank 0
WRITE  #91H      // EM65570 reset
WRITE  #F4H      // set RE FLAG 100 → INSTRUCTION Bank 4
WRITE  #A1H      // set NIB1~NIB0=01 → read CV5~CV4
WRITE  #50H      // set EEPROM operating mode → reading; read data
                    from EEPROM to the CV5~CV4 registers
DELAY  >10 uS    // wait >10 uS to finish reading
WRITE  #56H      // set EEPROM mode → reserve (finish reading data
                    from EEPROM to the CV5~CV4 registers)
WRITE  #A0H      // set NIB1~NIB0=00 → read CV3~CV0
WRITE  #50H      // set EEPROM operating mode → reading; read data
                    from EEPROM to the CV3~CV0 registers
DELAY  >10 uS    // wait >10 uS to finish reading
WRITE  #56H      // set EEPROM mode → reserve (finish reading data
                    from EEPROM to the CV3~CV0 registers)
```

NOTE

- *When setting CV5~CV0, you must set CV5~CV4 (upper nibble registers) first, then set CV3~CV0 (lower nibble registers), and then start to program.*
- *The programming sequence of CV5~CV4 and CV3~CV0 is not restricted.*

■ **Read**

```
WRITE  #F4H     // set RE FLAG 100 → INSTRUCTION Bank 4
WRITE  #A3H     // set NIB1~NIB0=11 → read Extension Command
WRITE  #50H     // set EEPROM operating mode → reading; read data
                   from EEPROM
DELAY  >10 uS   // wait >10 uS to finish reading
WRITE  #56H     // set EEPROM mode → reserve (finish reading data
                   from EEPROM
WRITE  #A2H     // set NIB1~NIB0=10 → read Extension Command
WRITE  #50H     // set EEPROM operating mode → reading; read data
                   from EEPROM
DELAY  >10 uS   // wait >10 uS to finish reading
WRITE  #56H     // set EEPROM mode → reserve (finish reading data
                   from EEPROM
WRITE  #A1H     // set NIB1~NIB0=01 → read CV5~CV4
WRITE  #50H     // set EEPROM operating mode → reading; read data
                   from EEPROM to the CV5~CV4 registers
DELAY  >10 uS   // wait >10 uS to finish reading
WRITE  #56H     // set EEPROM mode → reserve (finish reading data
                   from EEPROM to the CV5~CV4 registers)
WRITE  #A0H     // set NIB1~NIB0=00 → read CV3~CV0
WRITE  #50H     // set EEPROM operating mode → reading; read data
                   from EEPROM to the CV3~CV0 registers
DELAY  >10 uS   // wait >10 uS to finish reading
WRITE  #56H     // set EEPROM mode → reserve (finish reading data
                   from EEPROM to the CV3~CV0 registers)
```

NOTE

When reading from CV5~CV0, you must read the EEPROM data to CV5~CV4 (upper nibble register) first, then read the EEPROM data to CV3~CV0 (lower nibble registers).

■ **Erase**

```
WRITE  #F4H      // set RE FLAG 100 → INSTRUCTION Bank 4
WRITE  #A1H      // set NIB1~NIB0=01 → erase CV5~CV4
WRITE  #54H      // set EEPROM operating mode → erasing; EEPROM
                    power is from internal V0
DELAY > 4 MS     // wait > 4 ms to finish erasing
WRITE  #56H      // set EEPROM mode → reserve (finish erasing)
WRITE  #A0H      // set NIB1~NIB0=00 → erase CV3~CV0
WRITE  #54H      // set EEPROM operating mode → erasing; EEPROM
                    power is from internal V0
DELAY > 4 MS     // wait > 4 ms to finish erasing
WRITE  #56H      // set EEPROM mode → reserve (finish erasing)
WRITE  #F0H      // set RE FLAG 000 → INSTRUCTION Bank 0
WRITE  #91H      // EM65570 reset
WRITE  #F4H      // set RE FLAG 100 → INSTRUCTION Bank 4
WRITE  #A1H      // set NIB1~NIB0=01 → read CV5~CV4
WRITE  #50H      // set EEPROM operating mode → reading; read data
                    from EEPROM to the CV5~CV4 registers
DELAY  >10 uS    // wait >10 uS to finish reading
WRITE  #56H      // set EEPROM mode → reserve (finish reading data
                    from EEPROM to the CV5~CV4 registers)
WRITE  #A0H      // set NIB1~NIB0=00 → read CV3~CV0
WRITE  #50H      // set EEPROM operating mode → reading; read data
                    from EEPROM to the CV3~CV0 registers
DELAY  >10 uS    // wait >10 uS to finish reading
WRITE  #56H      // set EEPROM mode → reserve (finish reading data
                    from EEPROM to the CV3~CV0 registers)
```

NOTE

CV5~CV0 should be equal to 1111 after erasing

7.21 Partial Display Function

The EM65570 has the partial display function, which can display a part of the graphic display area. This function is used to set lower bias ratio, lower boost step, and lower LCD drive voltage. When setting the partial display function, the EM65570 consumes less power. Partial display function is most suitable for clock indication or calendar indication when portable equipment is on stand-by.

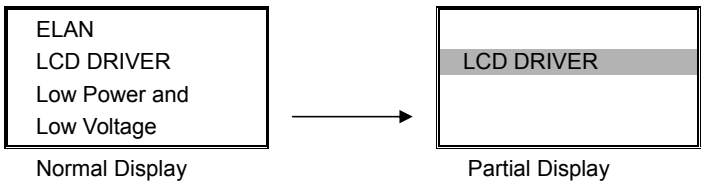


Figure 7-19 Partial Display Block Diagram

When using the partial display function, it is necessary to keep the following sequence.

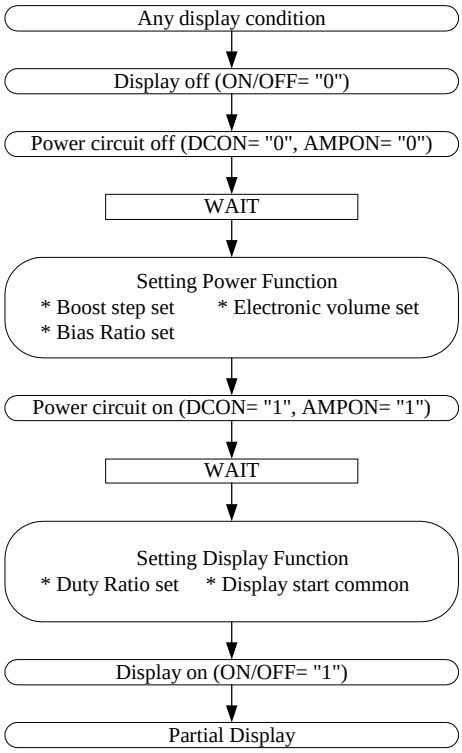


Figure 7-20 Partial Display Function Sequential Flow Diagram

Select a display duty ratio for the partial display from 1/10 to 1/68 using the DS (LCD duty ratio) register. Set the most suitable values for the LCD drive bias ratio, LCD drive voltage, electronic volume, the number of boosting steps, and others according to the actual LCD panel and the selected duty ratio in use.

7.22 Discharge Circuit

The EM65570 has a built-in the discharge circuit, which discharges electricity from capacitors to obtain stable power sources (V0~V4). The discharge circuit is valid when the DIS register is set to "1." When the built-in power supply is used, be sure to set DIS="1" after the power source is turned off (DCON, AMPON)=(0, 0).

CAUTION!!!

Do NOT turn on both the built-in power source and the external power source (V0~V4, VOUT) while DIS ="1."

7.23 Scroll Function

This function specifies the section of screen for scrolling. It sets the scroll top address, scroll bottom address, scroll specified address, scroll mode of the area scrolling, and scroll start address. Note that the scroll top address should be smaller than the scroll bottom address, i.e.;

0 <= scroll top address, scroll bottom address, scroll specified address <= 67;
scroll top address <= scroll start address <= scroll bottom address.

■ **Example:**

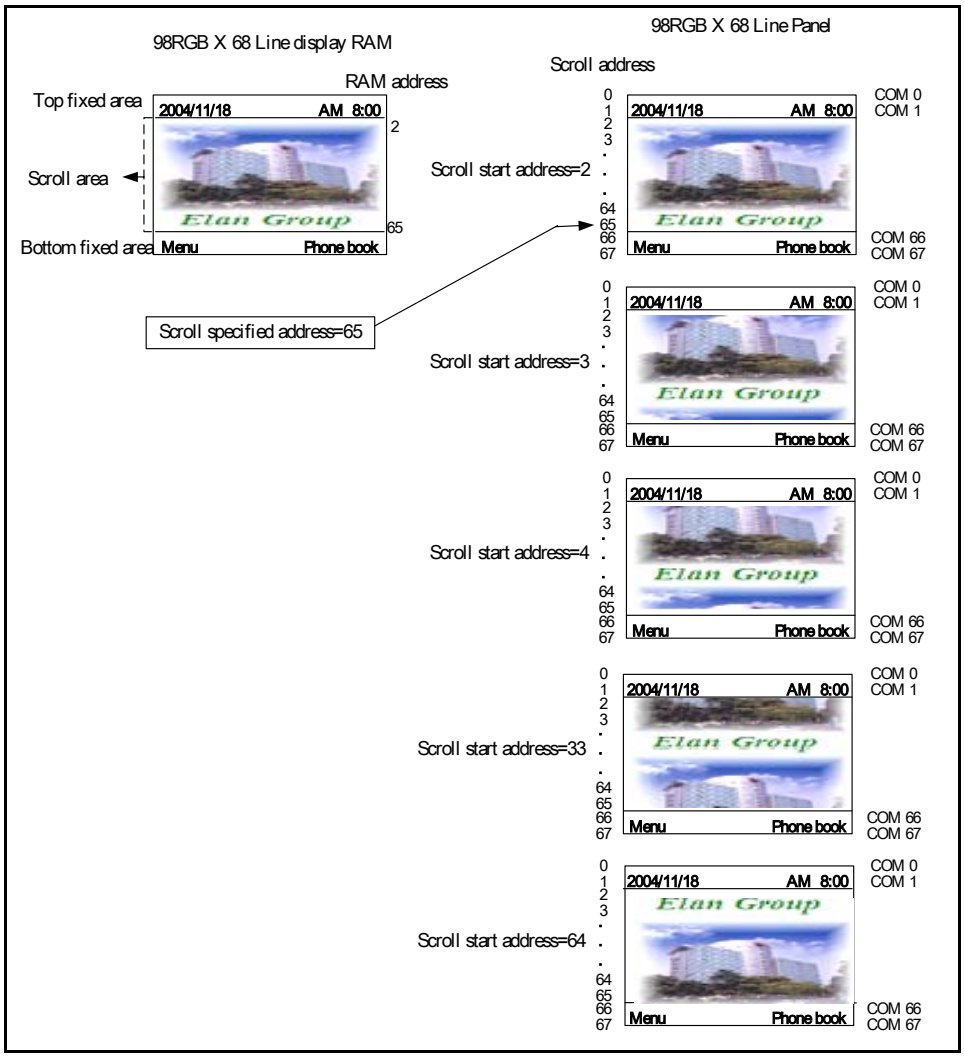


Figure 7-21 An Example of Scroll Function Display vs. Address Values

■ **Sample Code:**

```
------------set duty ratio=1/68-----------------------------------------
            WRITE 0xF0     //Bank 0
            WRITE 0xAF     //duty=1/68
------------scroll function setting-------------------------------------
            WRITE 0xF5     //Bank 5
            WRITE 0x10     //Scroll top address(up nibble)
            WRITE 0x02     //Scroll top address(low nibble)
            WRITE 0x34     //Scroll bottom address(up nibble)
```

```
            WRITE 0x21     //Scroll bottom address(low nibble)
            WRITE 0x54     //Scroll specified address(up nibble)
            WRITE 0x41     //Scroll specified address(low nibble)
            WRITE 0x80     //Center scroll mode
------------scroll start-------------------------------------------------
            MOV  A, #2
            MOV  INDEX1, A
            LOOP1:
            WRITE 0x70
            WRITE 0x60 + INDEX1
            INC_INDEX_1:
            INC  INDEX1
            MOV  A, INDEX1
            JLE  A, #15, LOOP1

            MOV  A, #1
            MOV  INDEX2, A
            LOOP2:
            MOV  A, #0
            MOV  INDEX1, A
            LOOP3:
            WRITE 0x70 + INDEX2
            WRITE 0x60 + INDEX1
            INC_INDEX_2:
            INC  INDEX1
            MOV  A, INDEX1
            JLE  A, #15, LOOP3
            INC  INDEX2
            MOV  A, INDEX2
            JLE  A, #3, LOOP2

            MOV  A, #0
            MOV  INDEX1, A
            LOOP4:
            WRITE 0x74
            WRITE 0x60 + INDEX1
            INC_INDEX_3:
            INC  INDEX1
            MOV  A, INDEX1
            JLE  A, #1, LOOP4
```

7.23.1 Settings Scrolling Data Area in RAM

Set the scroll top address and scroll bottom address to define an area of scrolling data in RAM

- **Example:**

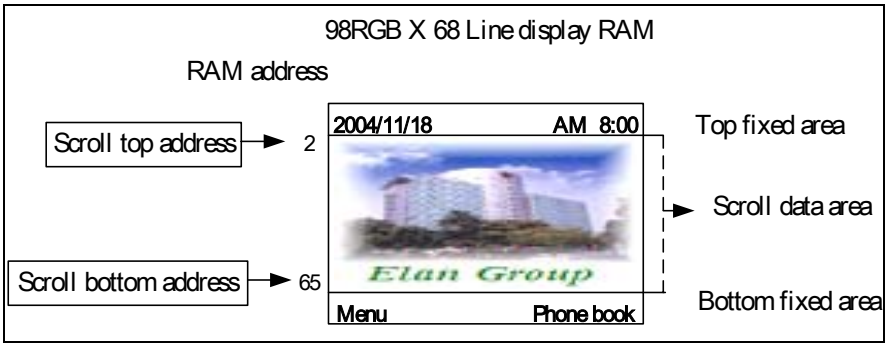


Figure 7-22a An Example of Setting Scrolling Data Area in RAM

Next, set the scroll specified address according to the panel size and duty selection to specify the address to which to jump relative to the scroll bottom address. Then display the fixed bottom data area.

Note that the scroll specified address = scroll top address + panel scroll area – 1.

- **Example (160 x 128 Line panel; 1/32 duty, partial display):**

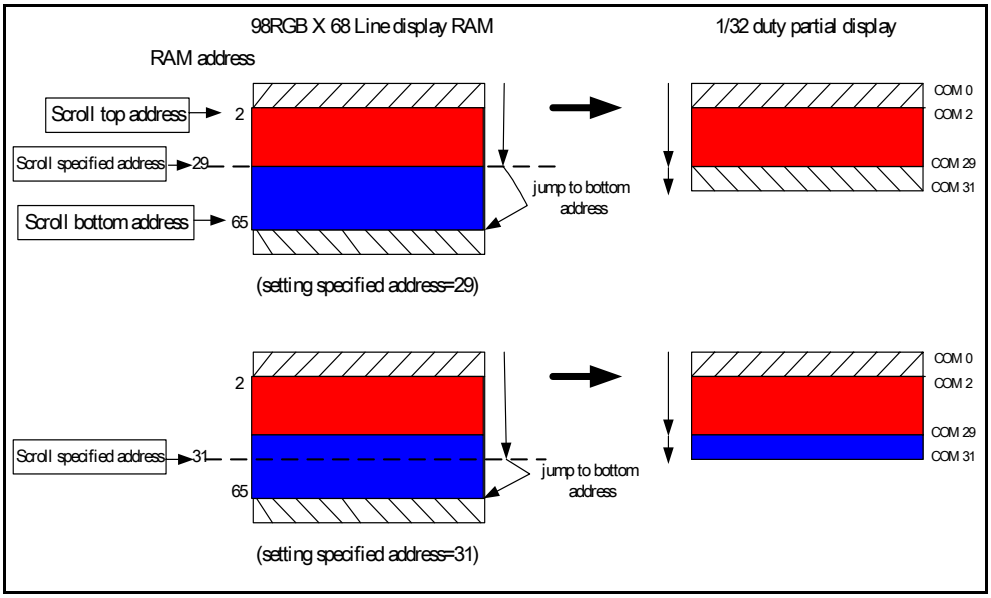


Figure 7-22b An Example of Scroll Bottom Address Settings in an Scrolling Area

NOTE

You must set the scroll top address, the scroll bottom address, the scroll specified address, and the scroll start address carefully when using the scroll function. If there is any error, the scrolling result will be inaccurate. Follow the guidelines shown below:

- *Scroll top address <= Scroll bottom address*
- *Scroll specified address = Scroll top address + panel scroll area – 1*
- *Scroll top address <= Scroll start address <= Scroll bottom address*

7.24 Initialization

Set the RESB pin to "L" to initialize the EM65570. Normally, the RESB pin is initialized together with MPU by connecting to the reset pin of MPU. When power ON, set RESB="L".

■ **65K color mode**

ITEM	Initial Value
Display RAM	Not fixed
X Address	00H set
Y Address	00H set
Display starting common	Set at the first common (0H)
Display ON/OFF	Display OFF
Display Normal/Reverse	Normal
Display duty	1/68
n-line alternated	Every frame unit
(BF1,BF0)	(0,0)
Common shift direction	COM0 → COM67
Increment mode	Increment OFF
Data SWAP Mode	OFF
Register in electronic volume	(0,0,0,0,0,0,0)
Power Supply	OFF
Display mode	65K color mode
Bias ratio	1/9 bias
Booster	6 times
Gradation LSB	0
RAM access data length	8-bits mode
Discharge Register	0

7.25 Safety Measures when Switching Power ON and OFF

The high current that may occur when a voltage is supplied to the LCD driver power supply while the system power supply is floating, could permanently damage the LSI. Hence, the precautionary actions as detailed below should be taken into considerations seriously when switching power on and off.

7.25.1 When Using the External Power Supply

■ **Power ON Proper Sequence:**

1) Logic system (VDD) power ON, perform a reset operation
2) Supply the external LCD drive voltage to the corresponding pins (V0, V1, V2, V3 and V4)

■ **Power OFF Proper Sequence:**

1) Set the HALT register to "1" or perform a reset operation
2) Cut off external LCD drive voltage
3) Logic system (VDD) power OFF

NOTE

Connect the serial resistor (50 to 100Ω) or fuse to the LCD drive power V0 or VOUT (when using the internal voltage conversion circuit) of the system as a current limiter. In addition, set a suitable resister value of the resistor depending on the quality of the LCD display.

7.25.2 When Using the Built-in Power Supply

■ **Power ON Proper Sequence:**

1) Logic system (VDD) power ON
2) Booster circuit system (VEE) power ON
3) Perform a reset operation and enable the booster and voltage conversion circuit.

NOTE

If the VDD and VEE voltages do NOT have the same potential, the logic system (VDD) is automatically powered on first.

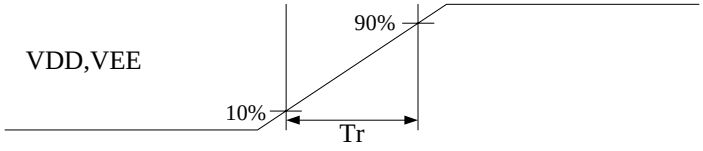
■ **Power OFF Proper Sequence:**

1) Set the HALT register to "1" or perform a reset operation
2) Booster circuit system (VEE) power OFF
3) Logic system (VDD) power OFF

If VDD and VEE do NOT have the same potential, cut off VEE first. After the VEE, VOUT, V0, V1, V2, V3, and V4 voltages are below the LCD ON voltage (threshold voltage when the Liquid Crystal is turned on), power off the logic system (VDD).

7.25.3 Power Supply Rising Time

Although there is no constraint on the rising time of the power supply, the Tr (rising time) as illustrated below is recommended for practical applications.



Item	Recommended Rising Time (Tr)	Applicable Power
Tr	30μS ~ 10ms*	VDD, VEE

* The rising time is the time between 10% adnd 90% of VDD, VEE

Figure 7-23 Recommended Rising Time (Tr) for Practical Application

7.26 Example of Setting Registers

7.26.1 Initialization

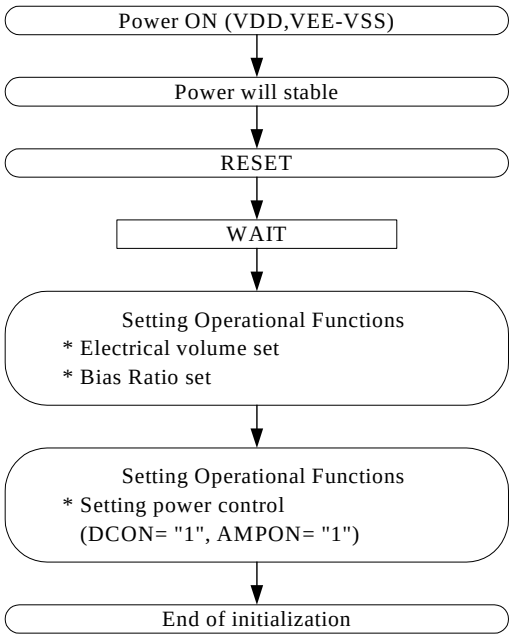


Figure 7-24a Initialization Register Setting Sequential Flow

7.26.2 Display Data

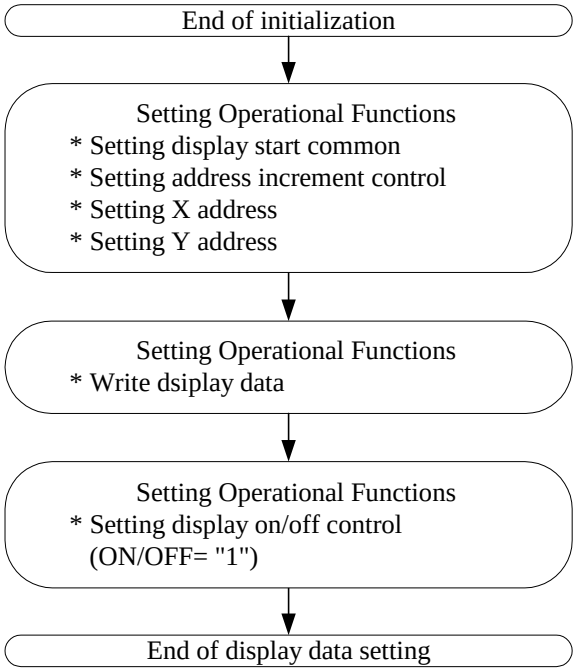


Figure 7-24b Display Data Register Setting Sequential Flow

7.26.3 Power OFF

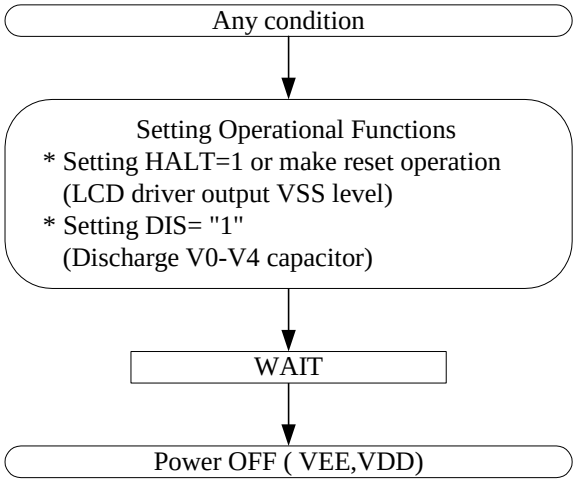


Figure 7-24c Power Off Register Setting Sequential Flow

8 Control Registers

8.1 Control Register

8.1.1 Control Register Table (Bank 0)

Control Register		Pins (for 80-Family) & Bank							Address & Code								Function
		CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
X Address (Lower nibble)	[0H]	0	1	0	1	0	0	0	0	0	0	0	AX3	AX2	AX1	AX0	Set of X direction Address in display RAM
X Address (Upper Nibble)	[1H]	0	1	0	1	0	0	0	0	0	0	1	AX7	AX6	AX5	AX4	
Y Address (Lower Nibble)	[2H]	0	1	0	1	0	0	0	0	0	1	0	AY3	AY2	AY1	AY0	Set of Y direction Address in display RAM
Y Address (Upper Nibble)	[3H]	0	1	0	1	0	0	0	0	0	1	1	*	AY6	AY5	AY4	
n-line Alternation (Lower Nibble)	[4H]	0	1	0	1	0	0	0	0	1	0	0	N3	N2	N1	N0	Set the number of alternated reverse line
n-line Alternation (Upper Nibble)	[5H]	0	1	0	1	0	0	0	0	1	0	1	*	N6	N5	N4	
Display Control (1)	[6H]	0	1	0	1	0	0	0	0	1	1	0	SHIFT	65K	ALLON	ON/OFF	SHIFT: Select common shift direction 65K: Select 65K gradation ALLON: All display ON ON/OFF: Display ON/OFF control
Display Control (2)	[7H]	0	1	0	1	0	0	0	0	1	1	1	*	REV	NLIN	SWAP	REV: Display normal/reverse NLIN: n line reverse control SWAP: Display data swapping
Increment Control	[8H]	0	1	0	1	0	0	0	1	0	0	0	WIN	AIM	AYI	AXI	WIN: Select window. AIM: Select increment mode AYI: Y increment, AXI: X increment
Power Control	[9H]	0	1	0	1	0	0	0	1	0	0	1	AMPON	HALT	DCON	ACL	AMPON: Internal AMP. ON HALT: Power saving DCON: Boosting circuit ON ACL: Resetting
LCD Duty Ratio	[AH]	0	1	0	1	0	0	0	1	0	1	0	DS3	DS2	DS1	DS0	Set LCD drive duty ratio
Booster	[BH]	0	1	0	1	0	0	0	1	0	1	1	0	VU2	VU1	VU0	Set number of boosting step for booster circuit
Bias Ratio Control	[CH]	0	1	0	1	0	0	0	1	1	0	0	*	B2	B1	B0	Set bias ratio for LCD driving voltage
Register Access Control	[FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test, must be set to "0" RE: set register bank number

NOTE: *Address for the control register are enclosed in brackets [ ].*

* *Don't Care*

8.1.2 Control Register Table (Bank 1)

Control Register		Pins (for 80-Family) & Bank							Address & Code								Function
		CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Display Start Common (Lower Nibble)	[0H]	0	1	0	1	1	0	1	0	0	0	0	SC3	SC2	SC1	SC0	Set Common Driver Start Line
Display Start Common (Upper Nibble)	[1H]	0	1	0	1	1	0	1	0	0	0	1	*	*	*	SC4	
Temperature Compensation	[2H]	0	1	0	1	1	0	1	0	0	1	0	*	*	TCS1	TCS0	Temperature compensation set
RAM Data Length Set	[3H]	0	1	0	1	1	0	1	0	0	1	1	C256	GLSB	ABS	WLS	Set data length on RAM access 8-bit access or 16-bit access
RAM Data Writing Select Control	[4H]	0	1	0	1	1	0	1	0	1	0	0	WBS	RD WS2	RD WS1	RD WS0	Set RAM data writing mode
Electronic Volume (Lower Nibble)	[5H]	0	1	0	1	1	0	1	0	1	0	1	DV3	DV2	DV1	DV0	Set electronic volume register
Electronic Volume (Upper Nibble)	[6H]	0	1	0	1	1	0	1	0	1	1	0	*	DV6	DV5	DV4	
Register Read Control	[7H]	0	1	0	1	1	0	1	0	1	1	1	RA3	RA2	RA1	RA0	Set register address for read
Select RF	[8H]	0	1	0	1	1	0	1	1	0	0	0	RF3	RF2	RF1	RF0	Select RF ratio of OSC circuit
Extended Power Control	[9H]	0	1	0	1	1	0	1	1	0	0	1	BF1	BF0	1	DIS	Set booster frequency Discharge capacitances of V0~V4
Window X end address (Lower nibble)	[AH]	0	1	0	1	1	0	1	1	0	1	0	EX3	EX2	EX1	EX0	Set X end address for window function
Window X End Address (Upper Nibble)	[BH]	0	1	0	1	1	0	1	1	0	1	1	EX7	EX6	EX5	EX4	
Window Y End Address (Lower Nibble)	[CH]	0	1	0	1	1	0	1	1	1	0	0	EY3	EY2	EY1	EY0	Set Y end address for window function
Window Y End Address (Upper Nibble)	[DH]	0	1	0	1	1	0	1	1	1	0	1	*	EY6	EY5	EY4	
Regulator Multiple Ratio Control	[EH]	0	1	0	1	1	0	1	1	1	1	0	*	RM2	RM1	RM0	Set regulator multiple ratio
Register Access Control	[FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test, Must set to "0" RE: set register bank number

NOTE: *Address for the control register are enclosed in brackets [ ].*

* *Don't Care*

NOTE

Use of Bank 2 and Bank 3 is prohibited.

8.1.3 Control Register Table (Bank 4)

Control Register	Pins (for 80-Family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Start Address for Line Reverse (Lower Nibble) [0H]	0	1	0	1	1	0	1	0	0	0	0	LS3	LS2	LS1	LS0	Set start line for line reverse display
Start Address for Line Reverse (Upper Nibble) [1H]	0	1	0	1	1	0	1	0	0	0	1	*	LS6	LS5	LS4	
End Address for Line Reverse (Lower Nibble) [2H]	0	1	0	1	1	0	1	0	0	1	0	LE3	LE2	LE1	LE0	Set end line for line reverse display
End Address for Line Reverse (Upper Nibble) [3H]	0	1	0	1	1	0	1	0	0	1	1	*	LE6	LE5	LE4	
Line Reverse & Burst RAM Write Control [4H]	0	1	0	1	1	0	1	0	1	0	0	*	BST	BT	LREV	Line reverse & burst RAM write control
EEPROM Mode Select [5H]	0	1	0	1	1	0	1	0	1	0	1	*	M1	M0	0	EEPROM mode select
Vop Calibration Offset (Lower Nibble) [6H]	0	1	0	1	1	0	1	0	1	1	0	CV3	CV2	CV1	CV0	Vop calibration offset select
Vop calibration offset (Upper Nibble) [7H]	0	1	0	1	1	0	1	0	1	1	1	*	*	CV5	CV4	
EEPROM address Select [AH]	0	1	0	1	1	0	1	1	0	1	0	*	*	NIB1	NIB0	Select EEPROM address
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test, Must set to "0" RE: set register bank number

NOTE: *Address for the control register are enclosed in brackets [ ].*

* *Don't Care*

NOTE

Use of Control Registers [8H], [9H], [BH] ~ [EH] is prohibited.

8.1.4 Control Register Table (Bank 5)

Control Register	Pins (for 80-Family) & Bank							Address & Code								Function
	CSB	RS	WRB	RDB	RE2	RE1	RE0	D7	D6	D5	D4	D3	D2	D1	D0	
Scroll top address (Lower nibble) [0H]	0	1	0	1	1	0	1	0	0	0	0	STA3	STA2	STA1	STA0	Set scroll top address
Scroll top address (Upper nibble) [1H]	0	1	0	1	1	0	1	0	0	0	1	*	STA6	STA5	STA4	
Scroll bottom address (Lower nibble) [2H]	0	1	0	1	1	0	1	0	0	1	0	SBA3	SBA2	SBA1	SBA0	Set scroll bottom address
Scroll bottom address (Upper nibble) [3H]	0	1	0	1	1	0	1	0	0	1	1	*	SBA6	SBA5	SBA4	
Scroll specified address (Lower nibble) [4H]	0	1	0	1	1	0	1	0	1	0	0	SSA3	SSA2	SSA1	SSA0	Set scroll specified address
Scroll specified address (Upper nibble) [5H]	0	1	0	1	1	0	1	0	1	0	1	*	SSA6	SSA5	SSA4	
Scroll start address (Lower nibble) [6H]	0	1	0	1	1	0	1	0	1	1	0	SAY3	SAY2	SAY1	SAY0	Set scroll start address
Scroll start address (Upper nibble) [7H]	0	1	0	1	1	0	1	0	1	1	1	*	SAY6	SAY5	SAY4	
Scroll mode select [8H]	0	1	0	1	1	0	1	1	0	0	0	*	*	SM1	SN0	Scroll mode select
Register Access Control [FH]	0	1	0	1	0/1	0/1	0/1	1	1	1	1	TST0	RE2	RE1	RE0	TST0: for LS1 test, Must set to "0" RE: set register bank number

NOTE: *Address for the control register are enclosed in brackets [ ].*

* *Don't Care*

8.2 Functions of Control Registers

The EM65570 has many control registers. When accessing the control registers, the upper nibble of the data bus (D7~D4) represents the register address while the lower nibble of the data bus (D3~D0) represents data. The following figure shows an access example. The Pins CSB, RS, RDB, & WRB) settings are for the 80-family MPU interface. Only the setting of the terminals RDB & WRB are different when it is accessed by the 68-family MPU.

■ **Example (X Address):**

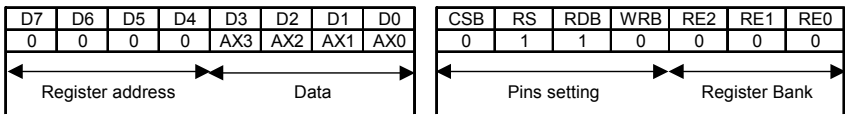


Figure 8-1 An Example of Accessing the Control Registers

When writing to the control register, it is used directly by addressing D7~D4 of the data bus. When reading, you must first set the RA register for the specific register address before you can read specific register. Therefore, a 2-step procedure is required to perform a read register operation. After reading, the specific register will output to D3~D0 of the data bus. All nibbles, except D3~D0, of the data bus are all "H." Access to undefined register address area is prohibited. When RS is "L," all read/write operations are accessed to display RAM. Then the data bus does not include the register address. When writing, D3~D0 data is written to the register designated at D7~D4 on the rising edge of the WRB signal. When reading, the register can output to data bus during RDB active period. The control register and display RAM have equal access sequence

8.2.1 X Address Register (AX)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	AX3	AX2	AX1	AX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX3, AX2, AX1, AX0} = 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	AX7	AX6	AX5	AX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AX7, AX6, AX5, AX4} = 0H, read address: 1H)

The AX register is set to the X-direction address of display RAM. In data setting, command is divided into lower and upper sections at 4-bit of data each in order to accommodate the required 8-bit of total data.

8.2.2 Y Address Register (AY)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	AY3	AX2	AY1	AY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AY3, AY2, AY1, AY0} =0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	AY6	AY5	AY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

* *Don't Care*

(At the time of reset: {AY6, AY5, AY4} =0H, read address: 3H)

The AY register is set to the Y-direction address of display RAM. In data setting, command is divided into lower and upper sections at 4-bit and 3-bit of data respectively in order to accommodate the required 7-bit total data. 00H to 43H are applicable to the values for AY6 to AY0, but 44H to FFH are not applicable.

8.2.3 n Line Alternate Register (N)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	N3	N2	N1	N0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {N3, N2, N1, N0} =0H, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	N6	N5	N4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

* *Don't Care*

(At the time of reset: {N6, N5, N4} =0H, read address: 5H)

A number of the reverse lines in the LCD alternate drive is required in setting the register. This number of lines is limited to between 2 and 67 lines. The values set up by the alternate register will be enabled when the NLIN control bit is "1." When the NLIN control bit is "0," the alternate drive waveform reverses when each frame is generated.

N6	N5	N4	N3	N2	N1	N0	Line Address
0	0	0	0	0	0	0	-
0	0	0	0	0	0	1	2
			:				:
			:				:
1	0	0	0	0	1	1	67

■ **NLIN = "0" (with 1/68 DUTY Display):**

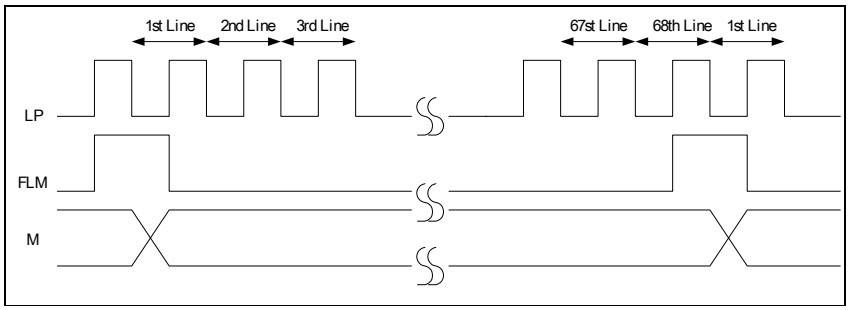


Figure 8-2a NLINE = "0" Alternate Timing Diagram

■ **NLIN = ”1”**

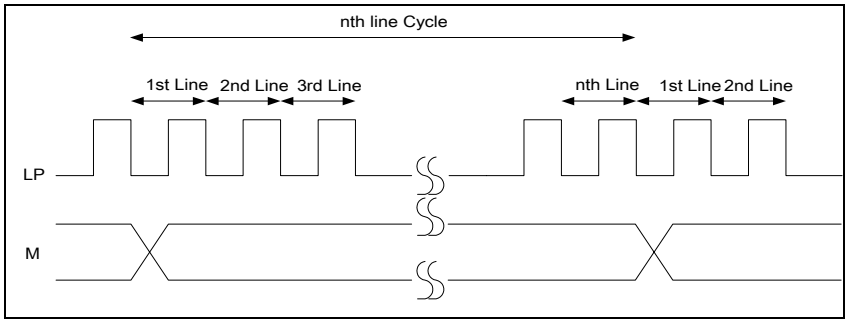


Figure 8-2b NLINE = “1” Alternate Timing Diagram

8.2.4 Display Control (1) Register

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	SHIFT	65K	ALL ON	ON/ OFF

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {SHIFT, 65K, ALLON, ON/OFF} = 4H, read address: 6H)

Various display control is set up as follows**:**

■ **ON/OFF**

To turn ON/OFF the display control–
ON/OFF = “0”**:** Display OFF
ON/OFF = “1”**:** Display ON

■ **ALLON**

Regardless of the display data, all is ON.
This control has priority over display normal/reverse commands.
ALLON = “0”**:** Normal display
ALLON = “1”**:** All display are lit

■ **65K**

Select 65K gradation display
65K=”0”**:** 4096 or 256 gradation display, decided by C256 control bit.
65K=”1”**:** 65K gradation display mode.

■ **SHIFT**

Select the shift direction of the display scanning data in the common driver output.
SHIFT = “0”**:** COM0→COM67 shift-scan
SHIFT = “1”**:** COM67→COM0 shift-scan

8.2.5 Display Control (2) Register

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	REV	NLIN	SWAP

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {REV, NLIN, SWAP} = 0H, read address: 7H)

Various display control is set up as follows**:**

■ **REV**

Sets LCD light ON/OFF control in combination with the display RAM data high/low status.

REV ="0"**:** When the RAM data is at "H," LCD is at ON voltage (normal)
When the RAM data is at "L," LCD is at OFF voltage (normal)

REV ="1"**:** When the RAM data is at "H," LCD is at OFF voltage (reverse)
When the RAM data is at "L," LCD is at ON voltage (reverse)

■ **NLIN**

The NLIN controls the n-line alternate drive ON/OFF.

NLIN = "0"**:** n-line alternate drive OFF. In each frame, the alternated signals (M) are reversed.

NLIN = "1"**:** n-line alternate drive ON. According to data set up in the n-line alternated register, the alternation is made.

■ **SWAP**

Swap the write data bit mode when writing data to display RAM.

SWAP = "0"**:** Normal mode.

SWAP = "1"**:** During data writing, exchange the R and B definitions of Segment outputs.

8.2.6 Increment Control Register Set

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	WIN	AIM	AYI	AXI

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the tine of reset: {WIN, AIM, AYI, AXI} = 0H, read address: 8H)

This register controls the increment mode and window function when accessing display RAM. The increment operation of the AX and AY registers is controlled by the AIM, AYI and AXI registers setting and by every write or every read access to display RAM. The AY register directly connects to display RAM as the Y address. The AX register connects to the address converter and the resulting output to display RAM as the X address in the auto increment mode. The AX and AY register are incremented, but the X and Y addresses are not incremented directly.

To set this control register, the increment operation of the address can be made without setting successive addresses for writing or reading data to display RAM from MPU.

The WIN register is used for window function control.

WIN="0"**:** Normal RAM access

WIN="1"**:** Window function access

When using the window function to access RAM, you should set the following registers before accessing.
WIN="1", AXI="1", AYI="1"
X Address, Y Address, Window X End Address, Window Y End Address

Moreover, the following address condition must be met.
Window end X address ≧ Window start X address
Window end Y address ≧ Window start Y address

The increment control of the X and Y addresses by AIM, AYI, and AXI registers are as follows.

AIM	Address Increment Timing
0	When writing to display RAM or reading from display RAM This is effective when accessing successive address area
1	Only when writing to display RAM This is used in the case of Read Modify Write

AYI	AXI	Select Address Increment Operation	Remarks
0	0	Address is not incremented	(1)
0	1	X-Address is incremented	(2)
1	0	Y-Address is incremented	(3)
1	1	X and Y both are incremented	(4)

NOTES: 1. Regardless of AIM value, the AX and AY registers do not increment
2. The X address automatically changes according to the AIM setting

Transition of AX Register	Transition of X Address
00H→01H→.....→maxH*	Same as AX register

3. The Y address automatically changes according to the AIM setting

Transition of AY Register	Transition of Y Address
00H→01H→.....→ 43H	Same as AY register

4. Change the X and Y address accordingly to the AIM setting. When the X address exceed maxH*, Y address increment occurs

Transition of AX and AY Register	Transition of X and Y Address
AX: 00H → 00H → – – → maxH* AY: When each AX exceeds maxH,* AY increments 00H → 00H → – – → 43H	Same as AX and AY register

*****maxH: The maximum internal X-address in each access mode*

5. The following shows address increment in window function access.

Transition of AX and AY Register	Transition of X and Y Address
AX: START Address → START Address+1 → _ _ → END Address AY: When each AX exceed AE, increment AY START Address → START Address+1 → _ _ → END Address	Same as AX and AY register

Under each operation mode, the following increment operation is performed**:**

- When gradation display mode and 8-bit access are selected, address is incremented as described above.
- When gradation display mode and 16-bit access are selected, the following increment processing occurs**:**
  1) Accessing the RAM after every two bytes are accessed.
  2) The X-addresses increments in the order of 00H, 01H,…2FH, and 30H.

8.2.7 Power Control Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	AMPON	HALT	DCON	ACL

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {AMPON, HALT, DCON, ACL} = 0H, read address: 9H)

■ **ACL**

The internal circuit can be initialized as follows**:**
ACL = “0”**:** Normal operation
ACL = “1”**:** Initialization ON

When the reset operation begins internally after the ACL register is set to “1,” the ACL register is automatically cleared to “0.” The internal reset signal is generated with a clock (built-in oscillation circuit or CK input) for the display. Therefore, install at least two cycles for the WAIT period for the clock display. After the WAIT period elapsed, the next operation is processed.

■ **DCON**

Sets ON/OFF the internal booster circuit**:**
DCON = “0”**:** Booster circuit OFF
DCON = ”1”**:** Booster circuit ON

■ **HALT**

The power saving operating condition is set ON/OFF with this command.
HALT = "0"**:** Normal operation
HALT = "1"**:** Power-saving operation

When the power-saving state is set, the power consumption can be decreased to almost equal the standby power consumption.

The internal condition during power saving are as follows**:**

1) The oscillating circuit and power supply circuit are stopped.
2) The LCD drive is stopped, and output of the segment and common drivers are at VSS level.
3) The clock input from CK pin is forbidden.
4) The contents of Display RAM data are stored.
5) The operational mode stores the state of command executed before executing the power saving command.

■ **AMPON**

Sets the internal OP-AMP circuit block ON/OFF (voltage regulator, electronic volume, and voltage conversion circuit).
AMPON = "0"**:** The internal OP-AMP circuit is OFF
AMPON = "1"**:** The internal OP-AMP circuit is ON

8.2.8 LCD Duty (DS)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	DS3	DS2	DS1	DS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {DS3, DS2, DS1, DS0} = FH, read address: AH)

The DS register set and its corresponding LCD display width and duty**:**

DS3	DS2	DS1	DS0	Display Width and Duty
0	0	0	0	1/8 duty
0	0	0	1	1/12 duty
0	0	1	0	1/16 duty
0	0	1	1	1/20 duty
0	1	0	0	1/24 duty
0	1	0	1	1/28 duty
0	1	1	0	1/32 duty
0	1	1	1	1/36 duty
1	0	0	0	1/40 duty
1	0	0	1	1/44 duty
1	0	1	0	1/48 duty
1	0	1	1	1/52 duty
1	1	0	0	1/56 duty
1	1	0	1	1/60 duty
1	1	1	0	1/64 duty
1	1	1	1	1/68 duty

Partial display can be made possible by setting an arbitrary duty ratio.

8.2.9 Booster Setup (VU)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	0	VU2	VU1	VU0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

(At the time of reset: {0,VU2,VU1,VU0} = 5H, read address: BH)

The booster steps set to VU register

VU2	VU1	VU0	Booster Operation
0	0	0	Booster disable (No operation)
0	0	1	2 times voltage output
0	1	0	3 times voltage output
0	1	1	4 times voltage output
1	0	0	5 times voltage output
1	0	1	6 times voltage output
1	1	0	Prohibit code
1	1	1	Prohibit code

8.2.10 Bias Sett ing Register (B)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	*	B2	B1	B0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	0

* Don'tCare

(At the time of reset: {B2, B1, B0} = 5H, read address**:** CH)

This register is used to set a bias ratio. A bias ratio can be selected from 1/4 to 1/9 by setting B2, B1, and B0.

B2	B1	B0	Bias
0	0	0	1/4 Bias
0	0	1	1/5 Bias
0	1	0	1/6 Bias
0	1	1	1/7 Bias
1	0	0	1/8 Bias
1	0	1	1/9 Bias

8.2.11 Register Access Control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	TST0	RE2	RE1	RE0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0/1	0/1	0/1

(At the time of reset: {TST0, RE2, RE1, RE0} = 0H, read address: FH)

Set the RE register to select the register bank number. To access each control register, set the RE register first.

The TST0 register is used to test LSI. Therefore this register must be set to "0"

8.2.12 Display Start Common

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	SC3	SC2	SC1	SC0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address=0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	*	*	SC4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

* *Don't Care*

(Read address=1H)

(At the time of reset:{SC4,SC3,SC2,SC1,SC0} = 0H)

The SC register sets the scanning start output of the common driver.

SC4	SC3	SC2	SC1	SC0	Display Starting Common	
					When SHIFT=0	When SHIFT=1
0	0	0	0	0	COM0~	COM67~
0	0	0	0	1	COM4~	COM63~
0	0	0	1	0	COM8~	COM59~
0	0	0	1	1	COM12~	COM55~
0	0	1	0	0	COM16~	COM51~
0	0	1	0	1	COM20~	COM47~
0	0	1	1	0	COM24~	COM43~
0	0	1	1	1	COM28~	COM39~
0	1	0	0	0	COM32~	COM35~
0	1	0	0	1	COM36~	COM31~
0	1	0	1	0	COM40~	COM27~
0	1	0	1	1	COM44~	COM23~
0	1	1	0	0	COM48~	COM19~
0	1	1	0	1	COM52~	COM15~
0	1	1	1	0	COM56~	COM11~
0	1	1	1	1	COM60~	COM7~
1	0	0	0	0	COM64~	COM3~

SHIFT="0": COM0 to COM67 shift-scan
SHIFT="1": COM67 down to COM0 shift-scan

8.2.13 Temperature Compensation Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	*	*	TCS1	TCS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

* Don'tCare

(At the time of reset:{ TCS1,TCS0 } = 0H, read address: 2H)

TCS1	TCS0	Temperature Compensation Slope
0	0	-0.05% per °C
0	1	-0.1% per °C
1	0	-0.15% per °C
1	1	-0.2% per °C

VREF (T) (Temperature compensation output voltage) is controlled by TCS1, TCS0, and previous environment temperature T.

$$V_{REF}(T) = V_{REF0}[(1 + TCS(T - 25^0C)]$$

- TCS is selected by TCS1 and TCS0
- VREF0 = 1.5V at 25°C

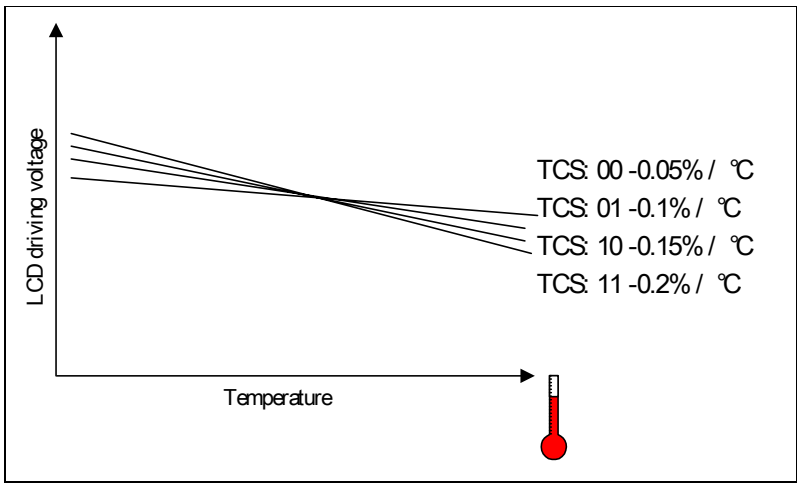


Figure 8-3 Temperature Compensation Slope

8.2.14 RAM Data Length Set

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	C256	GLSB	ABS	WLS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset**:** {C256, GLSB, ABS, WLS} = 0H, read address**:** 3H)

The WLS register selects data bus size for accessing from MPU.
WLS = "0"**:** The data bus size is 8-bit in width
WLS = "1"**:** The data bus size is 16-bit in width

When MPU accesses the control register using the 16-bit bus, high byte data is ignored.

■ **ABS**

ABS= "0"**:** normal mode
ABS= "1"**:** change corresponding bit from the input data bus

■ **GLSB**

In 256-color mode for segment driver of 4-gradation display, select 4 gradations from 8 gradations using the 2 bits written to the corresponding RAM area and the 1 bit supplemented by the gradation LSB circuit. Supplement the 1 bit of data by setting the gradation LSB register (GLSB).

Gradation LSB = "0"**:** Selects 0 as the LSB information on the RAM for the 4-gradation segment driver.

Gradation LSB = "1"**:** Selects 1 as the LSB information on the RAM for 4-gradation segment driver.

■ **C256**

C256= "0": 4096-color mode
C256= "1": 256-color mode

NOTE
When you use C256, you can NOT set 65K to 1.

8.2.15 RAM Data Writing Select Control

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	WBS	RDWS2	RDWS1	RDWS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {WBS, RDWS2, RDWS1, RDWS0} = 0H, read address: 4H)

The WBS bit selects the byte writing sequence while displaying RAM data.
WBS= 0**:** Write low byte first
WBS= 1**:** Write high byte first

The RDWS[2:0] selects the RAM data writing mode shown in the following figure.

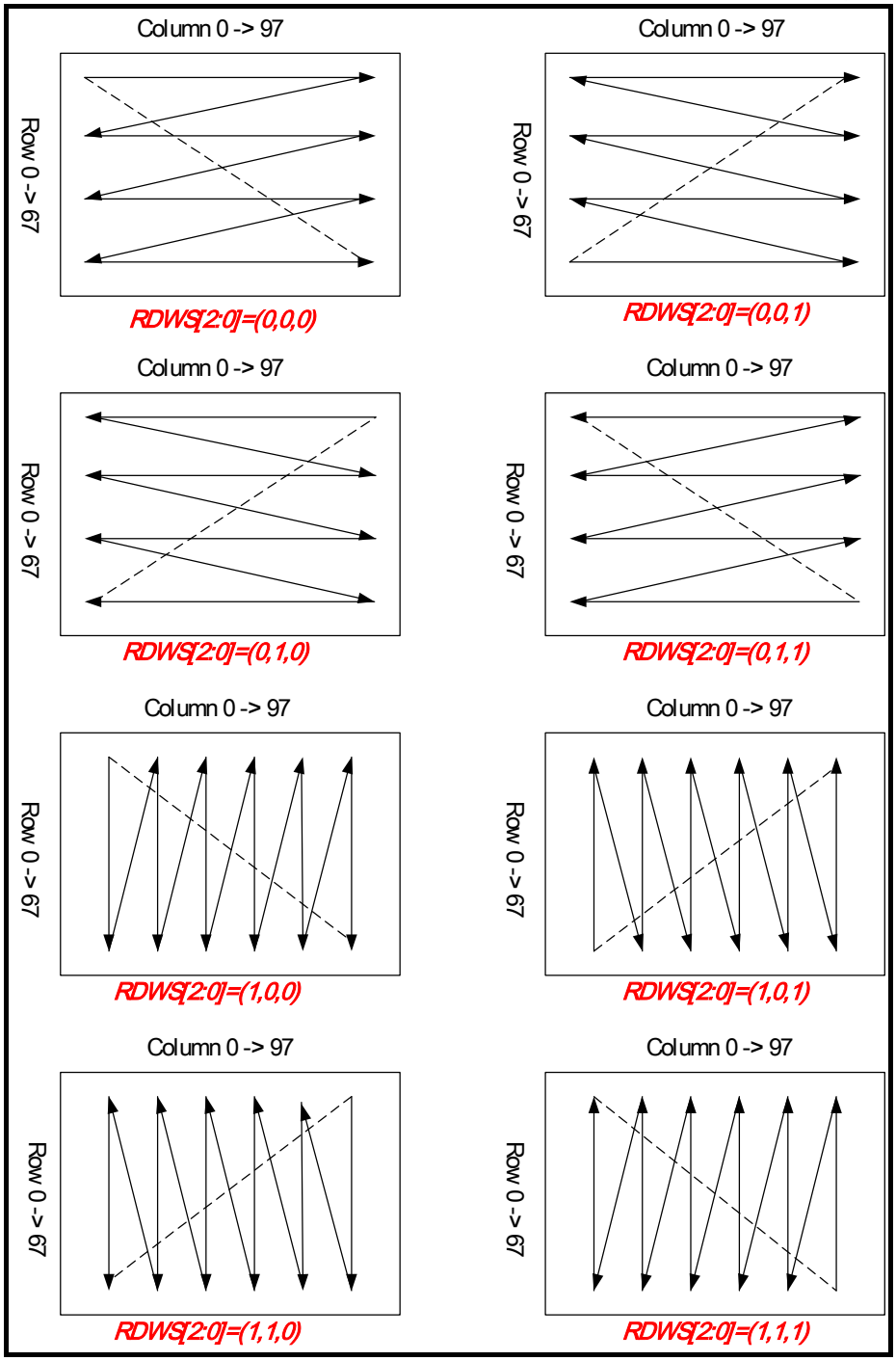


Figure 8-4 The RAM Data Writing Mode Selection by RDWS[2:0]

8.2.16 Electronic Volume Register

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	DV3	DV2	DV1	DV0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(Read address: 5H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	*	DV6	DV5	DV4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

* Don'tCare

(Read address: 6H)

(At the time of reset: {DV6~DV0} = 00H)

The DV register controls the VBA voltage.

DV6	DV5	DV4	DV3	DV2	DV1	DV0	Output Voltage
0	1	0	0	0	0	0	32
0	1	0	0	0	0	1	33
			:				:
1	0	1	1	1	1	1	95
1	1	0	0	0	0	0	96

The output voltage at VBA is specified by the following equation:

$$VBA = (1+ (M+offset)/381) * VREF$$

Where: ***M:*** *DV register value*

offset: *CV register value*

VREF: *temperature compensation output voltage*

The VBA range is from 1.5V to 2V at 25°C.

The LCD drive voltage V0 is determined by the VBA level and the RM register value as shown in the following equation:

$$V0 = VBA * N$$

N: *RM register value*

NOTE

When using EEPROM function (CV) to tune VBA offset, limit DV value to 32~96 to prevent getting incorrect VBA value due to (M+offset) overflow or underflow.

In order to prevent transient voltage generation when an electronic volume code is set, design the circuit in such a way that the set value is not reflected as a level immediately after the upper bits (DV6-DV4) of the set electronic code. The set value becomes valid only when the lower bits (DV3-DV0) of the electronic control volume code have also been set.

NOTE

When writing code to set the electronic volume register, you must set DV6~DV4 first, then followed by DV3~DV0 setting.

8.2.17 Internal Register Read Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	RA3	RA2	RA1	RA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {RA3, RA2, RA1, RA0} = 7H)

Use the RA register to specify the address for the register read operation. The EM65570 has many registers and register banks. Therefore, a 4-step operation is required to read the specific register.

1) Write 01H to the RE register for accessing the RA register
2) Write specific register address to the RA register
3) Write the specific register bank to the RE register
4) Read specific contents

8.2.18 Resistance Ratio of CR Oscillator

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	RF3	RF2	RF1	RF0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {RF3, RF2, RF1, RF0} = 0H, read address: 8H)

The RF registers control the resistance ratio of the CR oscillator. Therefore, the frame frequency will change the RF register settings.

When changing the RF register values, you need to check the LCD display quality.

RF3	RF2	RF1	RF0	Operation
0	0	0	0	Initial Resistance Ratio
0	0	0	1	0.72 times of initial Resistance Ratio
0	0	1	0	0.76 times of initial Resistance Ratio
0	0	1	1	0.8 times of initial Resistance Ratio
0	1	0	0	0.84 times of initial Resistance Ratio
0	1	0	1	0.88 times of initial Resistance Ratio
0	1	1	0	0.92 times of initial Resistance Ratio
0	1	1	1	0.96 times of initial Resistance Ratio
1	0	0	0	1.04 times of initial Resistance Ratio
1	0	0	1	1.08 times of initial Resistance Ratio
1	0	1	0	1.12 times of initial Resistance Ratio
1	0	1	1	1.16 times of initial Resistance Ratio
1	1	0	0	1.2 times of initial Resistance Ratio
1	1	0	1	1.24 times of initial Resistance Ratio
1	1	1	0	1.28 times of initial Resistance Ratio
1	1	1	1	Prohibit Code

8.2.19 Extended Power Control

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	BF1	BF0	1	DIS

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {DIS} = 0H, {BF1, BF0}=0H; read address: 9H)

The DIS register controls the capacitors (connected between the power supply V0-V4 for LCD drive voltage and VSS) discharge.

When using this register, refer to Section 7-22 (Discharge Circuit).
DIS = "0": Discharge OFF
DIS = "1": Discharge start

BF1~BF0: Select the operating frequency in the booster. When the boosting frequency is high, the driving ability of the booster becomes high, and the power consumption is increased. When you adjust the boosting frequency, you must take into considerations the external capacitors and the current consumption.

BF1	BF0	Operating Clock Frequency in the Booster
0	0	1.5K Hz * 8
0	1	1.5K Hz * 4
1	0	1.5K Hz * 2
1	1	1.5 K Hz

8.2.20 Window End X Address

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	EX3	EX2	EX1	EX0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {EX3, EX2, EX1, EX0} = 0H, read address: AH)

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	1	EX7	EX6	EX5	EX4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {EX7, EX6, EX5, EX4} = 0H, read address: BH)

The EX registers set the X direction end address for the window function.

8.2.21 Window End Y Address

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	EY3	EY2	EY1	EY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {EY3, EY2, EY1, EY0} = 0H, read address: CH)

D7	D6	D5	D4	D3	D2	D1	D0
1	1	0	1	*	EY6	EY5	EY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {EY6, EY5, EY4} = 0H, read address: DH)

The EY registers set the Y direction end address for the window function.

8.2.22 Regulator Multiple Ratio Control

D7	D6	D5	D4	D3	D2	D1	D0
1	1	1	0	*	RM2	RM1	RM0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	0	0	1

(At the time of reset: {RM2, RM1, RM0} = 5H, read address: EH)

Set the RM register to specify the booster step.

RM2	RM1	RM0	Regulator Multiple Ratio Control
0	0	0	3.0 times voltage output
0	0	1	3.6 times voltage output
0	1	0	4.5 times voltage output
0	1	1	5.0 times voltage output
1	0	0	5.5 times voltage output
1	0	1	6.0 times voltage output
1	1	0	7.0 times voltage output
1	1	1	8.0 times voltage output

8.2.23 Line Reverse Start Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	LS3	LS2	LS1	LS0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {LS3, LS2, LS1, LS0} = 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	LS6	LS5	LS4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

* Don'tCare

(At the time of reset: {LS6, LS5, LS4} = 0H, read address: 1H)

The LS registers set the line reverse start address under the following conditions:

00H ≦ LS ≦ 43H

LS ≦ LE

LE: *Line reverse end address*

8.2.24 Line Reverse End Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	LE3	LE2	LE1	LE0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {LE3, LE2, LE1, LE0} = 0H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	LE6	LE5	LE4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

* *Don't Care*

(At the time of reset: {LE6, LE5, LE4} = 0H, read address: 3H)

The LE registers set the line reverse end address under the following conditions:

00H ≦ LS ≦ 43H

LS ≦ LE

LS: *Line reverse start address*

8.2.25 Line Reverse Control

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	*	BST	BT	LREV

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

* *Don't Care*

(At the time of reset: {BST, BT, LREV} = 0H, read address: 4H)

The BST register controls the Fast Burst RAM write function
BST = "0": Burst RAM write function OFF
BST = "1": Burst RAM write function ON

The LREV registers control the line reverse display function.
LREV = "0": Normal display (not reversed)
LREV = "1": Line reverse display enabled

The area specified by the Line Reverse Start/End Register reverses the display. The reverse type is selected by the BT register.

When using the Line Reverse Display function, LS and LE registers must meet the following condition:

LS ≦ LE

The BT register controls the line reverse type. This is an option of the line reverse display function. This BT setting is only available when LREV="1"
BT = "0": Reverse display
BT = "1": Reverse display at each 32 frame.

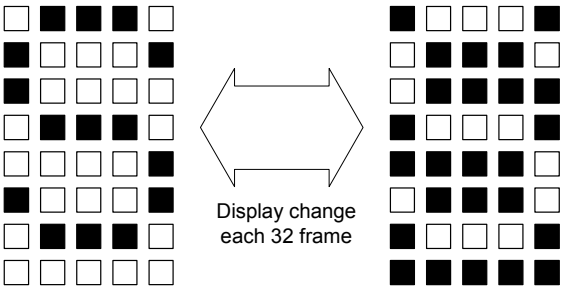


Figure 8-5a Blink Example (LREV = 1, BT = 1)

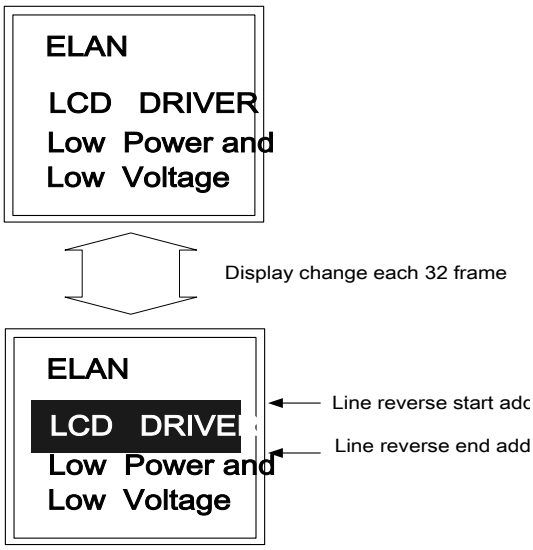


Figure 8-5b Blink Example (LREV = 1, BT = 1) Indicating Line Reverse Start/End Address Positions

8.2.26 EEPROM Mode Select Register

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	M1	M0	0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {M1, M0} = 3H, read address: 5H)

The (M1, M0) register controls the EEPROM operating mode as summarized below.

(M1,M0)	EEPROM Operating Mode	Delay Time	VDD Voltage Required
00	Read	≧ 10 uS	≧ 2.4V
01	Program	≧ 4 mS	≧ 2.8V
10	Erase	≧ 4 mS	≧ 2.8V
11	Reserve	-	-

8.2.27 Vop Calibration Offset Register

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	CV3	CV2	CV1	CV0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {CV4, CV3, CV2, CV1} = 0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	*	CV5	CV4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

(At the time of reset: {CV5, CV4} = 0H, read address: 7H)

The CV5~CV0 registers control the Vop calibration offset voltage selection.

VBA = (1+ (M + offset) / 381)* VREF

M: *DV register setting*
offset: *CV5~CV0 setting*

CV5~CV0	Calibration Offset
011111	+31
011110	+30
…	…
000001	+1
000000	0
100000	-32
100001	-31
…	…
111111	-1

8.2.28 EEPROM Address Select Register

D7	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	*	*	NIB1	NIB0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	0

* *Don't Care*

(At the time of reset**:** {NIB1, NIB0} = 0H, read address**:** AH)

The NIB register selects low nibble or high nibble data to access from EEPROM.

NIB1	NIB0	EEPROM Address
0	0	Bank 4[6H] (CV3~CV0)
0	1	Bank 4[7H] (CV5~CV4)

NOTE

1: When setting CV5~CV0, you must set CV5~CV4 (upper nibble register) first, then set CV3~CV0 (lower nibble register), and then start to program.

2: The programming sequence of CV5~CV4 and CV3~CV0 is not restricted.

3: When reading from CV5~CV0, you must read EEPROM data to CV5~CV4 (upper nibble register) first, then read the EEPROM data to CV3~CV0 (lower nibble register).

8.2.29 Scroll Top Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	STA3	STA2	STA1	STA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {STA3, STA2, STA1, STA0} = 0H, read address: 0H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	1	*	STA6	STA5	STA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

* *Don't Care*

(At the time of reset: {STA6, STA5, STA4} = 0H, read address: 1H)

Sets the top address of scroll data area in RAM under the following condition:
0 <= Scroll top address <= 67
Scroll top address < Scroll bottom address

8.2.30 Scroll Bottom Address

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	SBA3	SBA2	SBA1	SBA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {SBA3, SBA2, SBA1, SBA0} = 3H, read address: 2H)

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	1	*	SBA6	SBA5	SBA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

* *Don't Care*

(At the time of reset: {SBA6, SBA5, SBA4} = 4H, read address: 3H)

Set the bottom address of scroll data area in RAM under the following condition:
0 <= Scroll bottom address <= 67
Scroll top address < Scroll bottom address

8.2.31 Scroll Specified Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	0	SSA3	SSA2	SSA1	SSA0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {SSA3, SSA2, SSA1, SSA0} = 0H, read address: 4H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	0	1	*	SSA6	SSA5	SSA4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

* *Don't Care*

(At the time of reset: {SSA6, SSA5, SSA4} = 0H, read address: 5H)

Depending on the size of the display panel or of the duty ratio selection, set the specified address in RAM to jump to the scroll bottom address and then show the fixed data area.
Scroll specified address = scroll top address + panel scroll area – 1

8.2.32 Scroll Start Address

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	SAY3	SAY2	SAY1	SAY0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

(At the time of reset: {SAY3, SAY2, SAY1, SAY0} = 0H, read address: 6H)

D7	D6	D5	D4	D3	D2	D1	D0
0	1	1	1	*	SAY6	SAY5	SAY4

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

* *Don't Care*

(At the time of reset: {SAY6, SAY5, SAY4} = 0H, read address: 7H)

Set the starting address of the area scrolling and then execute the area scroll operation. The scroll start address must be in the scrolling area.

Scroll top address <= Scroll start address <= Scroll bottom address

> **NOTE**
>
> *To avoid any errors when setting the Scroll start address registers, set SAY[6:4] (Bank 5[7H]) first, then set SAY[3:0] (Bank 5[6H].*

8.2.33 Scroll Mode Select

D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	0	*	*	SM1	SM0

CSB	RS	RDB	WRB	RE2	RE1	RE0
0	1	1	0	1	0	1

* *Don't Care*

(At the time of reset: {SM1, SM0} = 0H, read address: 8H)

SM1	SM0	Type of Area Scroll
0	0	Center screen scroll
0	1	Top screen scroll
1	0	Bottom screen scroll
1	1	Whole screen scroll

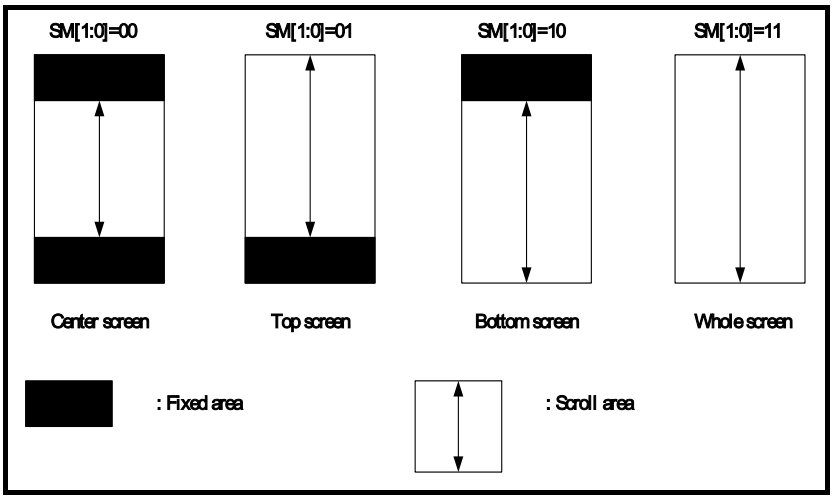


Figure 8-6 Types of Area Scroll Modes

9 Absolute Maximum Rating

9.1 Absolute Maximum Ratings

Item	Symbol	Condition	Pin Used	Rating	Unit
Supply voltage (1)	VDD	Ta=25□	VDD	–0.3 ~ + 4.0	V
Supply voltage (2)	VEE		VEE	–0.3 ~ + 4.0	
Supply voltage (3)	VOUT		VOUT	–0.3 ~ + 18.0	
Supply voltage (4)	VBA		VBA	1.5 ~ + 2.0	
Supply voltage (5)	V0		V0	–0.3 ~ + 16.0	
Supply voltage (6)	V1,V2,V3,V4		V1,V2,V3,V4	–0.3 ~ V0+ 0.3	
Input voltage	VI		*	–0.3 ~ VDD+ 0.3	
Storage temperature	Tstg		-	–45 ~ +125	C

** CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, TEST, and D0 ~ D15 pins*

9.2 Recommended Operating Conditions

Item	Symbol	Pin	Min.	Type	Max.	Unit	Remarks
Supply Voltage	VDD1	VDD	2.2	-	3.3	V	*1
	VDD2	VDD	2.4	-	3.3	V	*2
	VEE	VEE	2.4	-	3.3	V	*3
Operating Voltage	V0	V0	4.5	-	16	V	*4
	VOUT	VOUT		-	20	V	*5
	VBA	VBA	1.5	-	2.0	V	-
	VREF	VREF	-	1.5	-	V	-
Operating Temperature	Topr	-	–30	-	85	C	-

**1 Power supply for logic circuit*

**2 Power supply for analog circuit*

**3 Power supply for internal boosting circuit. If you applied the same voltage as VDD, connect to VDD*

**4 Voltage V0>V1>V2>V3>V4>VSS must always be satisfied*

**5 Voltage VOUT > V0 must always be satisfied*

10 DC Electrical Characteristics

VSS=0V, VDD = 2.2 ~3.3V, Ta = -30 ~85 C

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit	Pin Used
High level input voltage	VIH	-	0.8VDD	0.9VDD	VDD	V	*1
Low level input voltage	VIL	-	0	0.1VDD	0.2VDD	V	*1
High level output current	IOH1	VOH = VDD-0.4V	-2.7	-3.2	-3.5	mA	*2
Low level output current	IOL1	VOL= 0.4V	2.7	3.2	3.5	mA	*2
High level output current	IOH2	VOH = VDD-0.4V	–0.8	–1.0	–1.2	mA	*3
Low level output current	IOL2	VOL= 0.4V	0.8	1.0	1.2	mA	*3
Input leakage current	ILI1	VI = VSS or VDD	–2	0	2	µA	*4
Output leakage current	ILO	VI = VSS or VDD	–2	0	2	µA	*5
LCD driver output resistance	RON	Δ |Von| = 0.5V, V0=10V	1.0	1.3	1.6	KΩ	*6
		Δ |Von| = 0.5V, V0=6V	1.2	1.7	2.2		
Standby current through VDD pin	ISTB	CK=0, CSB=VDD, Ta=25 C, VDD=3V		5	15	µA	*7
Oscillator frequency (65k color mode)	$Fosc_1$	VDD=3V, Ta=25 C, Rf setting = (Rf3, Rf2, Rf1, Rf0) = (0000)	281	290	299	KHz	*8
Oscillator frequency (4k color mode)	$Fosc_2$	VDD=3V, Ta=25 C, Rf setting = (Rf3, Rf2, Rf1, Rf0) = (0000)	138	140	144	KHz	*9
Oscillator frequency (256 color mode)	$Fosc_3$	VDD=3V , Ta=25 C, Rf setting = (Rf3, Rf2, Rf1, Rf0) = (0000)	63	65	67	KHz	*10
Booster output voltage on VOUT pin	VOUT1	Six times boosting RL= 500KΩ (VOUT-VSS)	6*VEE *0.95	6*VEE *0.98	6*VEE *0.99	V	*11
	VOUT2	Five times boosting RL= 500KΩ (VOUT-VSS)	5*VEE *0.95	5*VEE *0.98	5*VEE *0.99	V	*12
	VOUT3	Four times boosting RL= 500KΩ (VOUT-VSS)	4*VEE *0.95	4*VEE *0.98	4*VEE *0.99	V	*13
	VOUT4	Three times boosting RL= 500KΩ (VOUT-VSS)	3*VEE *0.95	3*VEE *0.98	3*VEE *0.99	V	*14
	VOUT5	Two times boosting RL= 500KΩ(VOUT-VSS)	2*VEE *0.95	2*VEE *0.98	2*VEE *0.99	V	*15
Current consumption	IDD1	VDD= 3V, 6 times booster All ON pattern		300		µA	*16
	IDD2	VDD= 3V, 6 times booster Checker pattern		350		µA	*17

Item	Symbol	Condition	Minimum	Typical	Maximum	Unit	Pin Used
VBA output voltage	VBA	VDD =2.4V~3.3V	1.5	-	2.0	V	*18
VREF output voltage	VREF	VDD = 2.4 ~ 3.3V	-	1.5	-	-	*19
V0 output voltage	V0	VDD = 2.4 ~ 3.3V	0.99*V0	V0	1.01*V0	V	-

*1 *D0-D15, CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, & TEST pins.*

*2 *D0 ~ D15 pins*

*3 *CLK pins*

*4 *CSB, RS, M/S, M86, RDB, WRB, CK, CKS, P/S, RESB, & TEST pins*

*5 *Applied when D0 ~ D15 are in the state of high impedance.*

*6 *SEGA0 ~ SEGA97, SEGB0 ~ SEGB97, SEGC0 ~ SEGC97, COM0 ~ COM67 pin resistance when 0.5V is applied between each output pin and to each power supply (V0, V1, V2, V3, V4) and when applied 1/9 bias.*

*7 *VDD pin. VDD pin current is without load when the original oscillating clock is stopped and when CSB=VDD.*

*8 *Oscillator frequency, when using the built-in oscillating circuit (65k-color mode)*

*9 *Oscillator frequency, when using the built-in oscillating circuit (4k-color mode)*

*10 *Oscillator frequency, when using the built-in oscillating circuit (256-color mode)*

*11 *VOUT pin. This pin applies when the following conditions are met: The built-in oscillator circuit is used; the built-in power supply is used; the voltage (boosted 6 times) is used; VEE = 2.4 ~ 3.3; and the electronic control is preset (with code "1 1 1 1 1 1"). Measuring conditions: bias=1/4~1/9; 1/68 duty; LCD driver pin is without load; RL=500 KΩ (between VOUT and VSS); C1=C2=1.0μF; C3=0.1μF; DCON=AMPON="1"; BF="11".*

*12 *VOUT pin. This pin applies when the following conditions are met: The built-in oscillator circuit and built-in power supply are used; the voltage (boosted 5 times) is used; VEE = 2.4 ~ 3.3; and the electronic control is preset (with code "1 1 1 1 1 1"). Measuring conditions: bias=1/4~1/9; 1/68 duty; LCD driver pin is without load; RL=500 KΩ (between VOUT and VSS); C1=C2=1.0μF; C3=0.1μF; DCON=AMPON="1"; BF="11".*

*13 *VOUT pin. This pin applies when the following conditions are met: The built-in oscillator circuit and built-in power supply are used; the voltage (boosted 4 times) is used; VEE = 2.4 ~ 3.3; and the electronic control is preset (with code "1 1 1 1 1 1"). Measuring conditions: bias=1/4~1/9; 1/68 duty; without load; RL=500 KΩ (between VOUT and VSS); C1=C2=1.0μF; C3=0.1μF; DCON=AMPON="1," BF="11".*

*14 *VOUT pin. This pin applies when the following conditions are met: The built-in oscillator circuit and built-in power supply are used; the voltage (boosted 3 times) is used; VEE = 2.4 ~ 3.3; and the electronic control is preset (with code "1 1 1 1 1 1"). Measuring conditions: bias=1/4~1/9; 1/68 duty; LCD driver pin is without load; RL=500 KΩ (between VOUT and VSS); C1=C2=1.0μF; C3=0.1μF; DCON=AMPON="1"; BF="11".*

*15 *VOUT pin. This pin applies when the following conditions are met: The built-in oscillator circuit and built-in power supply are used; the voltage (boosted 2 times) is used; VEE = 2.4 ~ 3.3; and the electronic control is preset (with code "1 1 1 1 1 1 1"). Measuring conditions: bias=1/4~1/9; 1/68 duty; LCD driver pin is without load; RL=500 KΩ (between VOUT and VSS); C1=C2=1.0μF; C3=0.1μF; DCON=AMPON="1"; BF="11".*

*16 *VDD, VEE pins. These pins apply when the following conditions are met: The built-in oscillator circuit and built-in power supply are used; there is no access from MPU; voltage (boosted 6 times) is used; and the electronic control is preset (with code "1 1 1 1 1 1 1"); Display is ALL ON pattern {Rf3, Rf2, Rf1, Rf0 = ("0 0 0 0 ") }; and the LCD driver pin is without load. Measuring conditions: VDD=VEE; VBA=VREF; C1=C2=1.0μF; C3=0.1μF; DCON=AMPON="1"; NLIN="0"; (BF1,BF0)=(1,1); 1/68 duty; 1/9 bias; BF="11".*

*17 *VDD, VEE pins. These pins apply when the following conditions are met: The built-in oscillator circuit and built-in power supply are used; there is no access from MPU; voltage (boosted 6 times) is used; and the electronic control is preset (with code "1 1 1 1 1 1 1"); Display is ALL ON pattern {Rf3, Rf2, Rf1, Rf0 = ("0 0 0 0 ") }; and the LCD driver pin is without load. Measuring conditions: VDD=VEE; C1=C2=1.0μF; C3=0.1μF; DCON=AMPON="1"; NLIN="0"; (BF1,BF0)=(1,1); 1/68 duty; 1/9 bias; BF="11".*

*18 *VBA pin. Measuring conditions: N times boosting (N=2~6); electronic control = "1 1 1 1 1 1 1"; DCON=AMPON="1"; NLIN="0"; 1/68 duty; VDD=VEE; VBA=VREF; C1=C2=1.0μF; C3=0.1μF; and the LCD driver pin is without load.*

*19 *VREF pin. Measuring conditions: VDD = 3 volt; N times boosting (N=2 ~ 6); electronic control = "1 1 1 1 1 1 1"; DCON=AMPON="1"; NLIN="0"; 1/68 duty.*

The following shows the relationship of the oscillator frequency (fosc) and external clock frequency (fCK) with the LCD frame frequency (fFLM) under each display mode.

Original Oscillating Clock	Display Mode	Ratio of Display Duty Cycle (1/D)			
		1/68 to 1/44	1/40 to 1/24	1/20 to 1/12	1/8
When using built-in oscillator circuit (fosc)	Simple gradation (65K color)	fosc/(2*31*D)	fosc/(4*31*D)	fosc/(8*31*D)	fosc /(16*31*D)
	Simple gradation (4096 color)	fosc /(2*15*D)	fosc /(4*15*D)	fosc /(8*15*D)	fosc /(16*15*D)
	Simple gradation (256 color)	fosc /(2*7*D)	fosc /(4*7*D)	fosc /(8*7*D)	fosc /(16*7*D)
When using external clock from CK pin (fCK)	Simple gradation (65K color)	fCK /(2*31*D)	fCK /(4*31*D)	fCK /(8*31*D)	fCK /(16*31*D)
	Simple gradation (4096 color)	fCK /(2*15*D)	fCK /(4*15*D)	fCK /(8*15*D)	fCK /(16*15*D)
	Simple gradation (256 color)	fCK /(2*7*D)	fCK /(4*7*D)	fCK /(8*7*D)	fCK /(16*7*D)

11 AC Electrical Characteristics

NOTE

All the timings must be specified relative to 20% and 80% of theVDD voltage.

11.1 80-Family MCU Write Timing

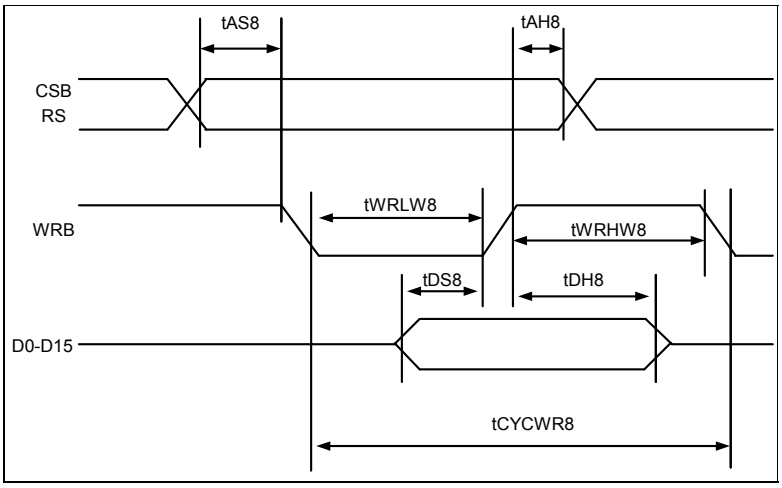


Figure 11-1 80-Family MCU Write Timing Diagram

VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
Write system cycle time	tCYCWR8		200			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		30			ns	
Write pulse “H” width	tWRHW8		135			ns	
Data setup time	tDS8		60			ns	D0~D15
Data hold time	tDH8		5			ns	

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
Write system cycle time	tCYCWR8		250			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		50			ns	
Write pulse “H” width	tWRHW8		160			ns	
Data setup time	tDS8		80			ns	D0~D15
Data hold time	tDH8		10			ns	

VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
Write system cycle time	tCYCWR8		500			ns	WRB (R/WB)
Write pulse “L” width	tWRLW8		100			ns	
Write pulse “H” width	tWRHW8		350			ns	
Data setup time	tDS8		100			ns	D0~D15
Data hold time	tDH8		20			ns	

11.2 80-Family MCU Read Timing

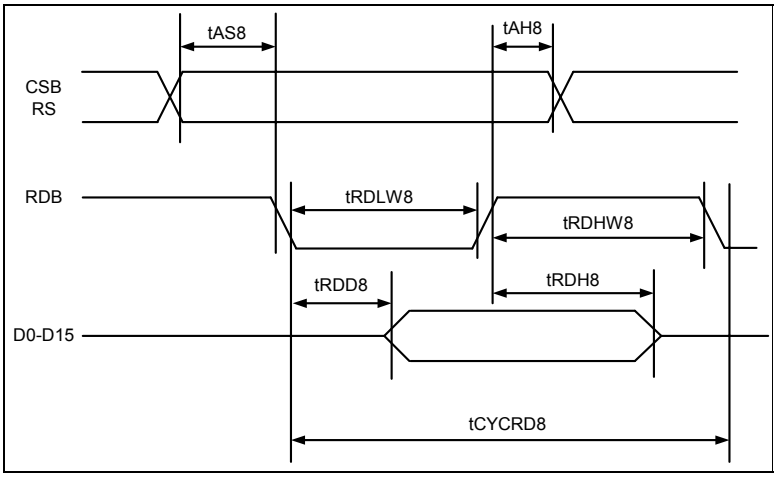


Figure 11-2 80-Family MCU Read Timing Diagram

VSS=0V , VDD = 2.7~3.3V , Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
Read system cycle time	tCYCRD8		380			ns	RDB(E)
Read pulse “L” width	tRDLW8		200			ns	
Read pulse “H” width	tRDHW8		170			ns	
Data setup time	tRDD8	CL = 80 pF			210	ns	D0~D15
Data hold time	tRDH8		10			ns	

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
Read system cycle time	tCYCRD8		540			ns	RDB(E)
Read pulse “L” width	tRDLW8		290			ns	
Read pulse “H” width	tRDHW8		230			ns	
Data setup time	tRDD8	CL = 80 pF			300	ns	D0~D15
Data hold time	tRDH8		10			ns	

VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85℃

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH8		0			ns	CSB RS
Address setup time	tAS8		0			ns	
Read system cycle time	tCYCRD8		840			ns	RDB(E)
Read pulse “L” width	tRDLW8		440			ns	
Read pulse “H” width	tRDHW8		380			ns	
Data setup time	tRDD8	CL = 80 pF			450	ns	D0~D15
Data hold time	tRDH8		10			ns	

11.3 68-Family MCU Write Timing

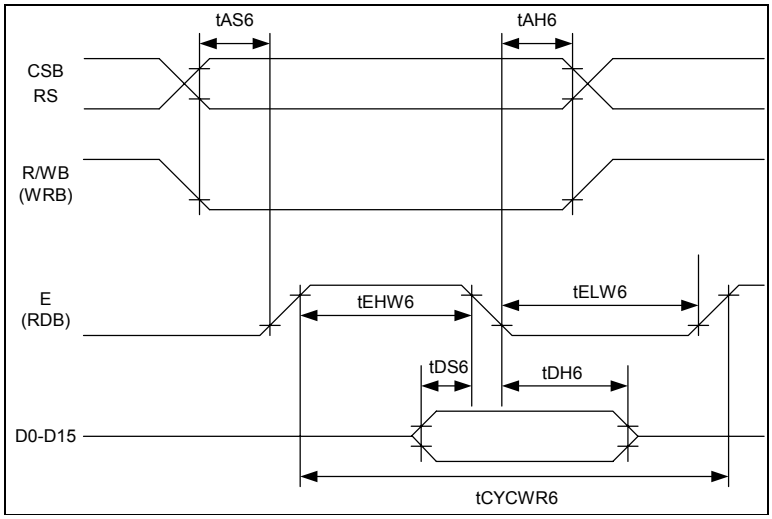


Figure 11-3 68-Family MCU Write Timing Diagram

VSS=0V, VDD = 2.7 ~3.3V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
Write system cycle time	tCYCWR6		200			ns	RDB(E)
Write pulse “L” width	tELW6		30			ns	
Write pulse “H” width	tEHW6		135			ns	
Data setup time	tDS6		60			ns	D0~D15
Data hold time	tDH6		5			ns	

VSS=0V, VDD = 2.4 ~2.7V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
Write system cycle time	tCYCWR6		250			ns	RDB(E)
Write pulse “L” width	tELW6		50			ns	
Write pulse “H” width	tEHW6		160			ns	
Data setup time	tDS6		80			ns	D0~D15
Data hold time	tDH6		10			ns	

VSS=0V, VDD = 2.2 ~2.4V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
Write system cycle time	tCYCWR6		500			ns	RDB(E)
Write pulse “L” width	tELW6		100			ns	
Write pulse “H” width	tEHW6		350			ns	
Data setup time	tDS6		100			ns	D0~D15
Data hold time	tDH6		20			ns	

11.4 68-Family MCU Read Timing

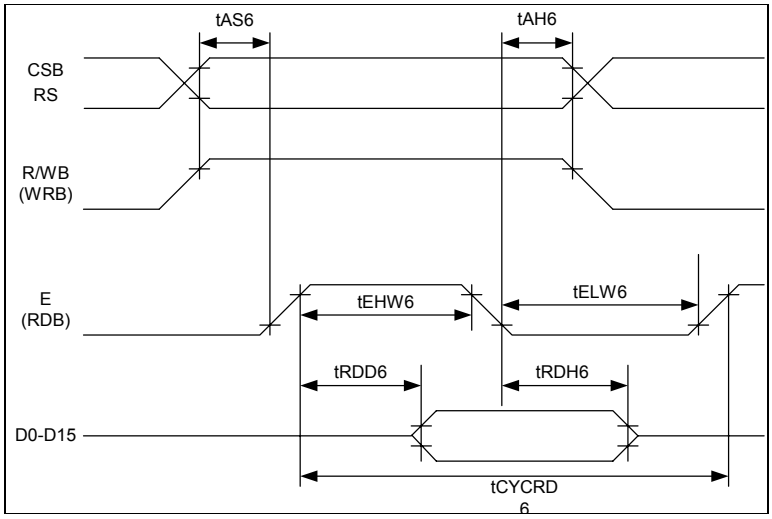


Figure 11-4 68-Family MCU Read Timing Diagram

VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
Read system cycle time	tCYCRD6		380			ns	RDB(E)
Write pulse “L” width	tELW6		200			ns	
Write pulse “H” width	tEHW6		170			ns	
Data setup time	tRDD6	CL=50pF			210	ns	D0~D15
Data hold time	tRDH6		10			ns	

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSB RS
Address setup time	tAS6		0			ns	
Read system cycle time	tCYCRD6		540			ns	RDB(E)
Write pulse “L” width	tELW6		290			ns	
Write pulse “H” width	tEHW6		230			ns	
Data setup time	tRDD6	CL=50pF			300	ns	D0~D15
Data hold time	tRDH6		10			ns	

VSS=0V , VDD = 2.2~2.4V , Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Address hold time	tAH6		0			ns	CSBRS
Address setup time	tAS6		0			ns	
Read system cycle time	tCYCRD6		1000			ns	RDB(E)
Write pulse “L” width	tELW6		450			ns	
Write pulse “H” width	tEHW6		500			ns	
Data setup time	tRDD6	CL=50pF			650	ns	D0~D15
Data hold time	tRDH6		10			ns	

11.5 Serial Interface Timing Diagram

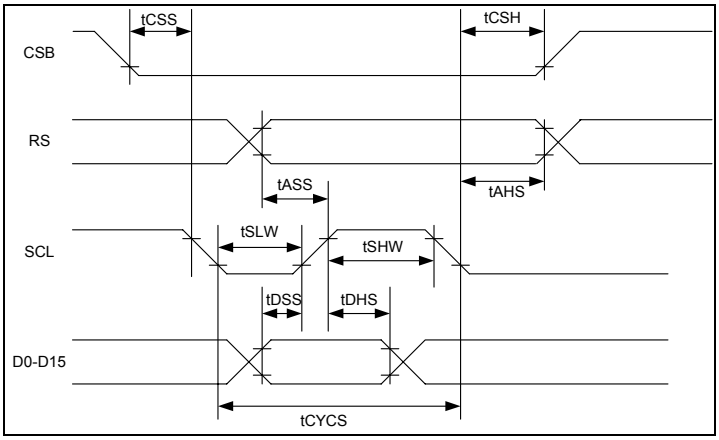


Figure 11-5 Serial Interface Timing Diagram

VSS=0V, VDD = 2.7~3.3V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		40			ns	RS
Address hold time	tAHS		40			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		40			ns	CSB
CSB hold time	tCSH		40			ns	

VSS=0V, VDD = 2.4~2.7V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Serial clock period	tCYCS		200			ns	SCL
SCL pulse “H” width	tSHW		80			ns	
SCL pulse “L” width	tSLW		80			ns	
Address setup time	tASS		50			ns	RS
Address hold time	tAHS		50			ns	
Data setup time	tDSS		80			ns	SDA
Data hold time	tDHS		80			ns	
CSB-SCL time	tCSS		50			ns	CSB
CSB hold time	tCSH		60			ns	

VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typical	Max.	Unit	Pin Used
Serial clock period	tCYCS		230			ns	SCL
SCL pulse “H” width	tSHW		100			ns	
SCL pulse “L” width	tSLW		100			ns	
Address setup time	tASS		80			ns	RS
Address hold time	tAHS		80			ns	
Data setup time	tDSS		100			ns	SDA
Data hold time	tDHS		100			ns	
CSB-SCL time	tCSS		80			ns	CSB
CSB hold time	tCSH		100			ns	

11.6 Clock Input Timing

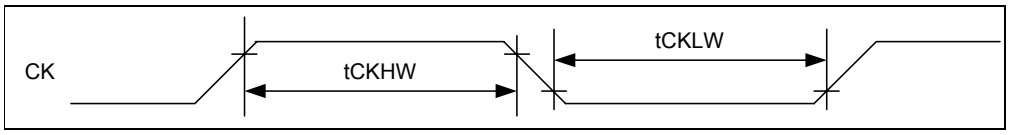


Figure 11-6 Clock Input Timing Diagram

VSS=0V, VDD = 2.4~3.3V, Ta = -30~+85 C

Item	Symbol	Min.	Typical	Max.	Unit	Pin Used
CK pulse “H” width	tTCKHW	1.5	-	1.6	µs	CK[1]
CK pulse “L” width	tCKLW					
CK pulse “H” width	tTCKHW	2.9	-	3.5	µs	CK[2]
CK pulse “L” width	tCKLW					
CK pulse “H” width	tTCKHW	6.3	-	7.6	µs	CK[3]
CK pulse “L” width	tCKLW					

VSS=0V, VDD = 2.2~2.4V, Ta = -30~+85 C

Item	Symbol	Min.	Typical	Max.	Unit	Pin Used
CK pulse “H” width	tTCKHW	1.5	-	1.6	µs	CK[1]
CK pulse “L” width	tCKLW					
CK pulse “H” width	tTCKHW	2.9	-	3.5	µs	CK[2]
CK pulse “L” width	tCKLW					
CK pulse “H” width	tTCKHW	6.3	-	7.6	µs	CK[3]
CK pulse “L” width	tCKLW					

[1] *Applicable only when the simple gradation 65K color mode is used.*
[2] *Applicable only when the simple gradation 4096 color mode is used.*
[3] *Applicable only when the simple gradation 256 color mode is used.*

11.7 Reset Timing

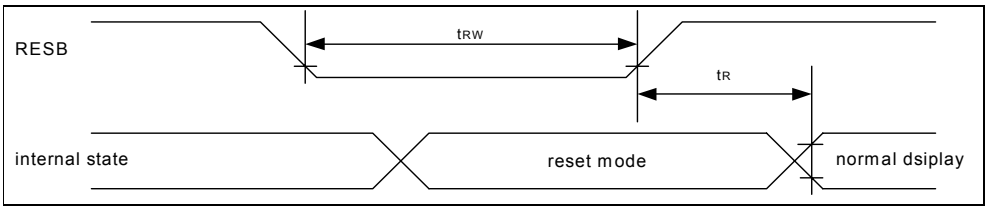


Figure 11-7 Reset Timing Diagram

VSS=0V, VDD = 2.2~3.3V, Ta = -30~+85 C

Item	Symbol	Condition	Min.	Typ.	Max.	Unit	Pin Used
Reset time	tR				1	µs	
Reset pulse “L” width	tRW		80			µs	RESB

12 Application Circuit

12.1 Connected to 80-Family MCU

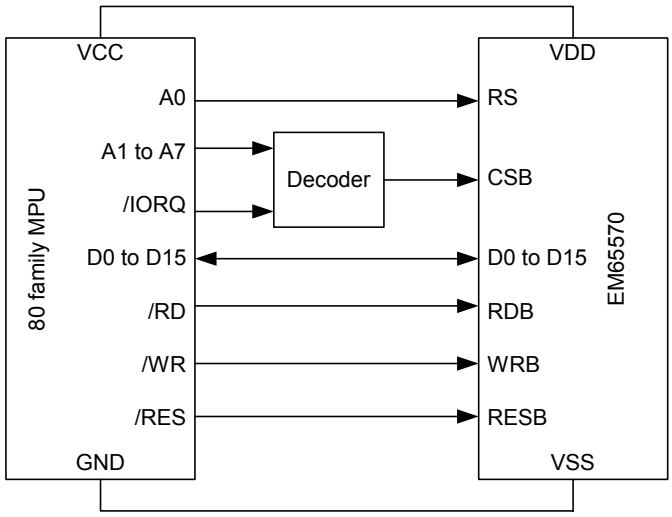


Figure 12-1 Connected to 80-Family MCU Application Circuit Diagram

12.2 Connected to 68-Family MCU

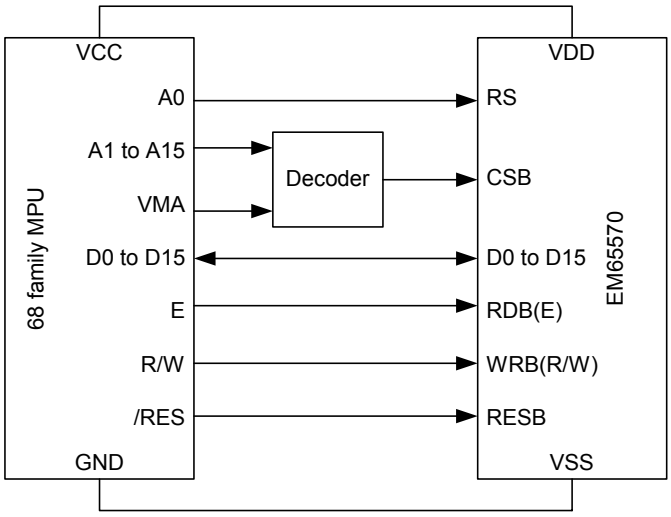


Figure 12-2 Connected to 68-Family MCU Application Circuit Diagram

12.3 Connected to Serial Interface MCU

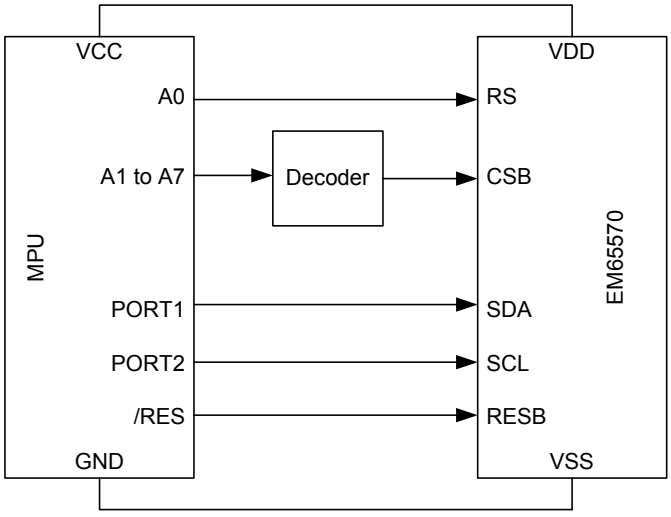


Figure 12-3 Connected to Serial Interface MCU Application Circuit Diagram

13 Packing Tray Dimensions

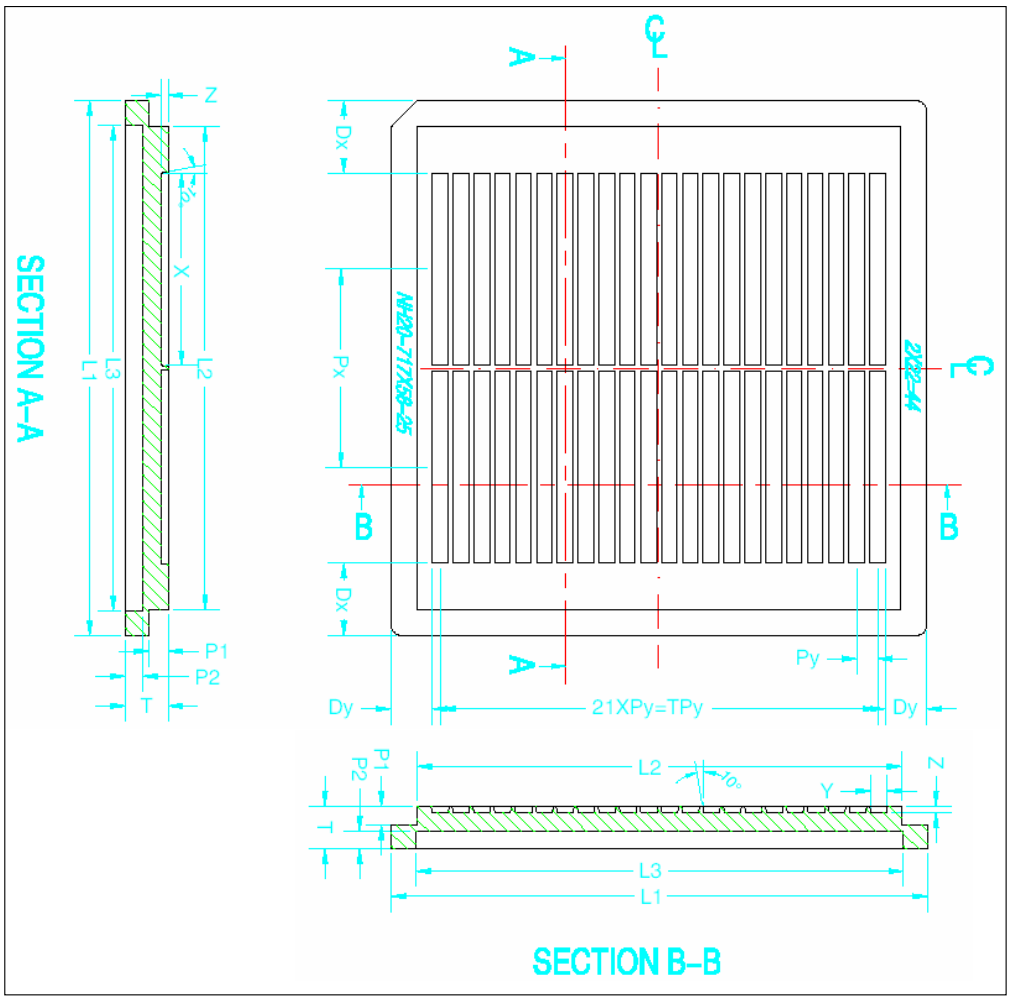


Figure 13-1 EM65570 Packing Tray Dimensional Diagram

Tray Dimensions (Unit: mm)

Symbol	Dimensions	Symbol	Dimensions
L1	50.80	Px	18.71
L2	45.50	Py	1.97
L3	45.80	Dx	6.94
T	4.00	Dy	5.94
X	18.21 ± 0.05	TPy	41.37
Y	1.47 ± 0.05	N	44
Z	0.64 ± 0.05	-	-