HT95R64/HT95R65
CID Phone 8-Bit MCU with CPT

Technical Document

- Application Note
  - HA0075E MCU Reset and Oscillator Circuits Application Note

Features

- Operating voltage:
  f_{SYS}=3.58MHz: 2.2V~5.5V
  f_{SYS}=7.16MHz: 3.0V~5.5V
  f_{SYS}=10.74MHz: 3.0V~5.5V
  f_{SYS}=14.32MHz: 4.5V~5.5V
- Program Memory:
  8K×16 (HT95R64)
  16K×16 (HT95R65)
- 2112×8 Data Memory
- 38 bidirectional I/Os with pull-high options
- 2 NMOS output-only lines
- External interrupt input
- Three 16-bit timers with interrupts
- Timer external input
- 8-level stack
- 32768Hz system oscillator
- 32768Hz up to 14.32MHz frequency-up circuit
- Real time clock function
- Watchdog timer function
- PFD driver output
- Serial Interfaces Module: SIM for SPI or I^2C
- Internal DTMF generator
- Internal DTMF receiver
- Internal FSK decoder
  - Support Bell 202 and V.23
  - Support ring and line reverse detection
- 12-bit Audio DAC output
- Power-down and wake-up feature for power-saving operation: Idle mode, Sleep mode, Green mode and Normal mode
- Up to 0.28μs instruction cycle with 14.32MHz system clock at V_{DD}=4.5V~5.5V
- Bit manipulation instructions
- Table read function
- 63 powerful instructions
- All instructions executed in 1 or 2 machine cycles
- Low voltage reset function
- Supported by comprehensive suite of hardware and software tools
- Internal low battery detector
- Software Controlled R-Type LCD Driver (SCOM)
- Internal Call Progress Tone (CPT) detector
- 64/80-pin LQFP package

General Description

The series of CID phone MCU are 8-bit high performance, RISC architecture microcontroller devices specially designed for telephone applications. Devices flexibility are enhanced with their internal special features such as power-down and wake-up functions, DTMF generator, DTMF receiver, FSK decoder, CPT detector, PFD driver, SPI and I^2C interface, audio DAC output, etc. These features combine to ensure applications require a minimum of external components and therefore reduce overall product costs.

Having the advantages of low-power consumption, high-performance, I/O flexibility as well as low-cost, these devices have the versatility to suit a wide range of application possibilities such as FSK & DTMF mode Caller ID phone, Home Security products, deluxe feature phones, cordless phones, fax and answering machines, etc.

The call progress tone detector is for Auto-dialing system use. Switched capacitors technology is implemented into the chip to get good performance characteristics of band pass filter in the range of 305Hz to 640Hz call progress tone which is dual tone multi-frequency signal. When it detected CPT signal then it generates relative envelopes for external microcontroller decision to finish different kinds of CPT signal detection such as dial tone, busy tone, ring-back tone and reorder tone.

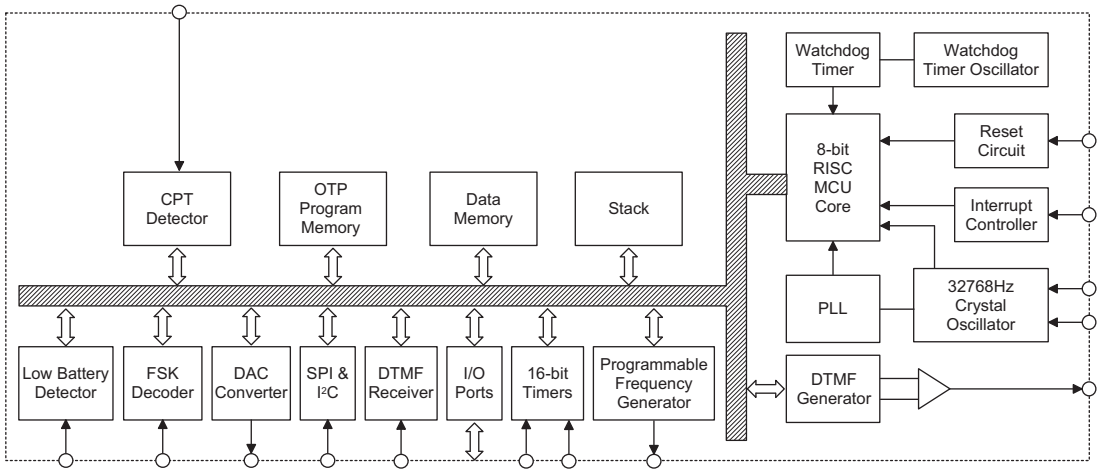
The device will be ideally suited for phone products that comply with versatile dialer specification requirements for different areas or countries. The device is fully supported by the Holtek range of fully functional development and programming tools, providing a means for fast and efficient product development cycles.

Selection Table

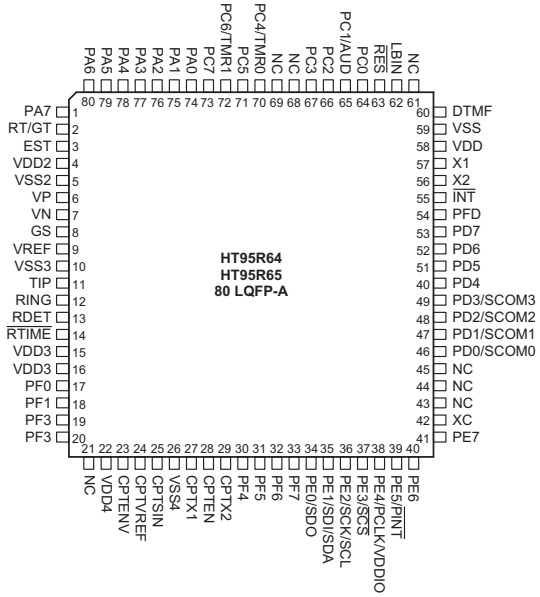
Part No.	Program Memory	Data Memory	I/O	Timer	External Interrupt	R-Type LCD	I²C/ SPI	D/A	DTMF Generator/ Receiver	FSK Decoder	CPT Detector	Stack	Package
HT95R64	8K×16	2112×8	40	16-bit×3	4	4COM	√	12-bit×1	√	√	√	8	64LQFP 80LQFP
HT95R65	16K×16	2112×8	40	16-bit×3	4	4COM	√	12-bit×1	√	√		8	64LQFP 80LQFP

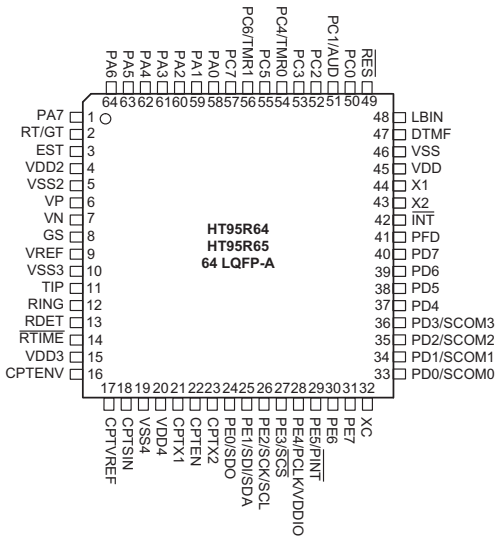
Note: These devices are only available in OTP versions.

Block Diagram



Pin Assignment





Pin Description

Pad Name	I/O	Options	Description
PA0~PA7	I/O	Pull-high Wake-up	Bidirectional 8-bit input/output port. Each individual pin on this port can be configured as a wake-up input by a configuration option. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine which pins on the port have pull-high resistors.
PC0, PC5, PC7	I/O	Pull-High	Bidirectional input/output port. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine which pins on the port have pull-high resistors. When the multi-function interrupt is enabled an interrupt will be generated whenever PC0 or PC5 has a falling edge, or PC7 has a rising edge. When in the idle mode such an interrupt will wake up the device.
PC1/AUD PC4/TMR0 PC6/TMR1	I/O	DAC Output Pull-High	Bidirectional input/output port. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine which pins on the port have pull-high resistors. PC1 is also D/A pin for audio output for driving an external transistor or power amplifier. Pin PC4 and PC6 are pin-shared with the external timer input pin TMR0 and TMR1 respectively.
PC2, PC3	O	—	NMOS output structures
PD0/SCOM0 PD1/SCOM1 PD2/SCOM2 PD3/SCOM3 PD4~PD7	I/O	Pull-High	Bidirectional 8-bit input/output port. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine which nibble on the port have pull-high resistors. PD0~PD3 also support LCD software COM port function.
PE0/SDO PE1/SDI/SDA PE2/SCK/SCL PE3/$\overline{SCS}$ PE4/PCLK/VDDIO PE5/$\overline{PINT}$ PE6~PE7	I/O	Pull-High	Schmitt Trigger input and CMOS output. I^2C and SPI functional pins: SDO, SDI/SDA, SCK/SCL, $\overline{SCS}$, PCLK, $\overline{PINT}$ are pin-shared with PE0~PE5 respectively. For I^2C, PE2 and PE1 used as SCL and SDA of I^2C respectively. For use as SPI, PE0~PE3 used as SDO, SDI, SCK, $\overline{SCS}$ of SPI respectively. SDO is a serial interface data output. SCK is a serial interface clock input/output (Initial is input). $\overline{SCS}$ is a chip select pin of the serial peripheral interface, input for slave mode and output for master mode. SDI is a serial interface data input. PCLK is a peripheral clock. $\overline{PINT}$ is external peripheral interrupt pin. Once the SPI/I^2C bus function is used, the PE0~PE3 could not be used as normal I/O pins. PE4/PCLK is pin shared with VDDIO which is selected by configuration option. PE4 I/O function & PCLK output function will be disabled when this pin used as VDDIO. VDDIO is used to provide the SPI/I^2C interface I/Os a pull high voltage, set by external power supplier, other than the device operating voltage. The purpose of this design is to cope with the voltage difference between Master device and Slave device, such as Voice Flash memory.
PF0~PF7	I/O	Pull-High	Bidirectional 8-bit input/output port. Software instructions determine if the pin is a CMOS output or Schmitt Trigger input. Configuration options determine which nibble on the port have pull-high resistors.
$\overline{INT}$	I	—	External interrupt Schmitt Trigger input. Edge trigger activated on high to low transition. No pull-high resistor.
DTMF	O	—	Dual Tone Multi Frequency Output
PFD	O	—	CMOS output structure Programmable Frequency Divider pin
LBIN	I	—	This pin detects battery low through external R1/R2 to determine threshold voltage.
RT/GT	I/O	—	Tone acquisition time and release time can be set through connection with external resistor and capacitor CMOS IN/OUT for DTMF receiver.
EST	O	—	Early steering output CMOS out for DTMF receiver.
VP	I	—	Operational amplifier non-inverting input for DTMF receiver.
VN	I	—	Operational amplifier inverting input for DTMF receiver.
GS	O	—	Operational amplifier output terminal for DTMF receiver.

Pad Name	I/O	Options	Description
VREF	O	—	Reference voltage output, normally $V_{DD}/2$ for DTMF receiver.
TIP	I	—	Input pin connected to the tip side of the twisted pair wires for FSK decoder. It is internally biased to 1/2 VDD when the device is in power-up mode. This pin must be DC isolated from the line.
RING	I	—	Input pin connected to the ring side of the twisted pair wires for FSK decoder. It is internally biased to 1/2 VDD when the device is in power-up mode. This pin must be DC isolated from the line.
RDET, LBIN	I	—	This pin detects ring energy on the line through an attenuating network for FSK decoder.
RTIMEB			Schmitt trigger input and NMOS output pin which functions with RDET1 pin to make an RC network that performs ring detection function for FSK decoder.
CPTENV	O		While an input signal for CPT detector is within specification, this pin will output the envelope relative to the input signal with a typical 40ms timing delay.
CPTVREF	I		1/2 VDD reference voltage output pin for CPT detector. When CPTENB = VDD, the device will be turned off and CPTVREF disabled.
CPTSIN	I		AC coupled analog signal input pin for CPT detector.
CPTENB	I		CPT detector enable control pin. CPTENB = VSS: normal operation mode. CPTENB = VDD: disabled mode.
CPTX1 CPTX2	I O		CPTX1 and CPTX2 are connected to an external 32768Hz crystal or resonator for the CPT detector clock source. The oscillator is turned off in the CPT detector disabled mode.
X1 X2	I O	—	X1 and X2 are connected to an external 32768Hz crystal or resonator for the system clock.
XC	—	—	External low pass filter pin used for the frequency up conversion circuit.
$\overline{RES}$	I	—	Schmitt trigger reset input. Active low.
VDD	—	—	Positive power supply
VSS	—	—	Negative power supply, ground.
VDD2	—	—	DTMF receiver positive power supply
VSS2	—	—	DTMF receiver negative power supply
VDD3	—	—	Positive power supply for FSK Decoder
VSS3	—	—	Negative power supply for FSK Decoder
VDD4	—	—	Positive power supply for CPT detector
VSS4	—	—	Negative power supply for CPT detector

Note: Each pin on PA can be programmed through a configuration option to have a wake-up function.

Absolute Maximum Ratings

Supply Voltage ..... V_{SS}–0.3V to V_{SS}+6.0V
Input Voltage ..... V_{SS}–0.3V to V_{DD}+0.3V
I_{OL} Total 150mA
Total Power Dissipation 500mW

Storage Temperature ..... –50°C to 125°C
Operating Temperature ..... –40°C to 85°C
I_{OH} Total ..... –100mA

Note: These are stress ratings only. Stresses exceeding the range specified under "Absolute Maximum Ratings" may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

D.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
General							
V_{DD}	Operating Voltage	—	—	2.2	—	5.5	V
CPU							
I_{IDL1}	Idle Mode Current 1	3V	32768Hz and 3.58MHz oscillator off, system HALT, WDT off, no load	—	—	1.5	μA
		5V		—	—	2	
I_{IDL2}	Idle Mode Current 2	3V	32768Hz and 3.58MHz oscillator off, system HALT, WDT on, no load	—	—	5	μA
		5V		—	—	10	
I_{SLP}	Sleep Mode Current	3V	32768Hz on, 3.58MHz oscillator off, system HALT, no load	—	—	15	μA
		5V		—	—	30	
I_{GRN}	Green Mode Current	3V	32768Hz on, 3.58MHz oscillator off, system on, no load	—	—	25	μA
		5V		—	—	50	
I_{NOR1}	Normal Mode Current 1	3V	32768Hz on, 3.58MHz oscillator on, system on, DTMF generator off, receiver off, FSK decoder off, no load	—	—	2	mA
		5V		—	—	3	
I_{NOR2}	Normal Mode Current 2	3V	32768Hz on, 3.58MHz oscillator on, system on, DTMF generator on, receiver on, FSK decoder on, no load	—	—	4	mA
		5V		—	—	6	
R_{PH}	Pull-high Resistor	3V	—	66	200	330	kΩ
		5V		33	100	166	
V_{IL1}	Input Low Voltage for I/O and INT	—	—	0	—	$0.3V_{DD}$	V
V_{IH1}	Input High Voltage for I/O and INT	—	—	$0.7V_{DD}$	—	V_{DD}	V
V_{IL2}	Input Low Voltage ($\overline{RES}$)	—	—	0	—	$0.4V_{DD}$	V
V_{IH2}	Input High Voltage ($\overline{RES}$)	—	—	$0.9V_{DD}$	—	V_{DD}	V
I_{OL1}	I/O Port Sink Current	3V	V_{OL}= $0.1V_{DD}$	3	4	—	mA
		5V		4	6	—	
I_{OL2}	PC2, PC3 Sink Current	5V	PC2/PC3= 0.5V	2.5	—	—	mA
I_{OH1}	I/O Port Source Current	3V	V_{OH}= $0.9V_{DD}$	–1	–2	—	mA
		5V		–2	–3	—	
I_{OH2}	PC2, PC3 Leakage Current	5V	PC2/PC3= 5V	—	—	2.5	μA
V_{LBIN}	Low Battery Detection Reference Voltage	5V	—	1.05	1.15	1.25	V
I_{SCOM}	SCOM Operating Current	5V	SCOMC, ISEL[1:0]=00	17.5	25.0	32.5	μA
			SCOMC, ISEL[1:0]=01	35	50	65	μA
			SCOMC, ISEL[1:0]=10	70	100	130	μA
			SCOMC, ISEL[1:0]=11	140	200	260	μA
V_{SCOM}	V_{DD}/2 Voltage for LCD COM	5V	No load	0.475	0.500	0.525	V_{DD}

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
DTMF Generator (Operating Temperature: –20°C to 85°C							
V_{TDC}	DTMF Output DC Level	—	—	$0.45V_{DD}$	—	$0.7V_{DD}$	V
V_{TOL}	DTMF Sink Current	—	V_{DTMF}= 0.5V	0.1	—	—	mA
DTMF Receiver							
R_{IN}	Input Impedance (VP, VN)	5V	—	—	10	—	MΩ
I_{OL3}	Sink Current (EST)	5V	V_{OUT}= 0.5V	1	2.5	—	mA
I_{OH3}	Source Current (EST)	5V	V_{OUT}= 4.5V	–0.4	–0.8	—	mA
Low-voltage Reset							
V_{LVR1}	Low Voltage Reset 1 (Note 2)	—	Configuration option= 4.2V	3.98	4.2	4.42	V
V_{LVR2}	Low Voltage Reset 2 (Note 2)	—	Configuration option= 3.15V	2.98	3.15	3.32	V
V_{LVR3}	Low Voltage Reset 3 (Note 2)	—	Configuration option= 2.1V	1.98	2.1	2.22	V

Note: 1. Distortion: T.H.D.=20×log $\left\{ \frac{\sqrt{V_1^2 + V_2^2 + \cdots + V_n^2}}{\sqrt{V_i^2 + V_h^2}} \right\}$

2. Vi, Vh: Row group and column group signals

3. V1, V2, ..., Vn: Harmonic signals (BW=300Hz~3500Hz)

A.C. Characteristics

Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
General							
f_{SYS1}	System Clock 1	—	Normal mode 32768Hz crystal oscillator	—	3.5795	—	MHz
			Normal Mode, X2 PLL	—	7.16	—	MHz
			Normal Mode, X3 PLL	—	10.74	—	MHz
			Normal Mode, X4 PLL	—	14.32	—	MHz
f_{SYS2}	System Clock 2	—	Green Mode, 32768Hz crystal oscillator	—	32	—	kHz
t_{SST}	System Start-up Timer Period	—	Power-up, Reset or wake-up from HALT	—	1024	—	t_{SYS}
t_{LVR}	Low Voltage Width to Reset	—	—	—	1	—	ms
t_{WAKE}	Wake-up Time for 32768Hz Crystal OSC	3V	32kHz oscillator off → on	—	—	200	ms
t_{FUP}	Settling Time for 32768Hz to HCLK: PLL (Frequency Up Conversion)	3V	32kHz oscillator is on; HCLK oscillator off → on	—	—	20	ms
t_{S2G}	Time from Sleep Mode to Green Mode	—	Wake-up from Sleep Mode	—	0	—	ms

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
MCU							
t_{WDTOSC}	Watchdog Oscillator Period	3V	—	45	90	180	μs
		5V	—	32	65	130	
t_{RES}	External Reset Low Pulse Width	—	—	1	—	—	μs
t_{INT}	Interrupt Pulse Width	—	—	1	—	—	μs
DTMF Generator (Operating Temperature: –20°C to 85°C							
f_{DTMFO}	Single Tone Output Frequency	2.5V	Microcontroller normal mode; DTMF generator single tone test mode	690	—	704	Hz
				762	—	778	
				843	—	861	
				932	—	950	
				1197	—	1221	
				1323	—	1349	
				1462	—	1492	
				1617	—	1649	
V_{TAC}	DTMF Output AC Level	—	Row group, R_L= 5kΩ	120	155	180	mV_{rms}
R_L	DTMF Output Load	—	T.H.D. ≤ –23dB	5	—	—	kΩ
A_{CR}	Column Pre-emphasis	—	Row group= 0dB	1	2	3	dB
THD	Tone Signal Distortion	—	R_L= 5kΩ	—	–30	–23	dB
DTMF Receiver – Signal (f_{SYS}= 3.5795MHz)							
	Input Signal Level	3V	—	–36	—	–6	dBm
		5V	—	–29	—	1	
	Twisted Accept Limit (Positive)	5V	—	—	10	—	dB
	Twisted Accept Limit (Negative)	5V	—	—	10	—	dB
	Dial Tone Tolerance	5V	—	—	18	—	dB
	Noise Tolerance	5V	—	—	–12	—	dB
	Third Tone Tolerance	5V	—	—	–16	—	dB
	Frequency Deviation Acceptance	5V	—	—	—	±1.5	%
	Frequency Deviation Rejection	5V	—	±3.5	—	—	%
t_{PU}	Power-up Time	5V	—	—	30	—	ms

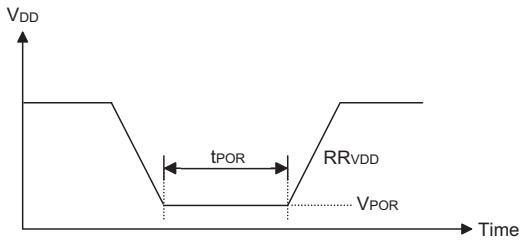
Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
DTMF Receiver – Gain Setting Amplifier (f_{SYS}= 3.5795MHz)							
R_{IN}	Input Resistance	5V	—	—	10	—	MΩ
I_{IN}	Input Leakage Current	5V	VSS<(WP, WN)<VDD	—	0.1	—	μA
V_{OS}	Offset Voltage	5V	—	—	±25	—	mV
P_{SRR}	Power Supply Rejection	5V	100Hz; –3V<V_{IN}<+3V	—	60	—	dB
C_{MRR}	Common Mode Rejection	5V	100Hz; –3V<V_{IN}<+3V	—	60	—	dB
A_{VO}	Open Loop Gain	5V	100Hz; –3V<V_{IN}<+3V	—	60	—	dB
f_T	Gain Bandwidth	5V	—	—	1.5	—	MHz
V_{OUT}	Output Voltage Swing	5V	R_L>100kΩ	—	4.5	—	V_{PP}
R_L	Load Resistance (GS)	5V	—	—	50	—	kΩ
C_L	Load Capacitance (GS)	5V	—	—	100	—	pF
V_{CM}	Common Mode Range	5V	No load	—	3	—	V_{PP}
DTMF Receiver – Steering Control (f_{SYS}= 3.5795MHz)							
t_{DP}	Tone Present Detection Time	5V	—	5	11	14	ms
t_{DA}	Tone Absent Detection Time	5V	—	—	4	8.5	ms
t_{ACC}	Acceptable Tone Duration	5V	—	—	—	42	ms
t_{REJ}	Rejected Tone Duration	5V	—	20	—	—	ms
t_{IA}	Acceptable Inter-Digit Pause	5V	—	—	—	42	ms
t_{IR}	Rejected Inter-Digit Pause	5V	—	20	—	—	ms
FSK Decoder							
	Input Sensitivity: TIP, RING	—	—	–40	–45	—	dBm
	Transmission Rate	5V	—	1188	1200	1212	baud
S/N	Signal to Noise Ratio	—	—	—	20	—	dB
	Band-pass Filter Frequency Response Relative to 1700Hz at 0dBm ≤60Hz 550Hz 2700Hz ≥3300Hz	—	—	 — — — —	 –64 –4 –3 –34	 — — — —	dB
	Carrier Detect Sensitivity	—	—	—	–48	—	dBm
t_{SUPD}	Power Up to FSK Signal Set Up Time	—	—	15	—	—	ms

CPT Detector Electrical Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{DD}	Operating Voltage	—	—	2.5	—	5.5	V
I_{DD}	Operating Current	5V	Functions enabled	—	—	2	mA
		2.5V	No load	—	—	0.8	mA
I_{STB}	Standby Current	2.5V	Functions disabled or $\overline{\text{CPTEN}}$=1	—	—	1	μA
G_{DV}	Detection Level	5V	f_{IN}=305~640Hz	–36	—	0	dBm
		2.5V	CPTENV=1	–42	—	–8	dBm
G_{RL}	Rejection Level	—	All frequency, CPTENV=0	—	—	–50	dBm
f_{RL}	Rejection Out-band Frequency	—	V≤0 dBm, CPTENV=0	—	—	200	Hz
f_{RH}				800	—	—	Hz
t_{QI}	Detection Pause Time	—	V_{SIN} ≤ –50dBm, CPTENV=0	40	—	—	ms
t_{DD}	Detection Signal Time	—	In-band signal input, CPTENV=1	40	—	—	ms
t_B	Rejection Pause Time	—	V_{SIN} ≤ –50dBm, CPTENV=1	—	—	20	ms
t_{DH}	Envelope Output Delay Time	—	Time for high output	—	40	—	ms
t_{DI}		—	Time for low output	—	40	—	ms
t_{RD}	Rejection Noise Time	—	V_{SIN}=Any signal, CPTENV=0	—	—	20	ms
t_{ST}	Oscillator Start-up Time	—	—	—	0.8	2	sec
Z_I	Input Impedance	—	f_{IN}=200~3.4kHz	1.0	—	—	MΩ
V_{REF}	Reference Voltage	—	No load	2.4	2.5	2.6	V
Z_{REF}	Output Impedance	—	—	—	10	20	MΩ
V_{IH}	Logic Input High Voltage	5V	—	3.5	—	—	V
V_{IL}	Logic Input Low Voltage	5V	—	—	—	1.5	V
I_{IH}	Logic Input High Current	5V	V_{IH}=0.5V	—	—	0.1	μA
I_{IL}	Logic Input Low Current	5V	V_{IL}=0V	–0.1	—	—	μA
I_{OH}	Output High Current	5V	V_{OH}=4.5V	—	—	–0.5	mA
I_{OL}	Output Low Current	5V	V_{OL}=0.5V	2.0	—	—	mA
I_{SO}	Pull-down Current	5V	—	—	25	35	μA

Power-on Reset Characteristics

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
V_{POR}	VDD Start Voltage to Ensure Power-on Reset	—	—	—	—	0	mV
RR_{VDD}	VDD raising rate to Ensure Power-on Reset	—	—	0.05	—	—	V/ms
t_{POR}	Minimum Time for VDD Stays at V_{POR} to Ensure Power-on Reset	—	—	200	—	—	ms



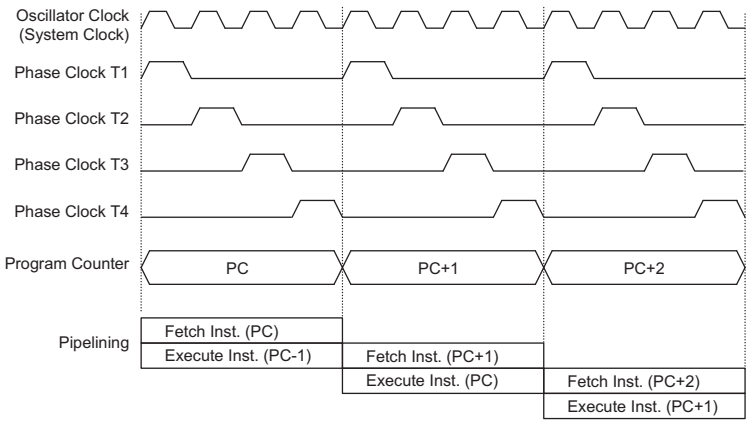
System Architecture

A key factor in the high-performance features of the Holtek range of microcontrollers is attributed to the internal system architecture. The range of devices take advantage of the usual features found within RISC microcontrollers providing increased speed of operation and enhanced performance. The pipelining scheme is implemented in such a way that instruction fetching and instruction execution are overlapped, hence instructions are effectively executed in one cycle, with the exception of branch or call instructions. An 8-bit wide ALU is used in practically all operations of the instruction set. It carries out arithmetic operations, logic operations, rotation, increment, decrement, branch decisions, etc. The internal data path is simplified by moving data through the Accumulator and the ALU. Certain internal registers are implemented in the Data Memory and can be directly or indirectly addressed. The simple addressing methods of these registers along with additional architectural features ensure that a minimum of external components is required to provide a functional I/O control system with maximum reliability and flexibility. This makes these devices suitable for low-cost, high-volume production for phone controller applications requiring up to 16K words of Program Memory and 2112 bytes of Data Memory storage.

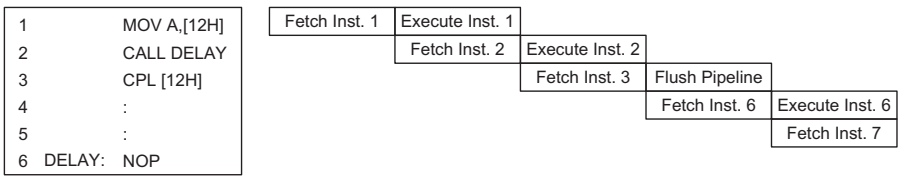
Clocking and Pipelining

The system clock is derived from an external 32768Hz Crystal/Resonator which then generates a high frequency on system clock using internal frequency-up converter circuitry. This internal clock is subdivided into four internally generated non-overlapping clocks, T1~T4. The Program Counter is incremented at the beginning of the T1 clock during which time a new instruction is fetched. The remaining T2~T4 clocks carry out the decoding and execution functions. In this way, one T1~T4 clock cycle forms one instruction cycle. Although the fetching and execution of instructions takes place in consecutive instruction cycles, the pipelining structure of the microcontroller ensures that instructions are effectively executed in one instruction cycle. The exception to this are instructions where the contents of the Program Counter are changed, such as subroutine calls or jumps, in which case the instruction will take one more instruction cycle to execute.

For instructions involving branches, such as jump or call instructions, two machine cycles are required to complete instruction execution. An extra cycle is required as the program takes one cycle to first obtain the actual jump or call address and then another cycle to actually execute the branch. The requirement for this extra cycle should be taken into account by programmers in timing sensitive applications.



System Clocking and Pipelining



Instruction Fetching

Program Counter

During program execution, the Program Counter is used to keep track of the address of the next instruction to be executed. It is automatically incremented by one each time an instruction is executed except for instructions, such as "JMP" or "CALL" that demand a jump to a non-consecutive Program Memory address. Only the lower 8 bits, known as the Program Counter Low Register, are directly addressable by user.

When executing instructions requiring jumps to non-consecutive addresses such as a jump instruction, a subroutine call, interrupt or reset, etc., the microcontroller manages program control by loading the required address into the Program Counter. For conditional skip instructions, once the condition has been met, the next instruction, which has already been fetched during the present instruction execution, is discarded and a dummy cycle takes its place while the correct instruction is obtained.

The lower byte of the Program Counter, known as the Program Counter Low register or PCL, is available for program control and is a readable and writable register. By transferring data directly into this register, a short program jump can be executed directly, however, as only this low byte is available for manipulation, the jumps are limited to the present page of memory, that is 256 locations. When such program jumps are executed it should also be noted that a dummy cycle will be inserted.

Stack

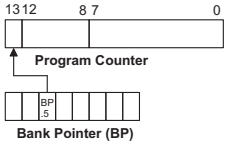
This is a special part of the memory which is used to save the contents of the Program Counter only. The stack has 8 levels and is neither part of the data nor part of the program space, and can neither be read from nor written to. The activated level is indexed by the Stack Pointer, SP, which can also neither be read from nor written to. At a subroutine call or interrupt acknowledge signal, the contents of the Program Counter are pushed onto the stack. At the end of a subroutine or an interrupt routine, signaled by a return instruction, RET or RETI, the Program Counter is restored to its previous value from the stack. After a device reset, the Stack Pointer will point to the top of the stack.

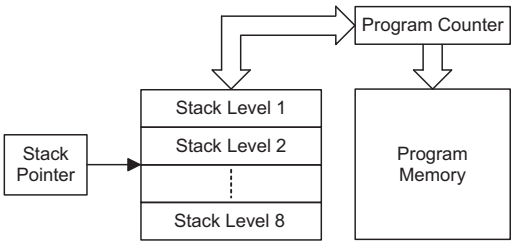
If the stack is full and an enabled interrupt takes place, the interrupt request flag will be recorded but the acknowledge signal will be inhibited. When the Stack Pointer is decremented, by RET or RETI, the interrupt will be serviced. This feature prevents stack overflow allowing the programmer to use the structure more easily. However, when the stack is full, a CALL subroutine instruction can still be executed which will result in a stack overflow. Precautions should be taken to avoid such cases which might cause unpredictable program branching.

Mode	Program Counter Bits													
	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Initial Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0
External Interrupt	0	0	0	0	0	0	0	0	0	0	0	1	0	0
Timer/Event Counter 0 Overflow	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Timer/Event Counter 1 Overflow	0	0	0	0	0	0	0	0	0	0	1	1	0	0
Peripheral Interrupt	0	0	0	0	0	0	0	0	0	1	0	0	0	0
RTC Interrupt	0	0	0	0	0	0	0	0	0	1	0	1	0	0
Multi-Function Interrupt	0	0	0	0	0	0	0	0	0	1	1	0	0	0
Skip	Program Counter + 2 (Within current bank)													
Loading PCL	PC13	PC12	PC11	PC10	PC9	PC8	@7	@6	@5	@4	@3	@2	@1	@0
Jump, Call Branch	BP.5	#12	#11	#10	#9	#8	#7	#6	#5	#4	#3	#2	#1	#0
Return from Subroutine	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0

Program Counter

Note: PC13~PC8: Current Program Counter bits
@7~@0: PCL bits
#12~#0: Instruction code address bits
S13~S0: Stack register bits
For the HT95R64, the Table address location is 13 bits,i.e. from b12~b0.
For the HT95R65, the Table address location is 14 bits,i.e. from b13~b0.
For the HT95R64, the BP5 bit is fixed at "0".





Arithmetic and Logic Unit – ALU

The arithmetic-logic unit or ALU is a critical area of the microcontroller that carries out arithmetic and logic operations of the instruction set. Connected to the main microcontroller data bus, the ALU receives related instruction codes and performs the required arithmetic or logical operations after which the result will be placed in the specified register. As these ALU calculation or operations may result in carry, borrow or other status changes, the status register will be correspondingly updated to reflect these changes. The ALU supports the following functions:

- Arithmetic operations ADD, ADDM, ADC, ADCM, SUB, SUBM, SBC, SBCM, DAA
- Logic operations AND, OR, XOR, ANDM, ORM, XORM, CPL, CPLA
- Rotation RRA, RR, RRCA, RRC, RLA, RL, RLCA, RLC
- Increment and Decrement INCA, INC, DECA, DEC
- Branch decision JMP, SZ, SZA, SNZ, SIZ, SDZ, SIZA, SDZA, CALL, RET, RETI

Program Memory

The Program Memory is the location where the user code or program is stored. For these devices the Program Memory is an OTP type, which means it can be programmed once.

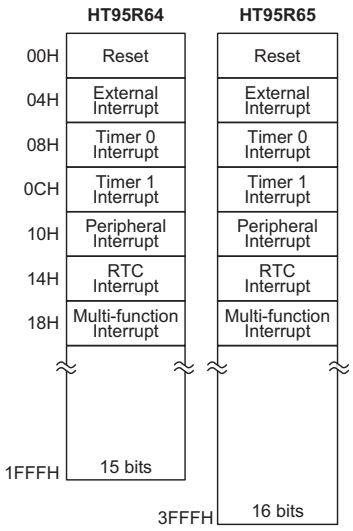
Device	Capacity
HT95R64	8K×16
HT95R65	16K×16

Structure

The Program Memory has a capacity of 8K×16 to 16K×16. The Program Memory is addressed by the Program Counter and also contains data, table information and interrupt entries. Table data, which can be setup in any location within the Program Memory, is addressed by a separate table pointer register.

Special Vectors

Within the Program Memory, certain locations are reserved for special usage such as reset and interrupts.



Program Memory Structure

- Location 000H
  This vector is reserved for use by the device reset for program initialisation. After a device reset is initiated, the program will jump to this location and begin execution.
- Location 004H
  This vector is used by the external interrupt. If the external interrupt pin on the device goes low, the program will jump to this location and begin execution if the external interrupt is enabled and the stack is not full.
- Location 008H
  This internal vector is used by the Timer/Event Counter 0. If a counter overflow occurs, the program will jump to this location and begin execution if the timer/event counter 0 interrupt is enabled and the stack is not full.
- Location 00CH
  This internal vector is used by the Timer/Event Counter 1. If a counter overflow occurs, the program will jump to this location and begin execution if the timer/event counter 1 interrupt is enabled and the stack is not full.
- Location 010H
  This internal vector is used by the DTMF receiver and FSK decoder. When the DTMF receiver and FSK decoder are enabled, if the DTMF receiver detects a valid character available or ring/line reversal is detected or FSK carrier is detected or FSK packet data is ready or FSK raw data has a falling edge, the program will jump to this location and begin execution if the peripheral interrupt is enabled and the stack is not full.
- Location 014H
  This location is used by the RTC. When the RTC is enabled and a time-out occurs, the program will jump to this location and begin execution if the RTC interrupt is enabled and the stack is not full.

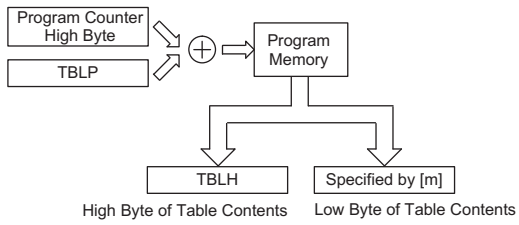
- Location 018H
  This location is used by the Multi-function Interrupt. If a falling edge transition is detected on PC0 or PC5, or a rising edge transition is detected on PC7 or an SPI/I2C interrupt occurs, or an external peripheral falling edge transition, or a timer 2 overflow, the program will jump to this location and begin execution if the multi-function interrupt is enabled and the stack is not full.

Look-up Table

Any location within the Program Memory can be defined as a look-up table where programmers can store fixed data. To use the look-up table, the table pointer must first be setup by placing the lower order address of the look up data to be retrieved in the table pointer register. This register defines the lower 8-bit address of the look-up table.

After setting up the table pointer, the table data can be retrieved from the current Program Memory page or last Program Memory page using the "TABRDC[m]" or "TABRDL [m]" instructions, respectively. When these instructions are executed, the lower order table byte from the Program Memory will be transferred to the user defined Data Memory register [m] as specified in the instruction. The higher order table data byte from the Program Memory will be transferred to the TBLH special register. Any unused bits in this transferred higher order byte will have uncertain values.

The following diagram illustrates the addressing/data flow of the look-up table:



Look-up Table

Table Program Example

The following example shows how the table pointer and table data is defined and retrieved from the device. This example uses raw table data located in the last page which is stored there using the ORG statement. The value at this ORG statement is "3F00H" which refers to the start address of the last page within the 16K Program Memory of the microcontroller. The table pointer is setup here to have an initial value of "06H". This will ensure that the first data read from the data table will be at the Program Memory address "3F06H" or 6 locations after the start of the last page. Note that the value for the table pointer is referenced to the first address of the present page if the "TABRDC [m]" instruction is being used. The high byte of the table data which in this case is equal to zero will be transferred to the TBLH register automatically when the "TABRDL [m]" instruction is executed.

Because the TBLH register is a read-only register and cannot be restored, care should be taken to ensure its protection if both the main routine and Interrupt Service Routine use table read instructions. If using the table read instructions, the Interrupt Service Routines may change the value of the TBLH and subsequently cause errors if used again by the main routine. As a rule it is recommended that simultaneous use of the table read instructions should be avoided. However, in situations where simultaneous use cannot be avoided, the interrupts should be disabled prior to the execution of any main routine table-read instructions. Note that all table related instructions require two instruction cycles to complete their operation.

Instruction	Table Location Bits													
	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
TABRDC [m]	PC13	PC12	PC11	PC10	PC9	PC8	@7	@6	@5	@4	@3	@2	@1	@0
TABRDL [m]	1	1	1	1	1	1	@7	@6	@5	@4	@3	@2	@1	@0

Table Location

Note: For the HT95R64, the Table address location is 13 bits,i.e. from b12~b0.
For the HT95R65, the Table address location is 14 bits,i.e. from b13~b0.
PC13~PC8: Current Program Counter bits
@7~@0: Table Pointer Lower-order bits (TBLP)

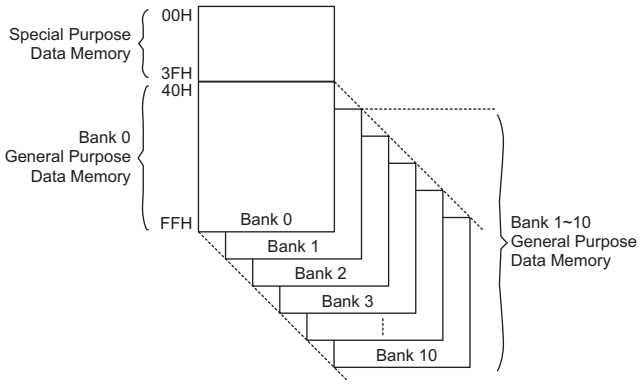
```
tempreg1    db      ?       ; temporary register #1
tempreg2    db      ?       ; temporary register #2
            :
            :

mov         a,06h           ; initialise table pointer - note that this address
                            ; is referenced

mov         tblp,a          ; to the last page or present page
            :
            :

tabrdl      tempreg1        ; transfers value in table referenced by table pointer
                            ; to tempreg1
                            ; data at prog. memory address "3F06H" transferred to
                            ; tempreg1 and TBLH

dec         tblp            ; reduce value of table pointer by one

tabrdl      tempreg2        ; transfers value in table referenced by table pointer
                            ; to tempreg2
                            ; data at prog.memory address "3F05H" transferred to
                            ; tempreg2 and TBLH
                            ; in this example the data "1AH" is transferred to
                            ; tempreg1 and data "0FH" to register tempreg2
                            ; the value "0FH" will be transferred to the high byte
                            ; register TBLH
            :
            :

org         3F00h           ; sets initial address of the last page

dc          00Ah, 00Bh, 00Ch, 00Dh, 00Eh, 00Fh, 01Ah, 01Bh
            :
            :
```

Data Memory

The Data Memory is a volatile area of 8-bit wide RAM internal memory and is the location where temporary information is stored. Divided into two sections, the first of these is an area of RAM where special function registers are located. These registers have fixed locations and are necessary for correct operation of the device. Many of these registers can be read from and written to directly under program control, however, some remain protected from user manipulation. The second area of RAM Data Memory is reserved for general purpose use. All locations within this area are read and write accessible under program control.

Structure

The Special Purpose and General Purpose Data Memory are located at consecutive locations. All are implemented in RAM and are 8 bits wide. The start address of the Data Memory is the address 00H. Registers which are common to all microcontrollers, such as ACC, PCL, etc., have the same Data Memory address. Note that after power-on, the contents of the Data Memory, will be in an unknown condition, the programmer must therefore ensure that the Data Memory is properly initialised. The Special Purpose Data Memory is located in Bank 0 while the General Purpose Data Memory is divided into 11 individual areas or Banks known as Bank 0 to Bank 10. Switching between different banks is achieved by setting the Bank Pointer to the correct value.



Data Memory Structure

General Purpose Data Memory

All microcontroller programs require an area of read/write memory where temporary data can be stored and retrieved for use later. It is this area of RAM memory that is known as General Purpose Data Memory. This area of Data Memory is fully accessible by the user program for both read and write operations. By using the ″SET [m].i″ and ″CLR [m].i″ instructions, individual bits can be set or reset under program control giving the user a large range of flexibility for bit manipulation in the Data Memory. As the General Purpose Data Memory is located within 11 different banks, it is first necessary to ensure that the Bank Pointer is properly set to the correct value before accessing the General Purpose Data Memory. Only Bank 0 data can be read directly. Indirect Addressing of Bank 0 is executed using Indirect Addressing Register IAR0 and Memory Pointer MP0. Data in Banks 1~10 can only be read indirectly using Indirect Addressing Register IAR1 and Memory Pointer MP1.

Special Purpose Data Memory

This area of Data Memory is where registers, necessary for the correct operation of the microcontroller, are stored. Most of the registers are both readable and writeable but some are protected and are readable only, the details of which are located under the relevant Special Function Register section. Note that for locations that are unused, any read instruction to these addresses will return the value ″00H″. Although the Special Purpose Data Memory registers are located in Bank 0, they will still be accessible even if the Bank Pointer has selected Banks 1~10.

Special Function Registers

To ensure successful operation of the microcontroller, certain internal registers are implemented in the RAM Data Memory area. These registers ensure correct operation of internal functions such as timers, interrupts, watchdog, etc., as well as external functions such as I/O data control. The location of these registers within the RAM Data Memory begins at the address ″00H″. Any unused Data Memory locations between these special function registers and the point where the General Purpose Memory begins is reserved for future expansion purposes, attempting to read data from these locations will return a value of ″00H″.

Indirect Addressing Register – IAR0, IAR1

The Indirect Addressing Registers, IAR0 and IAR1, although having their locations in normal RAM register space, do not actually physically exist as normal registers. The method of indirect addressing for RAM data manipulation uses these Indirect Addressing Registers and Memory Pointers, in contrast to direct memory addressing, where the actual memory address is specified. Actions on the IAR0 and IAR1 registers will result in

00H	IAR0
01H	MP0
02H	IAR1
03H	MP1
04H	BP
05H	ACC
06H	PCL
07H	TBLP
08H	TBLH
09H	WDTS
0AH	STATUS
0BH	INTC0
0CH	TMR0H
0DH	TMR0L
0EH	TMR0C
0FH	TMR1H
10H	TMR1L
11H	TMR1C
12H	PA
13H	PAC
14H	
15H	
16H	PC
17H	PCC
18H	PD
19H	PDC
1AH	PE
1BH	PEC
1CH	
1DH	
1EH	INTC1
1FH	
20H	DTMFC
21H	DTMFD
22H	DTRXC
23H	DTRXD
24H	RTCC
25H	MODE_1
26H	MODE
27H	SIMCTL0
28H	SIMCTL1
29H	SIMDR
2AH	SIMAR/SIMCTL2
2BH	SCOMC
2CH	MFIC0
2DH	MFIC1
2EH	PFDC
2FH	PFDD
30H	VOICEC
31H	DAL
32H	DAH
33H	VOL
34H	PF
35H	PFC
36H	
37H	
38H	TMR2H
39H	TMR2L
3AH	TMR2C
3BH	FSKC
3CH	FSKS
3DH	FSKD
3EH	LBDC
3FH	PERIC
40H ... FFH	

: Unused byte, read as "00"

Special Purpose Data Memory Structure

no actual read or write operation to these registers but rather to the memory location specified by their corresponding Memory Pointer, MP0 or MP1. Acting as a pair, IAR0 and MP0 can together only access data from Bank 0, while the IAR1 and MP1 register pair can access data from both Bank 0 and Bank 1. As the Indirect Addressing Registers are not physically implemented, reading the Indirect Addressing Registers indirectly will return a result of "00H" and writing to the registers indirectly will result in no operation.

Memory Pointer – MP0, MP1

For all devices, two Memory Pointers, known as MP0 and MP1 are provided. These Memory Pointers are physically implemented in the Data Memory and can be manipulated in the same way as normal registers providing a convenient way with which to address and track data. When any operation to the relevant Indirect Addressing Registers is carried out, the actual address that the microcontroller is directed to, is the address specified by the related Memory Pointer. MP0, together with Indirect Addressing Register, IAR0, are used to access data from Bank 0 only, while MP1 and IAR1 are used to access data from Banks 1~10.

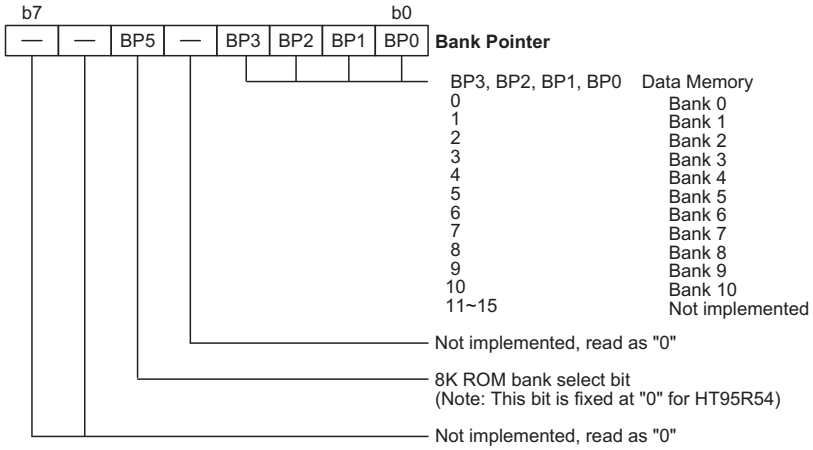
The following example shows how to clear a section of four RAM locations already defined as locations adres1 to adres4.

```
data .section  'data'
adres1       db ?
adres2       db ?
adres3       db ?
adres4       db ?
block        db ?
code .section at 0 'code'
org   00h

start:
            mov a,04h          ; setup size of block
            mov block,a
            mov a,offset adres1; Accumulator loaded with first RAM address
            mov mp0,a          ; setup memory pointer with first RAM address

loop:
            clr IAR0           ; clear the data at address defined by MP0
            inc mp0            ; increment memory pointer
            sdz block          ; check if last memory location has been cleared
            jmp loop

continue:
```

The important point to note here is that in the example shown above, no reference is made to specific RAM addresses.

Bank Pointer – BP

The Data Memory RAM is divided into eleven banks, known as Bank 0~Bank 10. All of the Special Purpose Registers are contained in Bank 0. Selecting the required Data Memory area is achieved using the Bank Pointer. If data in Bank 0 is to be accessed, then the BP register must be loaded with the value "00", while if data in Bank 1 is to be accessed, then the BP register must be loaded with the value "01" and so on for the other registers. Using Memory Pointer MP0 and Indirect Addressing Register IAR0 will always access data from Bank 0, irrespective of the value of the Bank Pointer.



Bank Pointer

The Data Memory is initialised to Bank 0 after a reset, except for a WDT time-out reset in the Power Down Mode, in which case, the Data Memory bank remains unaffected. It should be noted that Special Function Data Memory is not affected by the bank selection, which means that the Special Function Registers can be accessed from Bank 0 to Bank 10. Directly addressing the Data Memory will always result in Bank 0 being accessed irrespective of the value of the Bank Pointer.

Accumulator – ACC

The Accumulator is central to the operation of any microcontroller and is closely related with operations carried out by the ALU. The Accumulator is the place where all intermediate results from the ALU are stored. Without the Accumulator it would be necessary to write the result of each calculation or logical operation such as addition, subtraction, shift, etc., to the Data Memory resulting in higher programming and timing overheads. Data transfer operations usually involve the temporary storage function of the Accumulator; for example, when transferring data between one user defined register and another, it is necessary to do this by passing the data through the Accumulator as no direct transfer between two registers is permitted.

Program Counter Low Register – PCL

To provide additional program control functions, the low byte of the Program Counter is made accessible to programmers by locating it within the Special Purpose area of the Data Memory. By manipulating this register, direct jumps to other program locations are easily implemented. Loading a value directly into this PCL register will cause a jump to the specified Program Memory location, however, as the register is only 8-bit wide, only jumps within the current Program Memory page are permitted. When such operations are used, note that a dummy cycle will be inserted.

Look-up Table Registers – TBLP, TBLH

These two special function registers are used to control operation of the look-up table which is stored in the Program Memory. TBLP is the table pointer and indicates the location where the table data is located. Its value must be setup before any table read commands are executed. Its value can be changed, for example using the ″INC″ or ″DEC″ instructions, allowing for easy table data pointing and reading. TBLH is the location where the high order byte of the table data is stored after a table read data instruction has been executed. Note that the lower order table data byte is transferred to a user defined location.

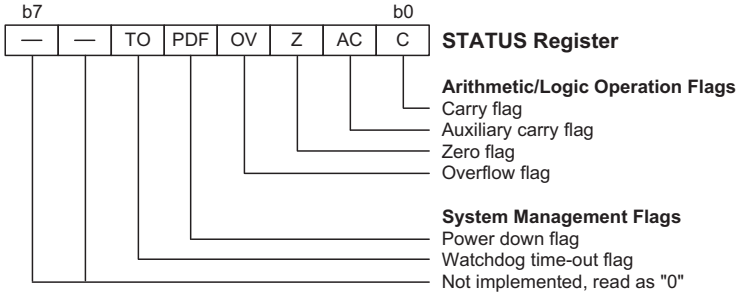
Watchdog Timer Register – WDTS

The Watchdog feature of the microcontroller provides an automatic reset function giving the microcontroller a means of protection against spurious jumps to incorrect Program Memory addresses. To implement this, a timer is provided within the microcontroller which will issue a reset command when its value overflows. To provide variable Watchdog Timer reset times, the Watchdog Timer clock source can be divided by various division ratios, the value of which is set using the WDTS register. By writing directly to this register, the appropriate division ratio for the Watchdog Timer clock source can be setup. Note that only the lower 3 bits are used to set division ratios between 1 and 128.

Status Register – STATUS

This 8-bit register contains the zero flag (Z), carry flag (C), auxiliary carry flag (AC), overflow flag (OV), power down flag (PDF), and watchdog time-out flag (TO). These arithmetic/logical operation and system management flags are used to record the status and operation of the microcontroller.

With the exception of the TO and PDF flags, bits in the status register can be altered by instructions like most other registers. Any data written into the status register will not change the TO or PDF flag. In addition, operations related to the status register may give different results due to the different instruction operations. The TO flag can be affected only by a system power-up, a WDT time-out or by executing the ″CLR WDT″ or ″HALT″ instruction. The PDF flag is affected only by executing the ″HALT″ or ″CLR WDT″ instruction or during a system power-up.



Status Register

The Z, OV, AC and C flags generally reflect the status of the latest operations.

- **C** is set if an operation results in a carry during an addition operation or if a borrow does not take place during a subtraction operation; otherwise C is cleared. C is also affected by a rotate through carry instruction.
- **AC** is set if an operation results in a carry out of the low nibbles in addition, or no borrow from the high nibble into the low nibble in subtraction; otherwise AC is cleared.
- **Z** is set if the result of an arithmetic or logical operation is zero; otherwise Z is cleared.
- **OV** is set if an operation results in a carry into the highest-order bit but not a carry out of the highest-order bit, or vice versa; otherwise OV is cleared.
- **PDF** is cleared by a system power-up or executing the ″CLR WDT″ instruction. PDF is set by executing the ″HALT″ instruction.
- **TO** is cleared by a system power-up or executing the ″CLR WDT″ or ″HALT″ instruction. TO is set by a WDT time-out.

In addition, on entering an interrupt sequence or executing a subroutine call, the status register will not be pushed onto the stack automatically. If the contents of the status registers are important and if the subroutine can corrupt the status register, precautions must be taken to correctly save it.

Interrupt Control Register – INTC0, INTC1

These two 8-bit register, known as the INTC0 and INTC1 registers, control the operation of all interrupts. By setting various bits within this register using standard bit manipulation instructions, the enable/disable function of the external and timer interrupts can be independently controlled. A master interrupt bit within this register, the EMI bit, acts like a global enable/disable and is used to set all of the interrupt enable bits on or off. This bit is cleared when an interrupt routine is entered to disable further interrupt and is set by executing the ″RETI″ instruction.

Timer/Event Counter Registers

This device contains three 16-bit Timer/Event Counters, which have associated register pairs known as TMR0L/TMR0H, TMR1L/TMR1H and TMR2L/TMR2H. These are the locations where the timers 16-bit value is located. Three associated control registers, known as TMR0C, TMR1C and TMR2C, contain the setup information for these three timers.

Input/Output Ports and Control Registers

Within the area of Special Function Registers, the I/O registers and their associated control registers play a prominent role. All I/O ports have a designated register correspondingly labeled as PA, PC, PD, PE and PF. These labeled I/O registers are mapped to specific addresses within the Data Memory as shown in the Data Memory table, which are used to transfer the appropriate output or input data on that port. With each I/O port there is an associated control register labeled PAC, PCC, PDC, PEC and PFC, also mapped to specific addresses with the Data Memory. Except PC2 and PC3, the control register specifies which pins of that port are set as inputs and which are set as outputs. PC2 or PC3 are NMOS outputs, so the corresponding bits of the control register are not implemented. To setup a pin as an input, the corresponding bit of the control register must be set high and for an output it must be set low. During program initialisation, it is important to first setup the control registers to specify which pins are outputs and which are inputs before reading data from or writing data to the I/O ports. One flexible feature of these registers is the ability to directly program single bits using the ″SET [m].i″ and ″CLR [m].i″ instructions. The ability to change I/O pins from output to input and vice versa by manipulating specific bits of the I/O control registers during normal program operation is a useful feature of these devices.

DTMF Registers – DTMFC, DTMFD, DTRXC, DTRXD

The device contains a fully integrated DTMF receiver and generator circuitry for decoding and generation of DTMF signals. The DTMF receiver requires two registers to control its operation, a DTRXC control register to control its overall function and a DTRXD register to store the DTMF decoded signal data. The DTMF generator also requires two registers for its operation, a DTMFC register for its overall control and DTMFD register to store the digital codes that are to be generated as DMTF signals.

FSK Registers – FSKC, FSKS, FSKD, PERIC

The device contains a fully integrated FSK decoder. The FSK interrupt function is controlled by two registers, PERIC and FSKC. The FSKS register is for the designer to check the interrupt status and a FSKD resister to store the decoded FSK cooked data.

Mode Register – MODE, MODE_1

The device supports two system clocks and four operation modes. The system clock can be ether a low frequency 32768Hz oscillator or a high frequency HCLK oscillator. The operation modes can be either Normal, Green, Sleep or Idle. These are all selected using software. MODE_1 register supports four high frequency clocks (HCLK) for the MCU which are 3.58MHz, 7.16MHz, 10.74MHz and 14.32 MHz.

MFIC Register – MFIC0

PC0, PC5 and PC7 can be used to trigger an extra interrupt. They are enabled or disabled individually by bit0~bit2 of MFIC0. When a multi-function interrupt oc-

curs, the programmer should check bit4~bit6 of MFIC0 to determine the cause of the interrupt.

MFIC1 Register – MFIC1

The SPI/I^2C interrupt, external peripheral interrupt, timer 2 interrupt are three additional multi-function interrupts. They are enabled or disabled individually by bit0~2 of MFIC1. When a multi-function interrupt occurs, the programmer should check bit4~bit6 of MFIC1 to determine the cause of the interrupt.

PFD Registers – PFDC/PFDD

The device contains a Programmable Frequency Divider function which can generate accurate frequencies based on the system clock. The clock source, enable function and output frequency is controlled using these two registers.

RTCC Register

The device contains a Real Time Clock function otherwise known as the RTC. To control this function a register known as the RTCC register is provided which provides the overall on/off control and time out flag.

DAC Registers – VOICEC/VOL/DAL/DAH

These four registers are for 12-bit DAC output data and volume control.

Low Battery Detect Register – LBDC

This register is to control the LBD function and to report the low battery status.

Software COM Register – SCOMC

The pins PD0~PD3 on Port D can be used as SCOM lines to drive an external LCD panel. To implement this function, the SCOMC register is used to setup the correct bias voltages on these pins.

Input/Output Ports

Holtek microcontrollers offer considerable flexibility on their I/O ports. With the input or output designation of every pin fully under user program control, pull-high options for all ports and wake-up options on certain pins, the user is provided with an I/O structure to meet the needs of a wide range of application possibilities. The device provides bidirectional input/output lines labeled with port names PA, PC, PD, PE and PF. These I/O ports are mapped to the Data Memory with specific addresses as shown in the Special Purpose Data Memory table. All of these I/O ports can be used for input and output operations. For input operation, these ports are non-latching, which means the inputs must be ready at the T2 rising edge of instruction "MOV A,[m]", where m denotes the port address. For output operation, all the data is latched and remains unchanged until the output latch is rewritten.

Unlike the other port lines, PC2 and PC3 are NMOS type output-only lines. They have neither pull high option nor a port control bit.

Pull-high Resistors

Many product applications require pull-high resistors for their switch inputs usually requiring the use of an external resistor. To eliminate the need for these external resistors, all I/O pins, when configured as an input have the capability of being connected to an internal pull-high resistor. These pull-high resistors are selectable via configuration options and are implemented using a weak PMOS transistor.

Port A Wake-up

Each device has a HALT instruction enabling the microcontroller to enter a Power Down Mode and preserve power, a feature that is important for battery and other low-power applications. Various methods exist to wake-up the microcontroller, one of which is to change the logic condition on one of the Port A pins from high to low. After a "HALT" instruction forces the microcontroller into entering the Power Down mode, the device will remain idle or in a low-power state until the logic condition of the selected wake-up pin on Port A changes from high to low. This function is especially suitable for applications that can be woken up via external switches. Note that each pin on Port A can be selected individually to have this wake-up feature.

I/O Port Control Registers

Each I/O port has its own control register PAC, PCC, PDC, PEC and PFC, to control the input/output configuration. with this control register, each CMOS output or input with or without pull-high resistor structures can be reconfigured dynamically under software control. Each pin of the I/O ports is directly mapped to a bit in its associated port control register. For the I/O pin to function as an input, the corresponding bit of the control register must be written as a "1". This will then allow the logic state of the input pin to be directly read by instructions. When the corresponding bit of the control register is written as a "0", the I/O pin will be setup as a CMOS output. If the pin is currently setup as an output, instructions can still be used to read the output register. However, it should be noted that the program will in fact only read the status of the output data latch and not the actual logic status of the output pin.

I/O Pin Structures

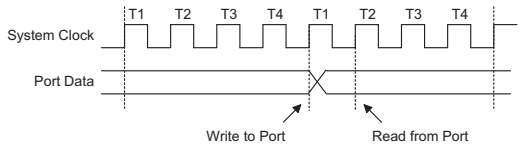
The following diagrams illustrate the I/O pin internal structures. As the exact logical construction of the I/O pin may differ from these drawings, they are supplied as a guide only to assist with the functional understanding of the I/O pins.

TMR0/1 pins

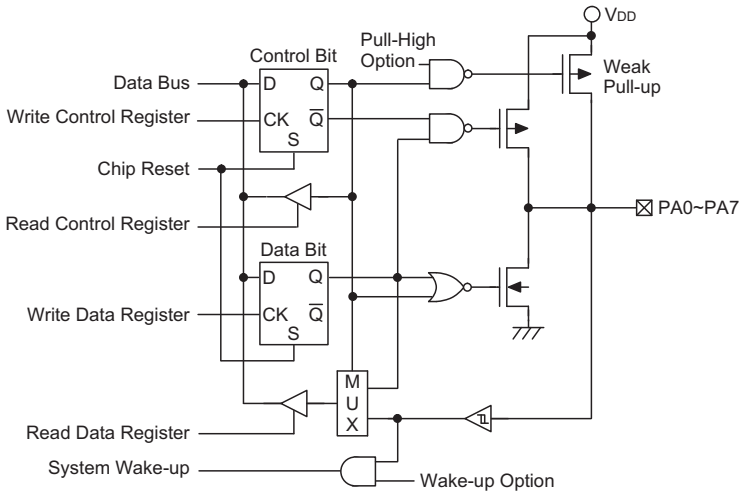
Pin PC4 and PC6 are pin-shared with the external timer input pin TMR0 and TMR1 respectively. For these pin-shared pins to function as timer inputs, the corresponding control bits in the timer control register must be correctly set. For applications that do not require an external timer input, the pin can be used as a normal I/O pin. Note that if used as a normal I/O pin the timer mode control bits in the timer control register must select the timer mode, which has an internal clock source, to prevent the input pin from interfering with the timer operation.

Programming Considerations

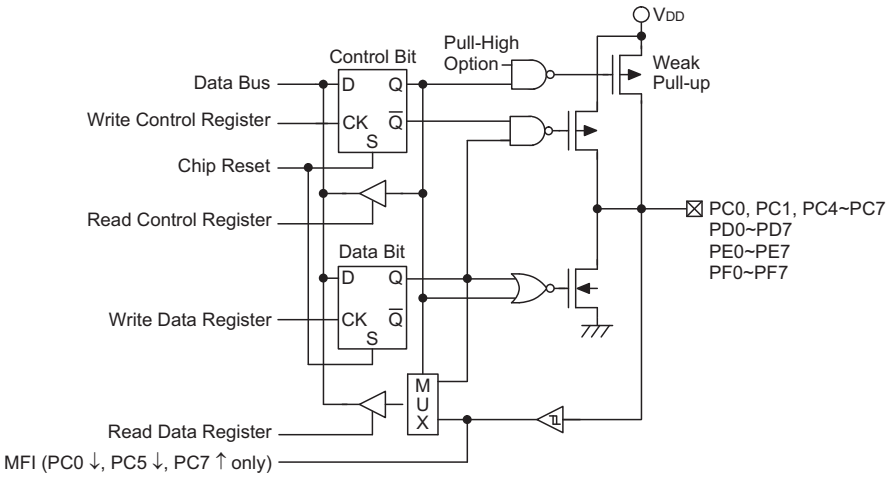
Within the user program, one of the first things to consider is port initialization. After a reset, all of the I/O data and port control registers will be set high. This means that all I/O pins will default to an input state, the level of which depends on the other connected circuitry and whether pull-high options have been selected. If the port control registers, PAC, PCC, PDC, PEC and PFC, are then programmed to setup some pins as outputs, these output pins will have an initial high output value unless the associated port data registers, PA, PC, PD, PE and PF, are first programmed. Selecting which pins are inputs and which are outputs can be achieved byte-wide by loading the correct values into the appropriate port control register or by programming individual bits in the port control register using the "SET [m].i" and "CLR [m].i" instructions. Note that when using these bit control instructions, a read-modify-write operation takes place. The microcontroller must first read in the data on the entire port, modify it to the required new bit values and then rewrite this data back to the output ports.



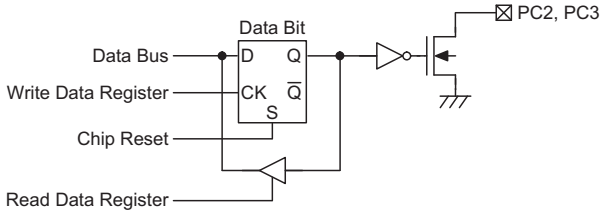
Read/Write Timing



PA Input/Output Port



PC (Except for PC2 and PC3), PD and PE Input/Output Ports



PC2, PC3 NMOS Output Port

Port A has the additional capability of providing wake-up functions. When the device is in the Power Down Mode, various methods are available to wake the device up. One of these is a high to low transition of any of the Port A pins. Single or multiple pins on Port A can be setup to have this function.

Timer/Event Counters

The provision of timers form an important part of any microcontroller, giving the designer a means of carrying out time related functions. The device contains three count-up timers of 16-bit capacity. Timer0 and Timer1 have three different operating modes, they can be configured to operate as a general timer, an external event counter or as a pulse width measurement device. Timer2 can be configured to operate in the timer mode only.

There are two types of registers related to the Timer/Event Counters. The first are the registers that contains the actual value of the Timer/Event Counter and into which an initial value can be preloaded, and are known as TMR0L/TMR0H, TMR1L/TMR1H and TMR2L/TMR2H. Reading these register pairs retrieves the contents of the Timer/Event Counters. The second type of associated register are the Timer Control Registers, which defines the timer options and determines how the Timer/Event Counters are to be used, and have the name TMR0C, TMR1C and TMR2C, Timer0 and Timer1 can have the timer clock configured to come from the internal clock source or from an external timer pin. Timer2 can have the timer clock come from internal system clock only.

Configuring the Timer/Event Counter Input Clock Source

For Timer/Event Counter 0, the internal timer clock source can originate from either the system clock/4 or from an external clock source. For Timer/Event Counter 1, the internal timer clock source can originate from the 32768Hz or from an external clock source.

An external clock source is used when the timer is in the event counting mode, the clock source being provided on the external timer pins TMR0 or TMR1. Depending upon the condition of the T0E or T1E bit, each high to low, or low to high transition on the external timer pin will increment the counter by one.

Timer Registers – TMR0L/TMR0H, TMR1L/TMR1H, TMR2L/TMR2H

The timer registers are special function register pairs located in the Special Purpose Data Memory and is the place where the 16-bit actual timer value is stored. These register pairs are known as TMR0L/TMR0H, TMR1L/TMR1H and TMR2L/TMR2H. The value in the timer register pair increases by one each time an internal clock pulse is received or an external transition occurs on the external timer pin. The timer will count from the initial value loaded by the preload register to the full count of FFFFH at which point the timer overflows and an internal interrupt signal is generated. The timer value will then be reset with the initial preload register value and continue counting.

To achieve a maximum full range count of FFFFH the preload register must first be cleared to all zeros. It should be noted that after power-on, the preload register will be in an unknown condition. Note that if the Timer/Event Counter is switched off and data is written to its preload register, this data will be immediately written into the actual timer register. However, if the Timer/Event Counter is enabled and counting, any new data written into the preload data register during this period will remain in the preload register and will only be written into the timer register the next time an overflow occurs.

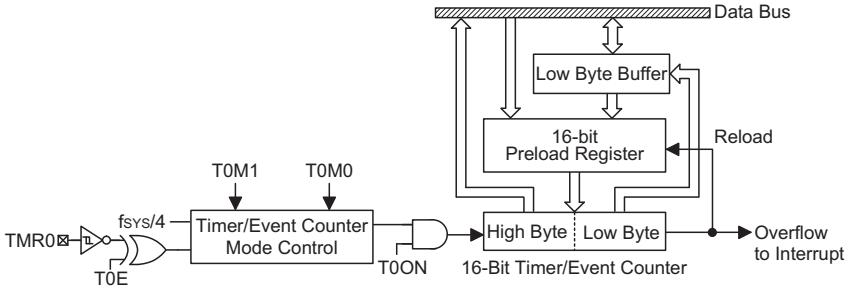
Reading from and writing to these registers is carried out in a specific way. It must be noted that when using instructions to preload data into the low byte register, namely TMR0L, TMR1L or TMR2L, the data will only be placed in a low byte buffer and not directly into the low byte register. The actual transfer of the data into the low byte register is only carried out when a write to its associated high byte register, namely TMR0H, TMR1H or TMR2H, is executed. Also, using instructions to preload data into the high byte timer register will result in the data being directly written to the high byte register. At the same time the data in the low byte buffer will be transferred into its associated low byte register. For this reason, when preloading data into the 16-bit timer registers, the low byte should be written first. It must also be noted that to read the contents of the low byte register, a read to the high byte register must first be executed to latch the contents of the low byte buffer from its associated low byte register. After this has been done, the low byte register can be read in the normal way. Note that

reading the low byte timer register directly will only result in reading the previously latched contents of the low byte buffer and not the actual contents of the low byte timer register.

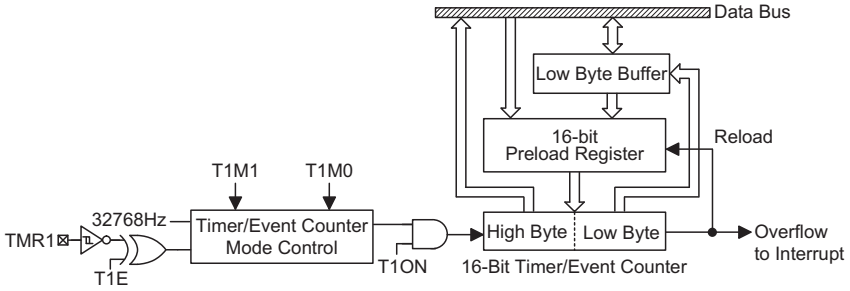
Timer Control Registers – TMR0C, TMR1C, TMR2C

The flexible features of the Holtek microcontroller Timer/Event Counters enable them to operate in three different modes, the options of which are determined by the contents of their control register, which has the name TMR0C/TMR1C/TMR2C. It is the Timer Control Register together with its corresponding timer register pair that control the full operation of each Timer/Event Counter. Before the Timer/Event Counter can be used, it is essential that the Timer Control Register is fully programmed with the right data to ensure its correct operation, a process that is normally carried out during program initialisation.

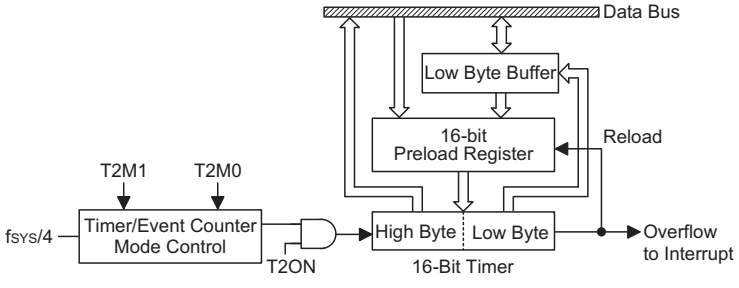
To choose which of the three modes the Timer/Event Counter is to operate in, either in the timer mode, the event counting mode or the pulse width measurement mode, bits 7 and 6 of the Timer Control Register, which are known as the bit pair T0M1/T0M0, T1M1/T1M0 and T2M1/T2M0, must be set to the required logic levels. The Timer/Event Counter on/off bit, which is bit 4 of the Timer Control Register, and known as T0ON, T1ON and T2ON, provides the basic on/off control of the Timer/Event Counter. Setting the bit high allows the Timer/Event Counter to run, clearing the bit stops it running. If the Timer/Event Counter is in the event count or pulse width measurement mode, the active transition edge level type is selected by the logic level of bit 3 of the Timer Control Register which is known as T0E and T1E.



16-bit Timer/Event Counter 0 Structure



16-bit Timer/Event Counter 1 Structure



16-bit Timer2 Structure

Configuring the Timer Mode

In this mode, the Timer/Event Counters can be utilised to measure fixed time intervals, providing an internal interrupt signal each time the Timer/Event Counter overflows. To operate in this mode, the Operating Mode Select bit pair in the Timer Control Register must be set to the correct value as shown.

Control Register Operating Mode Select Bits for the Timer Mode	Bit7	Bit6
	1	0

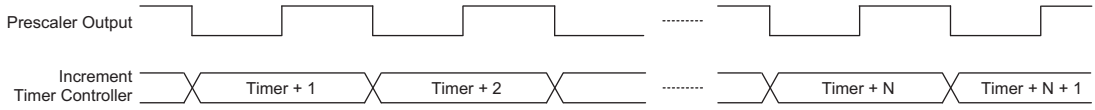
In this mode the internal clock, is used as the Timer/Event Counter clock. After the other bits in the Timer Control Register have been setup, the enable bit, which is bit 4 of the Timer Control Register, can be set high to enable the Timer/Event Counter to run. Each time an internal clock cycle occurs, the Timer/Event Counter increments by one. When it is full and overflows, an interrupt signal is generated and the Timer/Event Counter will reload the value already loaded into the preload register and continue counting. The interrupt can be disabled by ensuring that the Timer/Event Counter Interrupt Enable bit in the Interrupt Control Register, is reset to zero.

Configuring the Event Counter Mode

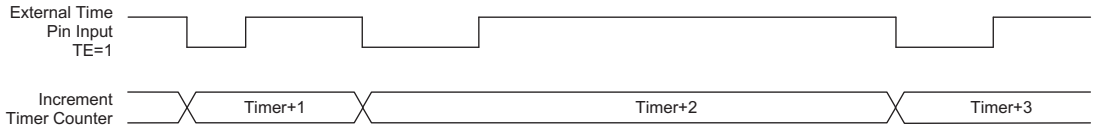
In this mode, a number of externally changing logic events, occurring on the external timer pin, can be recorded by the Timer/Event Counter. To operate in this mode, the Operating Mode Select bit pair in the Timer Control Register must be set to the correct value as shown.

Control Register Operating Mode Select Bits for the Event Counter Mode	Bit7	Bit6
	0	1

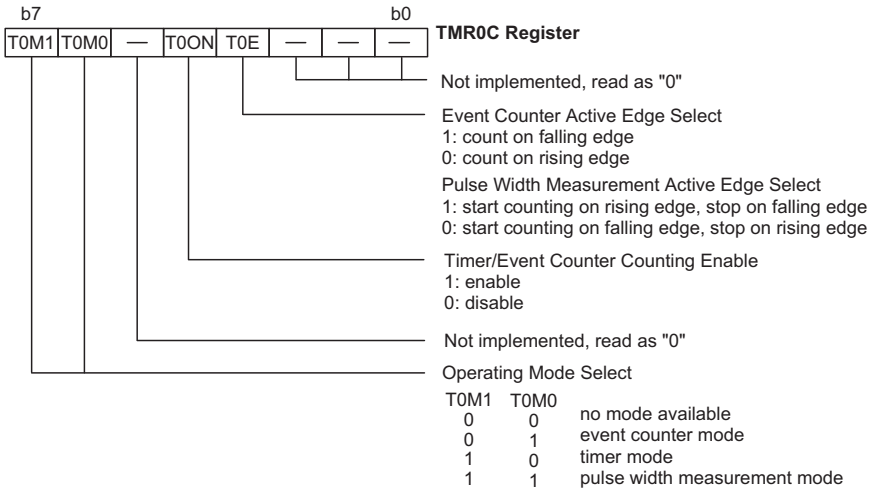
In this mode the external timer pin is used as the Timer/Event Counter clock source, however it is not divided by the internal prescaler. After the other bits in the Timer Control Register have been setup, the enable bit, which is bit 4 of the Timer Control Register, can be set high to enable the Timer/Event Counter to run. If the Active Edge Select bit, which is bit 3 of the Timer Control Register, is low, the Timer/Event Counter will increment each time the external timer pin receives a low to high transition. If the Active Edge Select bit is high, the counter will increment each time the external timer pin receives a high to low transition. When it is full and overflows, an interrupt signal is generated and the



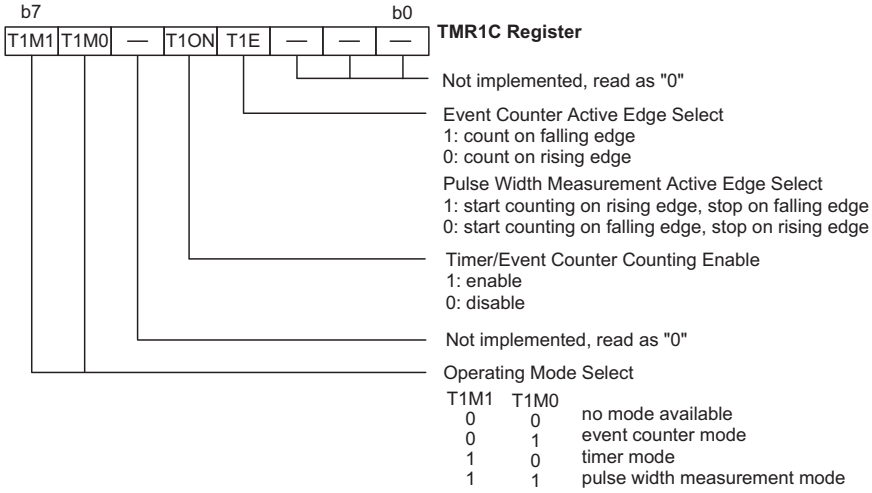
Timer Mode Timing Diagram



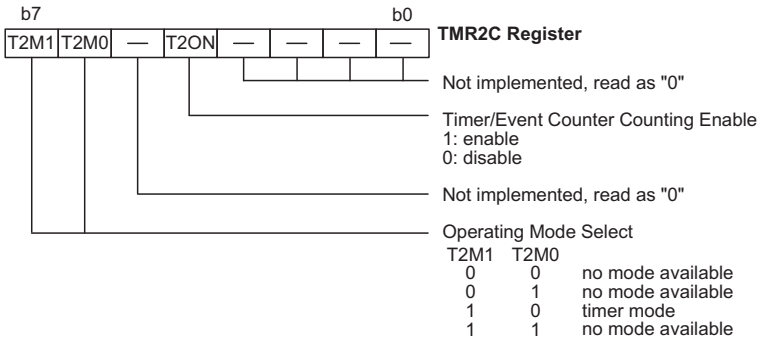
Event Counter Mode Timing Diagram



Timer/Event Counter 0 Control Register



Timer/Event Counter 1 Control Register



Timer2 Control Register

Timer/Event Counter will reload the value already loaded into the preload register and continue counting. The interrupt can be disabled by ensuring that the Timer/Event Counter Interrupt Enable bit in the Interrupt Control Register, is reset to zero.

To ensure that the timer pin is configured to operate as an event counter input pin the Timer Control Register must place the Timer/Event Counter in the Event Counting Mode. It should be noted that in the event counting mode, even if the microcontroller is in the Power Down Mode, the Timer/Event Counter will continue to record externally changing logic events on the timer input pin. As a result when the timer overflows it will generate a timer interrupt and corresponding wake-up source.

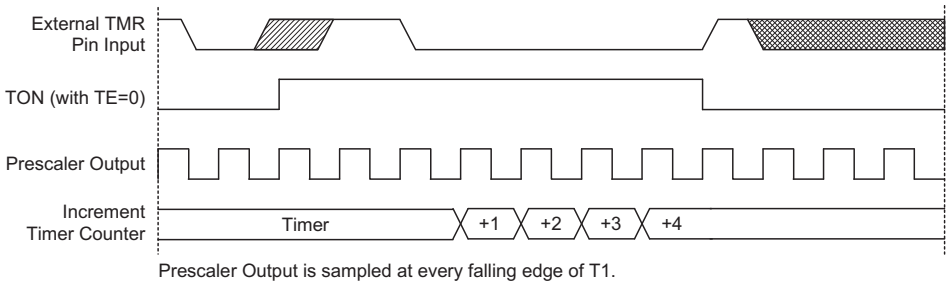
Configuring the Pulse Width Measurement Mode

In this mode, the Timer/Event Counter can be utilised to measure the width of external pulses applied to the external timer pin. To operate in this mode, the Operating Mode Select bit pair in the Timer Control Register must be set to the correct value as shown.

Control Register Operating Mode Select Bits for the Pulse Width Measurement Mode	Bit7	Bit6
	1	1

In this mode the internal clock is used as the Timer/Event Counter clock. After the other bits in the Timer Control Register have been setup, the enable bit, which is bit 4 of the Timer Control Register, can be set high to enable the Timer/Event Counter, however it will not actually start counting until an active edge is received on the external timer pin.

If the Active Edge Select bit, which is bit 3 of the Timer Control Register, is low, once a high to low transition has been received on the external timer pin, the Timer/Event Counter will start counting until the external timer pin returns to its original high level. At this point the enable bit will be automatically reset to zero and the Timer/Event Counter will stop counting. If the Active Edge Select bit is high, the Timer/Event Counter will begin counting once a low to high transition has been received on the external timer pin and stop counting when the external timer pin returns to its original low level. As before, the enable bit will be automatically reset to zero and the



Pulse Width Measure Mode Timing Diagram

Timer/Event Counter will stop counting. It is important to note that in the Pulse Width Measurement Mode, the enable bit is automatically reset to zero when the external control signal on the external timer pin returns to its original level, whereas in the other two modes the enable bit can only be reset to zero under program control.

The residual value in the Timer/Event Counter, which can now be read by the program, therefore represents the length of the pulse received on the external timer pin. As the enable bit has now been reset, any further transitions on the external timer pin will be ignored. Not until the enable bit is again set high by the program can the timer begin further pulse width measurements. In this way, single shot pulse measurements can be easily made.

It should be noted that in this mode the Timer/Event Counter is controlled by logical transitions on the external timer pin and not by the logic level. When the Timer/Event Counter is full and overflows, an interrupt signal is generated and the Timer/Event Counter will reload the value already loaded into the preload register and continue counting. The interrupt can be disabled by ensuring that the Timer/Event Counter Interrupt Enable bit in the Interrupt Control Register, is reset to zero.

To ensure that the timer pin is configured to operate as a pulse width measurement pin the Timer Control Register must place the Timer/Event Counter in the Pulse Width Measurement Mode.

Programming Considerations

When configured to run in the timer mode, the internal system clock is used as the timer clock source and is therefore synchronized with the overall operation of the microcontroller. In this mode, when the appropriate timer register is full, the microcontroller will generate an internal interrupt signal directing the program flow to the respective internal interrupt vector. For the pulse width measurement mode, the internal system clock is also used as the timer clock source but the timer will only run when the correct logic condition appears on the external timer input pin. As this is an external event and not synchronised with the internal timer clock, the microcontroller will only see this external event when the next timer clock pulse arrives. As a result there may be small differences in measured values requiring programmers to take this into account during programming. The same applies if the timer is configured to be in the event counting mode which again is an external event and not synchronised with the internal system or timer clock.

When the Timer/Event Counter is read or if data is written to the preload registers, the clock is inhibited to avoid errors, however as this may result in a counting error, this should be taken into account by the programmer. Care must be taken to ensure that the timers are properly initialised before using them for the first time. The associated timer enable bits in the interrupt control register must be properly set otherwise the internal interrupt associated with the timer will remain inactive. The edge select, timer mode control bits in timer control register must also be correctly set to ensure the timer is properly configured for the required application. It is also important to ensure that an initial value is first loaded into the timer register before the timer is switched on; this is because after power-on the initial value of the timer register is unknown. After the timer has been initialised the timer can be turned on and off by controlling the enable bit in the timer control register. Note that setting the timer enable bit high to turn the timer on, should only be executed after the timer mode bits have been properly setup. Setting the timer enable bit high together with a mode bit modification, may lead to improper timer operation if executed as a single timer control register byte write instruction.

When the Timer/Event counter overflows, its corresponding interrupt request flag in the interrupt control register will be set. If the timer interrupt is enabled this will in turn generate an interrupt signal. However irrespective of whether the interrupts are enabled or not, a Timer/Event counter overflow will also generate a wake-up signal if the device is in a Power-down condition. This situation may occur if the Timer/Event Counter is in the Event Counting Mode and if the external signal continues to change state. In such a case, the Timer/Event Counter will continue to count these external events and if an overflow occurs the device will be woken up from its Power-down condition. To prevent such a wake-up from occurring, the timer interrupt request flag should first be set high before issuing the HALT instruction to enter the Power Down Mode.

Timer Program Example

This program example shows how the Timer/Event Counter registers are setup, along with how the interrupts are enabled and managed. Note how the Timer/Event Counter is turned on, by setting bit 4 of the Timer Control Register. The Timer/Event Counter can be turned off in a similar way by clearing the same bit. This example program sets the Timer/Event Counter to be in the timer mode, which uses the internal system clock as the clock source.

```
Org          04h            ; external interrupt vector
reti
Org          08h            ; Timer/Event Counter 0 interrupt vector
jmp tmr0nt                  ; jump here when Timer 0 overflows
             :
org 20h                     ; main program
;internal Timer/Event Counter interrupt routine
tmr0nt:
             :
                            ; Timer/Event Counter main program placed here
             :
 reti
             :
             :
begin:
;setup Timer registers
             mov a,01fh     ; setup preload value – timer counts from this value to FFFFH
             mov tmr01,a
             mov a,09bh
             mov tmr0h,a
             mov a,080h     ; setup Timer control register
             mov tmr0c,a    ; timer mode
; setup interrupt register
             mov a,005h     ; enable master interrupt and timer interrupt
             mov intc0,a
             set tmrc0.4    ; start Timer – note mode bits must be previously setup
             :
             :
```

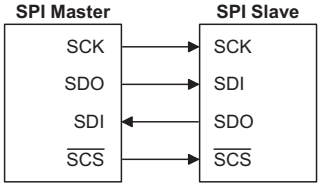
Serial Interface Function

The device contains a Serial Interface Function, which includes both the four line SPI interface and the two line I^2C interface types, to allow an easy method of communication with external peripheral hardware. Having relatively simple communication protocols, these serial interface types allow the microcontroller to interface to external SPI or I^2C based hardware such as sensors, Flash or EEPROM memory, etc. The SIM interface pins are pin-shared with other I/O pins therefore the SIM interface function must first be selected using a configuration option. As both interface types share the same pins and registers, the choice of whether the SPI or I^2C type is used is made using a bit in an internal register.

SPI Interface

The SPI interface is often used to communicate with external peripheral devices such as sensors, Flash or EEPROM memory devices etc. Originally developed by Motorola, the four line SPI interface is a synchronous serial data interface that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.

The communication is full duplex and operates as a slave/master type, where the MCU can be either master or slave. Although the SPI interface specification can control multiple slave devices from a single master, here, as only a single select pin, $\overline{SCS}$, is provided only one slave device can be connected to the SPI bus.



SPI Master/Slave Connection

- SPI Interface Operation
  The SPI interface is a full duplex synchronous serial data link. It is a four line interface with pin names SDI, SDO, SCK and $\overline{SCS}$. Pins SDI and SDO are the Serial Data Input and Serial Data Output lines, SCK is the Serial Clock line and $\overline{SCS}$ is the Slave Select line. As the SPI interface pins are pin-shared with normal I/O pins and with the I^2C function pins, the SPI interface must first be enabled by selecting the SIM enable configuration option and setting the correct bits in the SIMCTL0/SIMCTL2 register. After the SPI configuration option has been configured it can also be additionally disabled or enabled using the SIMEN bit in the SIMCTL0 register. Communication between devices connected to the SPI interface is carried out in a slave/master mode with all data transfer initiations being implemented by the master. The Master also controls the clock signal. As the device only contains a single $\overline{SCS}$ pin only one slave device can be utilised.

  The SPI function in this device offers the following features:
  - Full duplex synchronous data transfer
  - Both Master and Slave modes
  - LSB first or MSB first data transmission modes
  - Transmission complete flag
  - Rising or falling active clock edge
  - WCOL and CSEN bit enabled or disable select

  The status of the SPI interface pins is determined by a number of factors such as whether the device is in the master or slave mode and upon the condition of certain control bits such as CSEN, SIMEN and $\overline{SCS}$. In the table I, Z represents an input floating condition.
  There are several configuration options associated with the SPI interface. One of these is to enable the SIM function which selects the SIM pins rather than normal I/O pins. Note that if the configuration option does not select the SIM function then the SIMEN bit in the SIMCTL0 register will have no effect. Another two SIM configuration options determine if the CSEN and WCOL bits are to be used.

Configuration Option	Function
SIM Function	SIM interface or I/O pins
SPI CSEN bit	Enable/Disable
SPI WCOL bit	Enable/Disable

SPI Interface Configuration Options

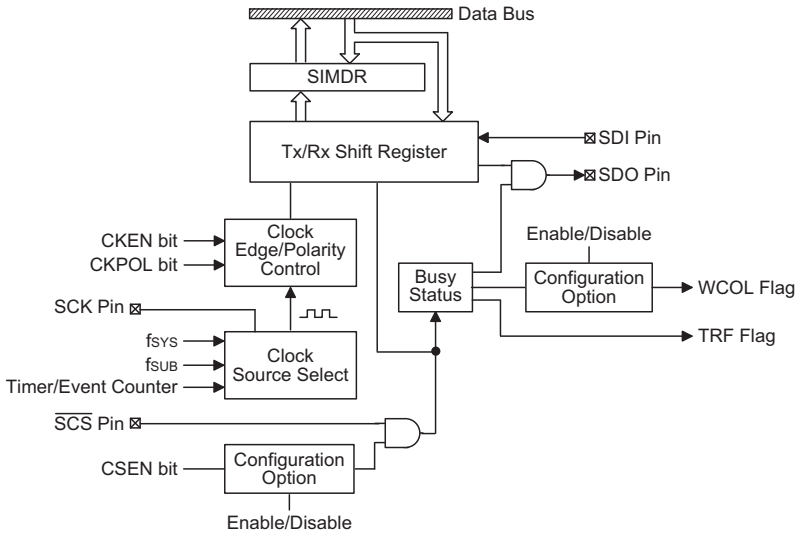
SPI Registers

There are three internal registers which control the overall operation of the SPI interface. These are the SIMDR data register and two control registers SIMCTL0 and SIMCTL2. Note that the SIMCTL1 register is only used by the I^2C interface.

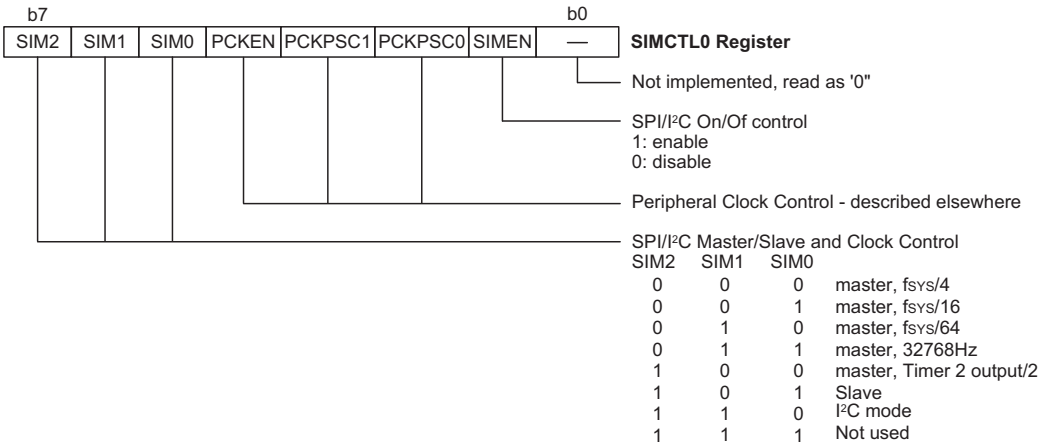
Pin	Master/Salve SIMEN=0	Master – SIMEN=1		Slave – SIMEN=1		
		CSEN=0	CSEN=1	CSEN=0	CSEN=1 SCS=0	CSEN=1 SCS=1
$\overline{SCS}$	Z	Z	L	Z	I, Z	I, Z
SDO	Z	O	O	O	O	Z
SDI	Z	I, Z	I, Z	I, Z	I, Z	Z
SCK	Z	H: CKPOL=0 L: CKPOL=1	H: CKPOL=0 L: CKPOL=1	I, Z	I, Z	Z

Note: ″Z″ floating, ″H″ output high, ″L″ output low, ″I″ Input, ″O″output level, ″I,Z″ input floating (no pull-high)

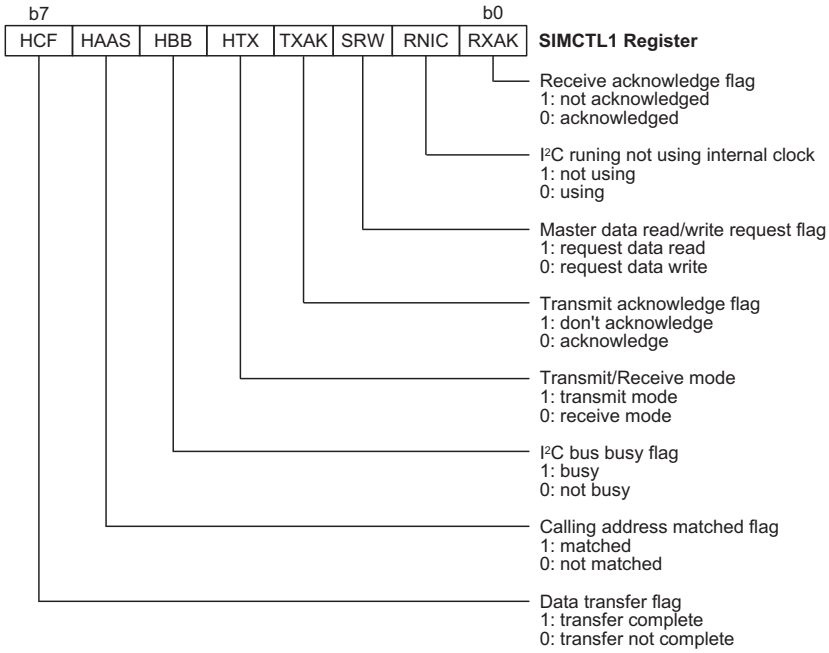
SPI Interface Pin Status



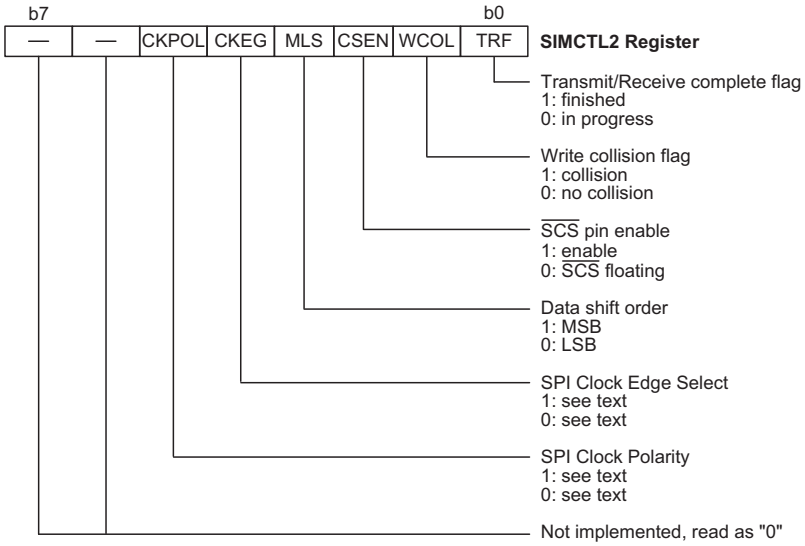
SPI Block Diagram



SPI/I²C Control Register – SIMCTL0



I²C Control Register – SIMCTL1



SPI Control Register – SIMCTL2

The SIMDR register is used to store the data being transmitted and received. The same register is used by both the SPI and I^2C functions. Before the microcontroller writes data to the SPI bus, the actual data to be transmitted must be placed in the SIMDR register. After the data is received from the SPI bus, the microcontroller can read it from the SIMDR register. Any transmission or reception of data from the SPI bus must be made via the SIMDR register.

Bit	7	6	5	4	3	2	1	0
Label	SD7	SD6	SD5	SD4	SD3	SD2	SD1	SD0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	X	X	X	X	X	X	X	X

There are also two control registers for the SPI interface, SIMCTL0 and SIMCTL2. Note that the SIMCTL2 register also has the name SIMAR which is used by the I^2C function. The SIMCTL1 register is not used by the SPI function, only by the I^2C function. Register SIMCTL0 is used to control the enable/disable function and to set the data transmission clock frequency. Although not connected with the SPI function, the SIMCTL0 register is also used to control the Peripheral Clock prescaler. Register SIMCTL2 is used for other control functions such as LSB/MSB selection, write collision flag etc.

The following gives further explanation of each SIMCTL1 register bit:

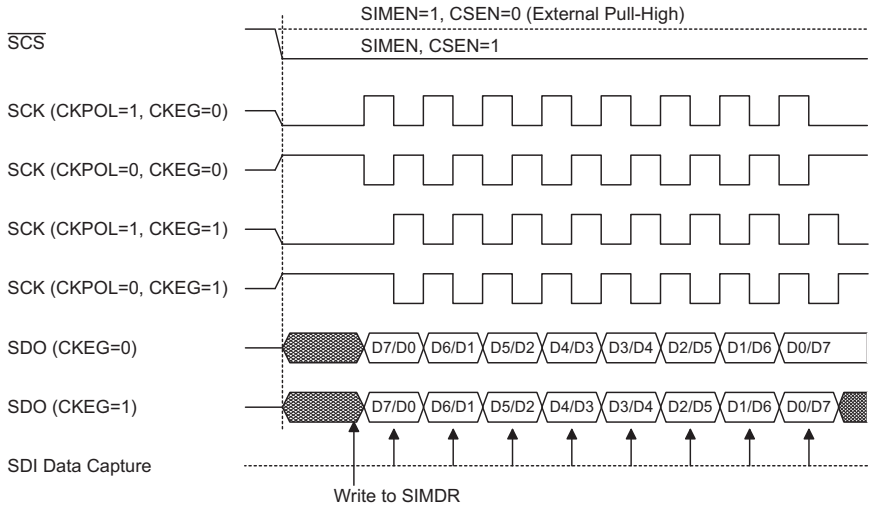
- SIMIDLE
  The SIMIDLE bit is used to select if the SPI interface continues running when the device is in the IDLE mode. Setting the bit high allows the SPI interface to maintain operation when the device is in the Idle mode. Clearing the bit to zero disables any SPI operations when in the Idle mode.
  This SPI/I^2C idle mode control bit is located at CLKMOD register bit4.
- SIMEN
  The bit is the overall on/off control for the SPI interface. When the SIMEN bit is cleared to zero to disable the SPI interface, the SDI, SDO, SCK and $\overline{SCS}$ lines will be in a floating condition and the SPI operating current will be reduced to a minimum value. When the bit is high the SPI interface is enabled. The SIMconfiguration option must have first enabled the SIM interface for this bit to be effective. Note that when the SIMEN bit changes from low to high the contents of the SPI control registers will be in an unknown condition and should therefore be first initialised by the application program.
- SIM0~SIM2
  These bits setup the overall operating mode of the SIM function. As well as selecting if the I^2C or SPI function, they are used to control the SPI Master/Slave selection and the SPI Master clock frequency. The SPI clock is a function of the system clock but can also be chosen to be sourced from the Timer. If the SPI Slave Mode is selected then the clock will be supplied by an external Master device.

SIM0	SIM1	SIM2	SPI Master/Slave Clock Control and I2C Enable
0	0	0	SPI Master, $f_{SYS}/4$
0	0	1	SPI Master, $f_{SYS}/16$
0	1	0	SPI Master, $f_{SYS}/64$
0	1	1	SPI Master, f_{SUB}
1	0	0	SPI Master Timer 2 output/2
1	0	1	SPI Slave
1	1	0	I^2C mode
1	1	1	Not used

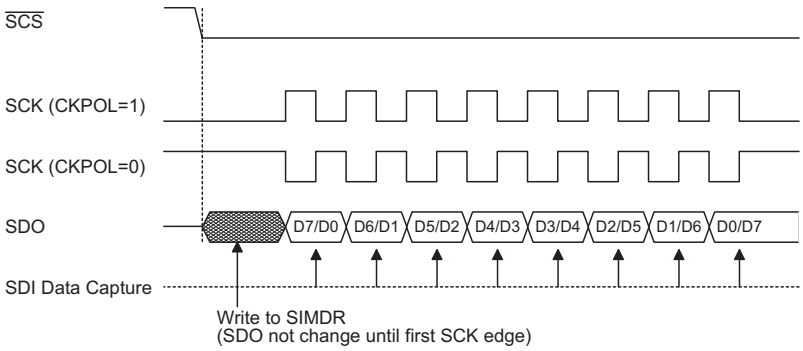
SPI Control Register – SIMCTL2

The SIMCTL2 register is also used by the I^2C interface but has the name SIMAR

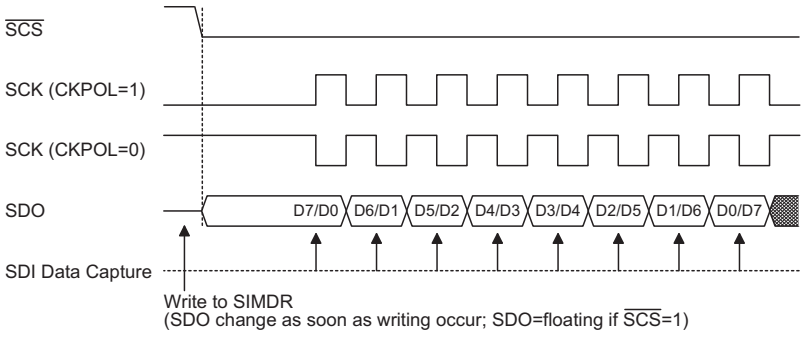
- TRF
  The TRF bit is the Transmit/Receive Complete flag and is set high automatically when an SPI data transmission is completed, but must be cleared by the application program. It can be used to generate an interrupt.
- WCOL
  The WCOL bit is used to detect if a data collision has occurred. If this bit is high it means that data has been attempted to be written to the SIMDR register during a data transfer operation. This writing operation will be ignored if data is being transferred. The bit can be cleared by the application program. Note that using the WCOL bit can be disabled or enabled via configuration option.
- CSEN
  The CSEN bit is used as an on/off control for the $\overline{SCS}$ pin. If this bit is low then the $\overline{SCS}$ pin will be disabled and placed into a floating condition. If the bit is high the $\overline{SCS}$ pin will be enabled and used as a select pin. Note that using the CSEN bit can be disabled or enabled via configuration option.
- MLS
  This is the data shift select bit and is used to select how the data is transferred, either MSB or LSB first. Setting the bit high will select MSB first and low for LSB first.
- CKEG and CKPOL
  These two bits are used to setup the way that the clock signal outputs and inputs data on the SPI bus. These two bits must be configured before data transfer is executed otherwise an erroneous clock edge may be generated. The CKPOL bit determines the base condition of the clock line, if the bit is high then the SCK line will be low when the clock is inactive. When the CKPOL bit is low then the SCK line will be high when the clock is inactive. The CKEG bit determines active clock edge type which depends upon the condition of CKPOL.



SPI Master Mode Timing

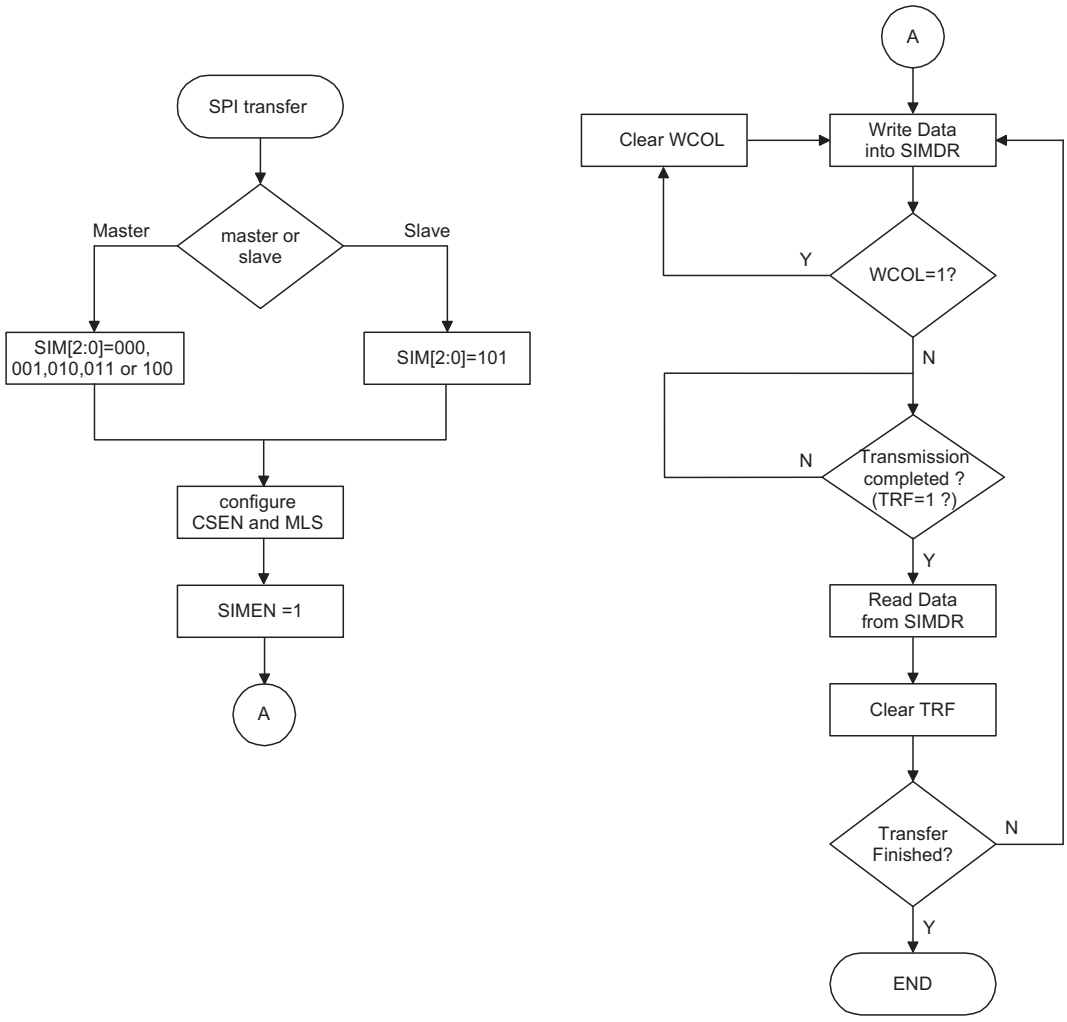


SPI Slave Mode Timing (CKEG=0)



Note: For SPI slave mode, if SIMEN=1 and CSEN=0, SPI is always enabled and ignore the $\overline{SCS}$ level.

SPI Slave Mode Timing (CKEG=1)



SPI Transfer Control Flowchart

CKPOL	CKEG	SCK Clock Signal
0	0	High Base Level Active Rising Edge
0	1	High Base Level Active Falling Edge
1	0	Low Base Level Active Falling Edge
1	1	Low Base Level Active Rising Edge

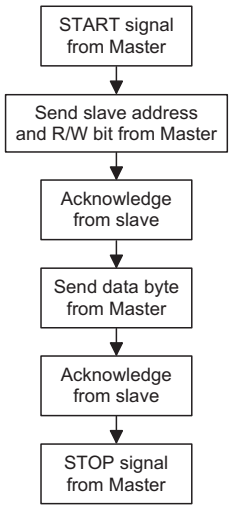
SPI Communication

After the SPI interface is enabled by setting the SIMEN bit high, then in the Master Mode, when data is written to the SIMDR register, transmission/reception will begin simultaneously. When the data transfer is complete, the TRF flag will be set automatically, but must be cleared using the application program. In the Slave Mode, when the clock signal from the master has been received, any data in the SIMDR register will be transmitted and any data on the SDI pin will be shifted into the SIMDR register. The master should output an $\overline{SCS}$ signal to enable the slave device before a clock signal is provided and slave data transfers should be enabled/disabled before/after an $\overline{SCS}$ signal is received.
The SPI will continue to function even after a HALT instruction has been executed.

I²C Interface

The I²C interface is used to communicate with external peripheral devices such as sensors, EEPROM memory etc. Originally developed by Philips, it is a two line low speed serial interface for synchronous serial data transfer. The advantage of only two lines for communication, relatively simple communication protocol and the ability to accommodate multiple devices on the same bus has made it an extremely popular interface type for many applications.

- I²C Interface Operation
  The I²C serial interface is a two line interface, a serial data line, SDA, and serial clock line, SCL. As many devices may be connected together on the same bus, their outputs are both open drain types. For this reason it is necessary that external pull-high resistors are connected to these outputs. Note that no chip select line exists, as each device on the I²C bus is identified by a unique address which will be transmitted and received on the I²C bus.
  When two devices communicate with each other on the bidirectional I²C bus, one is known as the master device and one as the slave device. Both master and slave can transmit and receive data, however, it is the master device that has overall control of the bus. For these devices, which only operates in slave mode, there are two methods of transferring data on the I²C bus, the slave transmit mode and the slave receive mode.

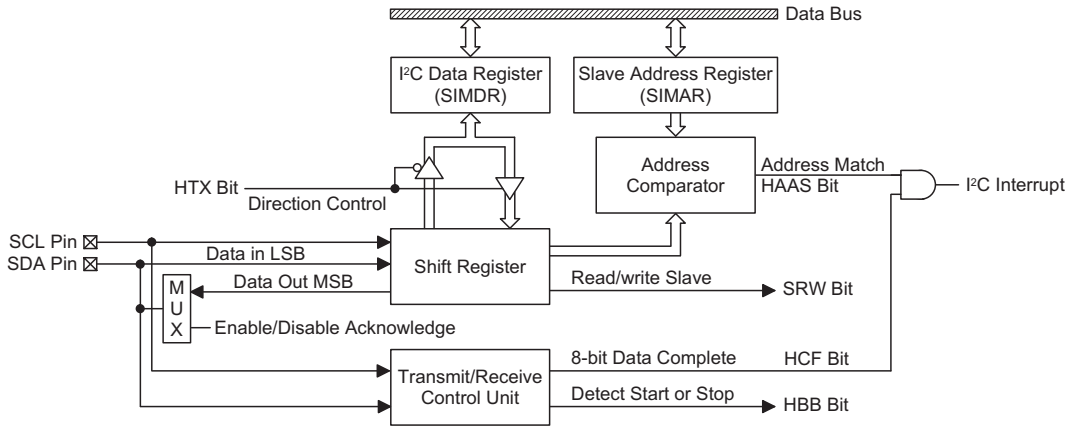


There are several configuration options associated with the I²C interface. One of these is to enable the function which selects the SIM pins rather than normal I/O pins. Note that if the configuration option does not select the SIM function then the SIMEN bit in the SIMCTL0 register will have no effect. A configuration option exists to allow a clock other than the system clock to drive the I²C interface. Another configuration option determines the debounce time of the I²C interface. This uses the internal clock to in effect add a debounce time to the external clock to reduce the possibility of glitches on the clock line causing erroneous operation. The debounce time, if selected, can be chosen to be either 1 or 2 system clocks.

SIM	Function
SIM function	SIM interface or SEG pins
I²C clock	I²C runs without internal clock Disable/Enable
I²C debounce	No debounce, 1 system clock; 2 system clocks

I²C Interface Configuration Options

- I²C Registers
  There are three control registers associated with the I²C bus, SIMCTL0, SIMCTL1 and SIMAR and one data register, SIMDR. The SIMDR register, which is shown in the above SPI section, is used to store the data being transmitted and received on the I²C bus. Before the microcontroller writes data to the I²C bus, the actual data to be transmitted must be placed in the SIMDR register. After the data is received from the I²C bus, the microcontroller can read it from the SIMDR register. Any transmission or reception of data from the I²C bus must be made via the SIMDR register.
  Note that the SIMAR register also has the name SIMCTL2 which is used by the SPI function. Bits SIMIDLE , SIMEN and bits SIM0~SIM2 in register SIMCTL0 are used by the I²C interface. The SIMCTL0 register is shown in the above SPI section.



I²C Block Diagram

- SIMIDLE
  The SIMIDLE bit is used to select if the I²C interface continues running when the device is in the IDLE mode. Setting the bit high allows the I²C interface to maintain operation when the device is in the Idle mode. Clearing the bit to zero disables any I²C operations when in the Idle mode.
  This SPI/I²C idle mode control bit is located at CLKMOD register bit4.
- SIMEN
  The SIMEN bit is the overall on/off control for the I²C interface. When the SIMEN bit is cleared to zero to disable the I²C interface, the SDA and SCL lines will be in a floating condition and the I²C operating current will be reduced to a minimum value. In this condition the pins can be used as SEG functions. When the bit is high the I²C interface is enabled. The SIM configuration option must have first enabled the SIM interface for this bit to be effective. Note that when the SIMEN bit changes from low to high the contents of the I²C control registers will be in an unknown condition and should therefore be first initialised by the application program.
- SIM0~SIM2
  These bits setup the overall operating mode of the SIM function. To select the I²C function, bits SIM2~SIM0 should be set to the value 110.
- RXAK
  The RXAK flag is the receive acknowledge flag. When the RXAK bit has been reset to zero it means that a correct acknowledge signal has been received at the 9th clock, after 8 bits of data have been transmitted. When in the transmit mode, the transmitter checks the RXAK bit to determine if the receiver wishes to receive the next byte. The transmitter will therefore continue sending out data until the RXAK bit is set high. When this occurs, the transmitter will release the SDA line to allow the master to send a STOP signal to release the bus.
- SRW
  The SRW bit is the Slave Read/Write bit. This bit determines whether the master device wishes to transmit or receive data from the I²C bus. When the transmitted address and slave address match, that is when the HAAS bit is set high, the device will check the SRW bit to determine whether it should be in transmit mode or receive mode. If the SRW bit is high, the master is requesting to read data from the bus, so the device should be in transmit mode. When the SRW bit is zero, the master will write data to the bus, therefore the device should be in receive mode to read this data.
- TXAK
  The TXAK flag is the transmit acknowledge flag. After the receipt of 8-bits of data, this bit will be transmitted to the bus on the 9th clock. To continue receiving more data, this bit has to be reset to zero before further data is received.
- HTX
  The HTX flag is the transmit/receive mode bit. This flag should be set high to set the transmit mode and low for the receive mode.
- HBB
  The HBB flag is the I²C busy flag. This flag will be high when the I²C bus is busy which will occur when a START signal is detected. The flag will be reset to zero when the bus is free which will occur when a STOP signal is detected.
- HASS
  The HASS flag is the address match flag. This flag is used to determine if the slave device address is the same as the master transmit address. If the addresses match then this bit will be high, if there is no match then the flag will be low.
- HCF
  The HCF flag is the data transfer flag. This flag will be zero when data is being transferred. Upon completion of an 8-bit data transfer the flag will go high and an interrupt will be generated.

I²C Control Register – SIMAR

The SIMAR register is also used by the SPI interface but has the name SIMCTL2.

The SIMAR register is the location where the 7-bit slave address of the microcontroller is stored. Bits 1~7 of the SIMAR register define the microcontroller slave address. Bit 0 is not defined. When a master device, which is connected to the I²C bus, sends out an address, which matches the slave address in the SIMAR register, the microcontroller slave device will be selected. Note that the SIMAR register is the same register as SIMCTL2 which is used by the SPI interface.

I²C Bus Communication

Communication on the I²C bus requires four separate steps, a START signal, a slave device address transmission, a data transmission and finally a STOP signal. When a START signal is placed on the I²C bus, all devices on the bus will receive this signal and be notified of the imminent arrival of data on the bus. The first seven bits of the data will be the slave address with the first bit being the MSB. If the address of the microcontroller matches that of the transmitted address, the HAAS bit in the SIMCTL1 register will be set and an I²C interrupt will be generated. After entering the interrupt service routine, the microcontroller slave device must first check the condition of the HAAS bit to determine whether the interrupt source originates from an address match or from the completion of an 8-bit data transfer. During a data transfer, note that after the 7-bit slave address has been transmitted, the following bit, which is the 8th bit, is the read/write bit whose value will be placed in the SRW bit. This bit will be checked by the microcontroller to determine whether to go into transmit or receive mode. Before any transfer of data to or from the I²C bus, the microcontroller must initialise the bus, the following are steps to achieve this:

Step 1

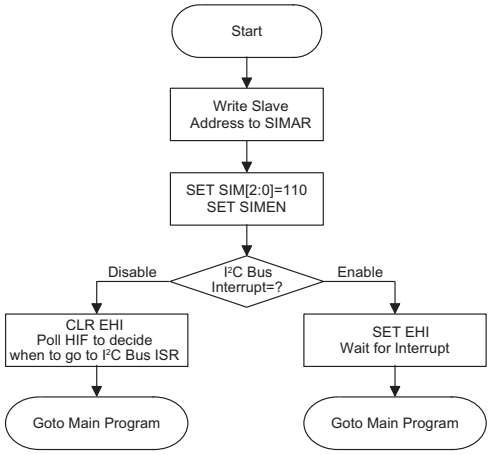
Write the slave address of the microcontroller to the I²C bus address register SIMAR.

Step 2

Set the SIMEN bit in the SIMCTL0 register to "1" to enable the I²C bus.

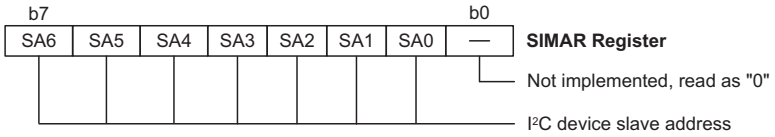
Step 3

Set the EHI bit of the interrupt control register to enable the I²C bus interrupt.

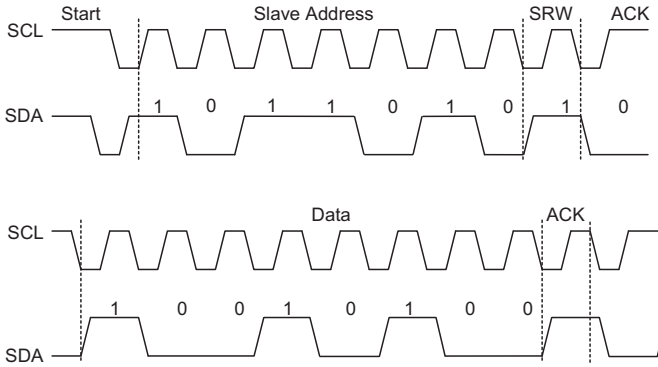


I²C Bus Initialisation Flow Chart

- Start Signal
  The START signal can only be generated by the master device connected to the I²C bus and not by the microcontroller, which is only a slave device. This START signal will be detected by all devices connected to the I²C bus. When detected, this indicates that the I²C bus is busy and therefore the HBB bit will be set. A START condition occurs when a high to low transition on the SDA line takes place when the SCL line remains high.
- Slave Address
  The transmission of a START signal by the master will be detected by all devices on the I²C bus. To determine which slave device the master wishes to communicate with, the address of the slave device will be sent out immediately following the START signal. All slave devices, after receiving this 7-bit address data, will compare it with their own 7-bit slave address. If the address sent out by the master matches the internal address of the microcontroller slave device, then an internal I²C bus interrupt signal will be generated. The next bit following the address, which is the 8th bit, defines the read/write status and will be saved to the SRW bit of the SIMCTL1 register. The device will then transmit an acknowledge bit, which is a low level, as the 9th bit. The microcontroller slave device will also set the status flag HAAS when the addresses match. As an I²C bus interrupt can come from two sources, when the program enters the interrupt subroutine, the HAAS bit should be examined to see whether the interrupt source has come from a matching slave address or from the completion of a data byte transfer. When a slave address is matched, the device must be placed in either the transmit mode and then write data to the SIMDR register, or in the receive mode where it must implement a dummy read from the SIMDR register to release the SCL line.



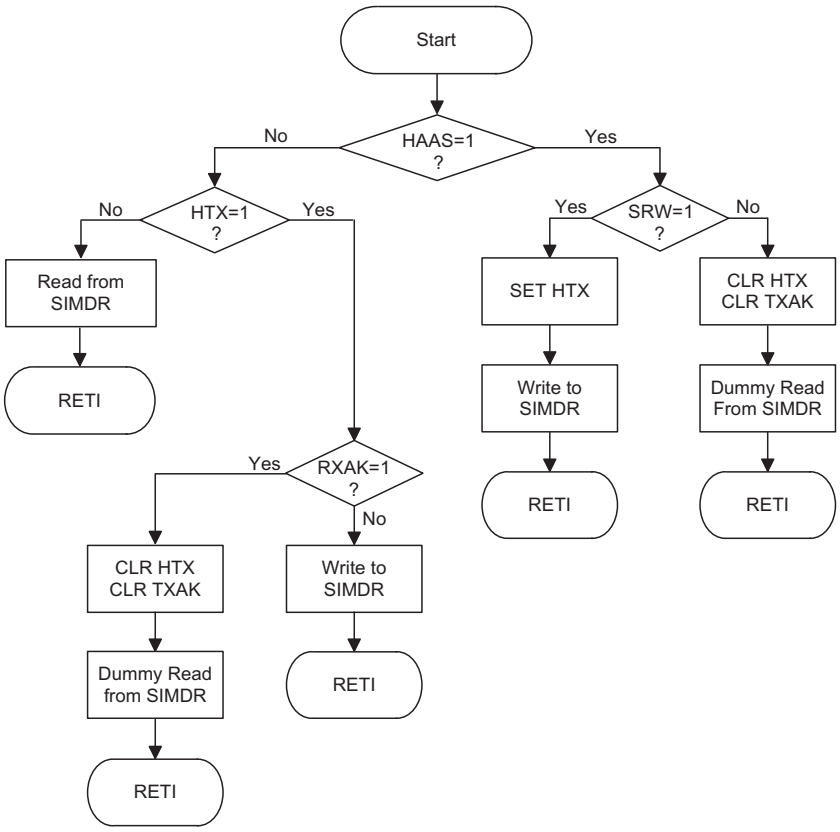
I²C Slave Address Register – SIMAR



S=Start (1 bit)
SA=Slave Address (7 bits)
SR=SRW bit (1 bit)
M=Slave device send acknowledge bit (1 bit)
D=Data (8 bits)
A=ACK (RXAK bit for transmitter, TXAK bit for receiver 1 bit)
P=Stop (1 bit)

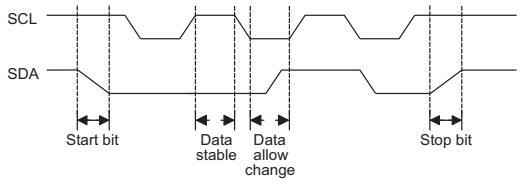
S	SA	SR	M	D	A	D	A	--------	S	SA	SR	M	D	A	D	A	--------	P

I²C Communication Timing Diagram



I²C Bus ISR Flow Chart

- SRW Bit
  The SRW bit in the SIMCTL1 register defines whether the microcontroller slave device wishes to read data from the I^2C bus or write data to the I^2C bus. The microcontroller should examine this bit to determine if it is to be a transmitter or a receiver. If the SRW bit is set to ″1″ then this indicates that the master wishes to read data from the I^2C bus, therefore the microcontroller slave device must be setup to send data to the I^2C bus as a transmitter. If the SRW bit is ″0″ then this indicates that the master wishes to send data to the I^2C bus, therefore the microcontroller slave device must be setup to read data from the I^2C bus as a receiver.
- Acknowledge Bit
  After the master has transmitted a calling address, any slave device on the I^2C bus, whose own internal address matches the calling address, must generate an acknowledge signal. This acknowledge signal will inform the master that a slave device has accepted its calling address. If no acknowledge signal is received by the master then a STOP signal must be transmitted by the master to end the communication. When the HAAS bit is high, the addresses have matched and the microcontroller slave device must check the SRW bit to determine if it is to be a transmitter or a receiver. If the SRW bit is high, the microcontroller slave device should be setup to be a transmitter so the HTX bit in the SIMCTL1 register should be set to ″1″ if the SRW bit is low then the microcontroller slave device should be setup as a receiver and the HTX bit in the SIMCTL1 register should be set to ″0″.
- Data Byte
  The transmitted data is 8-bits wide and is transmitted after the slave device has acknowledged receipt of its slave address. The order of serial bit transmission is the MSB first and the LSB last. After receipt of 8-bits of data, the receiver must transmit an acknowledge signal, level ″0″, before it can receive the next data byte. If the transmitter does not receive an acknowledge bit signal from the receiver, then it will release the SDA line and the master will send out a STOP signal to release control of the I^2C bus. The corresponding data will be stored in the SIMDR register. If setup as a transmitter, the microcontroller slave device must first write the data to be transmitted into the SIMDR register. If setup as a receiver, the microcontroller slave device must read the transmitted data from the SIMDR register.



Data Timing Diagram

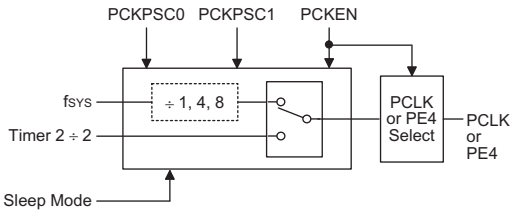
- Receive Acknowledge Bit
  When the receiver wishes to continue to receive the next data byte, it must generate an acknowledge bit, known as TXAK, on the 9th clock. The microcontroller slave device, which is setup as a transmitter will check the RXAK bit in the SIMCTL1 register to determine if it is to send another data byte, if not then it will release the SDA line and await the receipt of a STOP signal from the master.

Peripheral Clock Output

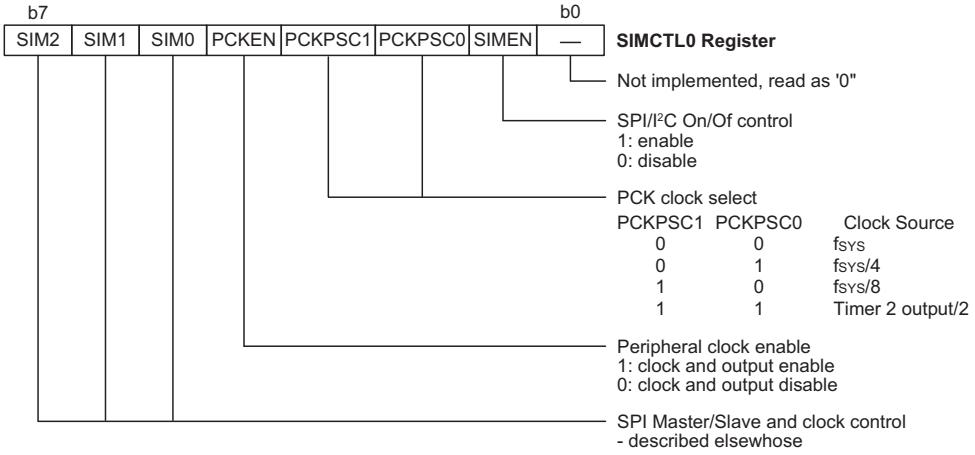
The Peripheral Clock Output allows the device to supply external hardware with a clock signal synchronised to the microcontroller clock.

Peripheral Clock Operation

As the peripheral clock output pin, PCLK, is shared with an I/O pin, the required pin function is chosen via PCKEN in the SIMCTL0 register. The Peripheral Clock function is controlled using the SIMCTL0 register. The clock source for the Peripheral Clock Output can originate from either the Timer 2 divided by two or a divided ratio of the internal f_{SYS} clock. The PCKEN bit in the SIMCTL0 register is the overall on/off control, setting the bit high enables the Peripheral Clock, clearing it disables it. The required division ratio of the system clock is selected using the PCKPSC0 and PCKPSC1 bits in the same register. If the system enters the Sleep Mode this will disable the Peripheral Clock output.



Peripheral Clock Block Diagram



Peripheral Clock Output Control – SIMCTL0

Interrupts

Interrupts are an important part of any microcontroller system. When an external event or an internal function such as a Timer/Event Counter requires microcontroller attention, their corresponding interrupt will enforce a temporary suspension of the main program allowing the microcontroller to direct attention to their respective needs. The external interrupt is controlled by the action of the external $\overline{INT}$, $\overline{PINT}$ pins, while the internal interrupt are controlled by Timer/Event Counter 0 or 1 overflow, a Real Time Clock overflow, a DTMF reciever valid character reception, an FSK decoder packet data reception or a multifunction interrupt.

Interrupt Register

Overall interrupt control, which means interrupt enabling and request flag setting, is controlled by two interrupt control registers, INTC0 and INTC1, located in the Data Memory. By controlling the appropriate enable bits in this register each individual interrupt can be enabled or disabled. Also when an interrupt occurs, the corresponding request flag will be set by the microcontroller. The global enable flag if cleared to zero will disable all interrupts.

Interrupt Operation

A Timer/Event Counter 0 or 1 overflow, a Real Time Clock overflow, a reception of a valid DTMF character, a FSK packet data, a rising edge on PC7 or a falling edge on INT/PC0/PC5 will all generate an interrupt request by setting their corresponding request flag, if their appropriate interrupt enable bit is set. When this happens, the Program Counter, which stores the address of the next instruction to be executed, will be transferred onto the stack. The Program Counter will then be loaded with a new address which will be the value of the corresponding interrupt vector. The microcontroller will then fetch its next instruction from this interrupt vector. The instruction at this vector will usually be a JMP statement which will take program execution to another section of program which is known as the interrupt service routine. Here is located the code to control the appropriate interrupt. The interrupt service routine must be terminated with a RETI statement, which retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution at the point where the interrupt occurred.

The various interrupt enable bits, together with their associated request flags, are shown in the accompanying diagram with their order of priority.

Once an interrupt subroutine is serviced, all the other interrupts will be blocked, as the EMI bit will be cleared automatically. This will prevent any further interrupt nesting from occurring. However, if other interrupt requests occur during this interval, although the interrupt will not be immediately serviced, the request flag will still be recorded. If an interrupt requires immediate servicing while the program is already in another interrupt service routine, the EMI bit should be set after entering the routine, to allow interrupt nesting. If the stack is full, the interrupt request will not be acknowledged, even if the related interrupt is enabled, until the Stack Pointer is decremented. If immediate service is desired, the stack must be prevented from becoming full.

Interrupt Priority

Interrupts, occurring in the interval between the rising edges of two consecutive T2 pulses, will be serviced on the latter of the two T2 pulses, if the corresponding interrupts are enabled. In case of simultaneous requests, the following table shows the priority that is applied. These can be masked by resetting the EMI bit.

Interrupt Source	All Devices Priority
Reset	1
External Interrupt	2
Timer 0 Interrupt	3
Timer 1 Interrupt	4
Peripheral Interrupt	5
Real Time Clock Interrupt	6
Multi-function Interrupt	7

In cases where both external and internal interrupts are enabled and where an external and internal interrupt occurs simultaneously, the external interrupt will always have priority and will therefore be serviced first. Suitable masking of the individual interrupts using the INTC register can prevent simultaneous occurrences.

External Interrupt

For an external interrupt to occur, the global interrupt enable bit, EMI, and external interrupt enable bit, EEI, must first be set. An actual external interrupt will take place when the external interrupt request flag, EIF, is set, a situation that will occur when a high to low transition appears on the $\overline{INT}$ line. When the interrupt is enabled, the stack is not full and a high to low transition appears on the external interrupt pin, a subroutine call to the external interrupt vector at location 04H, will take place. When the interrupt is serviced, the external interrupt request flag, EIF, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

Timer/Event Counter Interrupt

For a Timer/Event Counter interrupt to occur, the global interrupt enable bit, EMI, and the corresponding timer interrupt enable bit, ET0I or ET1I, must first be set. An actual Timer/Event Counter interrupt will take place when the Timer/Event Counter request flag, T0F or T1F, is set, a situation that will occur when the Timer/Event Counter overflows. When the interrupt is enabled, the stack is not full and a Timer/Event Counter overflow occurs, a subroutine call to the timer interrupt vector at location 08H or 0CH, will take place. When the interrupt is serviced, the timer interrupt request flag, T0F or T1F, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

Peripheral Interrupt

For a Peripheral interrupt to occur, the global interrupt enable bit, EMI, and the corresponding peripehral interrupt enable bit, EPERI, must first be set. An actual Peripheral interrupt will take place when the Peripheral interrupt request flag, PERF, is set. This will occur when the DTMF receiver detects a valid character, a ring/line reversal is detected, an FSK carrier detected, an FSK data packet is ready or the FSK raw data exhibit a falling edge. When the interrupt is enabled, the stack is not full and a Peripheral interrupt request occurs, a subroutine call to the peripheral interrupt vector at location 10H, will take place. When the interrupt is serviced, the peripheral interrupt request flag, PERF, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

Real Time Clock Interrupt

For a Real Time Clock interrupt to occur, the global interrupt enable bit, EMI, and the corresponding real timer clock interrupt enable bit, ERTCI, must first be set. An actual Real Time Clock interrupt will take place when the Real Time Clock request flag, RTCF, is set, a situation that will occur when the RTC times out which will occur every second. When the interrupt is enabled, the stack is not full and a Real Time Clock interrupt request occurs, a subroutine call to the real time clock interrupt vector at location 14H, will take place. When the interrupt is serviced, the timer interrupt request flag, RTCF, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

Multi-function Interrupt

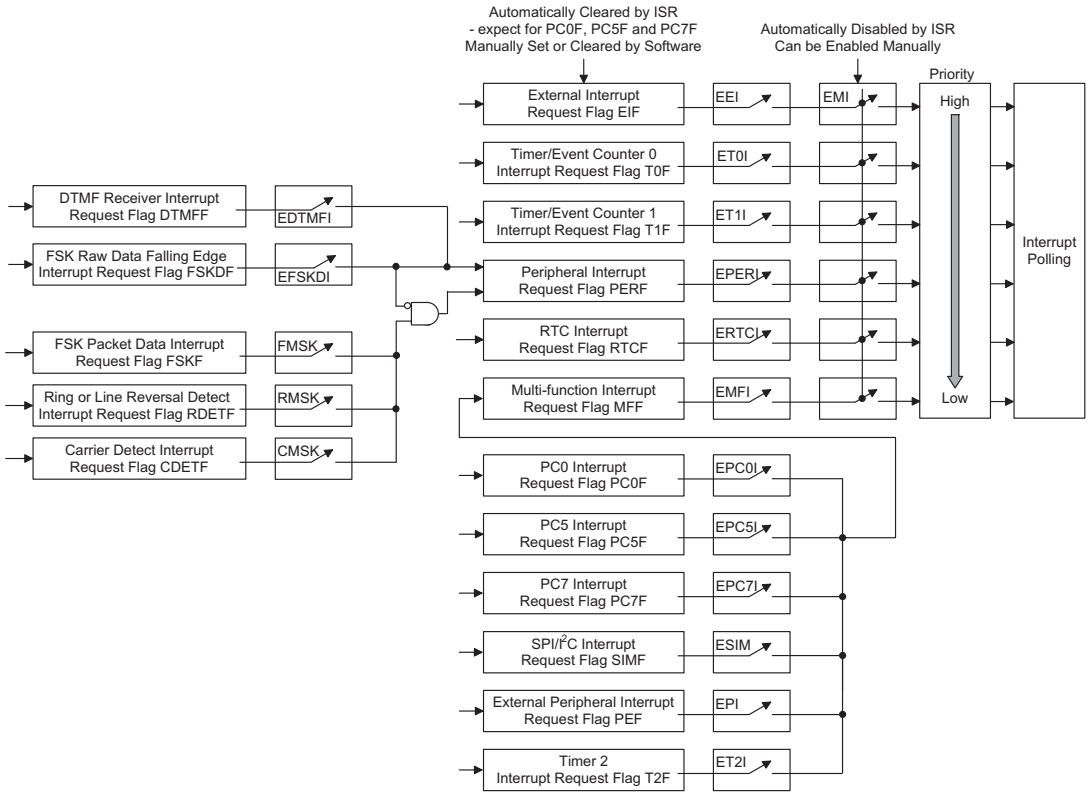
For a Multi-function interrupt to occur, the global interrupt enable bit, EMI, and the corresponding multi-function interrupt enable bit, EMFI, must first be set. An actual Multi-function interrupt will take place when the Multi-function interrupt request flag, MFF, is set, a situation that will occur when PC0 or PC5 receive a falling edge, PC7 receives a rising edge, an SPI/I^2C interrupt occurs, an external peripheral has a falling edge or a Timer2 overflow occurs. When the interrupt is enabled, the stack is not full and a Multi-function interrupt request occurs, a subroutine call to the multi-function interrupt vector at location 18H, will take place. When the interrupt is serviced, the multi-function interrupt request flag, MFF, will be automatically reset and the EMI bit will be automatically cleared to disable other interrupts.

Programming Considerations

By disabling the interrupt enable bits, a requested interrupt can be prevented from being serviced, however, once an interrupt request flag is set, it will remain in this condition in the INTC register until the corresponding interrupt is serviced or until the request flag is cleared by a software instruction.

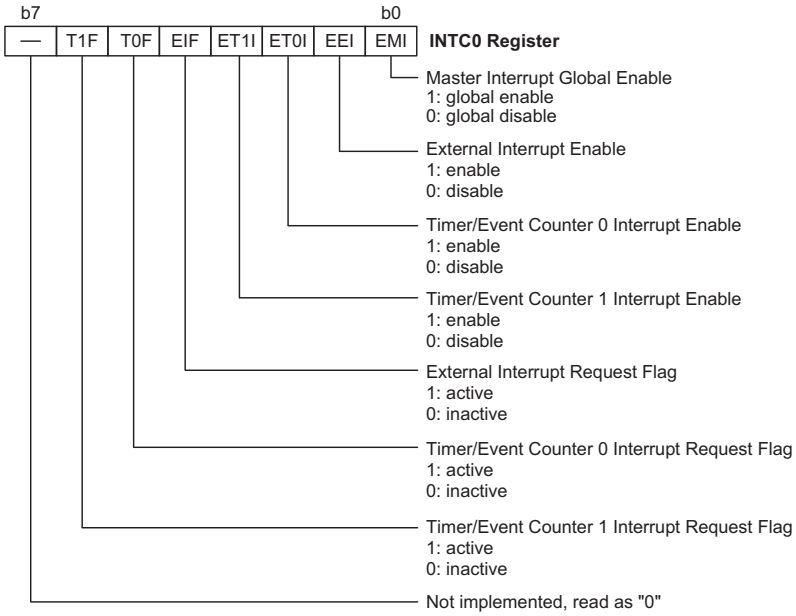
It is recommended that programs do not use the "CALL subroutine" instruction within the interrupt subroutine. Interrupts often occur in an unpredictable manner or need to be serviced immediately in some applications. If only one stack is left and the interrupt is not well controlled, the original control sequence will be damaged once a "CALL subroutine" is executed in the interrupt subroutine.

All of these interrupts have the capability of waking up the processor when in the Power Down Mode. Only the Program Counter is pushed onto the stack. If the contents of the register or status register are altered by the interrupt service program, which may corrupt the desired control sequence, then the contents should be saved in advance.

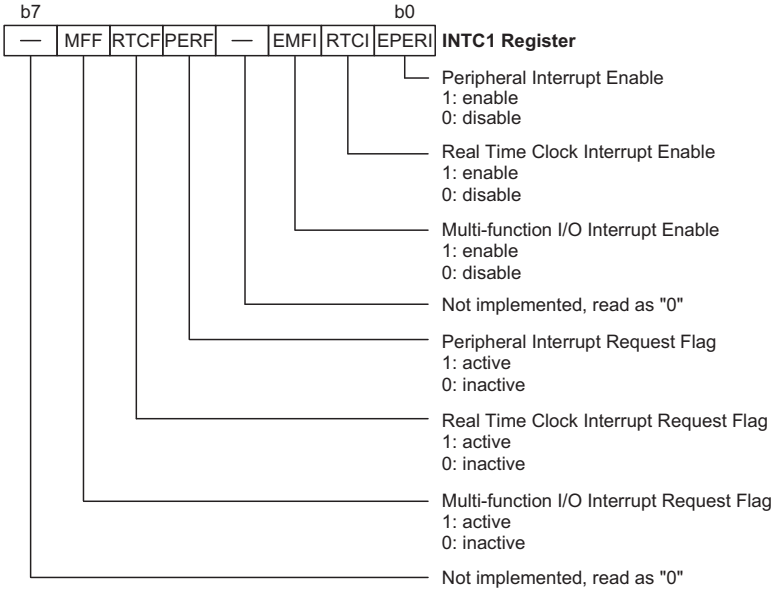


Note that :If the EFSKDI is enabled, that will disable FMSK, RMSK and CMSK, these three interrupts. The designer should take care this limitation.

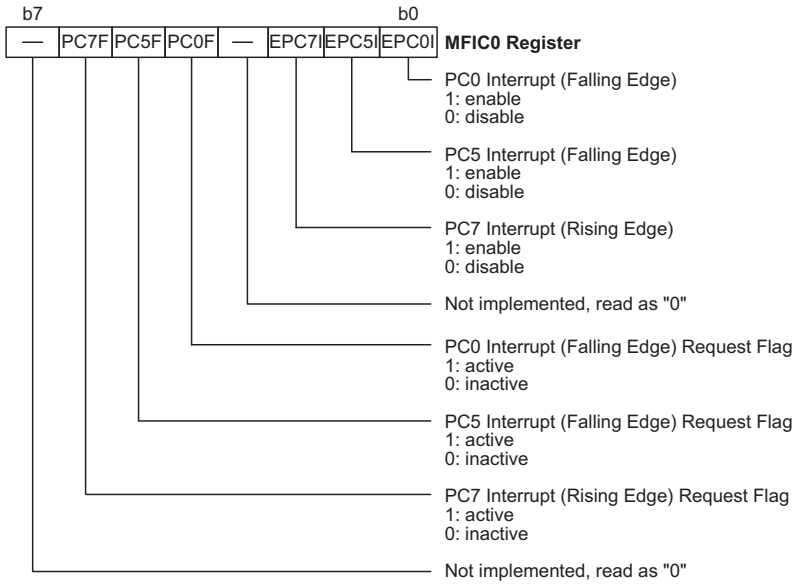
Interrupt Structure



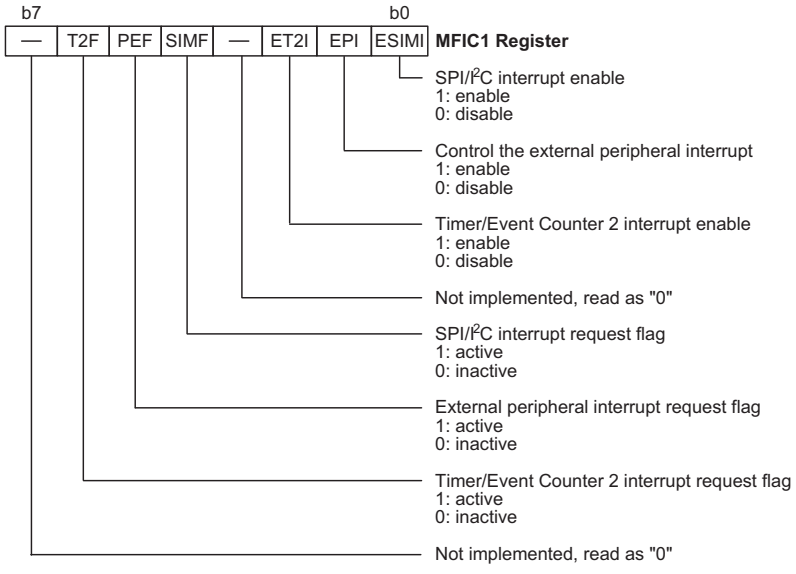
Interrupt Control 0 Register



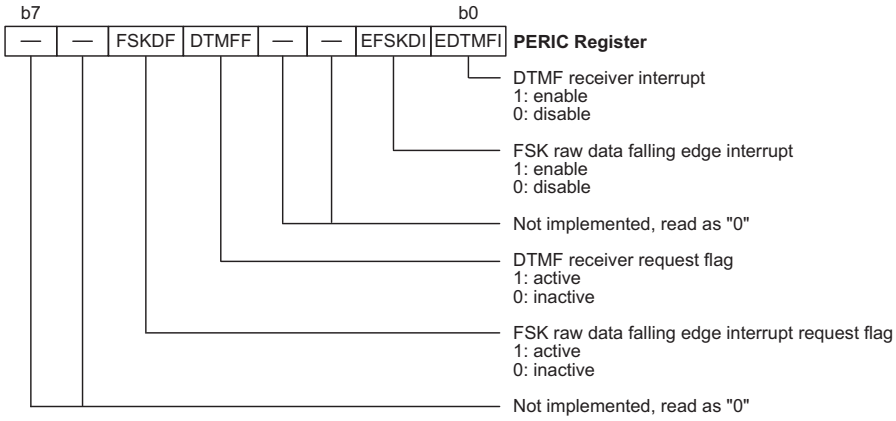
Interrupt Control 1 Register



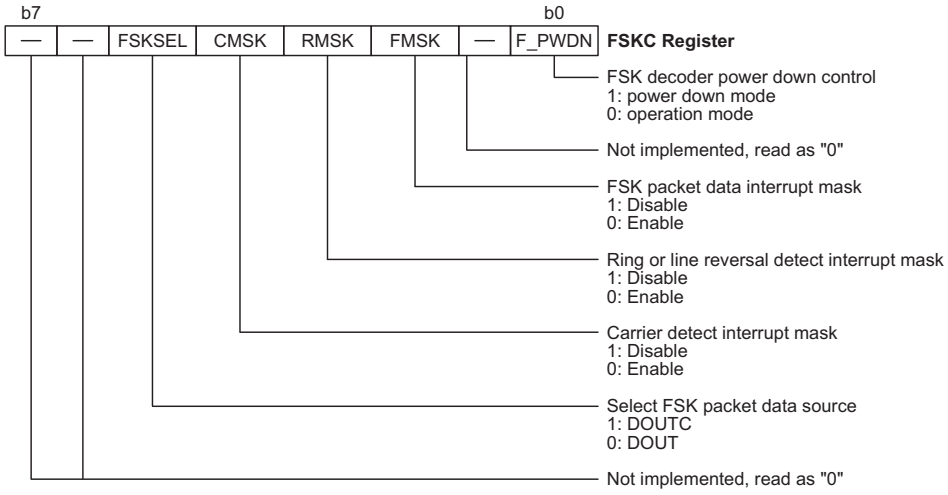
Multi-Function Interrupt Control 0 Register



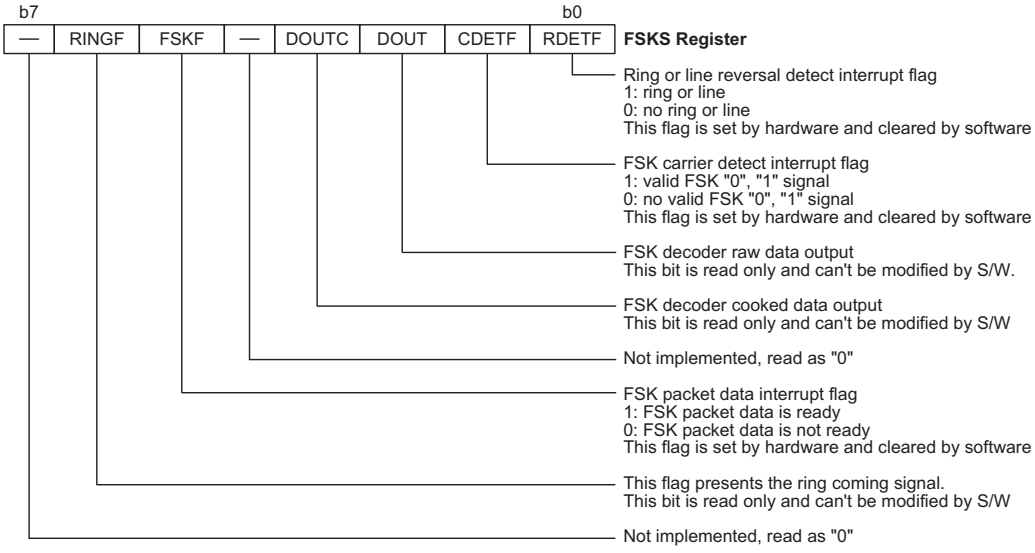
Multi-Function Interrupt Control 1 Register



Peripheral Interrupt Control Register



FSK Control Register



FSK Status Register

Reset and Initialisation

A reset function is a fundamental part of any microcontroller ensuring that the device can be set to some predetermined condition irrespective of outside parameters. The most important reset condition is after power is first applied to the microcontroller. In this case, internal circuitry will ensure that the microcontroller, after a short delay, will be in a well defined state and ready to execute the first program instruction. After this power-on reset, certain important internal registers will be set to defined states before the program commences. One of these registers is the Program Counter, which will be reset to zero forcing the microcontroller to begin program execution from the lowest Program Memory address.

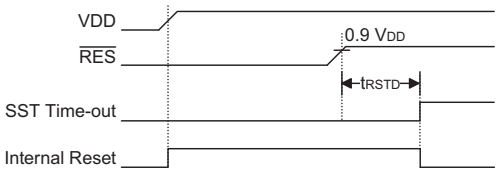
In addition to the power-on reset, situations may arise where it is necessary to forcefully apply a reset condition when the microcontroller is running. One example of this is where after power has been applied and the microcontroller is already running, the $\overline{RES}$ line is forcefully pulled low. In such a case, known as a normal operation reset, some of the microcontroller registers remain unchanged allowing the microcontroller to proceed with normal operation after the reset line is allowed to return high. Another type of reset is when the Watchdog Timer overflows and resets the microcontroller. All types of reset operations result in different register conditions being setup.

Another reset exists in the form of a Low Voltage Reset, LVR, where a full reset, similar to the $\overline{RES}$ reset is implemented in situations where the power supply voltage falls below a certain threshold.

Reset Functions

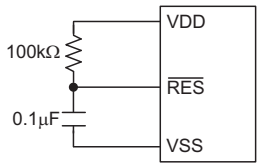
There are five ways in which a microcontroller reset can occur, through events occurring both internally and externally:

- Power-on Reset
  The most fundamental and unavoidable reset is the one that occurs after power is first applied to the microcontroller. As well as ensuring that the Program Memory begins execution from the first memory address, a power-on reset also ensures that certain other registers are preset to known conditions. All the I/O port and port control registers will power up in a high condition ensuring that all pins will be first set to inputs.
  Although the microcontroller has an internal RC reset function, if the VDD power supply rise time is not fast enough or does not stabilise quickly at power-on, the internal reset function may be incapable of providing proper reset operation. For this reason it is recommended that an external RC network is connected to the $\overline{RES}$ pin, whose additional time delay will ensure that the $\overline{RES}$ pin remains low for an extended period to allow the power supply to stabilise. During this time delay, normal operation of the microcontroller will be inhibited. After the $\overline{RES}$ line reaches a certain voltage value, the reset delay time t_{RSTD} is invoked to provide an extra delay time after which the microcontroller will begin normal operation. The abbreviation SST in the figures stands for System Start-up Timer.



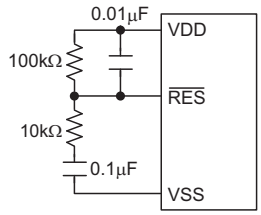
Power-On Reset Timing Chart

For most applications a resistor connected between VDD and the $\overline{RES}$ pin and a capacitor connected between VSS and the $\overline{RES}$ pin will provide a suitable external reset circuit. Any wiring connected to the $\overline{RES}$ pin should be kept as short as possible to minimise any stray noise interference.



Basic Reset Circuit

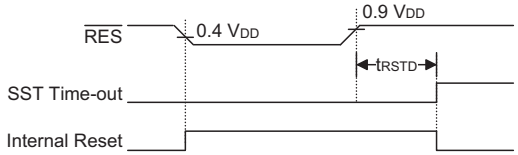
For applications that operate within an environment where more noise is present the Enhanced Reset Circuit shown is recommended.



Enhanced Reset Circuit

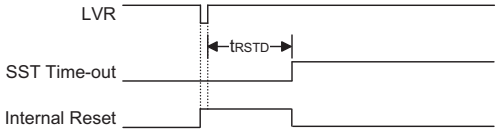
More information regarding external reset circuits is located in Application Note HA0075E on the Holtek website.

- $\overline{\text{RES}}$ Pin Reset
  This type of reset occurs when the microcontroller is already running and the $\overline{\text{RES}}$ pin is forcefully pulled low by external hardware such as an external switch. In this case as in the case of other reset, the Program Counter will reset to zero and program execution initiated from this point.



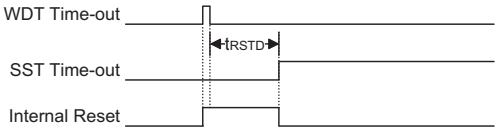
$\overline{\text{RES}}$ Reset Timing Chart

- Low Voltage Reset – LVR
  The microcontroller contains a low voltage reset circuit in order to monitor the supply voltage of the device. The LVR function is selected via a configuration option. If the supply voltage of the device drops to within a range of 0.9V~V_{LVR} such as might occur when changing the battery, the LVR will automatically reset the device internally. For a valid LVR signal, a low supply voltage, i.e., a voltage in the range between 0.9V~V_{LVR} must exist for a time greater than that specified by t_{LVR} in the A.C. characteristics. If the low supply voltage state does not exceed this value, the LVR will ignore the low supply voltage and will not perform a reset function. The actual V_{LVR} value can be selected via configuration options.



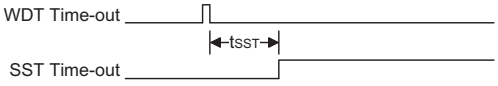
Low Voltage Reset Timing Chart

- Watchdog Time-out Reset during Normal Operation
  The Watchdog time-out Reset during normal operation is the same as a hardware $\overline{\text{RES}}$ pin reset except that the Watchdog time-out flag TO will be set to "1".



WDT Time-out Reset during Normal Operation Timing Chart

- Watchdog Time-out Reset during Power Down
  The Watchdog time-out Reset during Power Down is a little different from other kinds of reset. Most of the conditions remain unchanged except that the Program Counter and the Stack Pointer will be cleared to "0" and the TO flag will be set to "1". Refer to the A.C. Characteristics for t_{SST} details.



WDT Time-out Reset during Power Down Timing Chart

Reset Initial Conditions

The different types of reset described affect the reset flags in different ways. These flags, known as PDF and TO are located in the status register and are controlled by various microcontroller operations, such as the Power Down function or Watchdog Timer. The reset flags are shown in the table:

TO	PDF	RESET Conditions
0	0	$\overline{\text{RES}}$ reset during power-on
u	u	$\overline{\text{RES}}$ or LVR reset during normal operation
1	u	WDT time-out reset during normal operation
1	1	WDT time-out reset during Power Down

Note: "u" stands for unchanged

The following table indicates the way in which the various components of the microcontroller are affected after a power-on reset occurs.

Item	Condition After RESET
Program Counter	Reset to zero
Interrupts	All interrupts will be disabled
WDT	Clear after reset, WDT begins counting
Timer/Event Counters	The Timer Counters will be turned off
Input/Output Ports	I/O ports will be setup as inputs
Stack Pointer	Stack Pointer will point to the top of the stack

The different kinds of resets all affect the internal registers of the microcontroller in different ways. To ensure reliable continuation of normal program execution after a reset occurs, it is important to know what condition the microcontroller is in after a particular reset occurs. The following table describes how each type of reset affects each of the microcontroller internal registers.

Register	Reset (Power-on)	$\overline{RES}$ or LVR Reset (Normal/Green)	$\overline{RES}$ or LVR Reset (Sleep/Idle)	WDT Time-out (Normal/Green)	WDT Time-out (Sleep/Idle)
IAR0	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
MP0	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
IAR1	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
MP1	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
BP	--0- 0000	--0- 0000	--0- 0000	--0- 0000	--u- uuuu
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCL	0000H	0000H	0000H	0000H	0000H
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu
WDTS	0000 0111	0000 0111	0000 0111	0000 0111	uuuu uuuu
STATUS	--00 xxxx	--uu uuuu	-- 01 uuuu	-- 1u uuuu	--11 uuuu
INTC0	-000 0000	-000 0000	-000 0000	-000 0000	-uuu uuuu
TMR0H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR0C	00-0 1---	00-0 1---	00-0 1---	00-0 1---	uu-u u---
TMR1H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR1L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR1C	00-0 1---	00-0 1---	00-0 1---	00-0 1---	uu-u u---
TMR2H	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR2L	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
TMR2C	00-0 ----	00-0 ----	00-0 ----	00-0 ----	uu-u ----
FSKC	--11 11-1	--11 11-1	--11 11-1	--11 11-1	--uu uu-u
FSKS	-x0- 1100	-x0- 1100	-x0- 1100	-x0- 1100	-xu- uuuu
FSKD	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu
LBDC	---- --00	---- --uu	---- --uu	---- --uu	---- --uu
PERIC	--00 --00	--00 --00	--00 --00	--00 --00	--uu --uu
PA	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PAC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PCC	1111 --11	1111 --11	1111 --11	1111 --11	uuuu --uu
PD	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PDC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PE	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PEC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PF	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
PFC	1111 1111	1111 1111	1111 1111	1111 1111	uuuu uuuu
INTC1	-000 -000	-000 -000	-000 -000	-000 -000	-uuu -uuu

Register	Reset (Power-on)	$\overline{RES}$ or LVR Reset (Normal/Green)	$\overline{RES}$ or LVR Reset (Sleep/Idle)	WDT Time-out (Normal/Green)	WDT Time-out (Sleep/Idle)
DTMFC	---- -0-1	---- -0-1	---- -0-1	---- -0-1	---- -u-u
DTMFD	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu
DTRXC	---- -001	---- -001	---- -001	---- -001	---- -uuu
DTRXD	---- 0000	---- 0000	---- 0000	---- 0000	---- uuuu
RTCC	0-0- ----	u-u- ----	u-u- ----	u-u- ----	u-u- ----
MODE	000- ----	00u- ----	00u- ----	00u- ----	00u- ----
MODE_1	---- --00	---- --00	---- --00	---- --00	---- --00
MFIC0	-000 -000	-000 -000	-000 -000	-000 -000	-uuu -uuu
MFIC1	-000 -000	-000 -000	-000 -000	-000 -000	-uuu -uuu
PFDC	0000 ----	0000 ----	0000 ----	0000 ----	uuuu ----
PFDD	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu
SIMCTL0	1110 000-	1110 000-	1110 000-	1110 000-	uuuu uuu-
SIMCTL1	1000 0001	1000 0001	1000 0001	1000 0001	uuuu uuuu
SIMDR	xxxx xxxx	xxxx xxxx	xxxx xxxx	xxxx xxxx	uuuu uuuu
SIMAR/ SIMCTL2	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu
SCOMC	0000 0000	0000 0000	0000 0000	0000 0000	uuuu uuuu
VOICEC	---- ---0	---- ---0	---- ---0	---- ---0	---- ---u
VOL	xxxx ----	uuuu ----	uuuu ----	uuuu ----	uuuu ----
DAL	xxxx ----	uuuu ----	uuuu ----	uuuu ----	uuuu ----
DAH	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu	uuuu uuuu

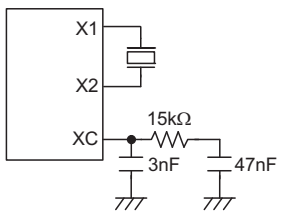
Note: "u" stands for unchanged
"x" stands for unknown
"-" stands for unimplemented

Oscillator

There are two oscillator circuits within the controller. One is for the system clock which uses an externally connected 32768Hz crystal. The other is an internal watchdog oscillator.

System Crystal/Ceramic Oscillator

The system clock is generated using an external 32768Hz crystal or ceramic resonator connected between pins X1 and X2. From this clock source an internal circuit generates a HCLK clock source which is also required by the system. This frequency generator circuit requires the addition of externally connected RC components to pin XC to form a low pass filter for the HCLK output frequency stabilisation.



Crystal/Ceramic Oscillator

Watchdog Timer Oscillator

The WDT oscillator is a fully integrated free running RC oscillator with a typical period of 65μs at 5V, requiring no external components. It is selected via configuration option. If selected, when the device enters the Power Down Mode, the system clock will stop running, however the WDT oscillator will continue to run and keep the watchdog function active. However, as the WDT will consume a certain amount of power when in the Power Down Mode, for low power applications, it may be desirable to disable the WDT oscillator by configuration option.

Operation Mode, Power-down and Wake-up

There are four operational modes, known as the idle mode, sleep mode, green mode, and normal mode. The chosen mode is selected using the MODE0, MODE1 and UPEN bits in the MODE register but also depends upon whether the HALT instruction has been executed or not.

HALT Instruction	MODE1	MODE0	UPEN	Operation Mode	32768Hz	HCLK	System Clock
Not executed	1	X	1	Normal	ON	ON	HCLK
Not executed	0	X	0	Green	ON	OFF	32768Hz
Executed	0	0	0	Sleep	ON	OFF	Stopped
Executed	0	1	0	Idle	OFF	OFF	Stopped

Note: "X" means don't care
MODE0 will be cleared to 0 automatically after wake-up from Idle Mode.
HCLK is frequency from PLL, which is 3.58MHz, 7.16MHz, 10.74MHz or 14.32MHz.

Idle Mode

When the device enters this mode, the normal operating current, will be reduced to an extremely low standby current level. This occurs because when the device enters the Power Down Mode, both the HCLK and 32768Hz system oscillators are stopped which reduces the power consumption to extremely low levels, however, as the device maintains its present internal condition, it can be woken up at a later stage and continue running, without requiring a full reset. This feature is extremely important in application areas where the microcontroller must have its power supply constantly maintained to keep the device in a known condition but where the power supply capacity is limited such as in battery applications.

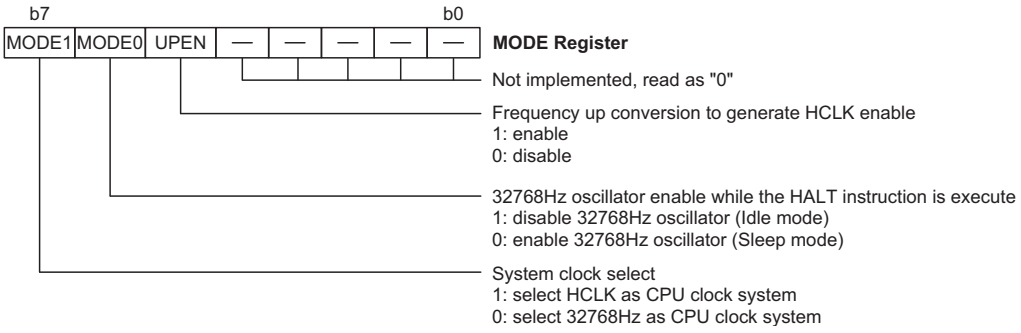
Sleep Mode

In the Sleep Mode is similar to the mode, except here the 32768Hz oscillator continues running after after the HALT instruction has been executed. This feature enables the device to continue with instruction execution immediately after wake-up.

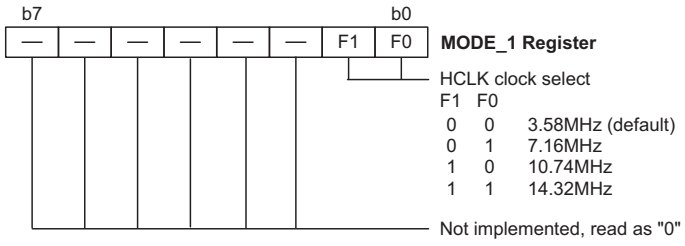
Green Mode

In the Green Mode, the 32768Hz oscillator is used as the system clock for instruction execution. The following conditions will force the microcontroller enter the Green Mode:

- Any reset condition from any operational mode
- Any interrupt occurring during the Sleep Mode or Idle Mode
- A Port A Wake-up from the Sleep Mode or Idle Mode



MODE Register



MODE_1 Register

Normal Mode

In the Normal mode the device uses the HCLK generated by the frequency-up conversion circuit as the system clock for instruction execution.

There are four high frequency clock (HCLK) for CPU which are 3.58MHz, 7.16MHz, 10.74MHz and 14.32MHz. Care must be taken with changing the system clock in Normal Mode:

Step 1: Clear bit MODE1 to ″0″
Step 2: Clear UPEN bit to ″0″
Step 3: Set bits of register MODE_1 for the frequency of HCLK
Step 4: Set bit UPEN to ″1″
Step 5: Execute a 20ms software delay
Step 6: Set bit MODE1 to ″1″

After Step 6, the system clock will be changed according to the setting in MODE_1.

Changing the Operational Mode

Holtek's telephone controllers support two system clocks and four operational modes. The system clock can be either 32768Hz or HCLK and the operational mode can be either Normal, Green, Sleep or Idle Mode. The operation mode is selected using software in the following way:

- Normal Mode to Green Mode:
  Clear bit MODE1 to ″0″, which will change the operational mode to the Green Mode.
  The UPEN bit status is not changed. However, the UPEN bit can be cleared by software.
- Normal Mode or Green Mode to Sleep Mode:
  Step 1: Clear bit MODE0 to ″0″
  Step 2: Clear bit MODE1 to ″0″
  Step 3: Clear bit UPEN to ″0″
  Step 4: Execute the HALT instruction
  After Step 4, the operational mode will be changed to the Sleep Mode.
- Normal mode or Green Mode to Idle Mode:
  Step 1: Set bit MODE0 to ″1″
  Step 2: Clear bit MODE1 to ″0″
  Step 3: Clear bit UPEN to ″0″
  Step 4: Execute the HALT instruction
  After Step 4, the operational mode will be changed to the Idle Mode.
- Green Mode to Normal Mode:
  Step 1: Set bit UPEN to ″1″
  Step 2: Execute a 20ms software delay
  Step 3: Set bit MODE1 to ″1″
  After Step 3, the operational mode will be changed to the Normal Mode.
- Sleep Mode or Idle Mode to Green Mode:
  Method 1: The occurrence of any reset condition
  Method 2: Any active interrupt
  Method 3: A Port A wake-up

Note that a Timer/Event Counter 0/1 and RTC interrupt will not be generated when in the Idle Mode as the 32768Hz crystal oscillator is stopped.

Standby Current Considerations

As the main reason for entering the Power Down Mode is to keep the current consumption of the MCU to as low a value as possible, perhaps only in the order of several micro-amps, there are other considerations which must also be taken into account by the circuit designer if the power consumption is to be minimised. Special attention must be made to the I/O pins on the device. All high-impedance input pins must be connected to either a fixed high or low level as any floating input pins could create internal oscillations and result in increased current consumption. Care must also be taken with the loads, which are connected to I/Os, which are setup as outputs. These should be placed in a condition in which minimum current is drawn or connected only to external circuits that do not draw current, such as other CMOS inputs. Also note that additional standby current will also be required if the configuration options have enabled the Watchdog Timer internal oscillator.

Wake-up

A reset, interrupt or port A wake-up can all wake up the device from the Sleep Mode or the Idle Mode. A reset can include a power-on reset, an external reset or a WDT time-out reset. By examining the device status flags, PDF and TO, the program can distinguish between the different reset conditions. Refer to the Reset section for a more detailed description.

A port A wake-up and an interrupt can be considered as a continuation of normal execution. Each bit in port A can be independently selected to wake-up the device using configuration options. When awakened by a Port A stimulus, the program will resume execution at the next instruction following the HALT instruction.

Any valid interrupt during the Sleep Mode or Idle Mode may have one of two consequences. One is if the related interrupt is disabled or the interrupt is enabled but the stack is full, the program will resume execution at the next instruction. The other is if the interrupt is enabled and the stack is not full, the regular interrupt response takes place. It is necessary to mention that if an interrupt request flag is set to ″1″ before entering the Sleep Mode or Idle Mode, the Wake-up function of the related interrupt will be disabled.

Once a Sleep Mode or Idle Mode Wake-up event occurs, it will take an SST delay time, which is 1024 system clock periods, to resume to the Green Mode. This means that a dummy period is inserted after a Wake-up. If the Wake-up results from an interrupt acknowledge signal, the actual interrupt subroutine execution will be delayed by one or more cycles. If the Wake-up results in the next instruction execution, this will be executed immediately after the dummy period has finished.

To minimise power consumption, all the I/O pins should be carefully managed before entering the Sleep Mode or Idle Mode.

The Sleep Mode or Idle Mode is initialised by a HALT instruction and results in the following.

- The system clock will be turned off.
- The WDT function will be disabled if the WDT clock source is the instruction clock.
- The WDT function will be disabled if the WDT clock source is the 32768Hz oscillator in the Idle mode.
- The WDT will still function if the WDT clock source is the WDT internal oscillator.
- If the WDT function is still enabled, the WDT counter and WDT prescaler will be cleared and resume counting.
- The contents of the on chip Data Memory and registers remain unchanged.
- All the I/O ports maintain their original status.
- The PDF flag is set and the TO flag is cleared by hardware.

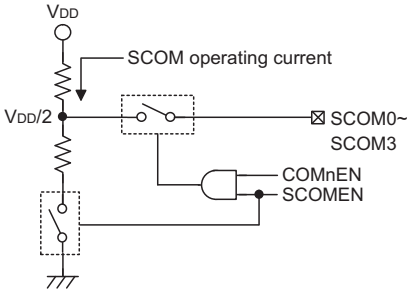
SCOM Function for LCD

The devices have the capability of driving external LCD panels. The common pins for LCD driving, SCOM0~SCOM3, are pin shared with certain pin on the PD0~PD3 port. The LCD signals (COM and SEG) are generated using the application program.

LCD Operation

An external LCD panel can be driven using this device by configuring the PD0~PD3 pins as common pins and using other output ports lines as segment pins. The LCD driver function is controlled using the SCOMC register which in addition to controlling the overall on/off function also controls the bias voltage setup function. This enables the LCD COM driver to generate the necessary $V_{DD}/2$ voltage levels for LCD 1/2 bias operation.

The SCOMEN bit in the SCOMC register is the overall master control for the LCD Driver, however this bit is used in conjunction with the COMnEN bits to select which Port D pins are used for LCD driving. Note that the Port Control register does not need to first setup the pins as outputs to enable the LCD driver operation.



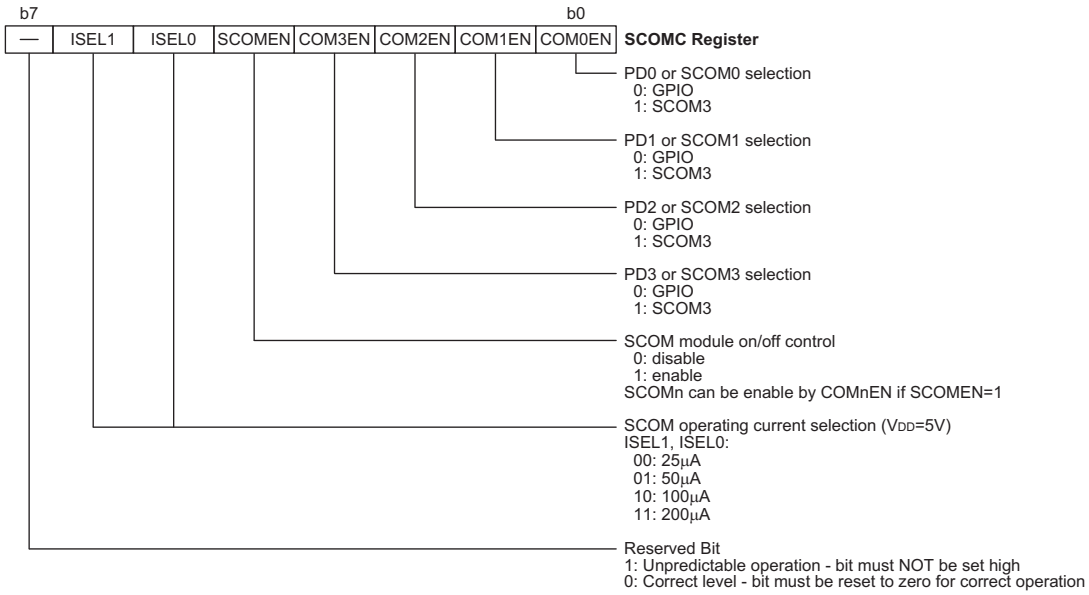
LCD COM Bias

SCOMEN	COMnEN	Pin Function	O/P Level
0	X	I/O	0 or 1
1	0	I/O	0 or 1
1	1	SCOMN	$V_{DD}/2$

Output Control

LCD Bias Control

The LCD COM driver enables a range of selections to be provided to suit the requirement of the LCD panel which is being used. The bias resistor choice is implemented using the ISEL1 and ISEL0 bits in the SCOMC register.



SCOMC Register

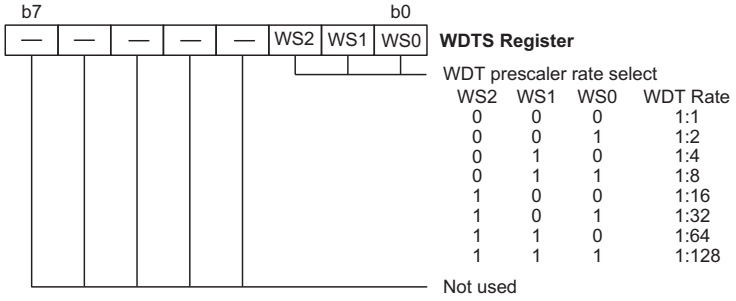
Watchdog Timer

The Watchdog Timer is provided to prevent program malfunctions or sequences from jumping to unknown locations, due to certain uncontrollable external events such as electrical noise. It operates by providing a device reset when the WDT counter overflows. The WDT clock is supplied by one of three sources selected by a configuration option. These can be its own self-contained dedicated internal WDT oscillator, external 32768Hz or the instruction clock which is the system clock divided by 4. Note that if the WDT configuration option has been disabled, then any instruction relating to its operation will result in no operation.

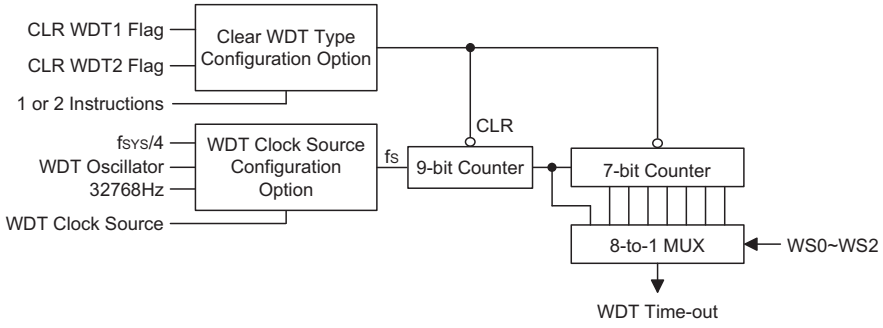
A configuration option can select the instruction clock, which is the system clock divided by 4, as the WDT clock source instead of the internal WDT oscillator. If the instruction clock is used as the clock source, it must be noted that when the system enters the Power Down Mode, as the system clock is stopped, then the WDT clock source will also be stopped. Therefore the WDT will lose its protecting purposes. In such cases the system cannot be restarted by the WDT and can only be restarted using external signals. For systems that operate in noisy environments, using the internal WDT oscillator or 32768Hz oscillator is therefore the recommended choice.

Under Normal Mode and Green Mode operation, a WDT time-out will initialise a device reset and set the status bit TO. However, if the system is in the Sleep Mode or Idle Mode, when a WDT time-out occurs, only the Program Counter and Stack Pointer will be reset. Three methods can be adopted to clear the contents of the WDT and the WDT prescaler. The first is an external hardware reset, which means a low level on the $\overline{RES}$ pin, the second is using the watchdog software instructions and the third is via a ″HALT″ instruction.

There are two methods of using software instructions to clear the Watchdog Timer, one of which must be chosen by configuration option. The first option is to use the single ″CLR WDT″ instruction while the second is to use the two commands ″CLR WDT1″ and ″CLR WDT2″. For the first option, a simple execution of ″CLR WDT″ will clear the WDT while for the second option, both ″CLR WDT1″ and ″CLR WDT2″ must both be executed to successfully clear the WDT. Note that for this second option, if ″CLR WDT1″ is used to clear the WDT, successive executions of this instruction will have no effect, only the execution of a ″CLR WDT2″ instruction will clear the WDT. Similarly, after the ″CLR WDT2″ instruction has been executed, only a successive ″CLR WDT1″ instruction can clear the Watchdog Timer.



Watchdog Timer Register



Watchdog Timer

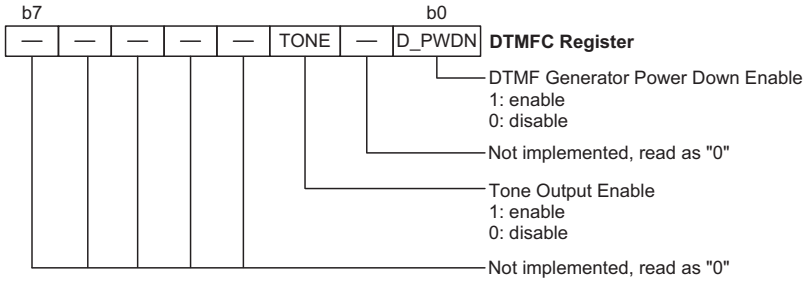
DTMF Generator

The device includes a fully integrated DTMF, Dual-Tone Multiple-Frequency, generator function. This functional block can generate the necessary16 dual tones and 8 single tones for DTMF signal generation. The signal will be provided on the DTMF pin of the device. The DTMF generator also includes a power down and a tone on/off function. The clock source for the DTMF generator is the 3.58MHz oscillator. Before the DTMF function is used, the device must have been placed into the Normal Mode.

Note that the clock source for the DTMF generator is fixed at 3.58MHz and it's not related to which HCLK is selected for the device. Therefore, the designer doesn't have to switch the HCLK to 3.58MHz for this DTMF generator function, if this device is operating under the other HCLKs, such as 7.16MHz, 10.74MHz and 14.32MHz.

DTMF Generator Control

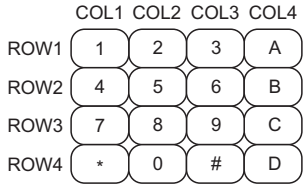
The DTMF Generator is controlled by two registers, a control register known as DTMFC and a data register known as DTMFD. The power down mode will terminate all the DTMF generator functions and can be activated by setting the D_PWDN bit in the DTMFC register to 1. These two registers, DTMFC and DTMFD are still accessible even if the DTMF function is in the power down mode. The generation duration time of the DTMF output signal should be determined by the software. The DTMFD register value can be changed as desired, at which point the DTMF pin will output the new dual-tone simultaneously.



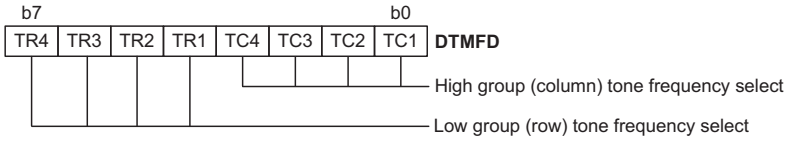
DTMF Generator Control Register

DTMF Generator Frequency Selection

The DTMF pin output is controlled using a combination of the D_PWDN, TONE, TR~TC bits.



DTMF Dialing Matrix



DTMF Generator Data Register

Control Register Bits			DTMF Pin Output Status
D_PWDN	TONE	TR4~TR1/TC4~TC1	
1	x	x	0
0	0	x	1/2 VDD
0	1	0	1/2 VDD
0	1	Any valid value	16 dual tones or 8 signal tones, bias at 1/2 VDD

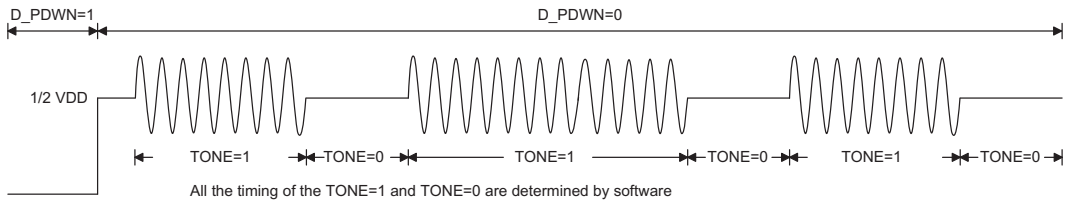
Output Frequency (Hz)		% Error
Specified	Actual	
697	699	+0.29%
770	766	–0.52%
852	847	–0.59%
941	948	+0.74%
1209	1215	+0.50%
1336	1332	–0.30%
1477	1472	–0.34%

% Error does not contain the crystal frequency shift

DTMF Frequency Selection Table

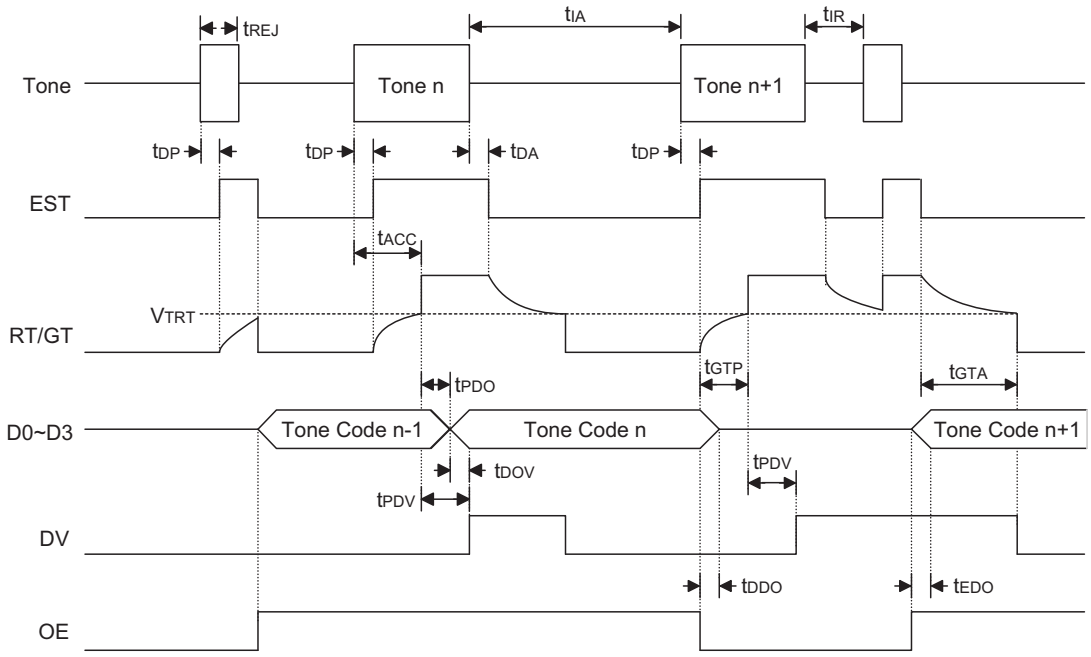
Low Group				High Group				DTMF Output		Code
TR4	TR3	TR2	TR1	TC4	TC3	TC2	TC1	Low	High	
0	0	0	1	0	0	0	1	697	1209	1
0	0	0	1	0	0	1	0	697	1336	2
0	0	0	1	0	1	0	0	697	1477	3
0	0	0	1	1	0	0	0	697	1633	A
0	0	1	0	0	0	0	1	770	1209	4
0	0	1	0	0	0	1	0	770	1336	5
0	0	1	0	0	1	0	0	770	1477	6
0	0	1	0	1	0	0	0	770	1633	B
0	1	0	0	0	0	0	1	852	1209	7
0	1	0	0	0	0	1	0	852	1336	8
0	1	0	0	0	1	0	0	852	1477	9
0	1	0	0	1	0	0	0	852	1633	C
1	0	0	0	0	0	0	1	941	1209	*
1	0	0	0	0	0	1	0	941	1336	0
1	0	0	0	0	1	0	0	941	1477	#
1	0	0	0	1	0	0	0	941	1633	D
Single tone for testing only										
0	0	0	1	0	0	0	0	697	x	x
0	0	1	0	0	0	0	0	770	x	x
0	1	0	0	0	0	0	0	852	x	x
1	0	0	0	0	0	0	0	941	x	x
0	0	0	0	0	0	0	1	x	1209	x
0	0	0	0	0	0	1	0	x	1336	x
0	0	0	0	0	1	0	0	x	1477	x
0	0	0	0	1	0	0	0	x	1633	x

Writing other values to TR4~TR1, TC4~TC1 may generate an unpredictable tone.

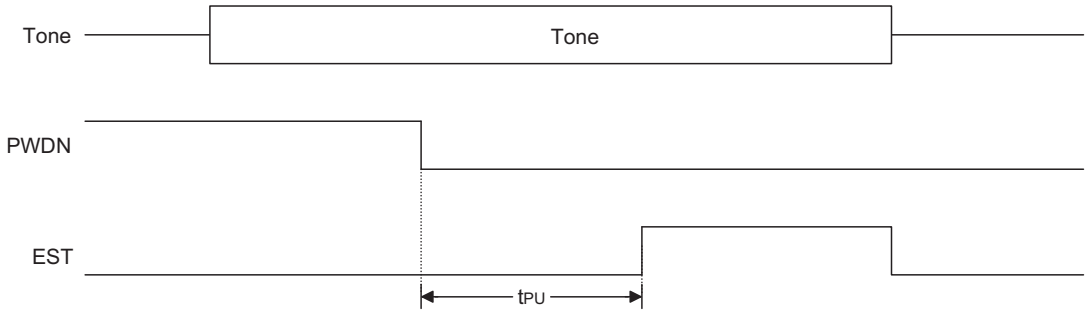


DTMF Output

Timing Diagrams



Steering Timing

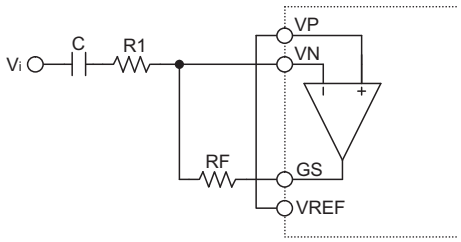


Power-up Timing

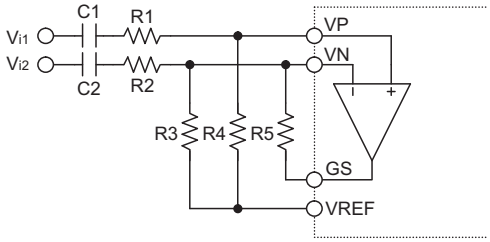
DTMF Receiver

The device contains a fully integrated DTMF receiver which will decode the DTMF frequency content of incoming analog DTMF signals. An internal operational amplifier is also supplied to adjust the input signal level as shown. There is also a pre-filter function which is a band rejection filter tp reject frequencies between 350Hz and 400Hz. The low group filter filters the low group frequency signal output, whereas the high group filter filters the high group frequency signal output. Each filter output is followed by a zero-crossing detector which includes hysteresis. When the signal amplitude at the output exceeds a specified level, it is transferred into a full swing logic signal.

(a) Standard Input Circuit



(b) Differential Input Circuit

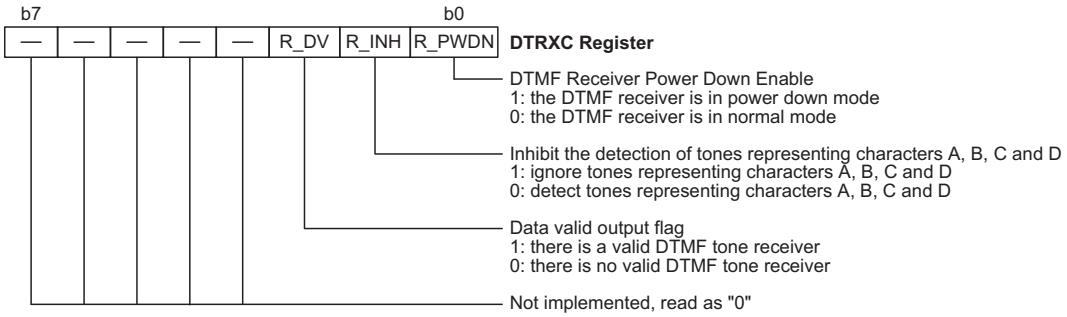


When the input signal is recognized as an effective DTMF tone, a peripheral interrupt will be generated, and the corresponding DTMF tone code will be generated.

Bit No.	Label	R/W	Function
0	R_PWDN	RW	DTMF Receiver Power Down Enable R_PWDN= 0 → The DTMF receiver is in normal mode; R_PWDN= 1 → The DTMF receiver is in power down mode After reset, R_PWDN = 1
1	R_INH	RW	Inhibit the detection of tones representing characters A, B, C and D R_INH= 0 → detect tones representing characters A, B, C and D R_INH= 1 → ignore tones representing characters A, B, C and D After reset, R_INH = 0
2	R_DV	RW	Data valid output flag R_DV= 0 → There is no valid DTMF tone received R_DV= 1 → There is a valid DTMF tone received
7~3	—	RO	Unused bit, read as ″0″

Note: R_DV should be cleared manually if necessary.

DTMF Receiver Status



DTMF Receiver Control Register

DTMF Receiver Data Register

DTMF Data Output Table

Low Group (Hz)	High Group (Hz)	Digit	D3, D2, D1, D0
697	1209	1	0001
697	1336	2	0010
697	1477	3	0011
770	1209	4	0100
770	1336	5	0101
770	1477	6	0110
852	1209	7	0111
852	1336	8	1000
852	1477	9	1001
941	1336	0	1010
941	1209	*	1011
941	1477	#	1100
697 (Note*)	1633	A	1101
770 (Note*)	1633	B	1110
842 (Note*)	1633	C	1111
941 (Note*)	1633	D	0000

(Note*): Available only when R_INH=0

Steering Control Circuit

The steering control circuit is used to measure the effective signal duration and for protecting against a valid signal drop out. This is achieved using an analog delay which is implemented using an external RC time-constant, controlled by the output line EST.

The timing diagram shows more details. The EST pin is normally low and will pull the RT/GT pin low via the external RC network. When a valid tone input is detected, the EST pin will go high, which will in turn pull the RT/GT pin high through the RC network.

When the voltage on RT/GT rises from 0 to V_{TRT}, which is 2.35V for a 5V power supply, the input signal is effective, and the corresponding code will be generated by the code detector. After D0~D3 have been latched, DV will go high. When the voltage on RT/GT falls from V_{DD} to V_{TRT}, i.e. when there is no input tone, the DV output will go low, and D0~D3 will maintain their present data until a next valid tone input is produced. By selecting suitable external RC values, the minimum acceptable input tone duration, t_{ACC}, and the minimum acceptable inter-tone rejection, t_{IR}, can be set. The values of the external RC components, can be chosen using the following formula.

$t_{ACC}=t_{DP}+t_{GTP}$;

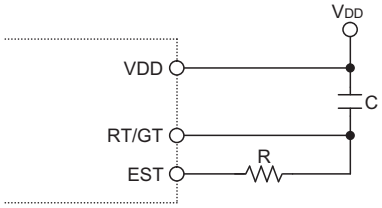
$t_{IR}=t_{DA}+t_{GTA}$;

Where t_{ACC}: Tone duration acceptable time
t_{DP}: EST output delay time (″L″ → ″H″)
t_{GTP}: Tone present time
t_{IR}: Inter-digit pause rejection time
t_{DA}: EST outptu delay time (″H″ → ″L″)
t_{GTA}: Tone absent time

(a) Fundamental circuit:

$t_{GTP} = R \times C \times Ln (V_{DD} / (V_{DD} - V_{TRT}))$

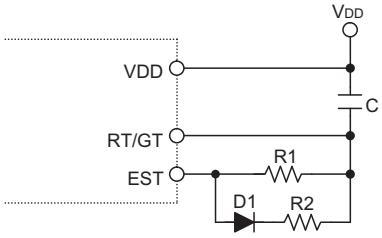
$t_{GTA} = R \times C \times Ln (V_{DD} / V_{TRT})$



(b) $t_{GTP} < t_{GTA}$:

$t_{GTP} = (R1 // R2) \times C \times Ln (V_{DD} - V_{TRT}))$

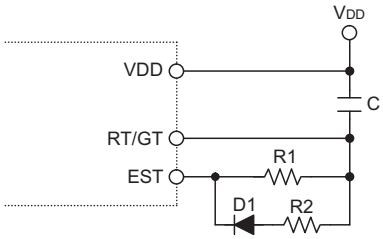
$t_{GTA} = R1 \times C \times Ln (V_{DD} / V_{TRT})$



(c) $t_{GTP} > t_{GTA}$:

$t_{GTP} = R1 \times C \times Ln (V_{DD} / (V_{DD} - V_{TRT}))$

$t_{GTA} = (R1 // R2) \times C \times Ln (V_{DD} / V_{TRT})$



Steering Time Adjustment Circuits

FSK Decoder

The FSK decoder supports four interrupt sources to the peripheral interrupt vector, which are FSK raw data falling edge, ring detect or line reversal detect, FSK carrier detect and FSK packet data. Write ″1″ to the control flag EFSKDI in PERIC register, or write ″0″ to the control flags, RMSK, CMSK and FMSK in FSKC register, will enable these interrupts. When any of these interrupts occurs, its interrupt flag (FSKDF in PERIC register; RDETF, CDETF, and FSKF in FSKS register) will be set to 1 by hardware even if the interrupt is disabled. These interrupts will cause a peripheral interrupt if the peripheral interrupt is enabled. When the peripheral interrupt occurs, the interrupt request flag PERF will be set and a subroutine call to location 10H will occur. Returning from the interrupt subroutine, the interrupt flag FSKDF, RDETF, CDETF or FSKF will not be cleared by hardware, the user should clear it by software. If interrupt flag RDETF is not cleared, next ring detect interrupt will be inhibited, other interrupt flags CDETF, FSKF, FSKDF have the same behavior. The Power Down Mode (F_PWDN=1) will terminate all the FSK decoder function, however, the registers FSKC, FSKS and FSKD are accessible at this Power Down Mode.

Care must be taken with FSK raw data falling edge interrupt. If the EFSKDI is enabled, then that will disable the RMSK, CMSK and FMSK interrupts. The designer should take care the software design flow to decoder the FSK signals.

Ring or Line Reversal Detect

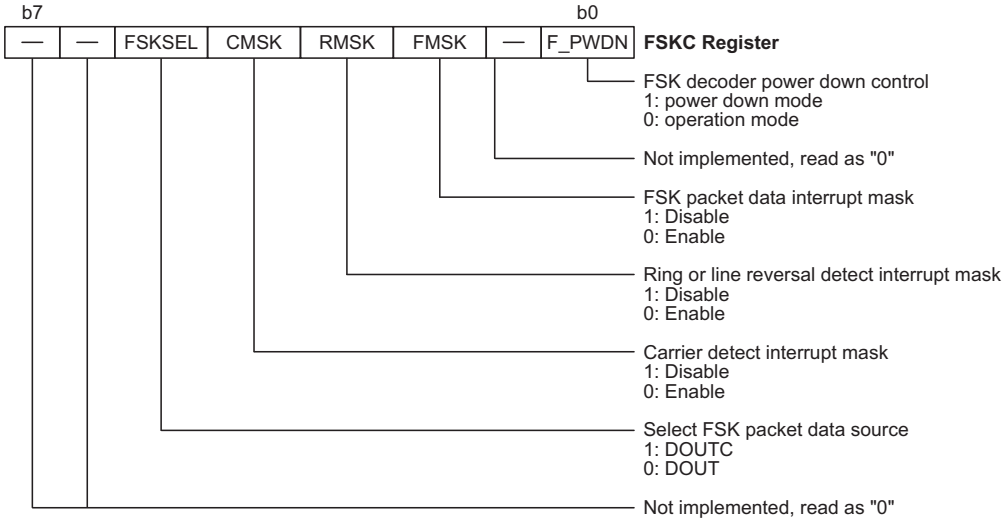
When no signal is present on the telephone line, RDET will be at GND and $\overline{\text{RTIME}}$ is pulled to VDD by R1. If a line reversal occurs, the RDET1 pin will become high. This causes $\overline{\text{RTIME}}$ and internal signal R_DET to be pulled low. The C1 and R1 ensure that the R_DET signal is low during such a time, so that processor can detect it. When a ring occurs on the line, internal signal R_DET is permanently low, indicating the envelope of the ring. If the frequency of the ring must be measured, C1 may be removed, $\overline{\text{RTIME}}$ and R_DET inverter follow RDET. The flag RDETF will go high when the R_DET signal falling edge is detected. This may cause a peripheral interrupt if RMSK is ″0″ and the peripheral interrupt is enabled (EPERI=1).

FSK Data Output

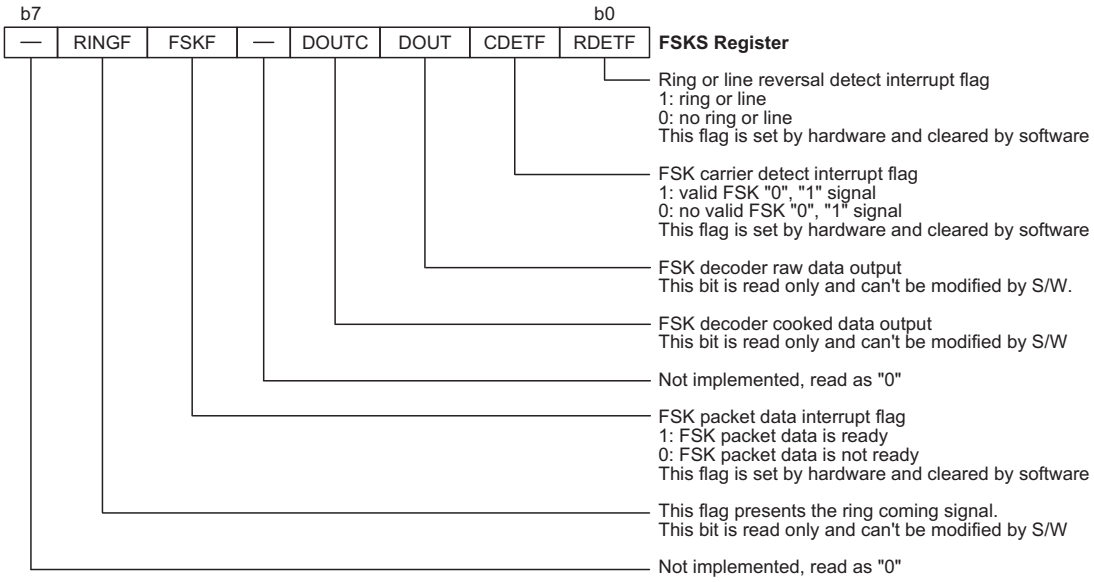
The FSK decoder will decode the FSK signal on the TIP and RING line and produce two kinds of data formats, the serial data and the 8-bit packet data. It also provides the FSK carrier detection signal. To enable the FSK decoder, the F_PWDN should be written as ″0″. Once the FSK carrier signal is detected, the flag CDETF will be set to ″1″. This may cause a peripheral interrupt if CMSK is ″0″ and the peripheral interrupt is enabled. The serial FSK data is present in two formats: RAW data and COOK data, and could be monitored by the flag DOUT, DOUTC, respectively. The flag DOUT presents the output of the decoder when the decoder is at operation mode. This data stream includes the alternate 1 and 0 patterns, the marking and the data. The flag DOUTC presents the output of the decoder when the decoder is at operation mode. This data stream is like the DOUT flag but does not include the alternate 1 and 0 patterns. If the FSK data is not detected, the DOUT and DOUTC are held high. User can use the FSK raw data falling edge interrupt with DOUT flag and a timer to implement data decoding by software or by the build-in decoding hardware which is described next.

Beside the serial data, the decoder also provides FSK packet data. When decoder receives an FSK signal, it will packet 10 bits data to 8 bits data, the first and 10th bits will be discarded. When the 8-bit packet data is valid, it will be stored in the FSK data register FSKD, the FSK packet data interrupt flag FSKF will be set to ″1″. This may cause a peripheral interrupt if FMSK is ″0″ and the peripheral interrupt is enabled. The FSK packet source could be DOUT or DOUTC, selected by FSKSEL. Note that the start bit of the 10 packet bit should be ″0″, so the MARK signal (one of the FSK data signals) will not be packeted.

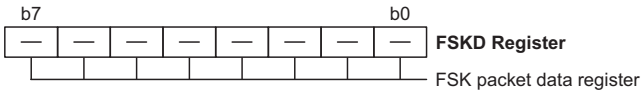
To detect the carrier signal or decode the serial data or packet 10-bit data to 8-bit data, the operation mode of the controller must be selected in Normal mode. When the operation mode is Green or Sleep, FSK decoder will decode the wrong signal. However, when the operation mode is Green or Sleep mode and the FSK decoder is at power down mode (F_PWDN=1), the ring and line reversal detect is still functional.



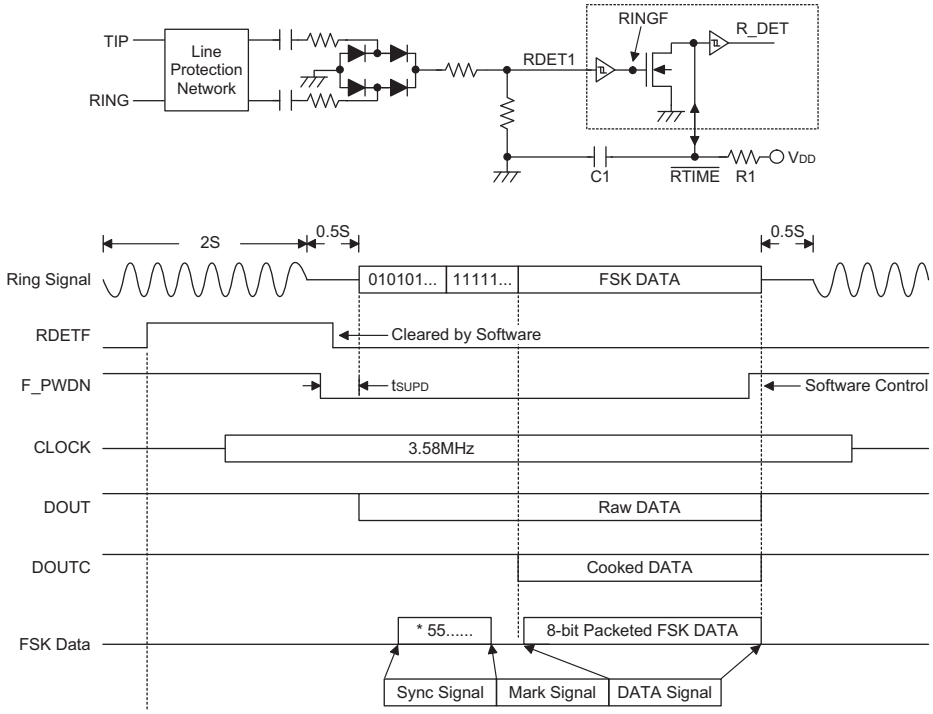
FSK Control Register



FSK Status Register



FSKD Register



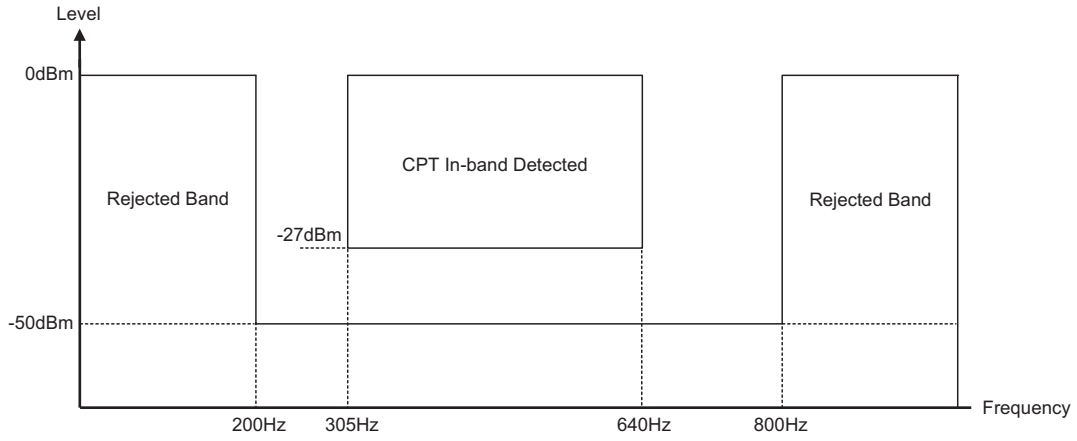
Note: "*" If the flag FSKSEL=1, the sync signal data will not be packeted.

Call Progress Tone Detector

This Device fully integrated the CPT detector, which has the advantages of low power consumption, wide CPT Band detection range from 305Hz to 640Hz, as well as high performance, is very suitable for Auto-dialing system in Telecom applications.

The internal call progress tone detector can be used in world wide countries. Below is an illustration of a call progress tone frequency band, and a table of U.S.A. CPT signal is shown for user reference.

The designer can use a GPIO pin to detect the output signal, through software to distinguish correct cadence of CTP to fit any country CPT SPEC requirement for world wide application purposes. Note that the CPT detector can be disabled by CPTEN pin. The designer can use an external GPIO pin to enable and disable the CPT decoder in order to reduce power consumption.

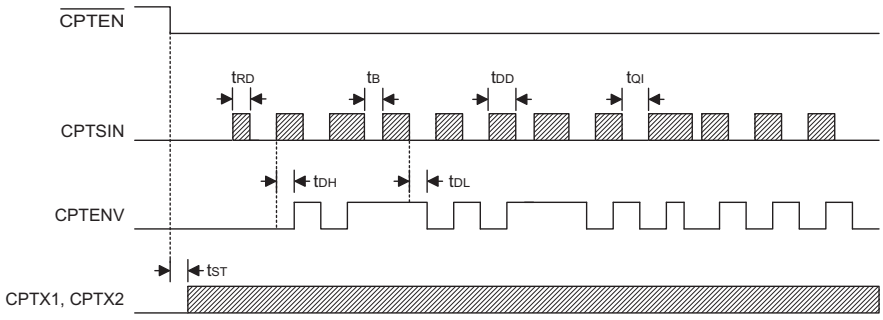


Call progress tone frequency band illustration

U.S.A. Call Progress Tone Signal Format

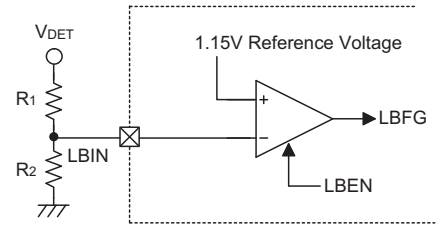
Tone	Frequency	Condition
Precision Dial Tone	350Hz+440Hz	Continuous high
Old Dial Tone	120Hz (or 133Hz, ..) +600Hz	Continuous high
Precision Busy Tone	480Hz+620Hz	0.5sec high and 0.5sec low
Old Busy Tone	120Hz+600Hz	0.5sec high and 0.5sec low
Precision Reorder Tone	480Hz+620Hz	0.3sec high and 0.2sec low
Old Reorder Tone	120Hz+600Hz	0.2sec high and 0.3sec low or 0.25sec high and 0.25sec low
Precision Ring-back Tone	440Hz+480Hz	2sec high and 4sec low
Old Ring-back Tone	40Hz (or the others) +420Hz	2sec high and 4sec low

Timing Diagram



Low Battery Detection

The phone controller provides a circuit that detects the LBIN pin voltage level. To enable this detection function, the LBEN should be written as 1. Once this function is enabled, the detection circuit needs 50us to be stable. After that, the user could read the result from LBFG. The low battery detect function will consume power. For power saving, write 0 to LBEN if the low battery detection function is unnecessary.

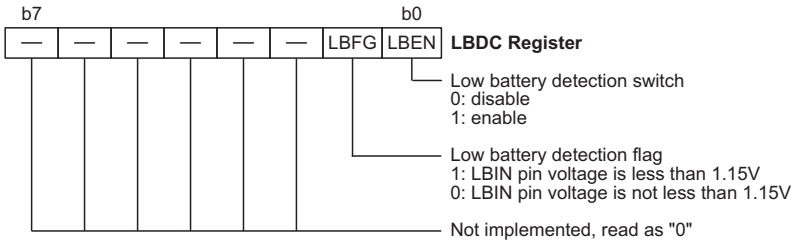


The battery low threshold is determined by external R1 and R2 resistors.

$$1.15=\frac{V_{DET}xR2}{R1+R2} \rightarrow V_{DET}=\frac{1.15x(R1+R2)}{R2}$$

If we want to detect V_{DET}=2.4V

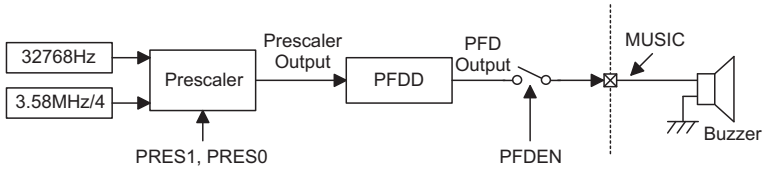
$$\text{then } 2.4V=\frac{1.15x(R1+R2)}{R2} \rightarrow R1=1.087R2$$



LBDC Register

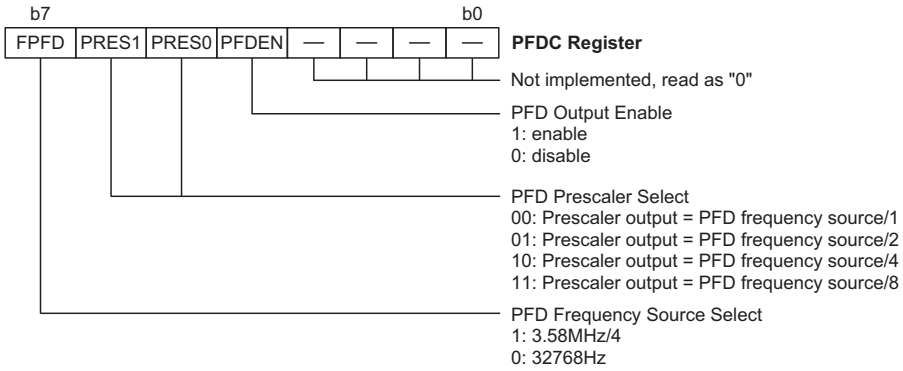
Programmable Frequency Divider (PFD) Generator – MUSIC

A Programmable Frequency Divider function, otherwise known as PFD, is integrated within the microcontroller, providing a means of accurate frequency generation. It is composed of two functional blocks: a prescaler and a general counter.



PFD Control Register

The overall PFD function is controlled using the PFDC register. The prescaler is controlled by the register bits, PRES0 and PRES1. The general counter is programmed by an 8-bit register PFDD. The clock source for the PFD can be selected to be either the 3.58MHz/4 or the 32768Hz oscillator. To enable the PFD output, the PFDEN bit should be set to 1. When the PFD is disabled the PFDD register is inhibited to be written to. To modify the PFDD contents, the PFD must be enabled. When the generator is disabled, the PFDD is cleared by hardware.



PFD Data Register

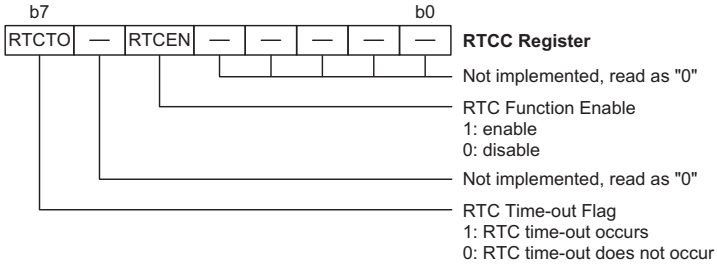
Bit No.	Label	R/W	Function
7~0	—	RW	PFD data register

PFDD (2FH) Register

$$PFD\_Output\_Frequency = \frac{Prescaler\_Output}{2x(N+1)}$$, where N = the value of the PFD Data

RTC Function

When RTC 1000ms time-out occurs, the hardware will set the interrupt request flag RTCF and the RTCTO flag to ″1″. When the interrupt service routine is serviced, the interrupt request flag (RTCF) will be cleared to 0, but the flag RTCTO remains in its original values. This bit (RTCTO) should be cleared only by software. However, next RTC interrupt will still occur, even though the RTCTO flag is not cleared.



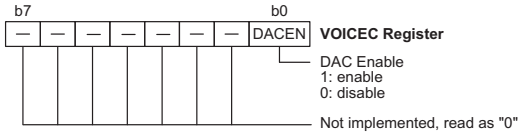
Voice Output

Voice Control

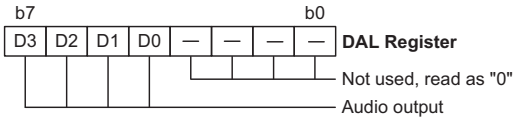
The voice control register controls the DAC circuit. If the DAC circuit is not enabled, any DAH/DAL outputs will be invalid. Selection the configuration option of PC1/AUD for DAC audio output first and writing a ″1″ to the DACEN bit will enable the DAC circuit, while writing a ″0″ to the DAC bit will disable the DAC circuit.

Audio Output and Volume Control – DAL, DAH, VOL, VOICEC

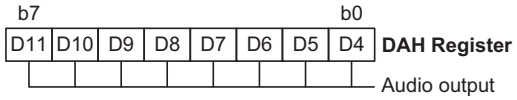
The audio output is 12-bits wide whose highest 8-bits are written into the DAH register and whose lowest four bits are written into the highest four bits of the DAL register. Bits 0~3 of the DAL register are always read as zero. There are 8 levels of volume which are setup using the VOL register. Only the highest 3-bits of this register are used for volume control, the other bits are not used and read as zero.



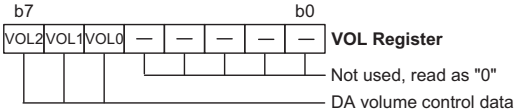
VOICE Control Register



Digital to Analog Data Low Register



Digital to Analog Data High Register



Volume Control Register

Configuration Options

Configuration options refer to certain options within the MCU that are programmed into the device during the programming process. During the development process, these options are selected using the HT-IDE software development tools. As these options are programmed into the device using the hardware programming tools, once they are selected they cannot be changed later by the application software.

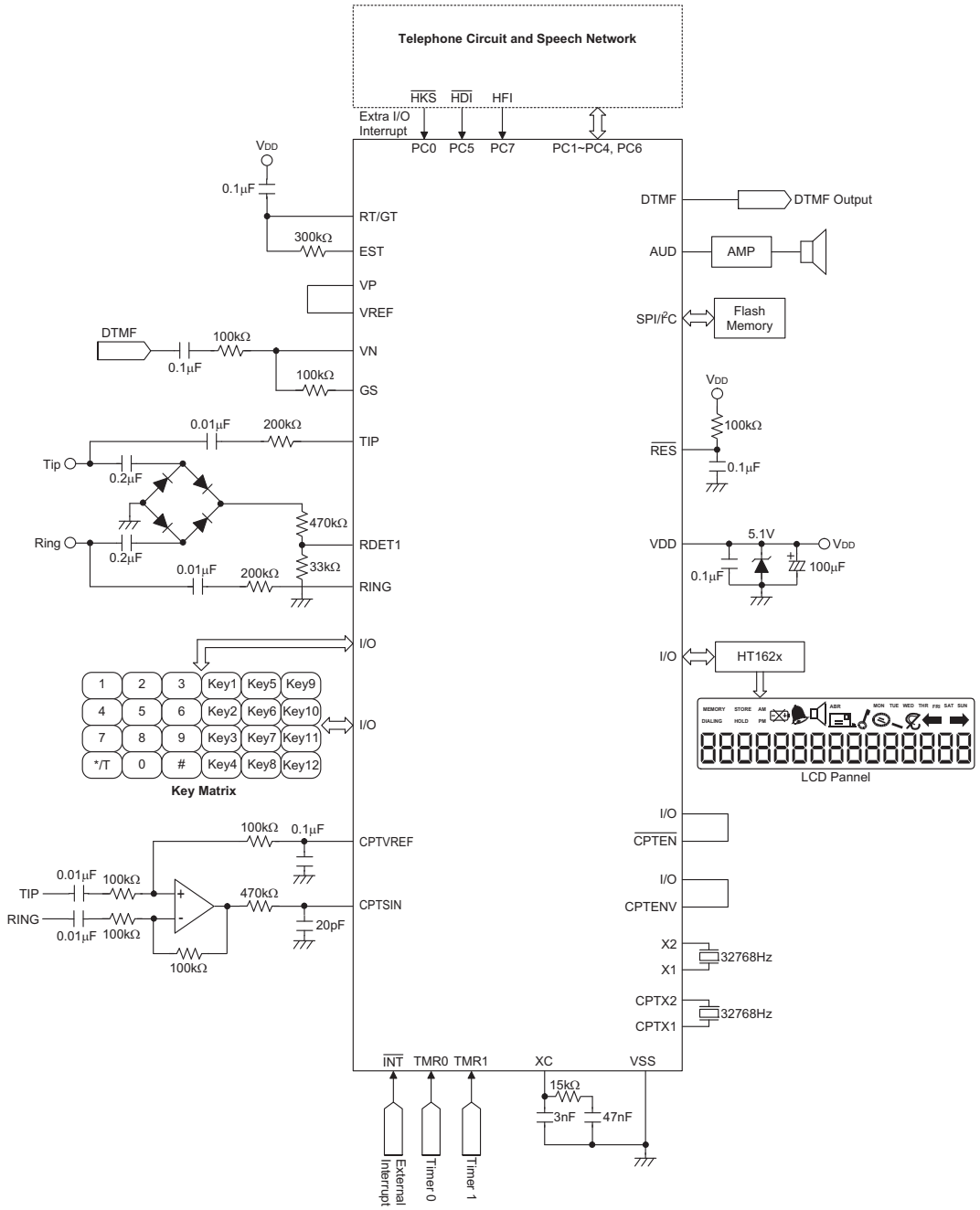
All options must be defined for proper system function, the details of which are shown in the table.

Name	Options
I/O Options	
Wake-up PA	Port A wake-up selection. Defines the activity of wake-up function. All port A have the capability to wake-up the device from a Power-down condition. This wake-up function is selected per bit.
Pull-high PA Pull-high PC0~PC1 Pull-high PC4~PC7 Pull-high PD Pull-high PE Pull-high PF	Pull-high option. This option determines whether the pull-high resistance is viable or not. Port A pull-high option is selected per bit. Port C pull-high option is selected per bit. Port D pull-high option is selected per nibble. Port E pull-high option is selected per nibble. Port F pull-high option is selected per nibble.
Watchdog Options	
CLRWDT	This option defines how to clear the WDT by instruction. One clear instruction → The ″CLR WDT″ can clear the WDT. Two clear instructions → Only when both of the ″CLR WDT1″ and ″CLR WDT2″ have been executed, then WDT can be cleared.
WDT	Watchdog enable/disable
WDT Clock Source	WDT clock source selection RC → Select the WDT OSC to be the WDT source. T1 → Select the instruction clock to be the WDT source. 32kHz → Select the external 32768Hz to be the WDT source.
PDF Options	
PA3	Normal I/O or PFD output
PFD source	Timer0 or Timer1 overflow
LVR Options	
LVR	Low Voltage Reset enable or disable
LVR Voltage	Low Voltage Reset voltage; 2.1V, 3.15V or 4.2V
SPI Options	
SIM	Enable/disable
SPI_WCOL	Enable/disable
SPI_CSEN	Enable/disable, used to enable/disable (1/0) software CSEN function
I^2C Option	
I^2C debounce Time	No debounce, 1 system clock debounce, 2 system clock debounce
	RNIC I^2C running not using internal clock
VDDIO Options	
VDDIO	disable/enable (This pin is used as GPIO/PE4 when disabled)
VDDIO	PE0 use VDD or VDDIO (when VDDIO is disabled, PE0~3 use VDD as power always)
VDDIO	PE1 use VDD or VDDIO
VDDIO	PE2 use VDD or VDDIO
VDDIO	PE3 use VDD or VDDIO

Name	Options
AUD Option	
DAC output	Enable/disable
Lock Options	
	Lock All
	Partial Lock

Application Circuits

DTMF Receiver Single-ended Input Application Circuits



Instruction Set

Introduction

Central to the successful operation of any microcontroller is its instruction set, which is a set of program instruction codes that directs the microcontroller to perform certain operations. In the case of Holtek microcontrollers, a comprehensive and flexible set of over 60 instructions is provided to enable programmers to implement their application with the minimum of programming overheads.

For easier understanding of the various instruction codes, they have been subdivided into several functional groupings.

Instruction Timing

Most instructions are implemented within one instruction cycle. The exceptions to this are branch, call, or table read instructions where two instruction cycles are required. One instruction cycle is equal to 4 system clock cycles, therefore in the case of an 8MHz system oscillator, most instructions would be implemented within 0.5μs and branch or call instructions would be implemented within 1μs. Although instructions which require one more cycle to implement are generally limited to the JMP, CALL, RET, RETI and table read instructions, it is important to realize that any other instructions which involve manipulation of the Program Counter Low register or PCL will also take one more cycle to implement. As instructions which change the contents of the PCL will imply a direct jump to that new address, one more cycle will be required. Examples of such instructions would be ″CLR PCL″ or ″MOV PCL, A″. For the case of skip instructions, it must be noted that if the result of the comparison involves a skip operation then this will also take one more cycle, if no skip is involved then only one cycle is required.

Moving and Transferring Data

The transfer of data within the microcontroller program is one of the most frequently used operations. Making use of three kinds of MOV instructions, data can be transferred from registers to the Accumulator and vice-versa as well as being able to move specific immediate data directly into the Accumulator. One of the most important data transfer applications is to receive data from the input ports and transfer data to the output ports.

Arithmetic Operations

The ability to perform certain arithmetic operations and data manipulation is a necessary feature of most microcontroller applications. Within the Holtek microcontroller instruction set are a range of add and subtract instruction mnemonics to enable the necessary arithmetic to be carried out. Care must be taken to ensure correct handling of carry and borrow data when results exceed 255 for addition and less than 0 for subtraction. The increment and decrement instructions INC, INCA, DEC and DECA provide a simple means of increasing or decreasing by a value of one of the values in the destination specified.

Logical and Rotate Operations

The standard logical operations such as AND, OR, XOR and CPL all have their own instruction within the Holtek microcontroller instruction set. As with the case of most instructions involving data manipulation, data must pass through the Accumulator which may involve additional programming steps. In all logical data operations, the zero flag may be set if the result of the operation is zero. Another form of logical data manipulation comes from the rotate instructions such as RR, RL, RRC and RLC which provide a simple means of rotating one bit right or left. Different rotate instructions exist depending on program requirements. Rotate instructions are useful for serial port programming applications where data can be rotated from an internal register into the Carry bit from where it can be examined and the necessary serial bit set high or low. Another application where rotate data operations are used is to implement multiplication and division calculations.

Branches and Control Transfer

Program branching takes the form of either jumps to specified locations using the JMP instruction or to a subroutine using the CALL instruction. They differ in the sense that in the case of a subroutine call, the program must return to the instruction immediately when the subroutine has been carried out. This is done by placing a return instruction RET in the subroutine which will cause the program to jump back to the address right after the CALL instruction. In the case of a JMP instruction, the program simply jumps to the desired location. There is no requirement to jump back to the original jumping off point as in the case of the CALL instruction. One special and extremely useful set of branch instructions are the conditional branches. Here a decision is first made regarding the condition of a certain data memory or individual bits. Depending upon the conditions, the program will continue with the next instruction or skip over it and jump to the following instruction. These instructions are the key to decision making and branching within the program perhaps determined by the condition of certain input switches or by the condition of internal data bits.

Bit Operations

The ability to provide single bit operations on Data Memory is an extremely flexible feature of all Holtek microcontrollers. This feature is especially useful for output port bit programming where individual bits or port pins can be directly set high or low using either the "SET [m].i" or "CLR [m].i" instructions respectively. The feature removes the need for programmers to first read the 8-bit output port, manipulate the input data to ensure that other bits are not changed and then output the port with the correct new data. This read-modify-write process is taken care of automatically when these bit operation instructions are used.

Table Read Operations

Data storage is normally implemented by using registers. However, when working with large amounts of fixed data, the volume involved often makes it inconvenient to store the fixed data in the Data Memory. To overcome this problem, Holtek microcontrollers allow an area of Program Memory to be setup as a table where data can be directly stored. A set of easy to use instructions provides the means by which this fixed data can be referenced and retrieved from the Program Memory.

Other Operations

In addition to the above functional instructions, a range of other instructions also exist such as the "HALT" instruction for Power-down operations and instructions to control the operation of the Watchdog Timer for reliable program operations under extreme electric or electromagnetic environments. For their relevant operations, refer to the functional related sections.

Instruction Set Summary

The following table depicts a summary of the instruction set categorised according to function and can be consulted as a basic instruction reference using the following listed conventions.

Table conventions:

x: Bits immediate data

m: Data Memory address

A: Accumulator

i: 0~7 number of bits

addr: Program memory address

Mnemonic	Description	Cycles	Flag Affected
Arithmetic			
ADD A,[m]	Add Data Memory to ACC	1	Z, C, AC, OV
ADDM A,[m]	Add ACC to Data Memory	1Note	Z, C, AC, OV
ADD A,x	Add immediate data to ACC	1	Z, C, AC, OV
ADC A,[m]	Add Data Memory to ACC with Carry	1	Z, C, AC, OV
ADCM A,[m]	Add ACC to Data memory with Carry	1Note	Z, C, AC, OV
SUB A,x	Subtract immediate data from the ACC	1	Z, C, AC, OV
SUB A,[m]	Subtract Data Memory from ACC	1	Z, C, AC, OV
SUBM A,[m]	Subtract Data Memory from ACC with result in Data Memory	1Note	Z, C, AC, OV
SBC A,[m]	Subtract Data Memory from ACC with Carry	1	Z, C, AC, OV
SBCM A,[m]	Subtract Data Memory from ACC with Carry, result in Data Memory	1Note	Z, C, AC, OV
DAA [m]	Decimal adjust ACC for Addition with result in Data Memory	1Note	C
Logic Operation			
AND A,[m]	Logical AND Data Memory to ACC	1	Z
OR A,[m]	Logical OR Data Memory to ACC	1	Z
XOR A,[m]	Logical XOR Data Memory to ACC	1	Z
ANDM A,[m]	Logical AND ACC to Data Memory	1Note	Z
ORM A,[m]	Logical OR ACC to Data Memory	1Note	Z
XORM A,[m]	Logical XOR ACC to Data Memory	1Note	Z
AND A,x	Logical AND immediate Data to ACC	1	Z
OR A,x	Logical OR immediate Data to ACC	1	Z
XOR A,x	Logical XOR immediate Data to ACC	1	Z
CPL [m]	Complement Data Memory	1Note	Z
CPLA [m]	Complement Data Memory with result in ACC	1	Z
Increment & Decrement			
INCA [m]	Increment Data Memory with result in ACC	1	Z
INC [m]	Increment Data Memory	1Note	Z
DECA [m]	Decrement Data Memory with result in ACC	1	Z
DEC [m]	Decrement Data Memory	1Note	Z

Mnemonic	Description	Cycles	Flag Affected
Rotate			
RRA [m]	Rotate Data Memory right with result in ACC	1	None
RR [m]	Rotate Data Memory right	1Note	None
RRCA [m]	Rotate Data Memory right through Carry with result in ACC	1	C
RRC [m]	Rotate Data Memory right through Carry	1Note	C
RLA [m]	Rotate Data Memory left with result in ACC	1	None
RL [m]	Rotate Data Memory left	1Note	None
RLCA [m]	Rotate Data Memory left through Carry with result in ACC	1	C
RLC [m]	Rotate Data Memory left through Carry	1Note	C
Data Move			
MOV A,[m]	Move Data Memory to ACC	1	None
MOV [m],A	Move ACC to Data Memory	1Note	None
MOV A,x	Move immediate data to ACC	1	None
Bit Operation			
CLR [m].i	Clear bit of Data Memory	1Note	None
SET [m].i	Set bit of Data Memory	1Note	None
Branch			
JMP addr	Jump unconditionally	2	None
SZ [m]	Skip if Data Memory is zero	1Note	None
SZA [m]	Skip if Data Memory is zero with data movement to ACC	1note	None
SZ [m].i	Skip if bit i of Data Memory is zero	1Note	None
SNZ [m].i	Skip if bit i of Data Memory is not zero	1Note	None
SIZ [m]	Skip if increment Data Memory is zero	1Note	None
SDZ [m]	Skip if decrement Data Memory is zero	1Note	None
SIZA [m]	Skip if increment Data Memory is zero with result in ACC	1Note	None
SDZA [m]	Skip if decrement Data Memory is zero with result in ACC	1Note	None
CALL addr	Subroutine call	2	None
RET	Return from subroutine	2	None
RET A,x	Return from subroutine and load immediate data to ACC	2	None
RETI	Return from interrupt	2	None
Table Read			
TABRDC [m]	Read table (current page) to TBLH and Data Memory	2Note	None
TABRDL [m]	Read table (last page) to TBLH and Data Memory	2Note	None
Miscellaneous			
NOP	No operation	1	None
CLR [m]	Clear Data Memory	1Note	None
SET [m]	Set Data Memory	1Note	None
CLR WDT	Clear Watchdog Timer	1	TO, PDF
CLR WDT1	Pre-clear Watchdog Timer	1	TO, PDF
CLR WDT2	Pre-clear Watchdog Timer	1	TO, PDF
SWAP [m]	Swap nibbles of Data Memory	1Note	None
SWAPA [m]	Swap nibbles of Data Memory with result in ACC	1	None
HALT	Enter power down mode	1	TO, PDF

Note: 1. For skip instructions, if the result of the comparison involves a skip then two cycles are required, if no skip takes place only one cycle is required.
2. Any instruction which changes the contents of the PCL will also require 2 cycles for execution.
3. For the ″CLR WDT1″ and ″CLR WDT2″ instructions the TO and PDF flags may be affected by the execution status. The TO and PDF flags are cleared after both ″CLR WDT1″ and ″CLR WDT2″ instructions are consecutively executed. Otherwise the TO and PDF flags remain unchanged.

Instruction Definition

ADC A,[m]	Add Data Memory to ACC with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + [m] + C
Affected flag(s)	OV, Z, AC, C
ADCM A,[m]	Add ACC to Data Memory with Carry
Description	The contents of the specified Data Memory, Accumulator and the carry flag are added. The result is stored in the specified Data Memory.
Operation	[m] ← ACC + [m] + C
Affected flag(s)	OV, Z, AC, C
ADD A,[m]	Add Data Memory to ACC
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + [m]
Affected flag(s)	OV, Z, AC, C
ADD A,x	Add immediate data to ACC
Description	The contents of the Accumulator and the specified immediate data are added. The result is stored in the Accumulator.
Operation	ACC ← ACC + x
Affected flag(s)	OV, Z, AC, C
ADDM A,[m]	Add ACC to Data Memory
Description	The contents of the specified Data Memory and the Accumulator are added. The result is stored in the specified Data Memory.
Operation	[m] ← ACC + [m]
Affected flag(s)	OV, Z, AC, C
AND A,[m]	Logical AND Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″AND″ [m]
Affected flag(s)	Z
AND A,x	Logical AND immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical AND operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″AND″ x
Affected flag(s)	Z
ANDM A,[m]	Logical AND ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical AND operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″AND″ [m]
Affected flag(s)	Z

CALL addr	Subroutine call
Description	Unconditionally calls a subroutine at the specified address. The Program Counter then increments by 1 to obtain the address of the next instruction which is then pushed onto the stack. The specified address is then loaded and the program continues execution from this new address. As this instruction requires an additional operation, it is a two cycle instruction.
Operation	Stack ← Program Counter + 1 Program Counter ← addr
Affected flag(s)	None
CLR [m]	Clear Data Memory
Description	Each bit of the specified Data Memory is cleared to 0.
Operation	[m] ← 00H
Affected flag(s)	None
CLR [m].i	Clear bit of Data Memory
Description	Bit i of the specified Data Memory is cleared to 0.
Operation	[m].i ← 0
Affected flag(s)	None
CLR WDT	Clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF
CLR WDT1	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT2 and must be executed alternately with CLR WDT2 to have effect. Repetitively executing this instruction without alternately executing CLR WDT2 will have no effect.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF
CLR WDT2	Pre-clear Watchdog Timer
Description	The TO, PDF flags and the WDT are all cleared. Note that this instruction works in conjunction with CLR WDT1 and must be executed alternately with CLR WDT1 to have effect. Repetitively executing this instruction without alternately executing CLR WDT1 will have no effect.
Operation	WDT cleared TO ← 0 PDF ← 0
Affected flag(s)	TO, PDF

CPL [m]	Complement Data Memory
Description	Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa.
Operation	[m] ← $\overline{[m]}$
Affected flag(s)	Z
CPLA [m]	Complement Data Memory with result in ACC
Description	Each bit of the specified Data Memory is logically complemented (1′s complement). Bits which previously contained a 1 are changed to 0 and vice versa. The complemented result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC ← $\overline{[m]}$
Affected flag(s)	Z
DAA [m]	Decimal-Adjust ACC for addition with result in Data Memory
Description	Convert the contents of the Accumulator value to a BCD (Binary Coded Decimal) value resulting from the previous addition of two BCD variables. If the low nibble is greater than 9 or if AC flag is set, then a value of 6 will be added to the low nibble. Otherwise the low nibble remains unchanged. If the high nibble is greater than 9 or if the C flag is set, then a value of 6 will be added to the high nibble. Essentially, the decimal conversion is performed by adding 00H, 06H, 60H or 66H depending on the Accumulator and flag conditions. Only the C flag may be affected by this instruction which indicates that if the original BCD sum is greater than 100, it allows multiple precision decimal addition.
Operation	[m] ← ACC + 00H or [m] ← ACC + 06H or [m] ← ACC + 60H or [m] ← ACC + 66H
Affected flag(s)	C
DEC [m]	Decrement Data Memory
Description	Data in the specified Data Memory is decremented by 1.
Operation	[m] ← [m] – 1
Affected flag(s)	Z
DECA [m]	Decrement Data Memory with result in ACC
Description	Data in the specified Data Memory is decremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC ← [m] – 1
Affected flag(s)	Z
HALT	Enter power down mode
Description	This instruction stops the program execution and turns off the system clock. The contents of the Data Memory and registers are retained. The WDT and prescaler are cleared. The power down flag PDF is set and the WDT time-out flag TO is cleared.
Operation	TO ← 0 PDF ← 1
Affected flag(s)	TO, PDF

INC [m]	Increment Data Memory
Description	Data in the specified Data Memory is incremented by 1.
Operation	[m] ← [m] + 1
Affected flag(s)	Z
INCA [m]	Increment Data Memory with result in ACC
Description	Data in the specified Data Memory is incremented by 1. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.
Operation	ACC ← [m] + 1
Affected flag(s)	Z
JMP addr	Jump unconditionally
Description	The contents of the Program Counter are replaced with the specified address. Program execution then continues from this new address. As this requires the insertion of a dummy instruction while the new address is loaded, it is a two cycle instruction.
Operation	Program Counter ← addr
Affected flag(s)	None
MOV A,[m]	Move Data Memory to ACC
Description	The contents of the specified Data Memory are copied to the Accumulator.
Operation	ACC ← [m]
Affected flag(s)	None
MOV A,x	Move immediate data to ACC
Description	The immediate data specified is loaded into the Accumulator.
Operation	ACC ← x
Affected flag(s)	None
MOV [m],A	Move ACC to Data Memory
Description	The contents of the Accumulator are copied to the specified Data Memory.
Operation	[m] ← ACC
Affected flag(s)	None
NOP	No operation
Description	No operation is performed. Execution continues with the next instruction.
Operation	No operation
Affected flag(s)	None
OR A,[m]	Logical OR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″OR″ [m]
Affected flag(s)	Z

OR A,x	Logical OR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical OR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″OR″ x
Affected flag(s)	Z
ORM A,[m]	Logical OR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical OR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″OR″ [m]
Affected flag(s)	Z
RET	Return from subroutine
Description	The Program Counter is restored from the stack. Program execution continues at the restored address.
Operation	Program Counter ← Stack
Affected flag(s)	None
RET A,x	Return from subroutine and load immediate data to ACC
Description	The Program Counter is restored from the stack and the Accumulator loaded with the specified immediate data. Program execution continues at the restored address.
Operation	Program Counter ← Stack ACC ← x
Affected flag(s)	None
RETI	Return from interrupt
Description	The Program Counter is restored from the stack and the interrupts are re-enabled by setting the EMI bit. EMI is the master interrupt global enable bit. If an interrupt was pending when the RETI instruction is executed, the pending Interrupt routine will be processed before returning to the main program.
Operation	Program Counter ← Stack EMI ← 1
Affected flag(s)	None
RL [m]	Rotate Data Memory left
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0.
Operation	[m].(i+1) ← [m].i; (i = 0~6) [m].0 ← [m].7
Affected flag(s)	None
RLA [m]	Rotate Data Memory left with result in ACC
Description	The contents of the specified Data Memory are rotated left by 1 bit with bit 7 rotated into bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.
Operation	ACC.(i+1) ← [m].i; (i = 0~6) ACC.0 ← [m].7
Affected flag(s)	None

RLC [m] Rotate Data Memory left through Carry

Description The contents of the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into bit 0.

Operation
[m].(i+1) ← [m].i; (i = 0~6)
[m].0 ← C
C ← [m].7

Affected flag(s) C

RLCA [m] Rotate Data Memory left through Carry with result in ACC

Description Data in the specified Data Memory and the carry flag are rotated left by 1 bit. Bit 7 replaces the Carry bit and the original carry flag is rotated into the bit 0. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation
ACC.(i+1) ← [m].i; (i = 0~6)
ACC.0 ← C
C ← [m].7

Affected flag(s) C

RR [m] Rotate Data Memory right

Description The contents of the specified Data Memory are rotated right by 1 bit with bit 0 rotated into bit 7.

Operation
[m].i ← [m].(i+1); (i = 0~6)
[m].7 ← [m].0

Affected flag(s) None

RRA [m] Rotate Data Memory right with result in ACC

Description Data in the specified Data Memory and the carry flag are rotated right by 1 bit with bit 0 rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation
ACC.i ← [m].(i+1); (i = 0~6)
ACC.7 ← [m].0

Affected flag(s) None

RRC [m] Rotate Data Memory right through Carry

Description The contents of the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7.

Operation
[m].i ← [m].(i+1); (i = 0~6)
[m].7 ← C
C ← [m].0

Affected flag(s) C

RRCA [m] Rotate Data Memory right through Carry with result in ACC

Description Data in the specified Data Memory and the carry flag are rotated right by 1 bit. Bit 0 replaces the Carry bit and the original carry flag is rotated into bit 7. The rotated result is stored in the Accumulator and the contents of the Data Memory remain unchanged.

Operation
ACC.i ← [m].(i+1); (i = 0~6)
ACC.7 ← C
C ← [m].0

Affected flag(s) C

SBC A,[m] Subtract Data Memory from ACC with Carry

Description The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation $ACC \leftarrow ACC - [m] - \overline{C}$

Affected flag(s) OV, Z, AC, C

SBCM A,[m] Subtract Data Memory from ACC with Carry and result in Data Memory

Description The contents of the specified Data Memory and the complement of the carry flag are subtracted from the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation $[m] \leftarrow ACC - [m] - \overline{C}$

Affected flag(s) OV, Z, AC, C

SDZ [m] Skip if decrement Data Memory is 0

Description The contents of the specified Data Memory are first decremented by 1. If the result is 0 the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation $[m] \leftarrow [m] - 1$
Skip if $[m] = 0$

Affected flag(s) None

SDZA [m] Skip if decrement Data Memory is zero with result in ACC

Description The contents of the specified Data Memory are first decremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.

Operation $ACC \leftarrow [m] - 1$
Skip if $ACC = 0$

Affected flag(s) None

SET [m] Set Data Memory

Description Each bit of the specified Data Memory is set to 1.

Operation $[m] \leftarrow FFH$

Affected flag(s) None

SET [m].i Set bit of Data Memory

Description Bit i of the specified Data Memory is set to 1.

Operation $[m].i \leftarrow 1$

Affected flag(s) None

SIZ [m] Skip if increment Data Memory is 0

Description The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation [m] ← [m] + 1
Skip if [m] = 0

Affected flag(s) None

SIZA [m] Skip if increment Data Memory is zero with result in ACC

Description The contents of the specified Data Memory are first incremented by 1. If the result is 0, the following instruction is skipped. The result is stored in the Accumulator but the specified Data Memory contents remain unchanged. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation ACC ← [m] + 1
Skip if ACC = 0

Affected flag(s) None

SNZ [m].i Skip if bit i of Data Memory is not 0

Description If bit i of the specified Data Memory is not 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is 0 the program proceeds with the following instruction.

Operation Skip if [m].i $\neq$ 0

Affected flag(s) None

SUB A,[m] Subtract Data Memory from ACC

Description The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation ACC ← ACC – [m]

Affected flag(s) OV, Z, AC, C

SUBM A,[m] Subtract Data Memory from ACC with result in Data Memory

Description The specified Data Memory is subtracted from the contents of the Accumulator. The result is stored in the Data Memory. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation [m] ← ACC – [m]

Affected flag(s) OV, Z, AC, C

SUB A,x Subtract immediate data from ACC

Description The immediate data specified by the code is subtracted from the contents of the Accumulator. The result is stored in the Accumulator. Note that if the result of subtraction is negative, the C flag will be cleared to 0, otherwise if the result is positive or zero, the C flag will be set to 1.

Operation ACC ← ACC – x

Affected flag(s) OV, Z, AC, C

SWAP [m] Swap nibbles of Data Memory

Description The low-order and high-order nibbles of the specified Data Memory are interchanged.

Operation [m].3~[m].0 ↔ [m].7 ~ [m].4

Affected flag(s) None

SWAPA [m] Swap nibbles of Data Memory with result in ACC

Description The low-order and high-order nibbles of the specified Data Memory are interchanged. The result is stored in the Accumulator. The contents of the Data Memory remain unchanged.

Operation ACC.3 ~ ACC.0 ← [m].7 ~ [m].4
ACC.7 ~ ACC.4 ← [m].3 ~ [m].0

Affected flag(s) None

SZ [m] Skip if Data Memory is 0

Description If the contents of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation Skip if [m] = 0

Affected flag(s) None

SZA [m] Skip if Data Memory is 0 with data movement to ACC

Description The contents of the specified Data Memory are copied to the Accumulator. If the value is zero, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0 the program proceeds with the following instruction.

Operation ACC ← [m]
Skip if [m] = 0

Affected flag(s) None

SZ [m].i Skip if bit i of Data Memory is 0

Description If bit i of the specified Data Memory is 0, the following instruction is skipped. As this requires the insertion of a dummy instruction while the next instruction is fetched, it is a two cycle instruction. If the result is not 0, the program proceeds with the following instruction.

Operation Skip if [m].i = 0

Affected flag(s) None

TABRDC [m] Read table (current page) to TBLH and Data Memory

Description The low byte of the program code (current page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.

Operation [m] ← program code (low byte)
TBLH ← program code (high byte)

Affected flag(s) None

TABRDL [m] Read table (last page) to TBLH and Data Memory

Description The low byte of the program code (last page) addressed by the table pointer (TBLP) is moved to the specified Data Memory and the high byte moved to TBLH.

Operation [m] ← program code (low byte)
TBLH ← program code (high byte)

Affected flag(s) None

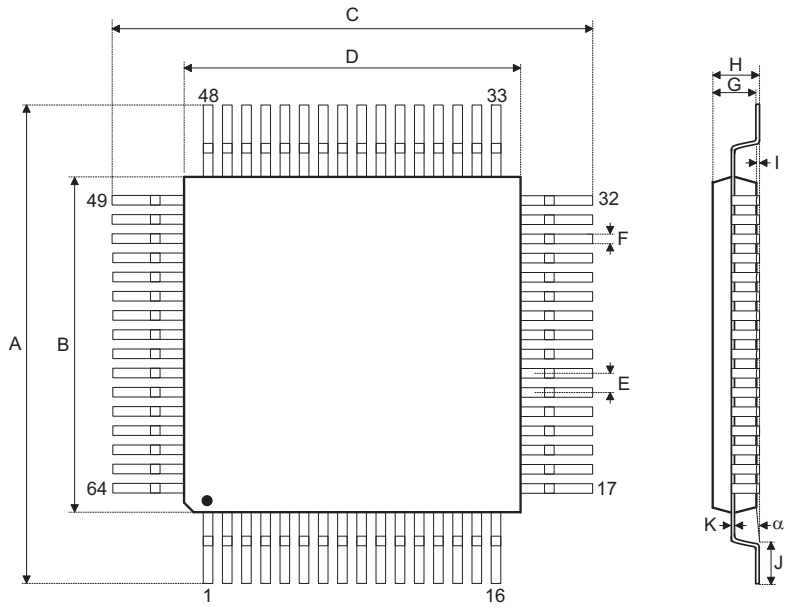
XOR A,[m]	Logical XOR Data Memory to ACC
Description	Data in the Accumulator and the specified Data Memory perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ [m]
Affected flag(s)	Z

XORM A,[m]	Logical XOR ACC to Data Memory
Description	Data in the specified Data Memory and the Accumulator perform a bitwise logical XOR operation. The result is stored in the Data Memory.
Operation	[m] ← ACC ″XOR″ [m]
Affected flag(s)	Z

XOR A,x	Logical XOR immediate data to ACC
Description	Data in the Accumulator and the specified immediate data perform a bitwise logical XOR operation. The result is stored in the Accumulator.
Operation	ACC ← ACC ″XOR″ x
Affected flag(s)	Z

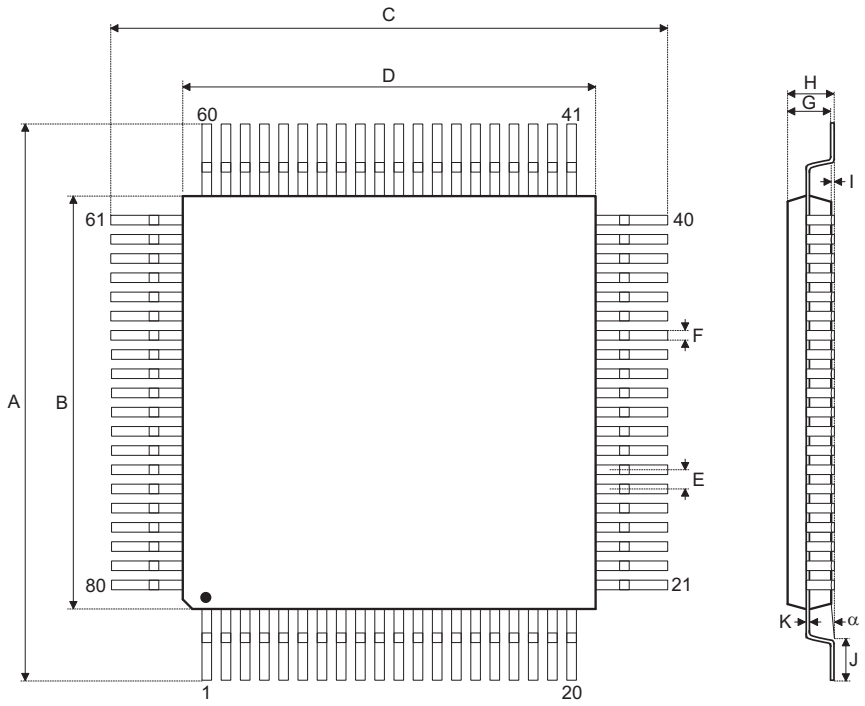
Package Information

64-pin LQFP (7mm×7mm) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	8.90	—	9.10
B	6.90	—	7.10
C	8.90	—	9.10
D	6.90	—	7.10
E	—	0.40	—
F	0.13	—	0.23
G	1.35	—	1.45
H	—	—	1.60
I	0.05	—	0.15
J	0.45	—	0.75
K	0.09	—	0.20
α	0°	—	7°

80-pin LQFP (10mm×10mm) Outline Dimensions



Symbol	Dimensions in mm		
	Min.	Nom.	Max.
A	11.90	—	12.10
B	9.90	—	10.10
C	11.90	—	12.10
D	9.90	—	10.10
E	—	0.40	—
F	—	0.16	—
G	1.35	—	1.45
H	—	—	1.60
I	—	0.10	—
J	0.45	—	0.75
K	0.10	—	0.20
α	0°	—	7°

Holtek Semiconductor Inc. (Headquarters)
No.3, Creation Rd. II, Science Park, Hsinchu, Taiwan
Tel: 886-3-563-1999
Fax: 886-3-563-1189
http://www.holtek.com.tw

Holtek Semiconductor Inc. (Taipei Sales Office)
4F-2, No. 3-2, YuanQu St., Nankang Software Park, Taipei 115, Taiwan
Tel: 886-2-2655-7070
Fax: 886-2-2655-7373
Fax: 886-2-2655-7383 (International sales hotline)

Holtek Semiconductor Inc. (Shenzhen Sales Office)
5F, Unit A, Productivity Building, No.5 Gaoxin M 2nd Road, Nanshan District, Shenzhen, China 518057
Tel: 86-755-8616-9908, 86-755-8616-9308
Fax: 86-755-8616-9722

Holtek Semiconductor (USA), Inc. (North America Sales Office)
46729 Fremont Blvd., Fremont, CA 94538
Tel: 1-510-252-9880
Fax: 1-510-252-9885
http://www.holtek.com