Digital

Memory

Peripherals

Gate Arrays

DIGITAL

ROMs

Organization	Max Access Time (ns)	I_{DD} Max(mA)	No. Pins	Package*	Temp Range*
4096 x 8 IM7332	300	80	24	J,P	C
8192 x 8 IM7364	350	150	24	J,P	C

EPROMs

Organization	Max Access Time (ns)	V_{CC} (V)	I_{CC} Max (mA) Operating	I_{CC} Max (μA) Standby	No. Pins	Package*	Temp Range
1024 x 4							
IM6653	550	5	6	140	24	J	I,M
IM6653A	300	10	12	140	24	J	I,M
512 x 8							
IM6654	550	5	6	140	24	J	I,M
IM6654A	300	10	12	140	24	J	I,M

PERIPHERAL

IM8048 Peripheral

IM82C43 — CMOS I/O Exponder

*Package and Temperature Key

F—Flatpack
J—Ceramic Dual In-Line
P—Plastic Dual In-Line
D–Ceramic Side Brazed (Not Recommended for High Volume)

C—Commercial, 0°C to +70°C
I—Industrial, -40°C to +85°C
M—Military, -55°C to +125°C

UARTS

Part Number	Max. Clock Frequency	XTAL Frequency	V Supply	I_{CC} Max.
IM6402	1.0 MHz	—	5.0	1.2 mA
IM6402A	4.0 MHz	—	4-11	9.0 mA
IM6402-1	2.0 MHz	—	5.0	1.9 mA
IM6403	2.46 MHz	2.46 MHz	5.0	3.7 mA
IM6403A	6.0 MHz	6.0 MHz	4-11	13.0 mA
IM6403-1	3.58 MHz	3.58 MHz	5.0	5.5 mA

GATE ARRAYS

Part Number	Delay	Input Nand Gate Equivalent	I/O Cells	V_{CC}
IGC10408	6 ns	408	34	3-9V
IGC10756	6 ns	756	44	3-9V
IGC11500	6 ns	1500	62	3-9V
IGC12001	6 ns	2001	70	3-9V

IM6402/IM6403 Universal Asynchronous Receiver Transmitter (UART)

FEATURES

- Low Power — Less Than 10mW Typ. at 2MHz
- Operation Up to 4MHz Clock (IM6402A)
- Programmable Word Length, Stop Bits and Parity
- Automatic Data Formatting and Status Generation
- Compatible with Industry Standard UART's (IM6402)
- On-Chip Oscillator with External Crystal (IM6403)
- Operating Voltage —
  IM6402-1/03-1: 5V
  IM6402A/03A: 4-11V
  IM6402/03: 5V

GENERAL DESCRIPTION

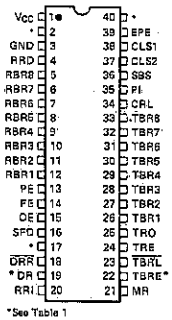
The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even, and parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 6.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits clock frequencies up to 4.0MHz (250K Baud), an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

The IM6402 differs from the IM6403 in the use of five device pins as indicated in Table 1 and Figure 1.

PIN CONFIGURATION (outline dwg DL, PL)



*See Table 1

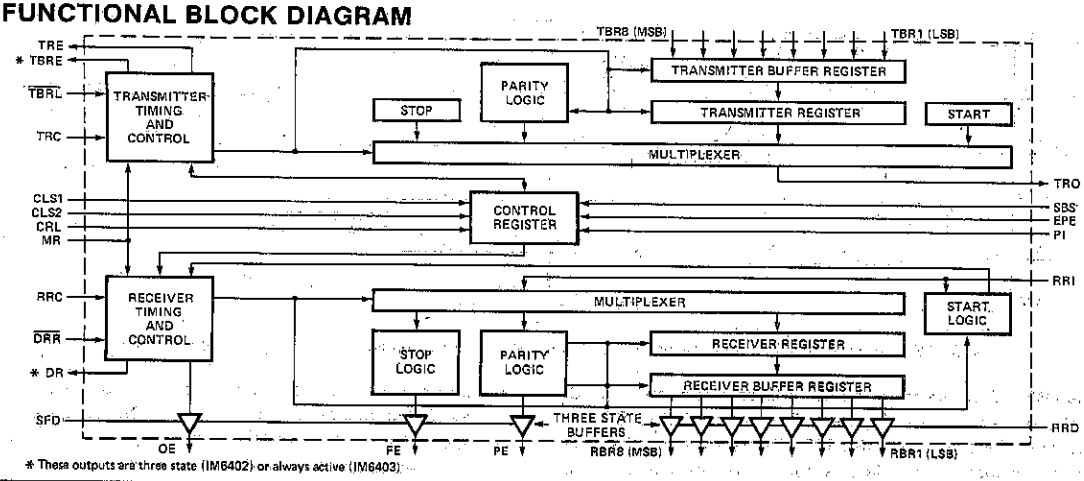
TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT CLOCK
2	N/C	Divide Control.	Divide Control
17	RRC	XTAL	External Clock Input
19	Tri-State	Always Active	Always Active
22	Tri-State	Always Active	Always Active
40	TRC	XTAL	GND

ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-1IPL	IM6402/03-AIPL	IM6402/03-IPL
CERAMIC PKG	IM6402-1/03-1IDL	IM6402/03-AIDL	IM6402/03IDL
MILITARY TEMP.	IM6402-1/03-1MDL	IM6402/03-AMDL	—
MILITARY TEMP. WITH 883B	IM6402-1/03-1 MDL/883B	IM6402/03-AMDL/ 883B	—

FUNCTIONAL BLOCK DIAGRAM



* These outputs are three state (IM6402) or always active (IM6403)

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
IM6402/03 ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0 \pm 10\%$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \leq V_{IN} \leq V_{CC}$	-5.0		5.0	µA
4	V_{OH}	Output Voltage High	$I_{OH} = -0.2mA$	2.4			V
5	V_{OL}	Output Voltage Low	$I_{OL} = 1.6mA$			0.45	V
6	I_{OLK}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-5.0		5.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	800	µA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_c = 500 KHz			1.2	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal}$ = 2.46MHz			3.7	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: $V_{CC} = 5V$, $T_A = 25°C$.

A.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = 5.0V \pm 10\%$, $C_L = 50pF$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	f_c	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.		1.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403				2.46	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		225	50		ns
4	t_{mr}	Pulse Width MR		600	200		ns
5	t_{ds}	Input Data Setup Time		75	20		ns
6	t_{dh}	Input Data Hold Time		90	40		ns
7	t_{en}	Output Enable Time			80	190	ns

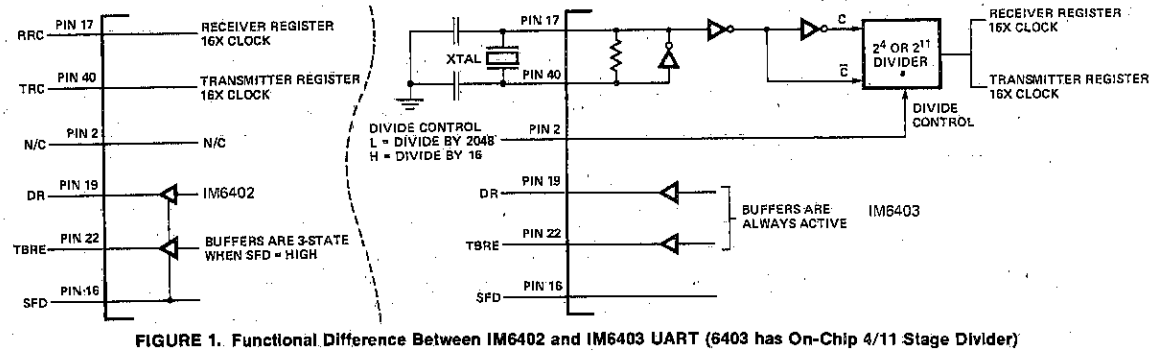


FIGURE 1. Functional Difference Between IM6402 and IM6403 UART (6403 has On-Chip 4/11 Stage Divider)

The IM6403 differs from the IM6402 on three inputs (RRC, TRC, pin 2) as shown in Figure 1. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 10). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402AI/03AI ..... -40°C to +85°C
- Military IM6402AM/03AM ..... -55°C to +125°C

Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4.0V to 11.0V, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	i_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		5.0	500	μA
8	I_{CC}	Power Supply Current IM6402A Dynamic	f_c=4MHz			9.0	mA
9	I_{CC}	Power Supply Current IM6403A Dynamic	$f_{crystal}$ = 3.58MHz			13.0	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10.0V ± 5%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_c	Clock Frequency IM6402A	See Timing Diagrams (Figures 2,3,4)	D.C.		4.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403A				6.0	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		100	40		ns
4	t_{mr}	Pulse Width MR		400	200		ns
5	t_{ds}	Input Data Setup Time		40	0		ns
6	t_{dh}	Input Data Hold Time		30	30		ns
7	t_{en}	Output Enable Time			40	70	ns

TIMING DIAGRAMS

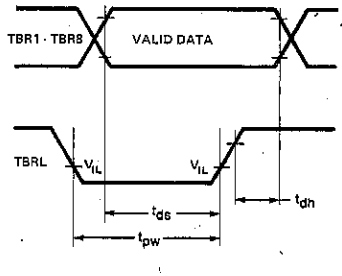


FIGURE 2. Data Input Cycle

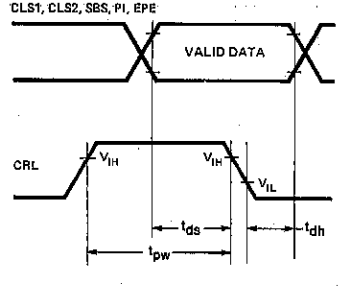


FIGURE 3. Control Register Load Cycle

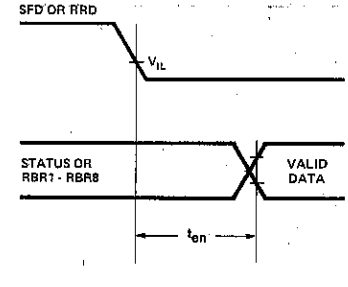


FIGURE 4. Status Flag Enable Time or Data Output Enable Time

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402-1I/03-1I ..... -40°C to +85°C
- Military IM6402-1M/03-1M ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

2

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0 ± 10%, T_A = Industrial or Military

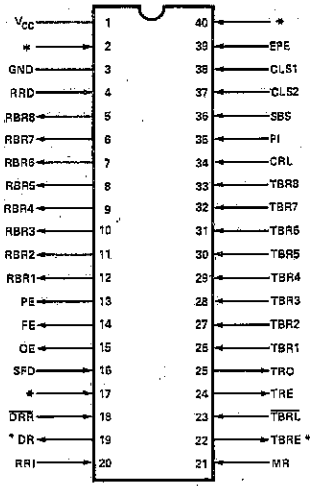
	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	µA
4	V_{OH}	Output Voltage High	I_{OH}=-0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OLK}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	µA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	100	µA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_c = 2MHz			1.9	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{crystal}$ = 3.58MHz			5.5	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_c	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.		2.0	MHz
2	$f_{crystal}$	Crystal Frequency IM6403				3.58	MHz
3	t_{pw}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		150	50		ns
4	t_{mr}	Pulse Width MR		400	200		ns
5	t_{ds}	Input Data Setup Time		50	20		ns
6	t_{dh}	Input Data Hold Time		60	40		ns
7	t_{en}	Output Enable Time			80	160	ns



*DIFFERS BETWEEN IM6402 AND IM6403.

FIGURE 5. Pin Configuration

IM6403 FUNCTIONAL PIN DEFINITION

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 (16) Divider Low: 2^{11} (2048) Divider
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if $\overline{DRR}$ has been performed (i.e., $\overline{DRR}$; active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR, *TBRE* to a high impedance state. See Block Diagram and Figure 4. *IM6402 only.
17	IM6402-RRC IM6403-XTAL or EXT CLK IN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 2.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR8	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 3.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL or GND	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

TABLE 2. Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 6) on the TROutput terminal.

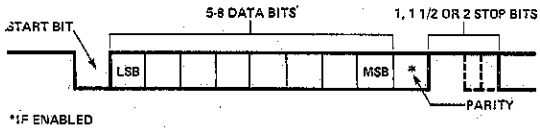


FIGURE 6. Serial Data Format

Transmitter timing is shown in Figure 7. Ⓐ Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{\text{TBRL}}$oad input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of $\overline{\text{TBRL}}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. Ⓑ The rising edge of $\overline{\text{TBRL}}$ clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register, TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRClock, which is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins.

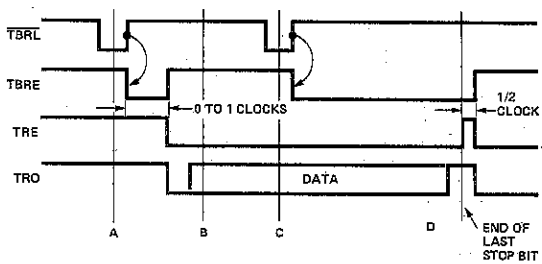


FIGURE 7. Transmitter Timing (Not to Scale)

RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked by the RRClock, which is 16 times the data rate. Receiver timing is shown in Figure 8.

Ⓐ A low level on $\overline{\text{DRR}}$eset clears the DReady line. Ⓑ During the first stop bit, data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates an overrun which occurs when DReady has not been cleared before the present character was transferred to the RBRegister. A logic high on PError indicates a parity error. Ⓒ 1/2 clock cycle later, DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

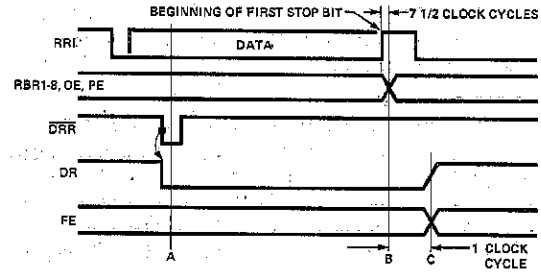


FIGURE 8. Receiver Timing (Not to Scale)

START BIT DETECTION

The receiver uses a 16X clock for timing (see Figure 9.) The start bit Ⓐ could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at the center of the first stop-bit.

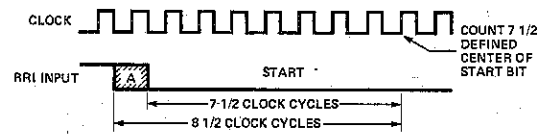


FIGURE 9. Start Bit Timing

TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 10 shows how the IM6403 can be interfaced to an IM6100 microcomputer system with the aid of an IM6101 Programmable Interface Element (PIE). The PIE interprets Input/Output transfer (IOT) instructions from the processor and generates read and write pulses to the UART. The SENSE lines on the PIE are also employed to allow the processor to detect UART status. In particular, the processor must know when the Receive Buffer Register has accumulated a character (DR active), and when the Transmit Buffer Register can accept another character to be transmitted.

In this example the characters to be received or transmitted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs should be committed.

The baud rate at which the transmitter and receiver will operate is determined by the external crystal and DIVIDE CONTROL pin on the IM6403. The internal divider can be set to reduce the crystal frequency by either 16 (PIN 2:HIGH) or 2048 (PIN 2:LOW) times. The frequency out of the internal divider should be 16 times the desired baud rate. To generate 110 baud, this example will use a 3.579545MHz color TV crystal

and DIVIDE CONTROL set low. The IM6402 may use different receive (RRC) and transmit (TRC) clock rates, but requires an external clock generator.

To ensure consistent and correct operation, the IM6402/03 must be reset after power-up. The Master Reset (MR) pin is active high, and can be driven reliably from a Schmitt trigger inverter and R-C delay. In this example, the IM6100 is reset through still another inverter. The Schmitt trigger between the processor and R-C network is needed to assure that a slow rising capacitor voltage does not re-trigger RESET. A long reset pulse after power-up (~100ms) is required by the processor to assure that the on-board crystal oscillator has sufficient time to start.

2

The IM6402 supports the processor's bi-directional data bus quite easily by tying the TBR and RBR buses together. A read command from the processor will enable the RECEIVER BUFFER REGISTER onto the bus by using the RECEIVER REGISTER DISABLE (RRD) pin. A write command from the processor clocks data from the bus into the TRANSMITTER BUFFER REGISTER using $\overline{TBRL}$. Figure 10 shows a NAND gate driving $\overline{TBRL}$ from the $\overline{WRITE_2}$ pin on the PIE. This gate is used to generate a rising edge to $\overline{TBRL}$ at the point where data is stable on the bus, and to hold $\overline{TBRL}$ high until the UART actually transfers the data to it's internal buffer. If $\overline{TBRL}$ were allowed to return low before TBRE went high, the intended output data would be overwritten, since the TBR is a transparent latch.

Although not shown in this example, the error flags (PE, FE, OE) could be read by the processor, using the other READ line from the PIE. Since an IM6403 is used, TBRE and DR are not affected by the STATUS FLAGS DISABLE pin; thus, the three error flags can be tied to the data bus and gated by connecting SFD to $\overline{READ_2}$.

If parity is not inhibited, a parity error will cause the PE pin to go high until the next valid character is received.

A framing error is generated when an expected stop bit is not received. FE will stay high after the error until the next complete character's stop bit is received.

The overrun error flag is set if a received character is transferred to the RECEIVER BUFFER REGISTER when the previous character has not been read. The OE pin will stay high until the next received stop bit after a $\overline{DRR}$ is performed.

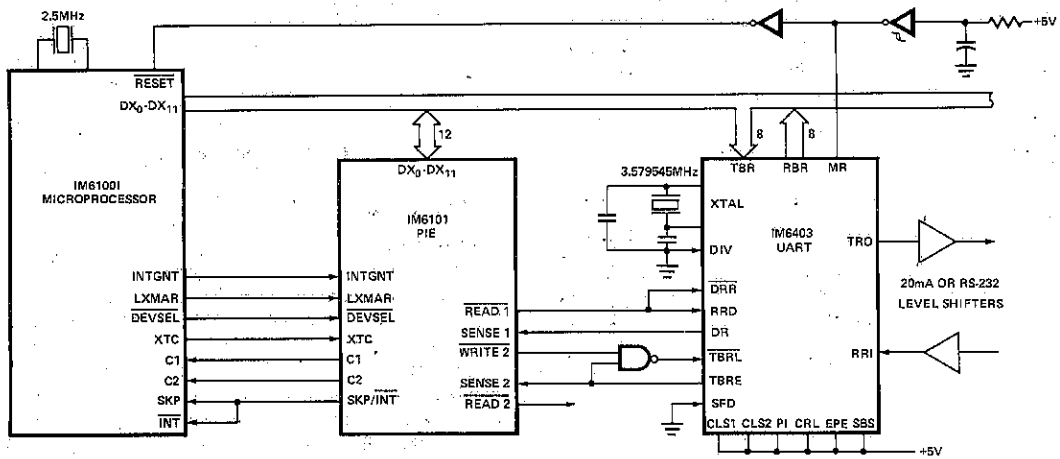


FIGURE 10. 110 Baud Serial Interface for IM6100 System

IM6653/IM6654
4096 Bit CMOS
UV Erasable PROM

FEATURES

- **Organization — IM6653: 1024 x 4**
  IM6654: 512 x 8
- **Low Power — 770μW Maximum Standby**
- **High Speed**
  — 300ns 10V Access Time for IM6653/54 AI
  — 450ns 5V Access Time for IM6653/54-1I
- **Single +5V supply operation**
- **UV erasable**
- **Synchronous operation for low power dissipation**
- **Three-state outputs and chip select for easy system expansion**
- **Full −55°C to +125°C MIL range devices— IM6653/54 M, IM6653A/64A M**

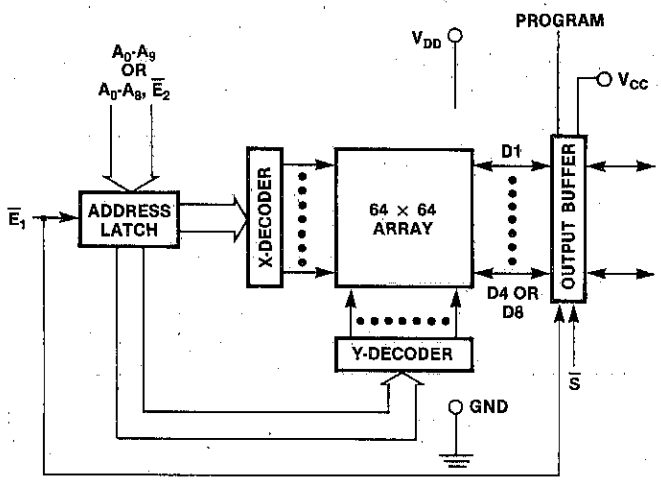
GENERAL DESCRIPTION

The Intersil IM6653 and IM6654 are fully decoded 4096 bit CMOS electrically programmable ROMs (EPROMs) fabricated with Intersil's advanced CMOS processing technology. In all static states these devices exhibit the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL compatible and allow for direct interface with common system bus structures. On-chip address registers and chip select functions simplify system interfacing requirements.

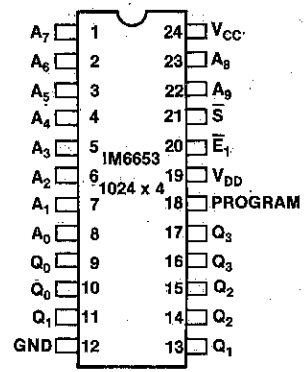
The IM6653 and IM6654 are specifically designed for program development applications where rapid turn-around for program changes is required. The devices may be erased by exposing their transparent lids to ultra-violet light, and then re-programmed.

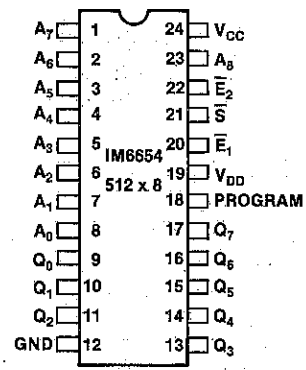
2

BLOCK DIAGRAM



PIN CONFIGURATION
(outline dwg JG/W)





ORDERING INFORMATION

24 PIN PACKAGE		SELECTION/TEMPERATURE RANGE				
		INDUSTRIAL			MILITARY	
		STD 5V	HI SPEED 5V	STD 10V	STD 5V	STD 10V
CERDIP (FRIT SEAL)	JG	IJG	-1I JG	AIJG	MJG	AMJG

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{DD} ..... +8.0V
- $V_{CC} = V_{DD}$ ..... +8.0V

Input or Output Voltage Supplied ..... GND – 0.3V to V_{DD} + 0.3V
Storage Temperature Range ..... – 65°C to + 150°C
Operating Range
- Temperature
  - Industrial ..... – 40°C to + 85°C
  - Military ..... – 55°C to + 125°C
- Voltage
  - 6653/54 I, – 1I ..... 4.5 – 5.5
  - 6653/54 M ..... 4.5 – 5.5

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 10\%$, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6653/54I, -1I,M		UNITS
			MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E}_1, \overline{S}$	$V_{DD} - 2.0$		V
	V_{IH}	Address Pins	2.7		
Logical "0" Input Voltage	V_{IL}			0.8	
Input Leakage	I_I	$GND \leq V_{IN} \leq V_{DD}$	– 1.0	1.0	µA
Logical "1" Output Voltage	V_{OH2}	$I_{OUT} = 0$	$V_{CC} - 0.01$		V
Logical "1" Output Voltage	V_{OH1}	$I_{OH} = -0.2mA$	2.4		
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$		GND + 0.01	
Logical "0" Output Voltage	V_{OL1}	$I_{OL} = 2.0mA$		0.45	
Output Leakage	I_{OLK}	$GND \leq V_O \leq V_{CC}$	– 1.0	1.0	µA
Standby Supply Current	I_{DDSB}	$V_{IN} = V_{DD}$		100	
	I_{CC}	$V_{IN} = V_{DD}$		40	
Operating Supply Current	I_{DDOP}	f = 1 MHz		6	mA
Input Capacitance	C_I	Note 1		7.0	pF
Output Capacitance	C_O	Note 1		10.0	

Note 1: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 10\%$, $C_L = 50pf$, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6653/54-1I		IM6653/54 I		IIM6653/54 M		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		450		550		600	ns
Output Enable Time	TSLQV		110		140		150	
Output Disable Time	TE_1HQZ		110		140		150	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	130		150		150		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	450		550		600		
Address Setup Time	$TAVE_1L$	0		0		0		
Address Hold Time	TE_1LAX	80		100		100		
Chip Enable Setup Time (6654)	TE_2VE_1L	0		0		0		
Chip Enable Hold Time (6654)	TE_1LE_2X	80		100		100		

ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{DD} ..... +11.0V
- $V_{CC} = V_{DD}$ ..... +11.0V

Input or Output Voltage Supplied ..... GND – 0.3V to V_{DD} + 0.3V
Storage Temperature Range ..... – 65°C to + 150°C
Operating Range
- Temperature
  - Industrial ..... – 40°C to + 85°C
  - Military ..... – 55°C to + 125°C
- Voltage
  - 6653/54 AI, AM ..... 4.5 to 10.5V

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 4.5V$ to 10.5V, T_A = Operational Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6653/54AI, AM		UNITS
			MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E}_1, S$	$V_{DD} - 2.0$		V
	V_{IH}	Address Pins	$V_{DD} - 2.0$		
Logical "0" Input Voltage	V_{IL}			0.8	
Input Leakage	I_I	$GND \le V_{IN} \le V_{DD}$	-1.0	1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	$V_{CC} - 0.01$		V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$		GND + 0.01	
Output Leakage	I_{OLK}	$GND \le V_O \le V_{CC}$	– 1.0	1.0	μA
Standby Supply Current	I_{DDSB}	$V_{IN} = V_{DD}$		100	
	I_{CC}	$V_{IN} = V_{DD}$		40	
Operating Supply Current	I_{DDOP}	f = 1 MHz		12	mA
Input Capacitance	C_I	Note 1		7.0	pF
Output Capacitance	C_O	Note 1		10.0	

Note 1: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 10V \pm 5\%$, $C_L = 50pf$, T_A = Operating Temperature Range

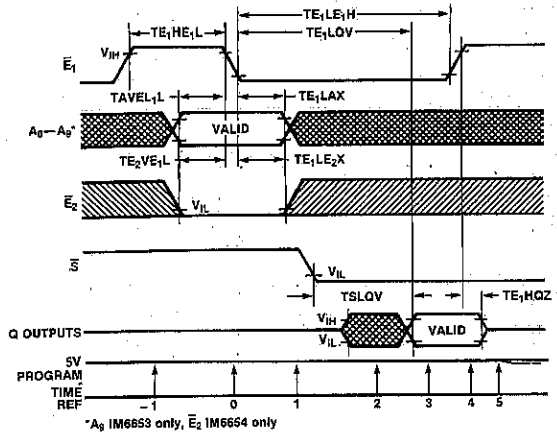
PARAMETER	SYMBOL	IM6653/54 AI		IM6653/54 AM		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\overline{E}_1$	TE_1LQV		300		350	ns
Output Enable Time	TSLQV		60		70	
Output Disable Time	TE_1HQZ		60		70	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	125		125		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	300		350		
Address Setup Time	$TAVE_1L$	0		0		
Address Hold Time	TE_1LAX	60		60		
Chip Enable Setup Time (6654)	TE_2VE_1L	0		0		
Chip Enable Hold Time (6654)	TE_1LE_2X	60		60		

PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8,23	A_0-A_7,A_8	—	Address Lines
9-11,13-17	Q_0-Q_7	—	Data Out lines, 6654
	Q_0-Q_3	—	Data Out lines, 6653
12	GND	—	
18	Program	—	Programming pulse input
19	V_{DD}	—	Chip V+ supply, normally tied to V_{CC}
20	$\overline{E}_1$	L	Strobe line, latches both address lines and, for 6654, Chip enable $\overline{E}_2$
21	$\overline{S}$	L	Chip select line, must be low for valid data out
22	A_9	—	Additional address line for 6653
	$\overline{E}_2$	L	Chip enable line, latched by Chip enable $\overline{E}_1$ on 6654
24	V_{CC}	—	Output buffer +V Supply

2

READ CYCLE TIMING



*A_9 IM6653 only, $\overline{E}_2$ IM6654 only

READ MODE OPERATION

In a typical READ operation address lines and chip enable $\overline{E}_2$* are latched by the falling edge of chip enable $\overline{E}_1$ (T = 0). Valid data appears at the outputs one access time (TELQV) later, provided level-sensitive chip select line $\overline{S}$ is low (T = 3). Data remains valid until either $\overline{E}_1$ or $\overline{S}$ returns to a high level (T = 4). Outputs are then forced to a high-Z state.

Address lines and $\overline{E}_2$ must be valid one setup time before (TAVEL), and one hold time after (TELAX), the falling edge of $\overline{E}_1$ starting the read cycle. Before becoming valid, Q output lines become active (T = 2). The Q output lines return to a high-Z state one output disable time (TE_1HQZ) after any rising edge on $\overline{E}_1$ or $\overline{S}$.

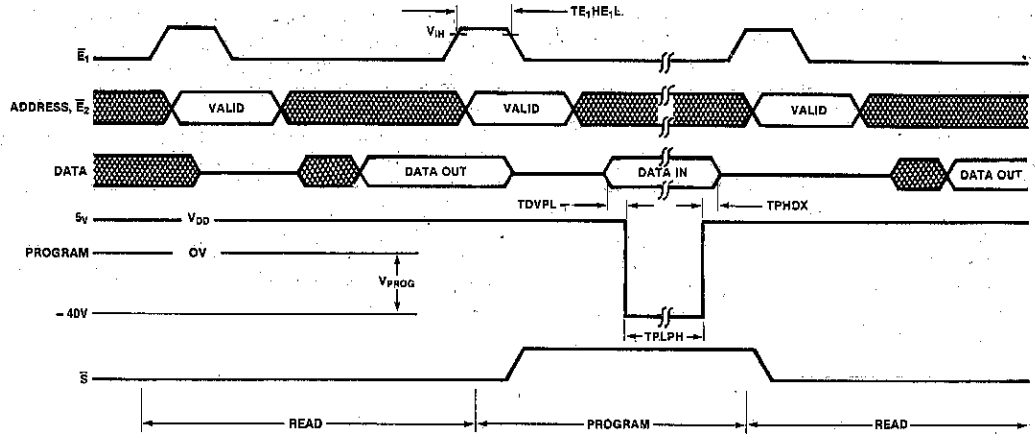
The program line remains high throughout the READ cycle.

Chip enable line $\overline{E}_1$ must remain high one minimum positive pulse width (TEHEL) before the next cycle can begin.

FUNCTION TABLE

TIME	INPUTS				OUTPUTS	NOTES
REF	$\overline{E1}$	$\overline{E2}$*	$\overline{S}$	A	Q	
-1	H	X	X	X	Z	DEVICE INACTIVE
0	↘	L	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E}_2$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF $\overline{E}_1$, $\overline{S}$
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↗	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS -1)

READ AND PROGRAM CYCLES



DC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pin Load Current	I_{PROG}			80	100	mA
Programming Pulse Amplitude	V_{PROG}		38	40	42	V
V_{CC} Current	I_{CC}			0.1	5	mA
V_{DD} Current	I_{DD}			40	100	
Address Input High Voltage	V_{IHA}		$V_{DD} - 2.0$			V
Address Input Low Voltage	V_{ILA}				0.8	
Data Input High Voltage	V_{IH}		$V_{DD} - 2.0$			
Data Input Low Voltage	V_{IL}				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pulse Width	TPLPH	$t_{rise} = t_{fall} = 5\mu s$	18	20	22	ms
Program Pulse Duty Cycle					75%	
Data Setup Time	TDVPL		9			μs
Data Hold Time	TPHDX		9			
Strobe Pulse Width	TE_1HE_1L		150			ns
Address Setup Time	$TAVE_1L$		0			
Address Hold Time	TE_1LE_1X		100			
Access Time	TE_1LQV				1000	

PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode for all EPROMs, V_{CC} and V_{DD} are tied together to a +5V operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at $V_{DD} - 2V$ minimum. Low logic levels must be set at GND + .8V maximum. Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\overline{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\overline{E}_1$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to −40V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. PULSE RISE AND FALL TIMES MUST NOT BE FASTER THAN 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences, such as the Intersil 6920 CMOS EPROM programmer, is recommended.

PROGRAMMING SYSTEM CHARACTERISTICS

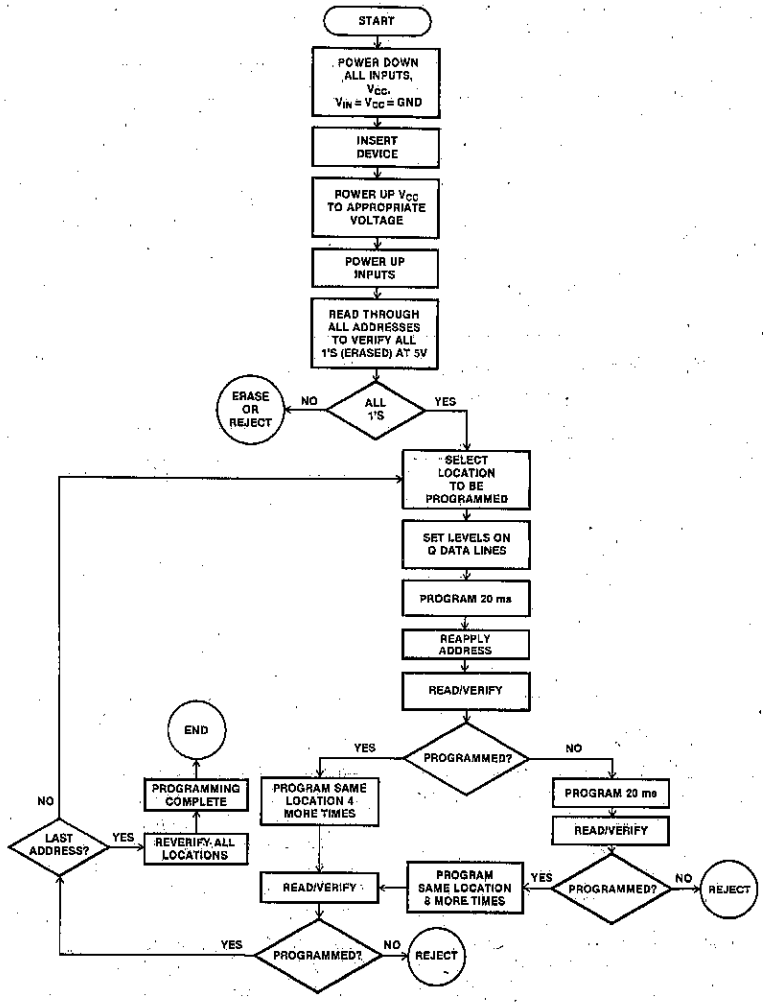
1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{DD} to −40 volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied in the sequence shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins. Both "A" (10V) and non "A" EPROMs are programmed at V_{CC}, V_{DD} of 5V ±5%.
4. Programming is to be done at room temperature.

ERASING PROCEDURE

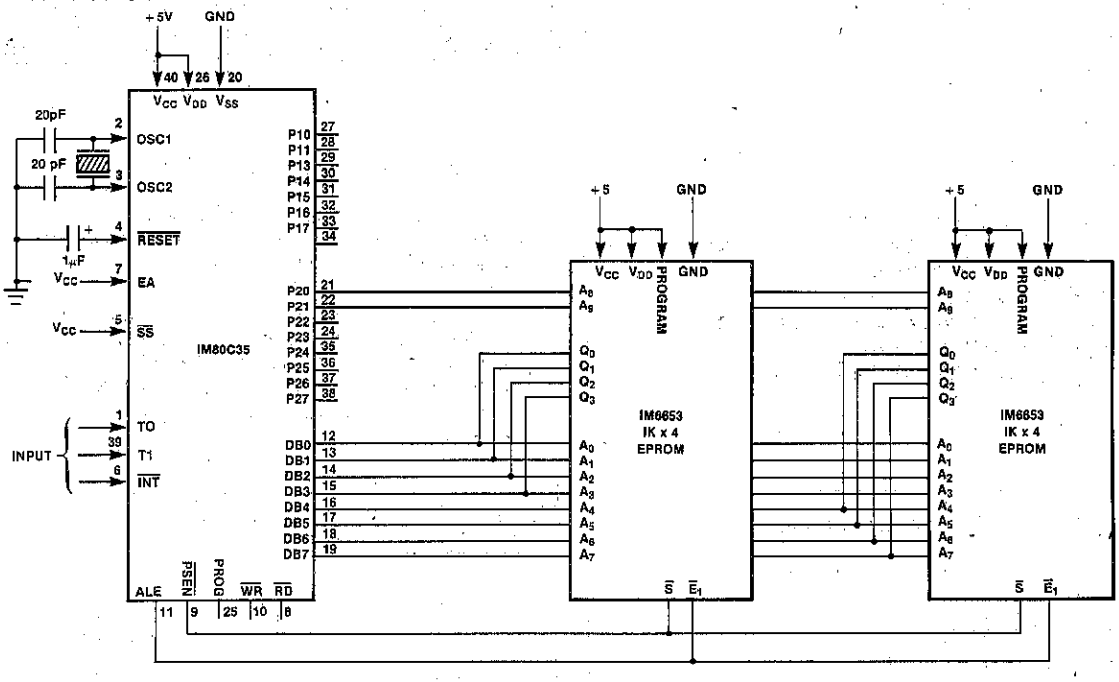
The IM6653/54 are erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537 Å. The recommended integrated dose (i.e.,UV intensity x exposure time) is 10W sec/cm². The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before reprogramming.

The erasing effect of UV light is cummulative. Care should be taken to protect EPROMs from exposure to direct sunlight or florescent lamps radiating UV light in the 2000Å to 4000Å range.

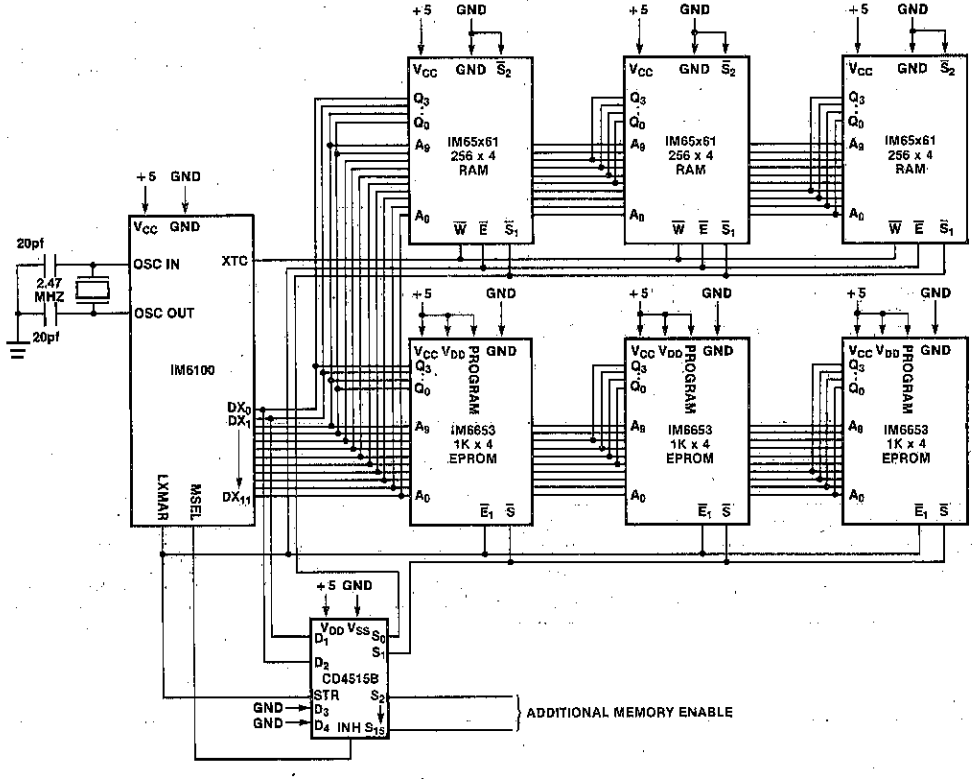
PROGRAMMING FLOW CHART



IM6653 CMOS EPROMS AS EXTERNAL PROGRAM MEMORY WITH THE IM80C35



IM6653 CMOS EPROMS AS PROGRAM MEMORY WITH THE IM6100



IM7332
32,768 BIT
(4096 x 8) HMOS ROM

2

FEATURES

- **High Speed — 300ns Maximum access time**
- **Completely static — no clock required**
- **Single +5V supply**
- **Fully TTL Compatible**
- **Two programmable Chip Selects**
- **Three-state outputs**
- **Industry standard 24 lead pinout**

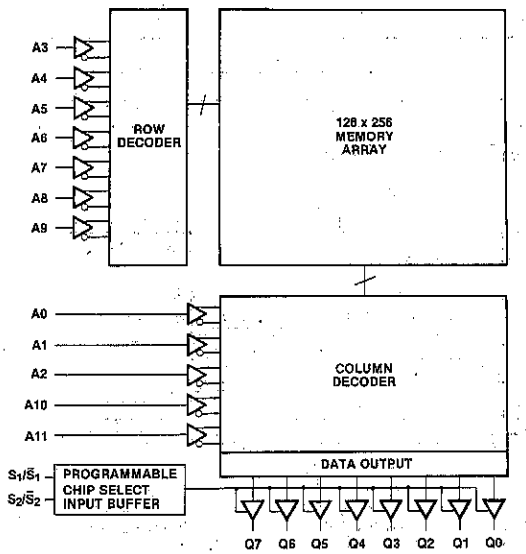
GENERAL DESCRIPTION

The IM7332 is a 32,768 bit read-only memory (ROM) organized 4096 words by 8 bits. The device is fabricated using Intersil's HMOS technology to minimize cell area and optimize circuit performance.

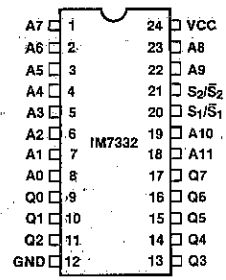
Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. Two chip select inputs which are programmable to either active high or active low, facilitate ease of memory expansion.

The IM7332 operates over 5V ±5% at 75mA with an access time of 300ns.

LOGICAL BLOCK DIAGRAM

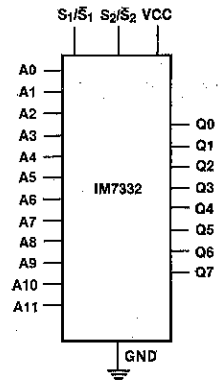


PIN CONFIGURATION



(outline dwgs JG, PG)

LOGIC SYMBOL



ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
IM7332CPG	24 Pin PLASTIC	0°C to +70°C
IM7332 CJG	24 Pin CERDIP	0°C to +70°C

PIN NAMES

$A_0 - A_{11}$	ADDRESS INPUTS
$Q_0 - Q_7$	DATA OUTPUTS
$S_1/\bar{S}_1$, $S_2/\bar{S}_2$	PROGRAMMABLE CHIP SELECTS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Voltage on Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

TEST CONDITIONS: V_{CC} = 5V ± 5%, T_A = 0°C to + 70°C

DESCRIPTION	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−0.5		0.8	V
Input Leakage Current	I_{ILK}	V_{IN} = 0V to 5.25V	−10		10	µA
Output High Voltage	V_{OH}	I_{OUT} = −400µA $S_1/\overline{S}_1 = S_2/\overline{S}_2$ = 2.0V/0.8V	2.4			V
Output Low Voltage	V_{OL}	I_{OUT} = 2.1mA $S_1/\overline{S}_1 = S_2/\overline{S}_2$ = 2.0V/0.8V			0.4	V
Output Leakage Current	I_{OLK}	V_{OUT} = 0V to 5.25V $S_1/\overline{S}_1 = S_2/\overline{S}_2$ = 0.8V/2.0V	−10		10	µA
Operating Supply Current	I_{CC}	T_A = 0°C, Data Out Open V_{IN} = 5.25V, $S_1/\overline{S}_1 = S_2/\overline{S}_2$ = 2.0V/0.8V			75	mA
Input Capacitance	C_{IN}	V_{CC} = 5.0V, V_{IN} = 2.0V			7	pF
Output Capacitance	C_{OUT}	V_{CC} = 5.0V, V_{OUT} = 2.0V			10	pF

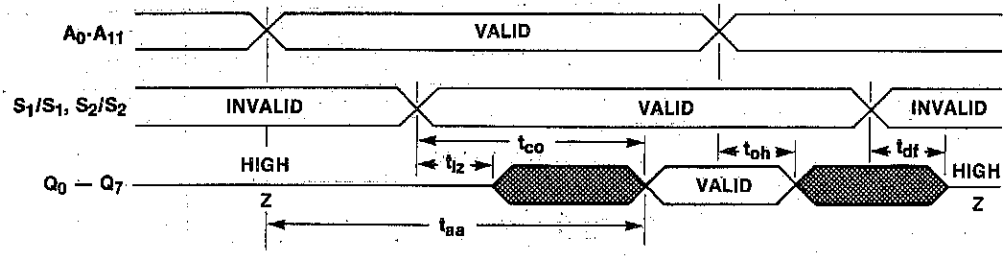
NOTE: 1. Typical values are measured at V_{CC} = 5.0V and T_A = +25°C.
2. Capacitance values are sampled, not 100% tested.

AC CHARACTERISTICS

DESCRIPTION	SYMBOL	JEDEC SYMBOL	MIN	TYP	MAX	UNIT
Address Access Time 7332-45 / 7332	t_{aa}	TAVQV			450 / 300	ns
Chip Select to Low Impedance	t_{lz}	TSVQX	20			ns
Chip Select Delay	t_{co}	TSVQV			100	ns
Chip Deselect Delay	t_{df}	TSXQZ			100	ns
Output Hold Time	t_{oh}	TAXQX	20			ns

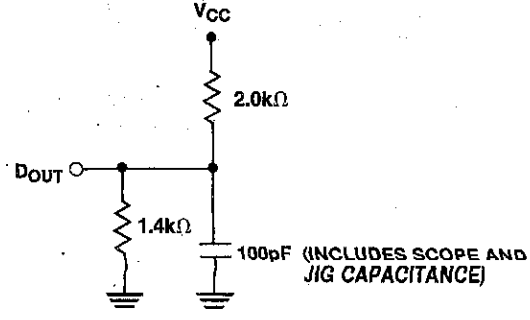
2

READ CYCLE TIMING



AC TEST CONDITIONS

V_{CC} ..... 5V ± 5%
T_A ..... 0°C to 70°C
Input rise and fall times ..... 20ns (10% to 90%)
Input and output reference level 1.5V



OUTPUT LOAD CIRCUIT

IM7364
65,536 BIT
(8192 x 8) HMOS ROM

FEATURES

- **High Speed — 350ns Maximum access time**
- **Completely static — no clock required**
- **Single +5V supply**
- **Fully TTL Compatible**
- **Two Programmable Chip Select**
- **Three-state outputs**
- **Industry standard 24 lead pinout**

GENERAL DESCRIPTION

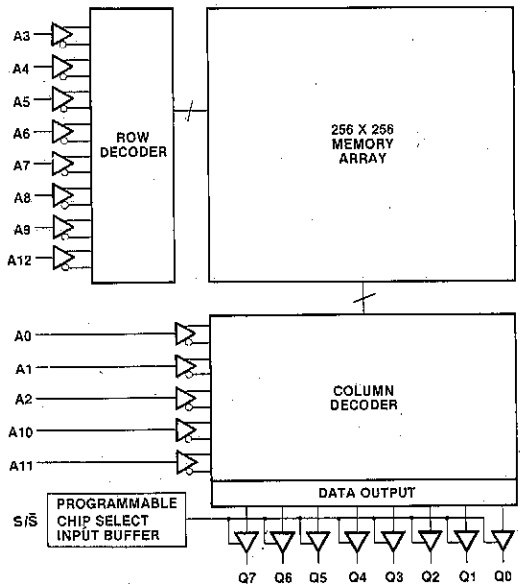
The IM7364 is a 65,536 bit read-only memory (ROM) organized 8192 words by 8 bits. The device is fabricated using Intersil's HMOS technology to minimize cell area and optimize circuit performance.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing to common bus structures. A chip select input, which is programmable to either active high or active low, facilitates ease of memory expansion.

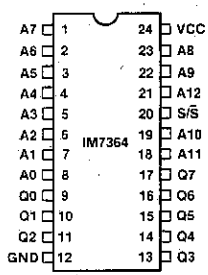
The IM7364 operates over 5V ± 5% at 90mA with an access time of 350ns.

2

LOGICAL BLOCK DIAGRAM

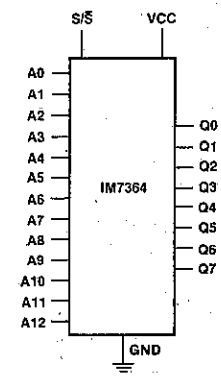


PIN CONFIGURATION



(outline dwgs JG, PG)

LOGIC SYMBOL



ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMP. RANGE
IM7364CPG	24 Pin PLASTIC	0°C to +70°C
IM7364 CJG	24 Pin CERDIP	0°C to +70°C

PIN NAMES

$A_0 - A_{12}$	ADDRESS INPUTS
$Q_0 - Q_7$	DATA OUTPUTS
S/S̄	PROGRAMMABLE CHIP SELECT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Voltage on Any Pin Relative to GND	−0.5V to +7.0V
Commercial Operating Temperature Range	0°C to +70°C
Storage Temperature	−65°C to +150°C
Power Dissipation	1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

2

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 5%, T_A = 0°C to + 70°C

DESCRIPTION	SYMBOL	TEST CONDITIONS	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
Input High Voltage	V_{IH}		2.0		V_{CC}	V
Input Low Voltage	V_{IL}		−0.5		0.8	V
Input Leakage Current	I_{ILK}	V_{IN} = 0V to 5.25V	−10		10	µA
Output High Voltage	V_{OH}	I_{OUT} = −400µA S/$\overline{S}$ = 2.0V/0.8V	2.4			V
Output Low Voltage	V_{OL}	I_{OUT} = 2.1mA S/$\overline{S}$ = 2.0V/0.8V			0.4	V
Output Leakage Current	I_{OLK}	V_{OUT} = 0V to 5.25V S/$\overline{S}$ = 0.8V/2.0V	−10		10	µA
Operating Supply Current	I_{CC}	T_A = 0°C, Data Out Open V_{IN} = 5.25V, S/$\overline{S}$ = 2.0V/0.8V			90	mA
Input Capacitance	C_{IN}	V_{CC} = 5.0V, V_{IN} = 2.0V			7	pF
Output Capacitance	C_{OUT}	V_{CC} = 5.0V, V_{OUT} = 2.0V			10	pF

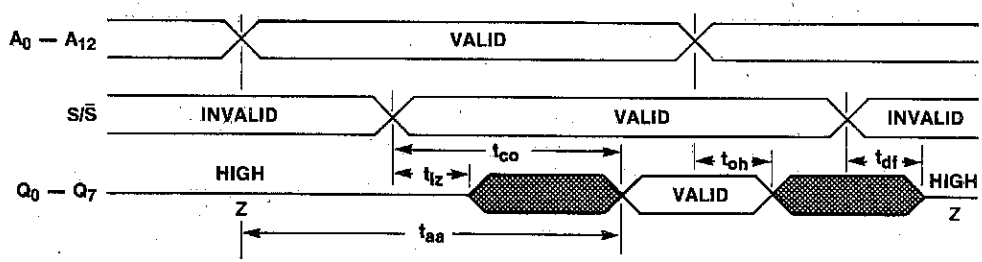
NOTE: 1. Typical values are measured at V_{CC} = 5.0V and T_A = +25°C.
2. Capacitance values are sampled, not 100% tested.

AC CHARACTERISTICS

DESCRIPTION	SYMBOL	JEDEC SYMBOL	MIN	TYP	MAX	UNIT
Address Access Time 7364-45 / 7364	t_{aa}	TAVQV			450 / 350	ns
Chip Select to Low Impedance	t_{lz}	TSVQX	20			
Chip Select Delay	t_{co}	TSVQV			120	
Chip Deselect Delay	t_{df}	TSXQZ			120	
Output Hold Time	t_{oh}	TAXQX	20			

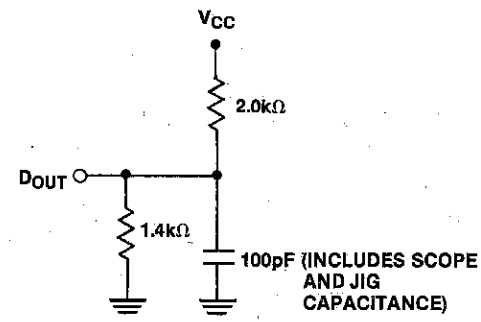
2

READ CYCLE TIMING



AC TEST CONDITIONS

V_{CC} ..... 5V ± 5%
T_A ..... 0°C to 70°C
Input rise and fall times ..... 20ns (10% to 90%)
Input and output reference level 1.5V



OUTPUT LOAD CIRCUIT

INTERSIL

PRELIMINARY

Specifications Subject To Change Without Notice

IM82C43
CMOS Input/Output Expander

2

FEATURES

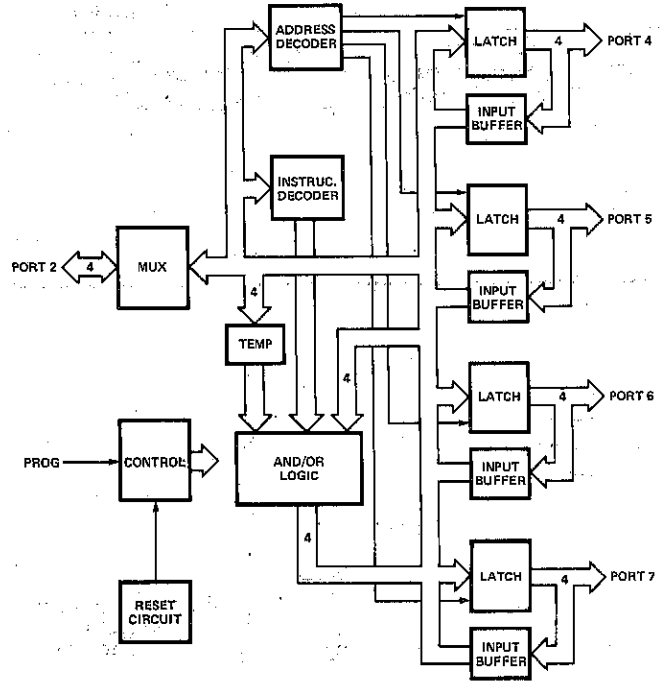
- 8048/41 compatible I/O expander
- CMOS pin-for-pin replacement for standard NMOS 8243
- Low power dissipation — maximum 25mW active
- Four 4-bit I/O ports in 24-pin DIP
- Logical AND/OR directly to ports
- High output drive
- Single +5V supply

DESCRIPTION

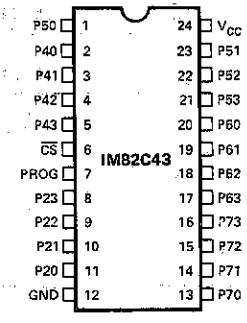
The Intersil IM82C43 is a CMOS input/output expander equivalent to the NMOS 8243. It is designed to provide I/O expansion for the CMOS IM80C48 and NMOS 8048 families of single-chip microcomputers.

The 24-pin IM82C43 provides four 4-bit bidirectional I/O ports: 8048/41 instructions control bidirectional transfers between the 82C43 and the 8048 family microcomputers, and can execute logical AND/OR operations directly on the data contained in the 82C43 ports.

LOGICAL BLOCK DIAGRAM



PIN CONFIGURATION



(outline drawings JG, PG)

ORDERING INFORMATION

PART NO.	PACKAGE
IM82C43CJG	24 PIN CERDIP
IM82C43CPG	24 PIN PLASTIC

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... -65°C to +150°C
Voltage on Any Pin
With Respect to Ground . .Ground -0.5V to Vcc +0.5V
Power Dissipation ..... 1 W

NOTE: Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. AND OPERATING CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Low Voltage	V_{IL}		-0.5		0.8	V
Input High Voltage	V_{IH}	$V_{CC} = 4.5$	2.0		$V_{CC}+0.5$	
		$V_{CC} = 5.5$	2.4		$V_{CC}+0.5$	
Output Low Voltage Ports 4-7	V_{OL}	$I_{OL} = 10mA$			0.4	
		$I_{OL} = 20mA$			0.8	
Output Low Voltage Port 2		$I_{OL} = 1.6mA$			0.4	
Output High Voltage Ports 4-7	V_{OH}	$I_{OH} = 3.2mA$	2.8			
Output Voltage Port 2	V_{OH2}	$I_{OH} = 1.6mA$	2.8			mA
Input Leakage Ports 4-7, Port 2, $\overline{CS}$, PROG	I_{ILK}	$V_{IN} = V_{CC}$ to 0V	-10		10	µA
Supply Current	I_{CC}	WRITE mode, All outputs open, $t_k = 700ns$		1.6	5.0	mA
Standby Current	I_{CCSB}	$V_{IN} = 0$ or V_{CC}, $\overline{CS} = V_{CC}$, All outputs open			100	µA
Sum of all I_{CL} from 16 Outputs	ΣI_{OL}	5 mA each pin average			80	mA

A.C. CHARACTERISTICS $T_A = 0°C$ to $70°C$, $V_{CC} = 5V \pm 10\%$

PARAMETER	SYMBOL	CONDITIONS	MIN.	MAX.	UNITS
Code Valid Before PROG	t_a	80 pF Load	100		ns
Code Valid After PROG	t_b	20 pF Load	60		
Data Valid Before PROG	t_c	80 pF Load	140		
Data Valid After PROG	t_d	20 pF Load	20		
Floating After PROG	t_h	20 pF Load	0	150	
PROG Negative Pulse Width	t_k		700		
$\overline{CS}$ Valid Before/After PROG	t_{cs}		50		
Ports 4-7 Valid After PROG	t_{po}	100 pF Load		700	
Ports 4-7 Valid Before/After PROG	t_{ip}		0		
Port 2 Valid After PROG	t_{acc}	80 pF Load		650	

FUNCTIONAL PIN DESCRIPTION

Designator	Pin Number	Function
PROG	7	**Strobe input.** The falling edge of PROG implies valid address and control information on P20-P23, while the rising edge implies valid data on P20-P23.
$\overline{CS}$	6	**Chip select input.** When HIGH, it disables PROG, thus inhibiting change in output or internal status.
P20-P23	8-11	**Four bit bidirectional port** carrying address and control bits on the falling edge of PROG and I/O data on the rising edge of PROG.
P40-P43 P50-P53 P60-P63 P70-P73	2-5 1,21-23 17-20 13-16	**Four bit bidirectional I/O ports.** May be configured for input, tri-state output (READ mode) or latched output. Data on pins P20-23 may be directly written, ANDed, or ORed with previous data.
GND	12	**Circuit ground potential**
Vcc	24	**+5 volt supply.**

FUNCTIONAL DESCRIPTION

The IM82C43 has four 4-bit I/O ports, which are addressed as Ports 4 thru 7 by the processor. The following operations may be performed on these ports:

- Transfer accumulator to port (write)
- Transfer port to accumulator (read)
- AND accumulator to port
- OR accumulator to port

All communication between the microcomputer and the 82C43 occurs over Port 2 (P20-P23) with timing provided by an output pulse on the PROG pin of the processor. Each data transfer consists of two 4-bit nibbles:

- The first contains the port address and command to the 82C43. This is latched from Port 2 during the high-to-low transition of PROG and is encoded as shown in the table on page 3.
- The second contains the four bits of data associated with the instruction. The low-to-high transition of PROG indicates the presence of data.

Port Address And Command Format

P23	P22	INSTRUCTION CODE	P21	P20	ADDRESS CODE
0	0	Read	0	0	Port 4
0	1	Write	0	1	Port 5
1	0	ORLD	1	0	Port 6
1	1	ANLD	1	1	Port 7

Write Modes

The device has three write modes. MOVD P,A directly writes new data into the selected port with old data being lost; ORLD P,A ORs the new data with the old data and writes it to the port; and ANLD P,A ANDs new data with old data and writes it to the selected port.

After the designated operation is performed, the data is latched and directed to the port. The old data remains latched until the new data is written by the rising edge of PROG.

Read Mode

The device has one read mode. The command and port address are latched from port 2 on the high-to-low transition of the PROG pin. As soon as the read operation and port address are decoded, the designated port output buffers are disabled and the input buffers enabled. The read operation is terminated by the low-to-high transition of the PROG pin. The port selected is switched to the high impedance state while port 2 is returned to the input mode.

Normally a port will be in an output mode (write) or input mode (read). The first read of a port, following a mode change from write to read should be ignored; all following reads are valid. This is to allow the external driver on the port to settle after the first read instruction removes the low impedance drive from the 82C43 output. A read of any port will leave that port in a high impedance state.

I/O Expansion

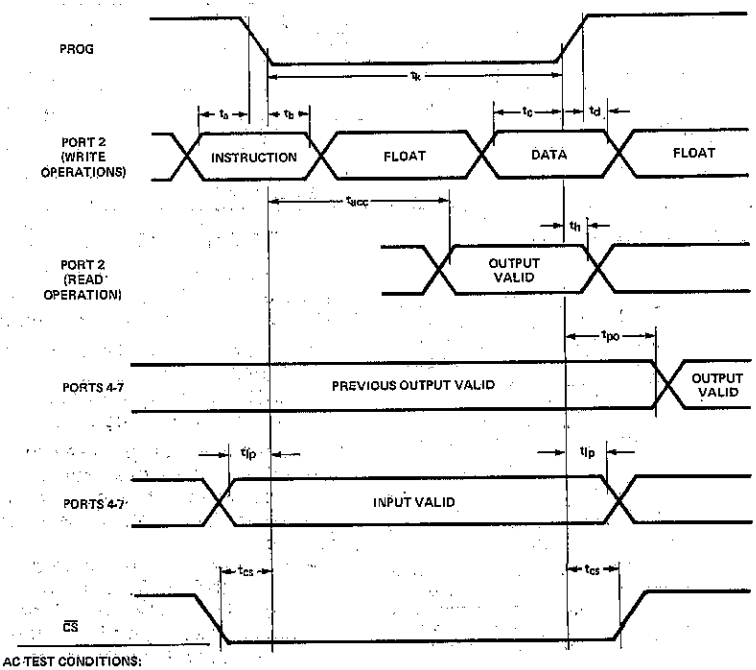
The use of a single 82C43 with an 8048 or 8021 is shown in figure 1. If more ports are required, more 82C43s can be added as shown in figure 2. Here, the upper nibble of port 2 is used to select one of the 82C43s. Two lines could have been decoded but that would require additional hardware. Assuming that the leftmost 82C43 chip select is connected to P24, the instructions to select and de-select would be:

```
MOV A, #0EFH      P24 = 0
OUTL P2, A        Enable 82C43
.
.
.
MOV A, #0FFH      Disable All
OUTL P2, A        Send It
```

Power On Initialization

Initial applicaiton of power to the device forces ports 4, 5, 6, and 7 to the high impedance state. Port 2 will be in an input state if PROG or $\overline{CS}$ are high when power is applied. The first high-to-low transition of PROG causes the device to exit the power-on mode. The power-on sequence is initiated if Vcc drops below one volt.

WAVEFORMS



AC TEST CONDITIONS:
V_{IH} = 2.8V

INPUT RISE AND FALL TIMES: 5ns (10 TO 90%)
INPUT AND OUTPUT TIMING VOLTAGE REFERENCE LEVELS: 0.8V AND 2.0V

TYPICAL APPLICATIONS

EXPANDER INTERFACE

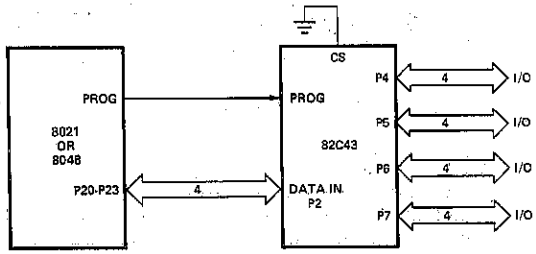
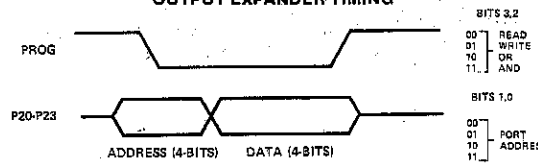


Figure 1

OUTPUT EXPANDER TIMING



Note:
The 82C43 does not have the same quasi-bidirectional port structure as P1/P2 of the 8048. When a "1" is written to P4-7 of the 82C43 it is a "hard 1" (low impedance to +5V) which cannot be pulled low by an external device. All 4 bits of any port can be switched from output mode to input mode by executing a dummy read which leaves the port in a high impedance (no pullup or pulldown) state.

2

USING MULTIPLE 82C43s

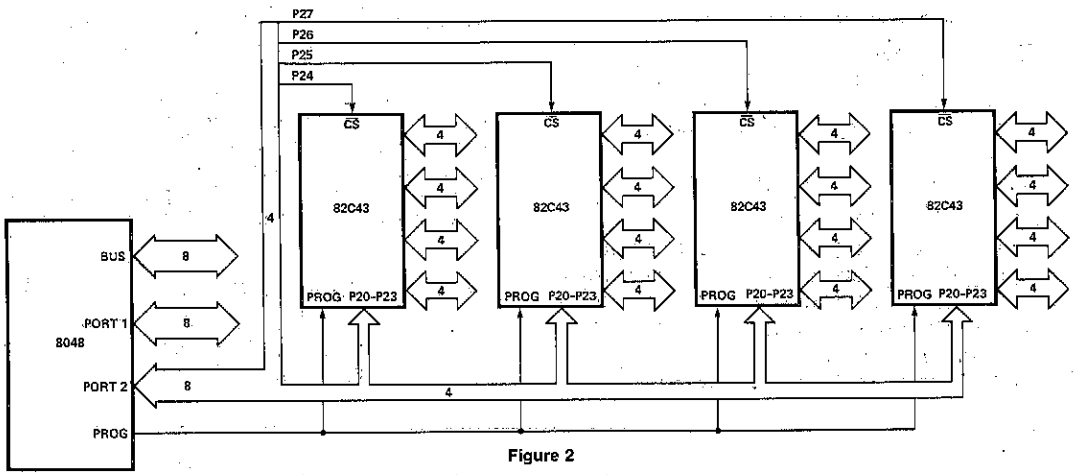


Figure 2

The IGC10000 Series CMOS Gate Arrays

FEATURES

- Complexity from 408 to 1500 Equivalent 2-input Gates
- Mature Silicon Gate CMOS Technology
  - —Low development cost
  - —3.3 to 9V nominal power supply range ±10%
  - —Full CMOS temperature range: −55°C to +125°C
  - —Resistance to latch-up and electrostatic discharge
- Extensive Macro Cell Library
  - —Numerous combinational and sequential macros
  - —Facilitates 7400 and 4000-based designs
  - —TTL or CMOS compatible I/O
  - —Analog capability
- Fully Integrated CAD Software Support
  - —Highly efficient auto-routing capability
  - —Layout fully verified against input logic
  - —Accurate post-layout simulation with calculated RC delays
  - —Automatic test code conversion

GENERAL DESCRIPTION

An IGC10000 Gate Array is a matrix of identical cells, each containing 3 uncommitted N-P transistor pairs. Large numbers of identical arrays are prefabricated and stockpiled. A particular circuit is constructed from a prefabricated array by specifying the interconnections among the transistors within and between cells on the final metal layer. Because all except the final metal layer are prefabricated, the cost advantages of mass production can be realized even for low-volume applications. In addition, prefabrication provides a saving in both design and manufacturing time; in some cases customers can receive prototype chips in as few as 6 weeks after initiation of the project.

In most cases IGC10000 gate arrays are processed with one mask step (a customized metal mask along with a standardized contact mask). For some analog applications or where more routing flexibility is needed, users have the option of programming the contact mask in addition to the metal mask.

THE IGC10000 FAMILY OF GATE ARRAYS

Figure 1 shows a structural representation of an IGC10000 Gate Array. Each rectangle in the body of the matrix represents an array cell; the rectangles

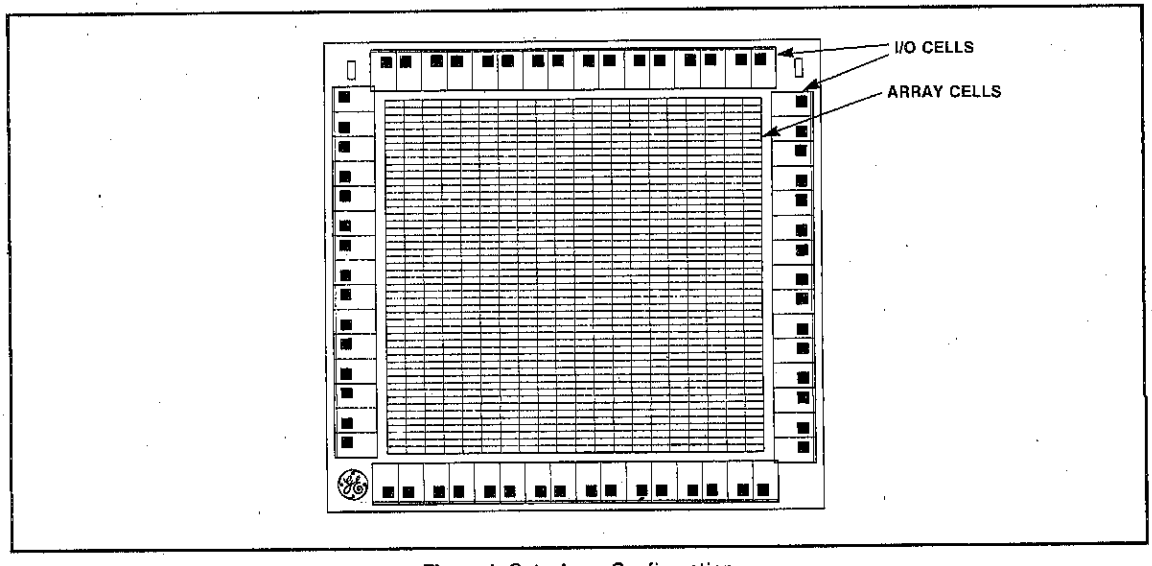


Figure 1. Gate Array Configuration

INTERSIL, INC., 10710 N. TANTAU AVE., CUPERTINO, CA 95014
(408) 996-5000 TWX: 910-338-0171

along each of the four sides of the chip represent I/O cells. Table 1 lists the members of the IGC10000 Gate Array family with their capacities and cell counts.

Table 1. The IGC10000 Gate Array Family

Part No.	Equivalent 2-Input Gates	Number of Array Cells	Bonding Pads and I/O Cells
IGC10408	408	272	34
IGC10756	756	504	44
IGC11500	1500	1000	62

TECHNOLOGY

IGC10000 gate arrays are fabricated using Intersil's high performance selectively oxidized 4-micron silicon gate CMOS process with single-layer metal interconnect. Wafers are processed using state-of-the-art processing technology with these features:

- Positive photoresist
- 1-1 scanning projection lithography
- Polysilicon, nitride and silicon dioxide plasma etching
- Ion implantation for source/drain doping and threshold adjustment
- Sputter metal deposition
- Industry standard oxidation and diffusion techniques
- Nitride and polysilicon Low Pressure Chemical Vapor Deposition (LPCVD)

ARRAY CELLS

An array cell, shown in topographical form in Figure 2, consists of three complementary transistor pairs and five strips of polysilicon (called crossunder strips) for making horizontal interconnections among array cells. Power (V_{DD}) and ground (V_{SS}) buses run vertically as shown. Metal strips (not shown) on top of the crossunder strips make the vertical interconnections within the array. The top and bottom polysilicon strips (called feed-throughs) are used for feeding horizontal connections through the array cell beneath the power and ground buses.

Figure 3 shows the circuit diagram for the array cell. Small hollow circles represent possible connection points; V_{SS} and V_{DD} metal strips are shown as dotted lines.

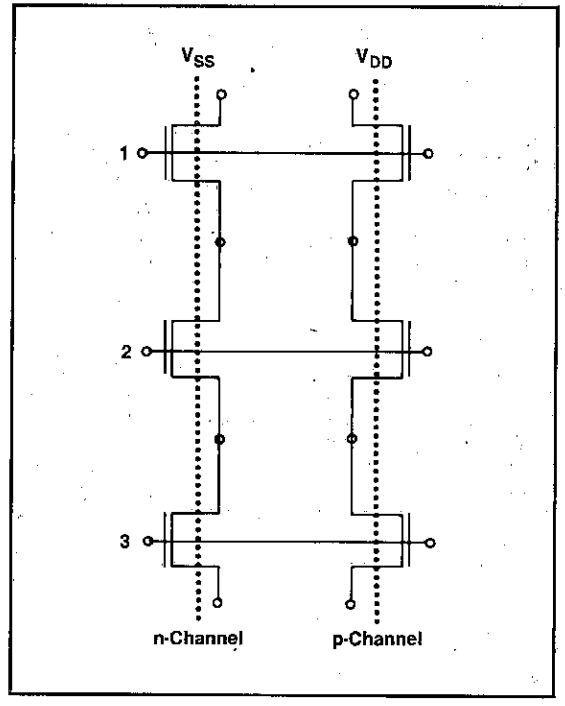


Figure 3. Schematic Diagram of the Array Cell

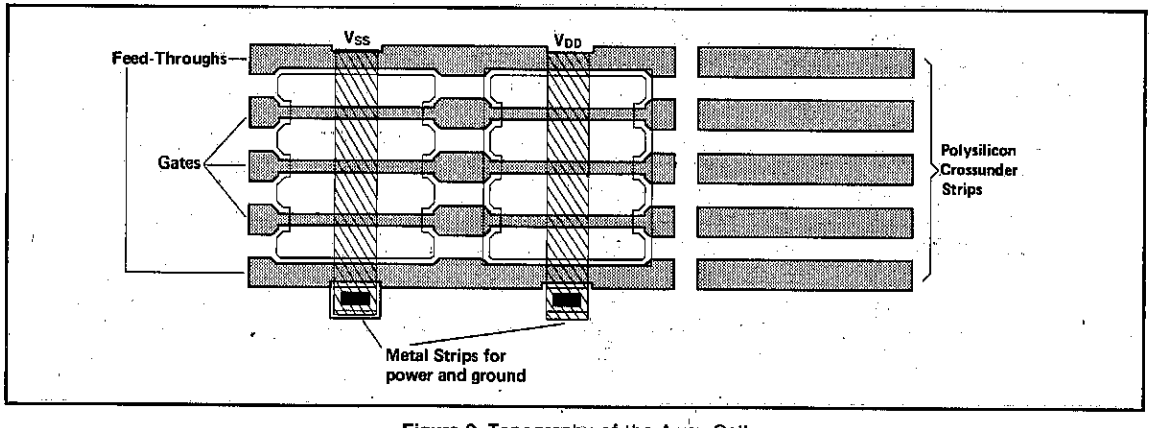


Figure 2. Topography of the Array Cell

I/O CELLS

I/O cells are used to interface the array with external circuitry. Each I/O cell consists of an array of transistors of varying sizes, and allows construction of normal digital I/O interface circuits as well as analog circuitry of simple to moderate complexity.

I/O cells have these features:

- Protection against electrostatic discharge (ESD)
- Logic level translation (CMOS-to-TTL and TTL-to-CMOS)
- Bonding pad for connecting the cell to its corresponding package pin
- Ratioed transistors for analog implementation

The output drive capability of a single output buffer is one TTL load. Applications that require additional drive capability can be handled by using multiple I/O cells in parallel. (In a typical application, not all available I/O cells are needed for external connections; unused cells will thus usually be available to provide added drive capability where needed.)

MACROS

A macro is a physical implementation of a functional block and is realized by interconnections among transistors in one or more array cells. For example, the NOR function is constructed by connecting two p-channel transistors in series to V_{DD} and two n-channel transistors in parallel to V_{SS}, as shown in the topographical and schematic diagrams, Figures 4 and 5.

Designers implement their circuits by selecting and interconnecting the macros in the Macro Library, listed in Table 2.

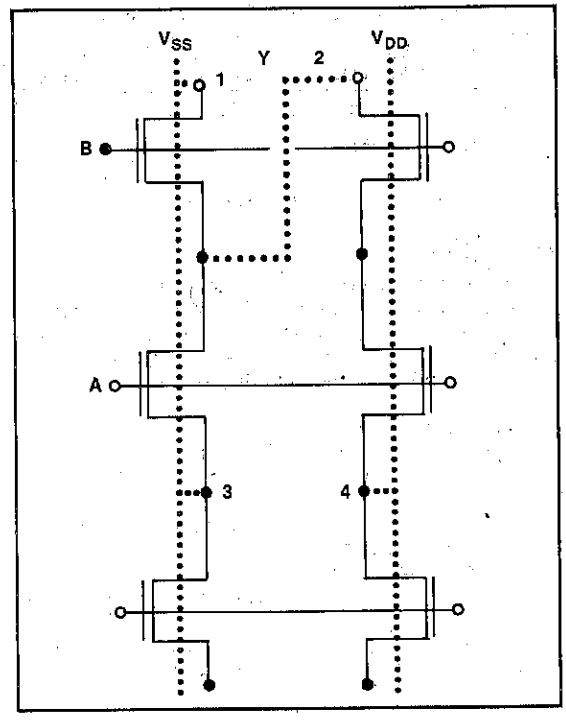


Figure 5. Schematic Diagram for the 2-Input NOR

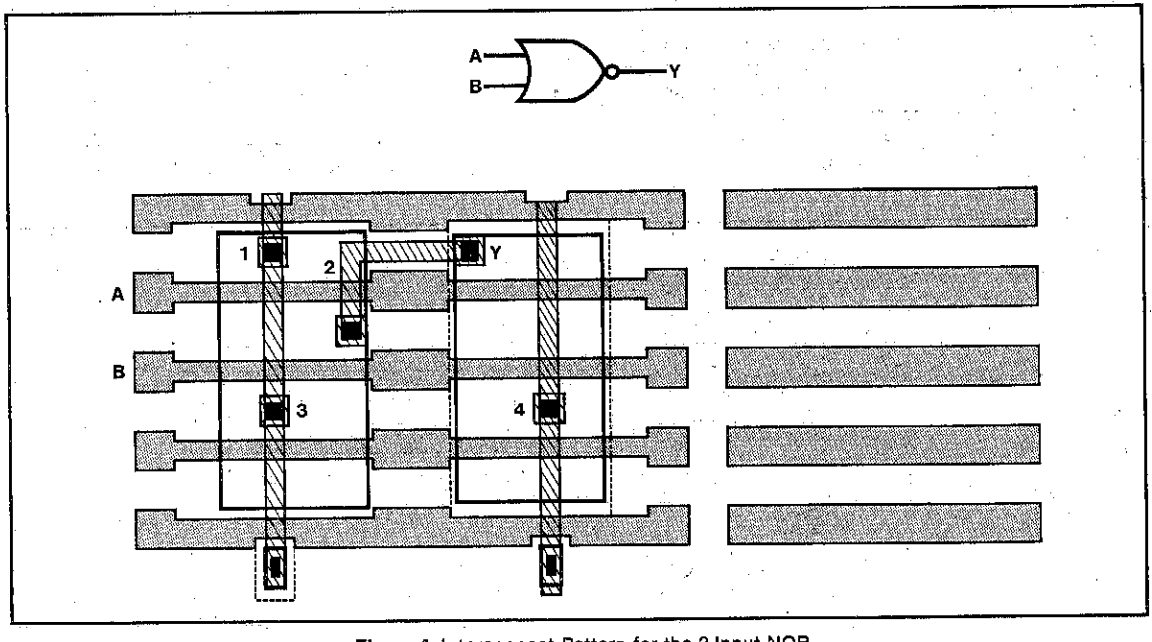


Figure 4. Interconnect Pattern for the 2-Input NOR

Table 2. IGC10000 MACRO Library

IGC10000 Combinational Macros	
Type	**Description**
NOR/NAND	2-input NAND 3-input NAND 4-input NAND 2-input NOR 3-input NOR 4-input NOR
XOR/XNOR	2-input XOR 2-input XNOR
Adder	One-bit full adder
Buffers and Inverters	1X inverter 2X inverter 3X inverter 4X inverter
Multifunction	2-1 AND-OR invert 2-2-2 AND-OR invert 3-2 AND-OR invert 2-1 OR-AND invert
Multiplexer	2 to 1 multiplexer
Schmitt Trigger	Schmitt Trigger
Transmission Gate	Buffered transmission gate Unbuffered transmission gate
Tristate Control	Tristate control

IGC10000 Sequential Macros		Set	Reset	Jam Load
D Flip-Flops	D flip-flop with reset	—	Yes	—
	D flip-flop with set	Yes	—	—
	D flip-flop with set and reset	Yes	Yes	—
	Divide by 2 flip-flop w/jam load and reset	—	Yes	Yes
	Divide by 2 flip-flop w/reset	—	Yes	—
	D flip-flop w/jam load and reset	—	Yes	Yes
	D flip-flop shift register with reset	—	Yes	—
JK Flip-Flops	JK flip-flop with reset	—	Yes	—
	JK flip-flop with set	Yes	—	—
T Flip-Flops	T flip-flop with reset	—	Yes	—
Latches	D latch	—	—	—
	D latch w/single input control	—	—	—
	D latch with reset	—	Yes	—
	D latch w/reset and single input control	—	Yes	—
	D latch w/transmission gate on output	—	—	—
Counters	Down counter with reset	—	Yes	—
	Down counter w/jam load and reset	—	Yes	Yes
	Up counter with reset	—	Yes	—
	Up counter w/jam load and reset	—	Yes	Yes
	Up/down counter with reset	—	Yes	—
	Up/down counter w/jam load and reset	—	Yes	Yes

Table 2. IGC10000 MACRO Library (continued)

IGC10000 Digital I/O Cell Macros	
Type	**Description**
Bidirectional	Tristate output/unbuffered input Tristate output/inverting TTL input buffer
Feedthrough	Input feedthrough
Internal Buffer	Inverting internal buffer Internal tristate buffer
Input Buffer	Non-inverting TTL input buffer Non-inverting CMOS input buffer with pull-up options
Output Buffer	Open drain output buffer Non-inverting TTL output buffer Inverting TTL output buffer Tristate output buffer Symmetrical drive output buffer

IGC10000 Analog I/O Cell Macros

The list below represents a sample of custom macros developed for specific analog applications. Consult your Intersil Representative for suitability to your design.

Analog Transmission Gate
Auto Null Comparator
Comparator
Compensated Op Amp
Crystal Oscillator
Current Multiplier
Current Reference
Op Amp
Power-on Reset
RC Oscillator
Schmitt Trigger

COMPUTER AIDED DESIGN SOFTWARE TOOLS

The IGC10000 family is supported by a proprietary computer aided design (CAD) system developed at the General Electric Microelectronics Center. The system provides CAD tools for logic simulation, accurate prediction of circuit speed performance, automated design of interconnect circuitry, electrical and design rule checking, post-layout simulation using RC delays extracted from the layout, and automatic conversion of simulation test pattern files into tester format.

The CAD tools are integrated under a supervisory program called the CADEXEC (for CAD Executive) that runs on a Digital Equipment Corporation VAX computer. Once the user has entered the circuit's interconnect information into the computer, this information is converted into a common database accessed by all other parts of the software through the CADEXEC.

Logic Simulation: Users have access to the TEGAS logic simulator. For pre-layout logic (functional) verification, customers may perform TEGAS simulation using our Unit Delay Macro Library database; for design verification (pre-layout timing analysis), calculated delays based on fanout are used in conjunction with Best, Typical, and Worst Case libraries, whose parameters are described in Table 3.

Table 3. Best, Typical, and Worst Case Parameters

Parameter	Best	Typical	Worst
Voltage (V)	5.5	5.0	4.5
Temperature (°C)	0	27	70
Process	Best	Typical	Worst

Routing: The SILICA layout system uses a proprietary automatic router developed at the General Electric Microelectronics Center. The SILICA router has consistently performed with higher completion rate and lower CPU time than other commercially available routers; in addition, the router improves the overall performance of the circuit by selecting paths that produce the smallest delay. Like many routers, the SILICA router has a Critical Net feature that minimizes polysilicon and total net length by routing the critical net first. Unique to the SILICA router is the Super Critical Net feature, which prohibits the use of polysilicon gates in a specified net.

Electrical and Design Rule Checking: SILICA DRC (Design Rule Checker) performs electrical and design rule checking in minutes instead of hours and extracts geometric data from the layout for input into the RC delay extraction software.

Manual editing: In rare instances manual layout editing may be done on one of our CALMA workstations. CALMA output is fed into SILICA DRC for convenient verification of electrical integrity.

Post-layout simulation: A specialized circuit simulator has been developed at the General Electric Microelectronics Center to compute the delays of the RC-interconnect nets from the topology of the network after performing layout. The RC Delay extraction software uses a full transient analysis for each net; delays are based on resistance as well as capacitance of the interconnection nets. The software calculates delays as a function both of load switching voltage and driver output impedance and handles loops, bidirectional drivers, and multiple drivers on the net.

After the RC delay information is extracted, the CADEXEC system inserts the delays into the network database for post-layout TEGAS simulation and critical path analysis, thus providing an additional opportunity for refining the layout prior to PG tape generation.

Tester Tape Generation: Test program conversion software automatically translates the customer's final TEGAS simulation output file into a test vector pattern file to be used in testing the finished device.

PACKAGING

Five types of packages are available for the IGC10000 gate arrays. Dual inline packages are available in plastic (Plastic DIP), ceramic (CerDIP) and multilayer ceramic (Side Brazed DIP); leadless chip carriers and pin grid arrays are provided in multilayer ceramic. Table 4 presents recommended package types for each pin count and array size.

Table 4. Recommended Package Types

Number of Pins	Plastic DIP	CerDIP	Side Brazed DIP	Leadless Chip Carrier	Pin Grid Array
8	408		408		
14	408	408	408		
16	408	408	408		
18	408	408	408		
20		408	408		
24	408	408	408		
	756	756	756		
	1500	1500	1500		
28	408	408	408		
	756	756	756		
	1500	1500	1500		
40	408	408	408		
	756	756	756		
	1500	1500	1500		
44				756	
				1500	
48			756		
			1500		
52				1500	
68				1500	1500

DEVELOPMENT

An overview of the gate array development process is shown in the flow chart of Figure 6. During Phase 1 (Design Translation), most of the responsibility lies with the customer; during Phase 3 (Fabrication), with Intersil. In Phase 2 (Design Implementation), most of the activities are performed by Intersil, but require customer interaction and approval. Figure 6 delineates the responsibilities of the customer and of Intersil. For more information, contact either your local Intersil representative, or Semicustom Marketing at the General Electric Microelectronics Center, Research Triangle Park, NC, telephone 919-549-3607.

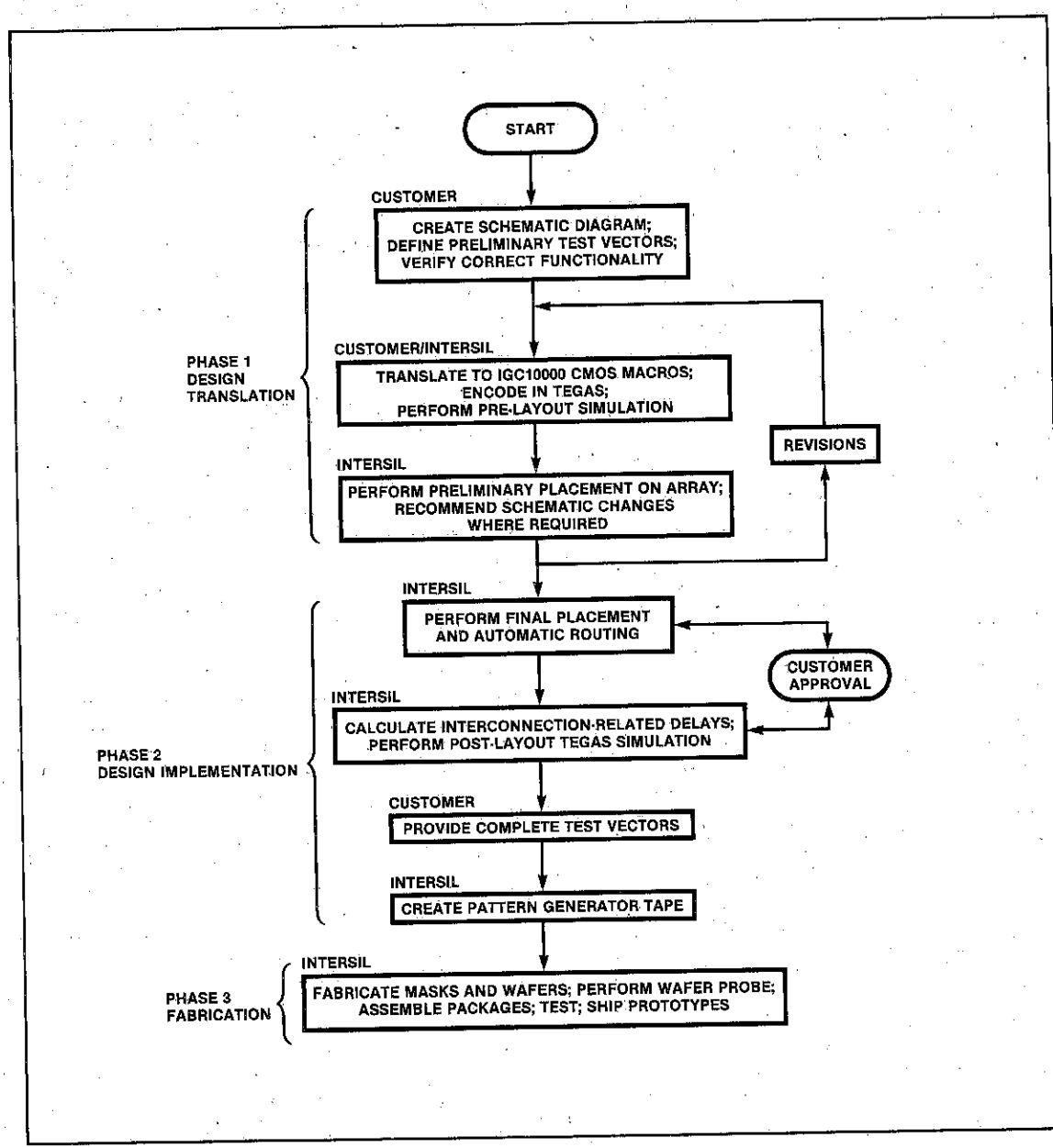


Figure 6. Simplified Flowchart for Gate Array Development

OPERATING CHARACTERISTICS[1]

Absolute Maximum Ratings[2] (Referenced to V_{SS})

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	−0.5 to +10.0	V
Input Voltage	V_I	−0.5 to V_{DD} + 0.5	V
DC Input Current	I_I	±10	mA
Operating Ambient Temperature Range	T_A	−55 to +125	°C
Storage Temperature Range (Ceramic)	T_{STG}	−65 to +150	°C
Storage Temperature Range (Plastic)	T_{STG}	−40 to +125	°C

NOTE 1: Stress ratings only. Functional operation of the device at these or any conditions beyond those indicated as Recommended Operating Conditions is not implied.

NOTE 2: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Limits	Units
DC Supply Voltage	V_{DD}	3.3±0.3V to 9.0±0.9V	V
Typical Operating Frequency	f_{CK}	8.0	MHz
Operating Ambient Temperature Range[1]	T_A	−55 to +125	°C

NOTE 1: IGC10000 gate array macros are currently characterized between 0 and 70°C.

AC CHARACTERISTICS

Specified for nominal processing = 5V, 27°C.
Calculated for a fanout of 1.

	Parameter	Typical Delay (ns)
Array Cell Macros		
2-input NAND	D to Output	6
2-input NOR	D to Output	6
4-input NAND	D to Output	8
4-input NOR	D to Output	18
1X inverter	D to Output	5
4X inverter	D to Output	4
2-1 AND-OR invert	D to Output	9
D flip-flop with reset	CK to Output	9
Schmitt trigger	Input to Output	18
Up counter with reset	CK to Output	11
I/O Cell Macros		
Input feedthrough	Pad to Output	1
Non-inverting Input Buffer	Pad to Output	9
Non-inverting Output Buffer	D to Pad	10 (15 pF) 19 (50 pF)

DC CHARACTERISTICS

V_{DD} = 5V ±10%

Symbol	Parameter	Condition	Limits[1]							
			0°C		25°C			70°C		
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Units
I_{DD}[2]	Quiescent Device Current	$V_I = V_{DD}$ or V_{SS}				0.3			100	µA
V_{OL}	Low Level Output Voltage	$\|I_O\| \leq 1\mu A$		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\|I_O\| \leq 1\mu A$	V_{DD} – 0.05		V_{DD} – 0.05			V_{DD} – 0.05		V
V_{IL}	Low Level Input Voltage	CMOS I/O Macro		1.5			1.5		1.5	V
V_{IH}	High Level Input Voltage	CMOS I/O Macro	3.5		3.5			3.5		V
V_{IL}	Low Level Input Voltage	TTL I/O Macro		0.8			0.8		0.8	V
V_{IH}	High Level Input Voltage	TTL I/O Macro	2.0		2.0			2.0		V
I_{OL}[3]	Output Low[4] (Sink Current)	$V_O = 0.4V$	1.8		1.8	3.6		1.6		mA
		$V_O = 2.5V$	3.8		3.8	7.6		3.4		mA
I_{OH}[3]	Output High (Source Current)	$V_O = 4.6V$	0.3		0.3	0.6		0.25		mA
		$V_O = 2.5V$	1.8		1.8	3.6		1.6		mA
I_{IN}	Input Leakage Current	$V_{IN} = 0$ or V_{DD}		±0.1		±.001	±0.1		±1.0	µA
I_{OZ}	Tristate Output Leakage Current	$V_O = 0$ or V_{DD}		±1.0		±.001	±1.0		±10	µA
C_{IN}	Input Capacitance	Any Input				5.0				pF

NOTES:

1. IGC10000 gate arrays are designed to perform under conditions up to 125°C. Limits reflect temperature range at which the macro library is characterized.
2. Any internal oscillators disabled.
3. Results depend on specific output macro used.
4. There may be limitations on maximum current when many outputs are simultaneously low.