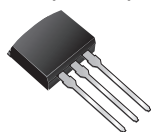
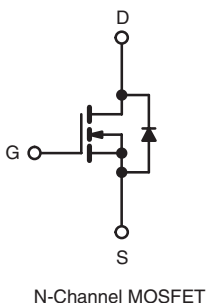
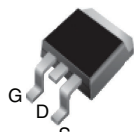


Power MOSFET

PRODUCT SUMMARY

V_{DS} (V)	60	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	0.018
Q_g (Max.) (nC)	110	
Q_{gs} (nC)	29	
Q_{gd} (nC)	36	
Configuration	Single	

I²PAK (TO-262)

D²PAK (TO-263)


FEATURES

- Advanced Process Technology
- Surface Mount (IRFZ48S/SiHFZ48S)
- Low-Profile Through-Hole (IRFZ48L/SiHFZ48L)
- 175 °C Operating Temperature
- Fast Switching
- Lead (Pb)-free Available



Available
RoHS*
COMPLIANT

DESCRIPTION

Third generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The D²PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on-resistance in any existing surface mount package. The D²PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2 W in a typical surface mount application.

The through-hole version (IRFZ48L/SiHFZ48L) is available for low-profile applications.

ORDERING INFORMATION

Package	D ² PAK (TO-263)	D ² PAK (TO-263)	I ² PAK (TO-262)
Lead (Pb)-free	IRFZ48SPbF	-	IRFZ48LPbF
	SiHFZ48S-E3	-	SiHFZ48L-E3
SnPb	IRFZ48S	IRFZ48STRL	-
	SiHFZ48S	SiHFZ48STL	-

Note

a. See device orientation.

ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ °C}$, unless otherwise noted

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ^f	V_{GS} at 10 V	$T_C = 25\text{ °C}$	A
		$T_C = 100\text{ °C}$	
Pulsed Drain Current ^{a, e}	I_{DM}	290	
Linear Derating Factor		1.3	W/°C
Single Pulse Avalanche Energy ^{b, e}	E_{AS}	100	mJ
Maximum Power Dissipation	P_D	$T_C = 25\text{ °C}$	W
		$T_A = 25\text{ °C}$	
Peak Diode Recovery dV/dt ^{c, e}	dV/dt	4.5	V/ns
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to + 175	°C
Soldering Recommendations (Peak Temperature) ^d	for 10 s	300	

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. $V_{DD} = 25\text{ V}$, Starting $T_J = 25\text{ °C}$, $L = 22\text{ }\mu\text{H}$, $R_G = 25\text{ }\Omega$, $I_{AS} = 72\text{ A}$ (see fig. 12).

c. $I_{SD} \leq 72\text{ A}$, $dI/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 175\text{ °C}$.

d. 1.6 mm from case.

e. Uses IRFZ48/SiHFZ48 data and test conditions.

f. Calculated continuous current based on maximum allowable junction temperature.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS

PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	40	°C / W
Maximum Junction-to-Case (Drain)	R_{thJC}	-	0.8	

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

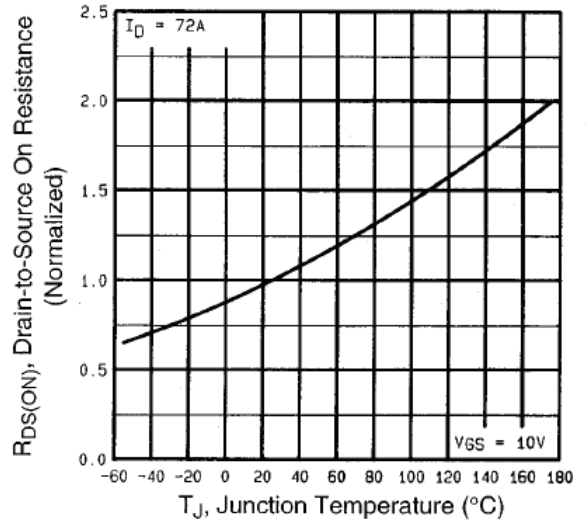
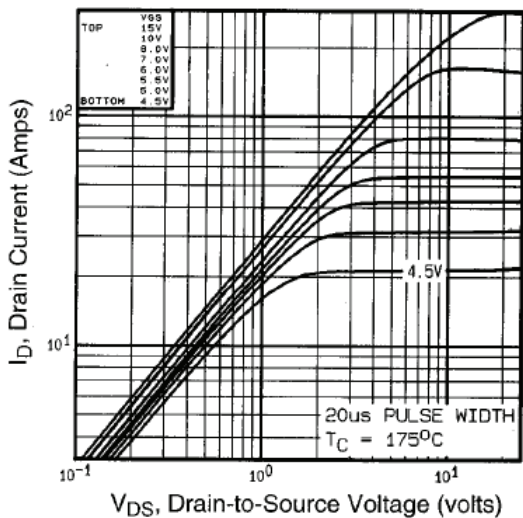
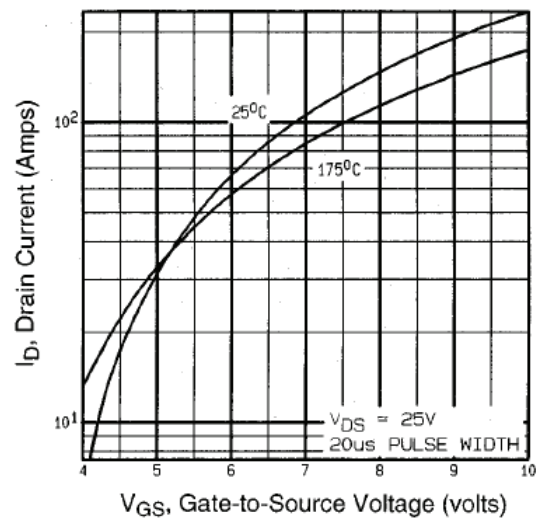
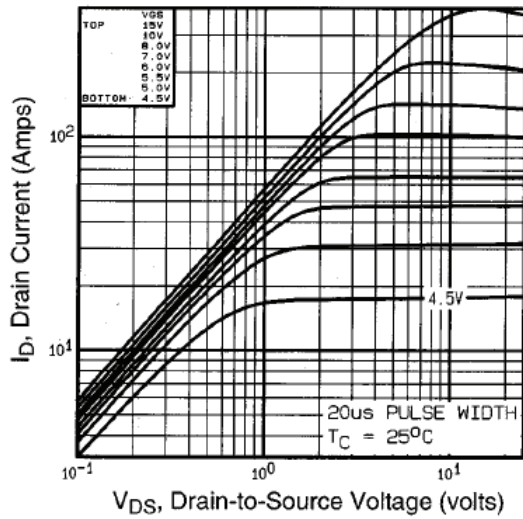
SPECIFICATIONS $T_J = 25\text{ }^{\circ}\text{C}$, unless otherwise noted

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA		60	-	-	V
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	Reference to 25 °C, I _D = 1 mA ^c		-	0.060	-	V/°C
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA		2.0	-	4.0	V
Gate-Source Leakage	I _{GSS}	V _{GS} = ± 20 V		-	-	± 100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V		-	-	25	μA
		V _{DS} = 48 V, V _{GS} = 0 V, T _J = 150 °C		-	-	250	
Drain-Source On-State Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 43 A ^b	-	-	0.018	Ω
Forward Transconductance	g _{fs}	V _{DS} = 25 V, I _D = 43 A ^b		27	-	-	S
Dynamic							
Input Capacitance	C _{iss}	V _{GS} = 0 V, V _{DS} = 25 V, f = 1.0 MHz, see fig. 5 ^c		-	2400	-	pF
Output Capacitance	C _{oss}			-	1300	-	
Reverse Transfer Capacitance	C _{rss}			-	190	-	
Total Gate Charge	Q _g	V _{GS} = 10 V	I _D = 72 A, V _{DS} = 48 V, see fig. 6 and 13 ^{b, c}	-	-	110	nC
Gate-Source Charge	Q _{gs}			-	-	29	
Gate-Drain Charge	Q _{gd}			-	-	36	
Turn-On Delay Time	t _{d(on)}	V _{DD} = 30 V, I _D = 72 A, R _G = 9.1 Ω, R _D = 0.34 Ω, see fig. 10 ^{b, c}		-	8.1	-	ns
Rise Time	t _r			-	250	-	
Turn-Off Delay Time	t _{d(off)}			-	210	-	
Fall Time	t _f			-	250	-	
Internal Source Inductance	L _S	Between lead, and center of die contact		-	7.5	-	nH
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	50 ^c	A
Pulsed Diode Forward Current ^a	I _{SM}			-	-	290	
Body Diode Voltage	V _{SD}	T _J = 25 °C, I _S = 72 A, V _{GS} = 0 V ^b		-	-	2.0	V
Body Diode Reverse Recovery Time	t _{rr}	T _J = 25 °C, I _F = 72 A, dI/dt = 100 A/μs ^{b, c}		-	120	180	ns
Body Diode Reverse Recovery Charge	Q _{rr}			-	500	800	μC
Forward Turn-On Time	t _{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L _S and L _D)					

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- Uses IRFZ48/SiHFZ48 data and test conditions.
- Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



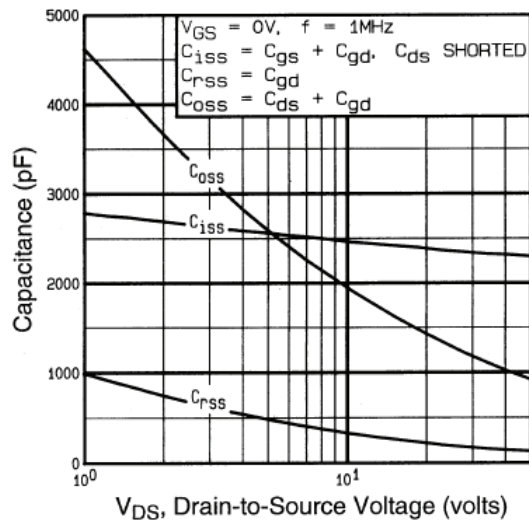


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

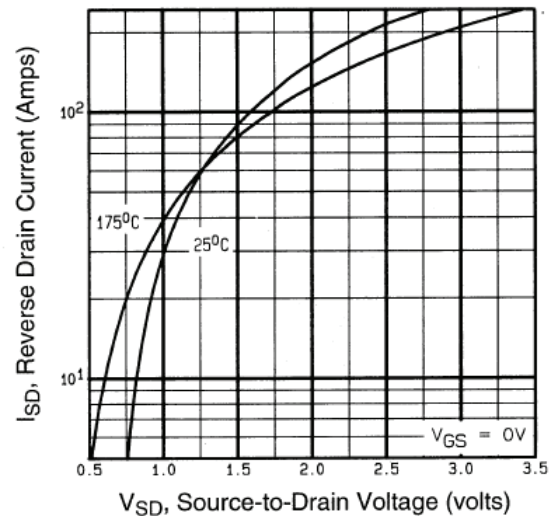


Fig. 7 - Typical Source-Drain Diode Forward Voltage

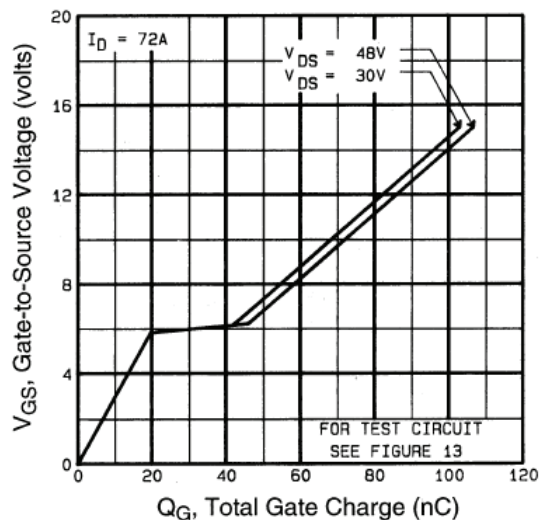


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

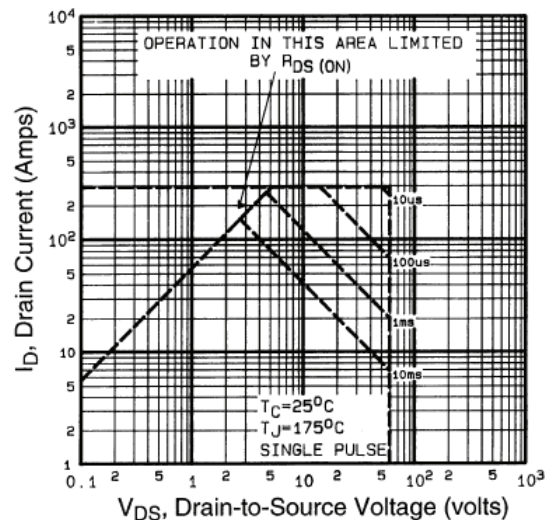


Fig. 8 - Maximum Safe Operating Area

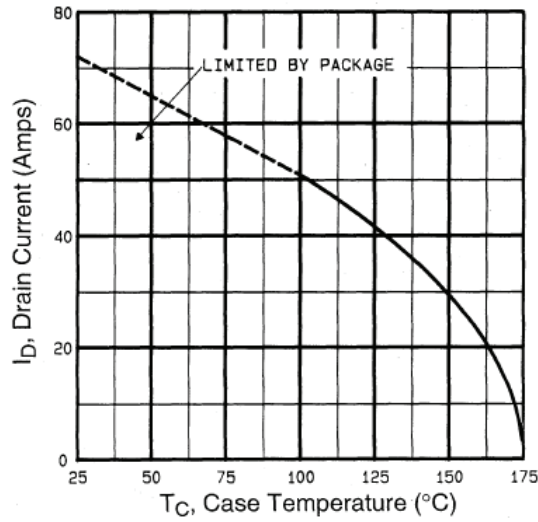


Fig. 9 - Maximum Drain Current vs. Case Temperature

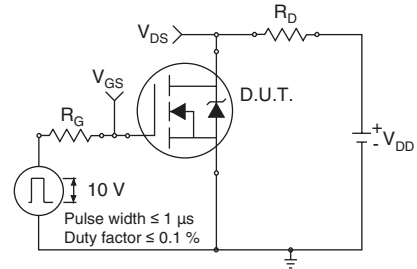


Fig. 10a - Switching Time Test Circuit

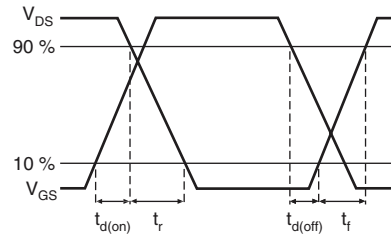


Fig. 10b - Switching Time Waveforms

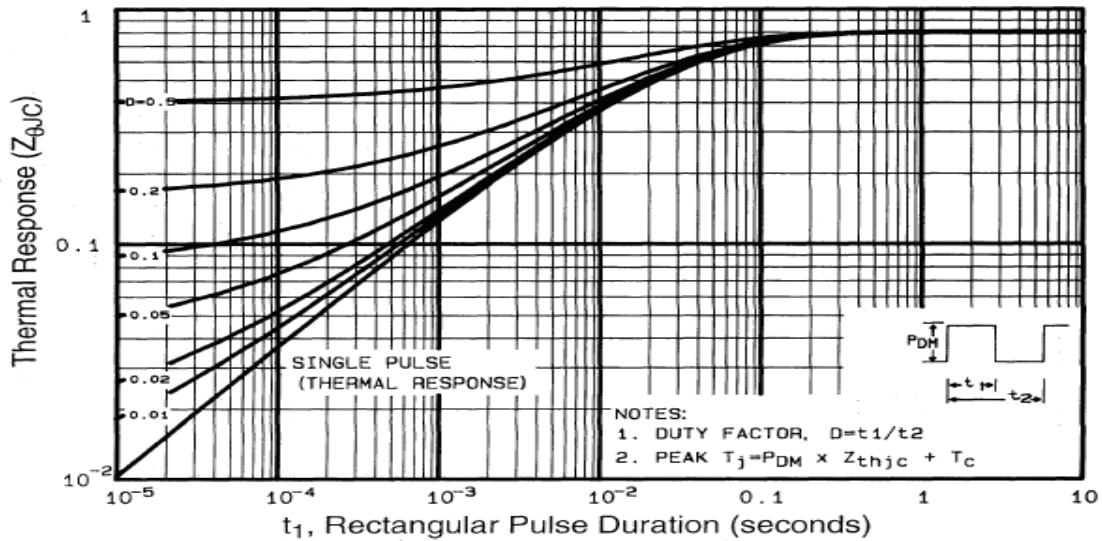


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

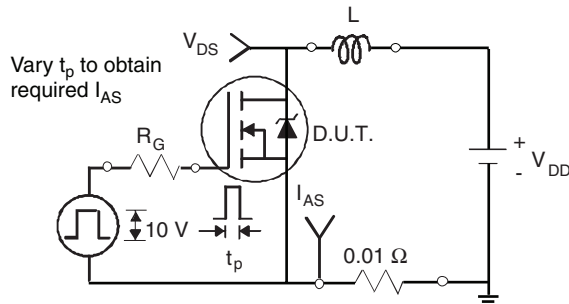


Fig. 12a - Unclamped Inductive Test Circuit

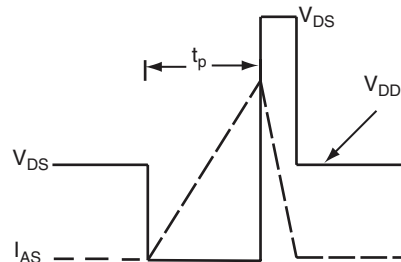


Fig. 12b - Unclamped Inductive Waveforms

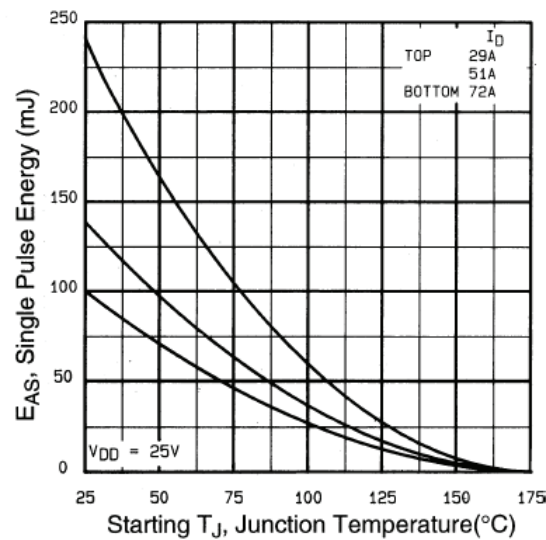


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

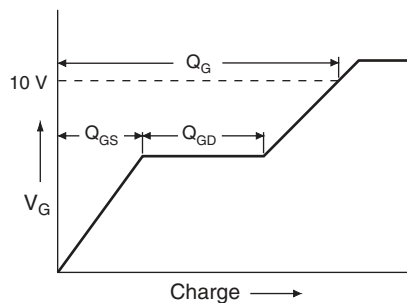


Fig. 13a - Maximum Avalanche Energy vs. Drain Current

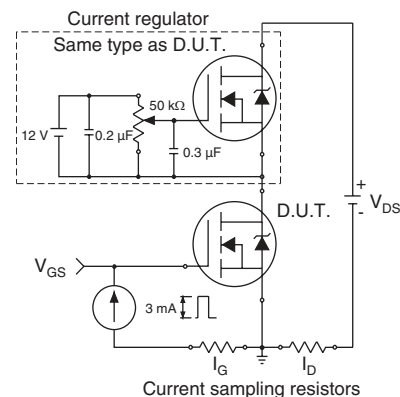


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit

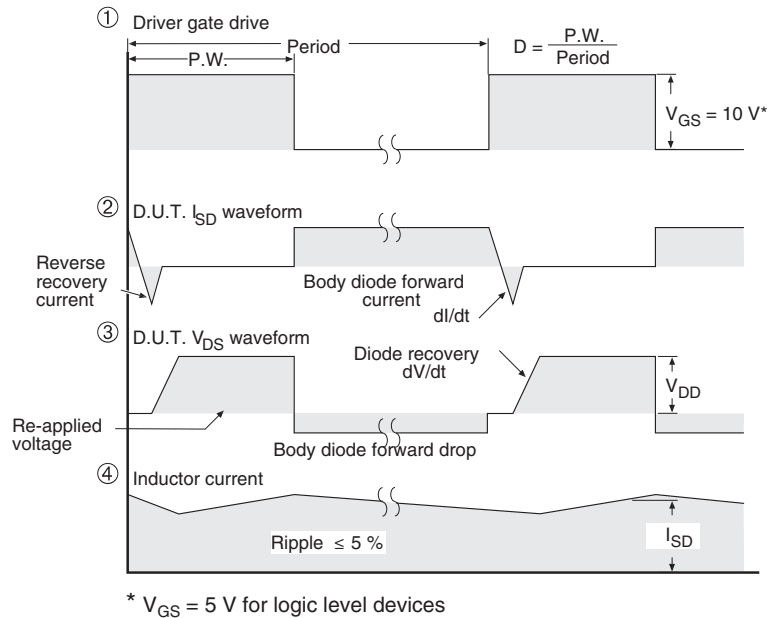
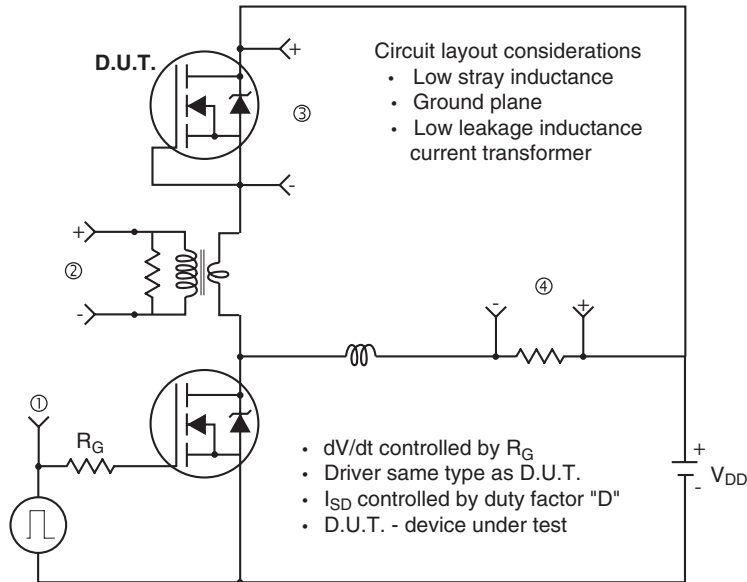


Fig. 14 - For N-Channel

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