Low-Power Dual Digital Isolators

Check for Samples: ISO7420, ISO7420M, ISO7421, ISO7421M

FEATURES

- **Highest Signaling Rate: up to 250 Mbps**
- **Low Power Consumption, Typical I_{CC} per Channel:**
  - **2.2 mA at 25 Mbps, 4.2 mA at 100 Mbps**
- **Very Low Propagation Delay – 9 ns Typ. and Very Low Skew – 300 ps Typ.**
- **Widest T_A Range Specified: –55°C to 125°C**
- **4-kVpeak Maximum Isolation, 2.5 kVrms per UL 1577, IEC/VDE and CSA Approved, IEC 60950-1, IEC 61010-1 End Equipment Standards Approved. All Approvals Pending.**
- **50 kV/μs Transient Immunity, Typical**
- **Over 25-Year Isolation Integrity at Rated Voltage**
- **Operates From 3-V to 5.5-V Supply and Logic Levels**

APPLICATIONS

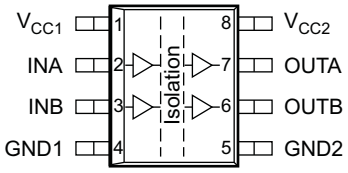
- **Optocoupler Replacement in:**
  - **Industrial Fieldbus**
    - **Profibus**
    - **Modbus**
    - **DeviceNet™ Data Buses**
  - **Servo Control Interface**
  - **Motor Control**
  - **Power Supplies**
  - **Battery Packs**

DESCRIPTION

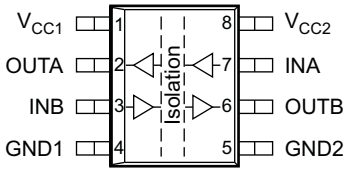
The ISO7421 and ISO7421M provide galvanic isolation up to 2.5 kVrms for 1 minute per UL. These digital isolators have two isolated channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry.

The devices have TTL input thresholds and require two supply voltages from 3 V to 5.5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3-V supply.

ISO7420
D Package
(Top View)



ISO7421
D Package
(Top View)



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TERMINAL FUNCTIONS

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
INA	7	I	Input, channel A
INB	3	I	Input, channel B
GND1	4	–	Ground connection for V_{CC1}
GND2	5	–	Ground connection for V_{CC2}
OUTA	2	O	Output, channel A
OUTB	6	O	Output, channel B
V_{CC1}	1	–	Power supply, V_{CC1}
V_{CC2}	8	–	Power supply, V_{CC2}

Table 1. FUNCTION TABLE(1)

INPUT SIDE VCC	OUTPUT SIDE VCC	INPUT IN	OUTPUT OUT
PU	PU	H	H
		L	L
		Open	H
PD	PU	X	H

(1) PU = Powered up (V_{CC} ≥ 3 V); PD = Powered down (V_{CC} ≤ 2.4 V); X = Irrelevant; H = High level; L = Low level

AVAILABLE OPTIONS

PRODUCT	RATED ISOLATION	PACKAGE	INPUT THRESHOLD	RATED T_A	CHANNEL DIRECTION	MARKED AS	ORDERING NUMBER
ISO7420	2.5 kVrms	D-8	~1.5 V (TTL) (CMOS compatible)	–40°C to 105°C	Same direction	IS7420	ISO7420D (rail)
							ISO7420DR (reel)
ISO7420M				–55°C to 125°C		I7420M	ISO7420MD (rail)
							ISO7420MDR (reel)
ISO7421				–40°C to 105°C	Opposite directions	IS7421	ISO7421D (rail)
							ISO7421DR (reel)
ISO7421M (PREVIEW)				–55°C to 125°C		I7421M	ISO7421MD (rail)
							ISO7421MDR (reel)

ABSOLUTE MAXIMUM RATINGS(1)

					VALUE
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}				–0.5 V to 6 V
V_I	Voltage at IN, OUT				–0.5 V to 6 V
I_O	Output current				±15 mA
ESD	Electrostatic discharge	Human-body model	JEDEC Standard 22, Test Method A114-C.01	All pins	±4 kV
		Field-induced charged-device model	JEDEC Standard 22, Test Method C101		±1.5 kV
		Machine model	ANSI/ESDS5.2-1996		±200 V
$T_{J(Max)}$	Maximum junction temperature				150°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.

RECOMMENDED OPERATING CONDITIONS

		MIN	TYP	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage	3		5.5	V
I_{OH}	High-level output current			4	mA
I_{OL}	Low-level output current	–4			
V_{IH}	High-level input voltage	2		V_{CC}	V
V_{IL}	Low-level input voltage	0		0.8	
T_J(1)	Junction temperature	–55		136	°C

(1) To maintain the recommended operating conditions for T_J, see the *Package Thermal Characteristics* table and the *Icc Equations* section of this data sheet.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ±10%; T_A = –55°C to 125°C for ISO7421M, T_A = –40°C to 105°C for ISO7421

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.		V_{CC} – 0.8	4.6		V
		I_{OH} = –20 µA; see Figure 1.		V_{CC} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1.2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	50		kV/µs
SUPPLY CURRENT							
	ISO7420						
I_{CC1}	Supply current for V_{CC1}	Quiescent	V_I = V_{CC} or 0 V, no load		0.4	0.8	mA
		25 Mbps			1.5	2.5	
		100 Mbps			5	8	
		200 Mbps			8	17	
I_{CC2}	Supply current for V_{CC2}	Quiescent	V_I = V_{CC} or 0 V, no load		2.7	4.5	mA
		25 Mbps			3.8	6	
		100 Mbps			7	11	
		200 Mbps			15	20	
	ISO7421						
I_{CC1}	Supply current for V_{CC1}	Quiescent	V_I = V_{CC} or 0 V, no load		2	3	mA
		25 Mbps			3.5	5	
		100 Mbps			7.5	11	
		200 Mbps			12	17	
I_{CC2}	Supply current for V_{CC2}	Quiescent	V_I = V_{CC} or 0 V, no load		2	3	mA
		25 Mbps			3.5	5	
		100 Mbps			7.5	11	
		200 Mbps			12	17	

SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 5 V ±10%; T_A = –55°C to 125°C for ISO7421M, T_A = –40°C to 105°C for ISO7421

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.		9	12	ns
PWD (1)	Pulse duration distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.3	1.5	ns
$t_{sk(pp)}$	Part-to-part skew time				2	ns
$t_{sk(o)}$	Channel-to-channel output skew time				1.6	ns
t_r	Output signal rise time	See Figure 1.		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		6		µs
t_{ui}	Input pulse duration		5	4		ns
1 / t_{ui}	Signaling rate		0	250	200	Mbps

(1) Also known as pulse skew.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 5 V ±10%, V_{CC2} at 3.3 V ±10%; T_A = –55°C to 125°C for ISO7421M, T_A = –40°C to 105°C for ISO7421

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.	ISO7421 (5-V side)	V_{CC} – 0.8			V
		I_{OH} = –20 µA; see Figure 1.		V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.				0.4	V
		I_{OL} = 20 µA; see Figure 1.				0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1.2		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	40		kV/µs
SUPPLY CURRENT							
	ISO7420						
I_{CC1}	Supply current for V_{CC1}	Quiescent	V_I = V_{CC} or 0 V, no load		0.4	0.8	mA
		25 Mbps			1.5	2.5	
		100 Mbps			5	8	
		200 Mbps			8	17	
I_{CC2}	Supply current for V_{CC2}	Quiescent	V_I = V_{CC} or 0 V, no load		2	3.5	mA
		25 Mbps			2.7	5	
		100 Mbps			4.5	7.5	
		200 Mbps			7	12	
	ISO7421						
I_{CC1}	Supply current for V_{CC1}	Quiescent	V_I = V_{CC} or 0 V, no load		2	3	mA
		25 Mbps			3.5	5	
		100 Mbps			7.5	11	
		200 Mbps			12	17	
I_{CC2}	Supply current for V_{CC2}	Quiescent	V_I = V_{CC} or 0 V, no load		1.5	2.5	mA
		25 Mbps			2.2	3.5	
		100 Mbps			4.2	6	
		200 Mbps			7.2	9	

SWITCHING CHARACTERISTICS

V_{CC1} at 5 V ±10%, V_{CC2} at 3.3 V ±10%; T_A = –55°C to 125°C for ISO7421M, T_A = –40°C to 105°C for ISO7421

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.		10	15	ns
PWD(1)	Pulse duration distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	2	ns
$t_{sk(pp)}$	Part-to-part skew time				3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				2	ns
t_r	Output signal rise time	See Figure 1.		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		6		µs
t_{ui}	Input pulse duration		10	5		ns
1 / t_{ui}	Signaling rate		0	200	100	Mbps

(1) Also known as pulse skew.

ELECTRICAL CHARACTERISTICS

V_{CC1} at 3.3 V ±10%, V_{CC2} at 5 V ±10%; T_A = –55°C to 125°C for ISO7421M, T_A = –40°C to 105°C for ISO7421

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.	ISO7421 (3.3-V side)	V_{CC} – 0.4			V
		I_{OH} = –20 µA; see Figure 1.		V_{CC} – 0.1			
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.				0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	40		kV/µs
SUPPLY CURRENT							
	ISO7420						
I_{CC1}	Supply current for V_{CC1}	Quiescent	V_I = V_{CC} or 0 V, no load		0.2	0.5	mA
		25 Mbps			0.8	1.3	
		100 Mbps			2.1	3.5	
		200 Mbps			4	7	
I_{CC2}	Supply current for V_{CC2}	Quiescent	V_I = V_{CC} or 0 V, no load		2.7	4.5	mA
		25 Mbps			3.8	6	
		100 Mbps			7	11	
		200 Mbps			15	20	
	ISO7421						
I_{CC1}	Supply current for V_{CC1}	Quiescent	V_I = V_{CC} or 0 V, no load		1.5	2.5	mA
		25 Mbps			2.2	3.5	
		100 Mbps			4.2	6	
		200 Mbps			7.2	9	
I_{CC2}	Supply current for V_{CC2}	Quiescent	V_I = V_{CC} or 0 V, no load		2	3	mA
		25 Mbps			3.5	5	
		100 Mbps			7.5	11	
		200 Mbps			12	17	

SWITCHING CHARACTERISTICS

V_{CC1} at 3.3 V ±10%, V_{CC2} at 5 V ±10%, T_A = –55°C to 125°C for ISO7421M, T_A = –40°C to 105°C for ISO7421

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.		10	15	ns
PWD(1)	Pulse duration distortion $\lvert t_{PHL} - t_{PLH} \rvert$			0.5	2	ns
$t_{sk(pp)}$	Part-to-part skew time				3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				2	ns
t_r	Output signal rise time	See Figure 1.		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		6		µs
t_{ui}	Input pulse duration		10	5		ns
1 / t_{ui}	Signaling rate		0	200	100	Mbps

(1) Also known as pulse skew.

ELECTRICAL CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ±10%, T_A = –55°C to 125°C for ISO7421M, T_A = –40°C to 105°C for ISO7421

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 1.		V_{CC} – 0.4	3		V
		I_{OH} = –20 µA; see Figure 1.		V_{CC} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 1.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 1.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	IN from 0 V or V_{CC}				10	µA
I_{IL}	Low-level input current			–10			µA
C_I	Input capacitance to ground	IN at V_{CC}, V_I = 0.4 sin (4E6πt)			1		pF
CMTI	Common-mode transient immunity	V_I = V_{CC} or 0 V; see Figure 3.		25	40		kV/µs
SUPPLY CURRENT							
	ISO7420						
I_{CC1}	Supply current for V_{CC1}	Quiescent	V_I = V_{CC} or 0 V, no load		0.2	0.5	mA
		25 Mbps			0.8	1.3	
		100 Mbps			2.1	3.5	
		200 Mbps			4	7	
I_{CC2}	Supply current for V_{CC2}	Quiescent	V_I = V_{CC} or 0 V, no load		2	3.5	mA
		25 Mbps			2.7	5	
		100 Mbps			4.5	7.5	
		200 Mbps			7	12	
	ISO7421						
I_{CC1}	Supply current for V_{CC1}	Quiescent	V_I = V_{CC} or 0 V, no load		1.5	2.5	mA
		25 Mbps			2.2	3.5	
		100 Mbps			4.2	6	
		200 Mbps			7.2	9	
I_{CC2}	Supply current for V_{CC2}	Quiescent	V_I = V_{CC} or 0 V, no load		1.5	2.5	mA
		25 Mbps			2.2	3.5	
		100 Mbps			4.2	6	
		200 Mbps			7.2	9	

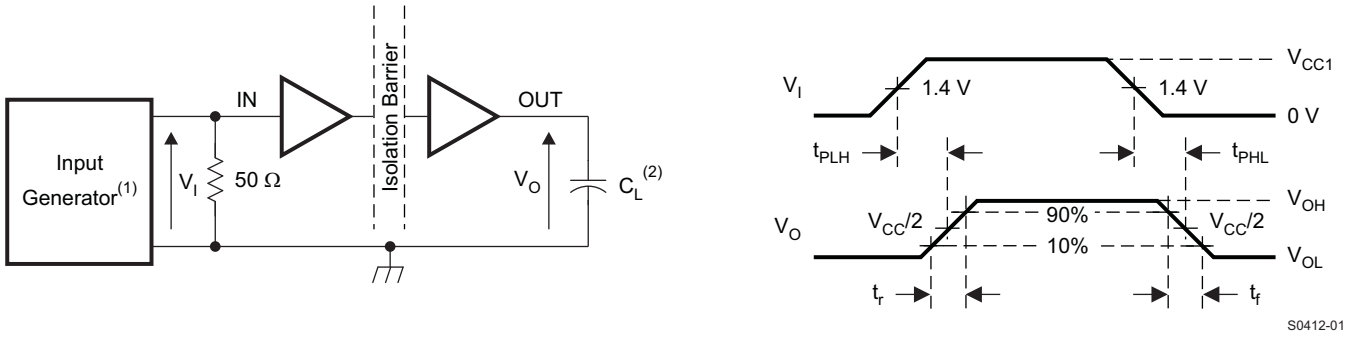
SWITCHING CHARACTERISTICS

V_{CC1} and V_{CC2} at 3.3 V ± 10%, T_A = –55°C to 125°C for ISO7421M, T_A = –40°C to 105°C for ISO7421

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 1.		12	18	ns
PWD(1)	Pulse duration distortion $\lvert t_{PHL} - t_{PLH} \rvert$			1	3	ns
$t_{sk(pp)}$	Part-to-part skew time				4	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.5	ns
t_r	Output signal rise time	See Figure 1.		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 2.		6		µs
t_{ui}	Input pulse duration		10	5		ns
1 / t_{ui}	Signaling rate		0	200	100	Mbps

(1) Also known as pulse skew.

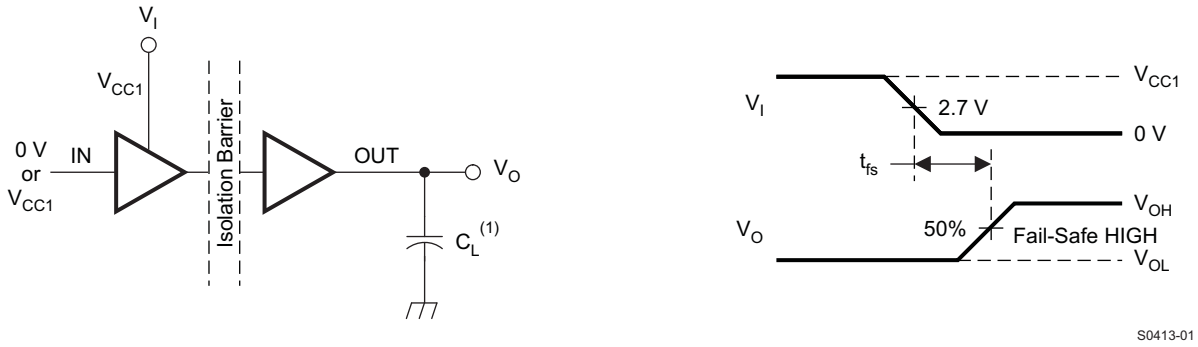
PARAMETER MEASUREMENT INFORMATION



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω.

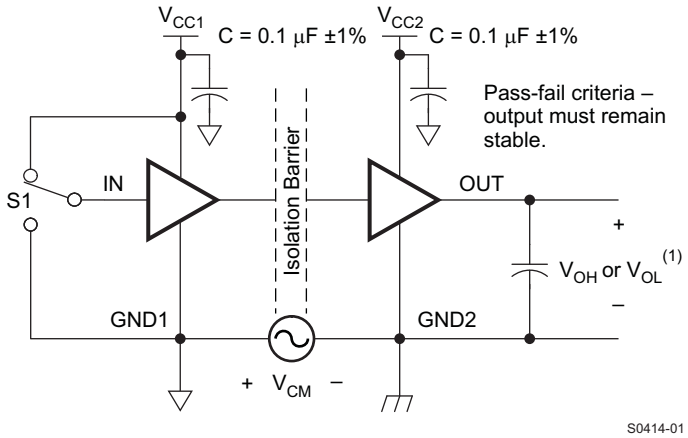
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 1. Switching Characteristic Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 2. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 3. Common-Mode Transient Immunity Test Circuit

DEVICE INFORMATION

PACKAGE CHARACTERISTICS

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4.8			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4.3			mm
CTI	Tracking resistance (comparative tracking index)	DIN IEC 60112 / VDE 0303 Part 1	>175			V
	Minimum internal gap (internal clearance)	Distance through the insulation	0.008			mm
R_{IO}	Isolation resistance	Input to output, V_{IO} = 500 V, all pins on each side of the barrier tied together creating a two-terminal device, T_A < 100°C		$>10^{12}$		Ω
		Input to output		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output	V_I = 0.4 sin (4E6πt)		1		pF

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal according to the measurement techniques shown in the Isolation Glossary. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

INSULATION CHARACTERISTICS(1)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	SPECIFICATION	UNIT
V_{IORM}	Maximum working insulation voltage		560	V
V_{PR}	Input-to-output test voltage	t = 1 s (100% production), partial discharge 5 pC	1050	V
V_{IOTM}	Transient overvoltage	t = 60 s (qualification)	4000	V
		t = 1 s (100% production)		
V_{ISO}	Isolation voltage per UL	t = 60 s (qualification)	2500	Vrms
		t = 1 s (100% production)	3000	
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	

(1) Climatic Classification 40/125/21

Table 2. IEC 60664-1 RATINGS TABLE

PARAMETER	TEST CONDITIONS	SPECIFICATION
Basic isolation group	Material group	III-a
Installation classification	Rated mains voltage ≤ 150 Vrms	I–IV
	Rated mains voltage ≤ 300 Vrms	I–III
	Rated mains voltage ≤ 400 Vrms	I–II

REGULATORY INFORMATION

VDE	CSA	UL
Certified according to IEC 60747-5-2	Approved under CSA Component Acceptance Notice	Recognized under 1577 Component Recognition Program(1)
File number: pending (40016131)	File number: pending (1698195)	File number: pending (E181974)

(1) Production tested ≥ 3000 Vrms for 1 second in accordance with UL 1577.

LIFE EXPECTANCY vs WORKING VOLTAGE

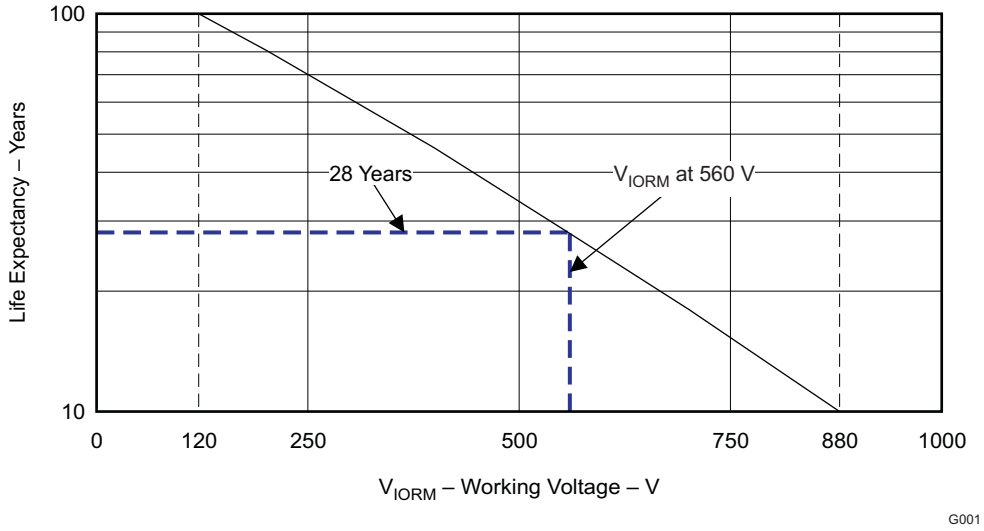


Figure 4. Life Expectancy vs Working Voltage

IEC SAFETY LIMITING VALUES

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	θ_{JA} = 212°C/W, V_I = 5.5 V, T_J = 170°C, T_A = 25°C			124	mA
		θ_{JA} = 212°C/W, V_I = 3.6 V, T_J = 170°C, T_A = 25°C			190	
T_S	Maximum case temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Characteristics* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leaded Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

PACKAGE THERMAL CHARACTERISTICS

(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JA}	Junction-to-air thermal resistance	Low-K thermal resistance(1)		212		°C/W
		High-K thermal resistance(1)		122		

(1) Tested in accordance with the low-K or high-K thermal metric definitions of EIA/JESD51-3 for leaded surface-mount packages

(over recommended operating conditions unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
θ_{JB}	Junction-to-board thermal resistance			37		°C/W
θ_{JC}	Junction-to-case thermal resistance			69.1		°C/W
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.5 V, T_J = 150°C, C_L = 15 pF, Input a 150-Mbps 50% duty-cycle square wave			390	mW

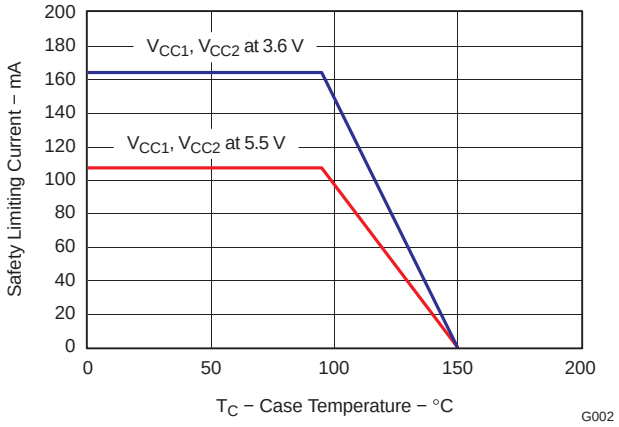


Figure 5. θ_{JC} Thermal Derating Curve per IEC 60747-5-2

I_{CC} EQUATIONS

$I_{CC}1,2 = I_{CC}1,2\_quiescent + Sum\ of\ all\ dynamic\ I_{CC}\ inputs\ on\ side\ 1,2 + sum\ of\ all\ dynamic\ I_{CC}\ outputs\ on\ side\ 1,2$ (1)

I_{CC}_quiescent can be determined from the electrical specification tables for concerned product included in the datasheet for the appropriate V_{CC}.

Dynamic I_{CC} can be calculated as follows.

At V_{CC} = 3.6, worst case

$I_{CC}\_input = 0.016 \times f$ (2)

$I_{CC}\_output = 0.02 \times f + 0.002 \times f \times (C_L - 0.5)$ (3)

At V_{CC} = 5.5, worst case

$I_{CC}\_input = 0.036 \times f$ (4)

$I_{CC}\_output = 0.033 \times f + 0.0032 \times f \times (C_L - 0.5)$ (5)

where I_{CC} is in mA, f = data rate in Mbps, C_L = capacitive load in pF.

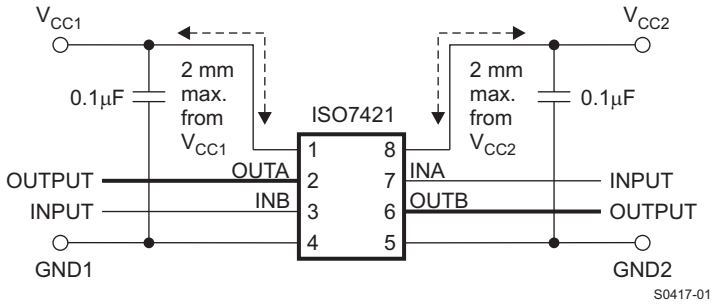


Figure 6. Typical ISO7421 Application Circuit

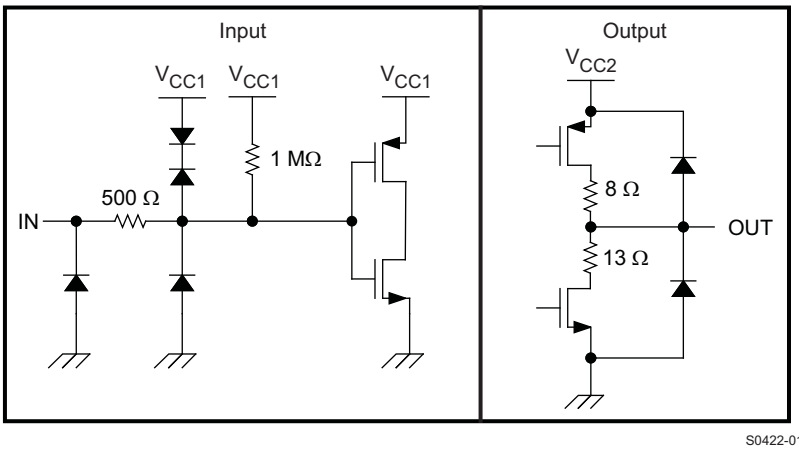


Figure 7. Device I/O Schematics

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs SIGNAL RATE (ALL CHANNELS)

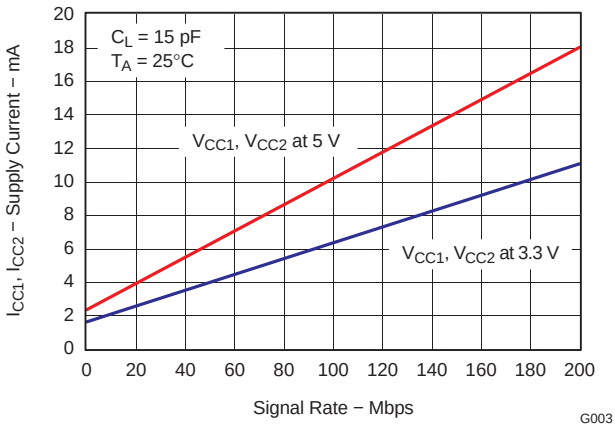


Figure 8. ISO7421

SUPPLY CURRENT vs SIGNAL RATE (ALL CHANNELS)

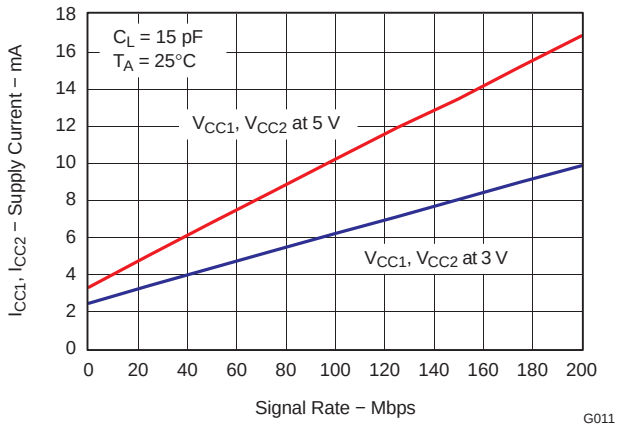


Figure 9. ISO7420

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

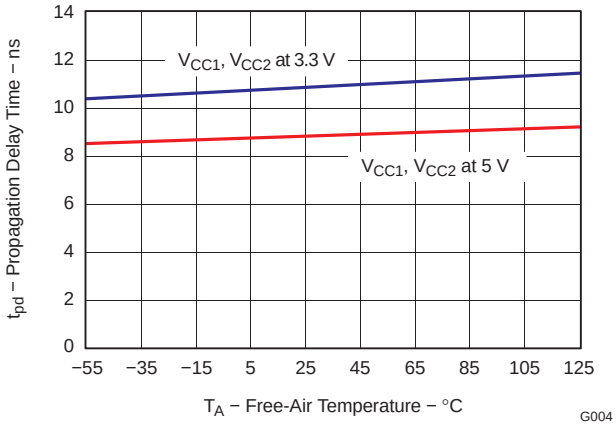


Figure 10.

INPUT VOLTAGE SWITCHING THRESHOLD vs FREE-AIR TEMPERATURE

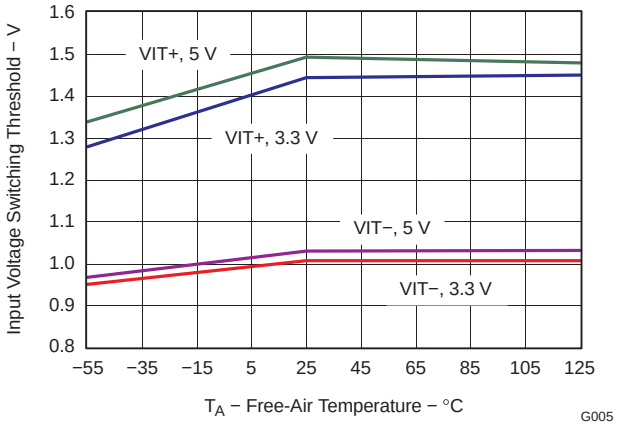


Figure 11.

TYPICAL CHARACTERISTICS (continued)

FAIL-SAFE VOLTAGE THRESHOLD vs FREE-AIR TEMPERATURE

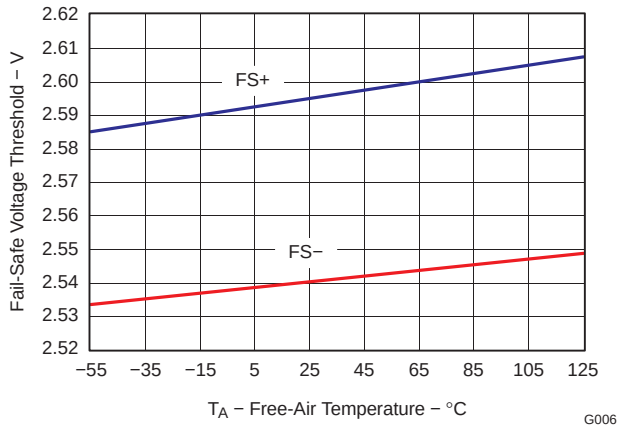


Figure 12.

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

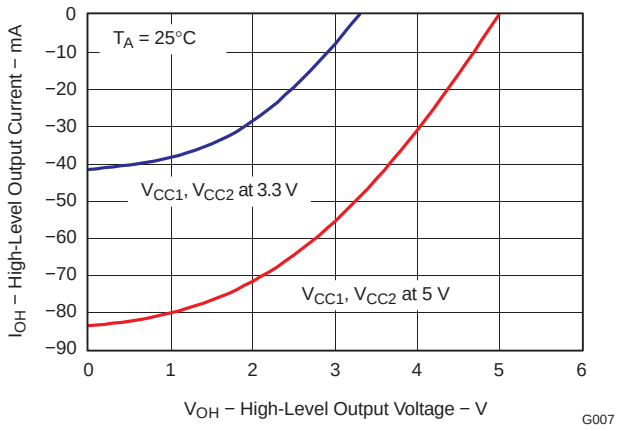


Figure 13.

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

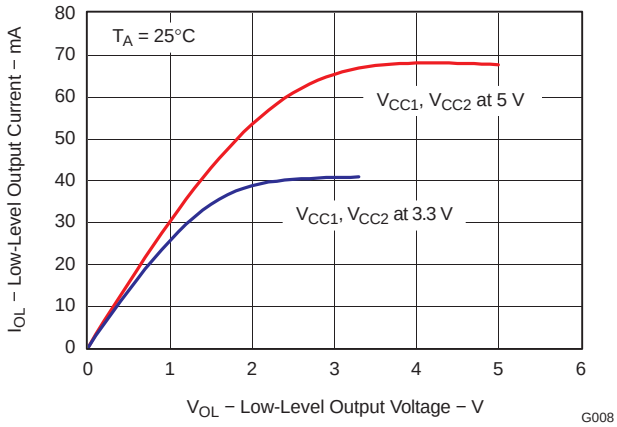


Figure 14.

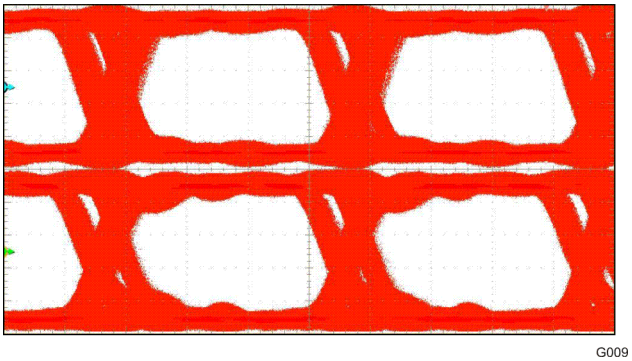


Figure 15. Eye Diagram at 250 MBPS, 5-V V_{CC}, Typical

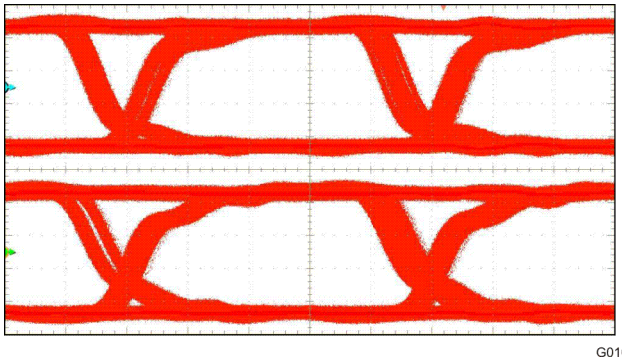


Figure 16. Eye Diagram at 200 MBPS, 5-V V_{CC}, 125°C

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ISO7420D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7420DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7420MD	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7420MDR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7421D	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7421DR	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
ISO7421MD	PREVIEW	SOIC	D	8	75	TBD	Call TI	Call TI
ISO7421MDR	PREVIEW	SOIC	D	8	2500	TBD	Call TI	Call TI

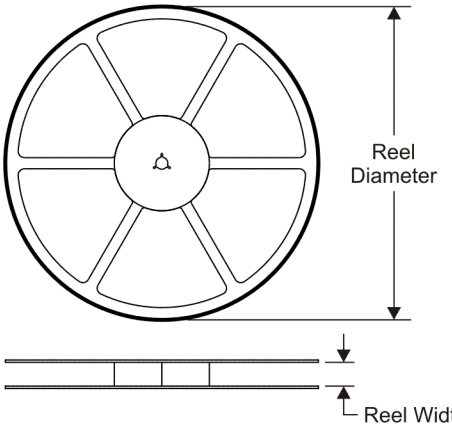
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

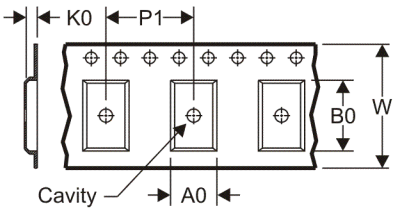
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

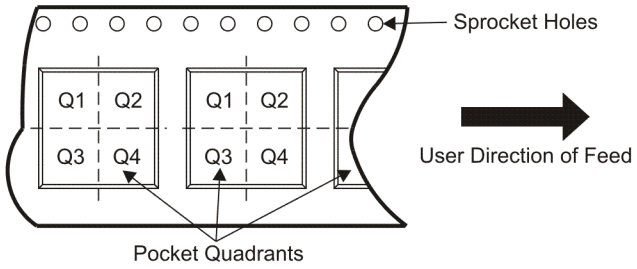


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

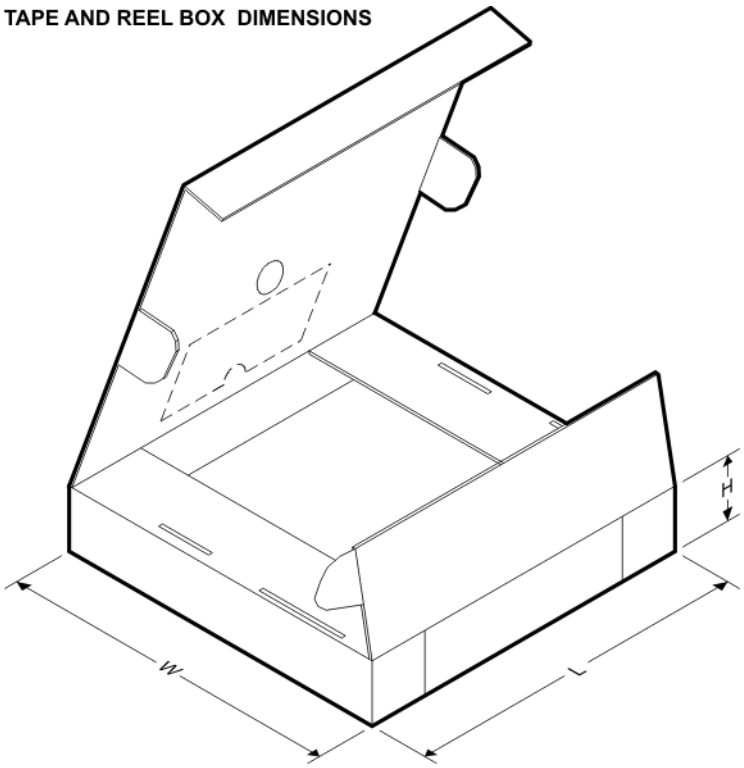
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7421DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

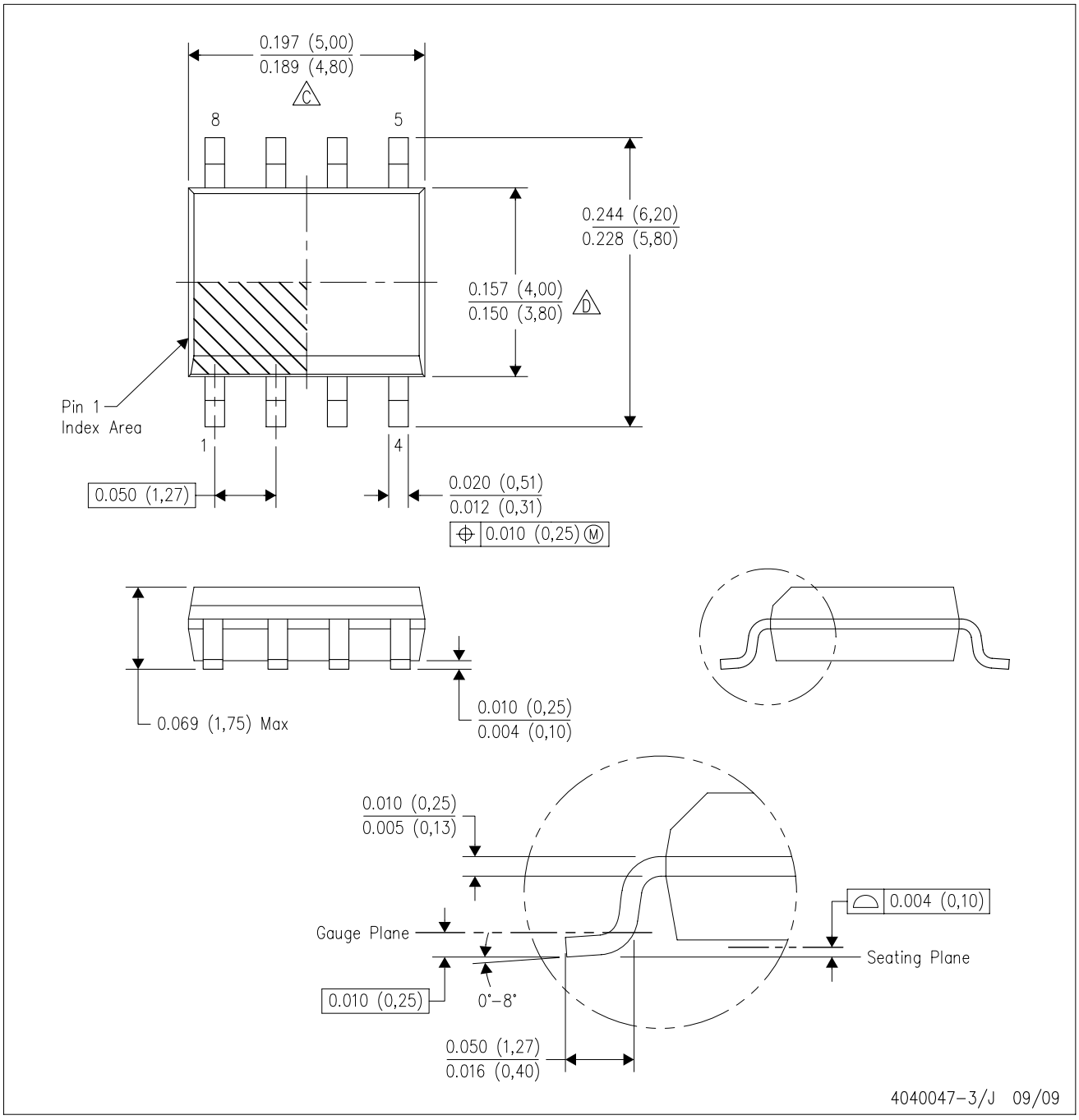
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7421DR	SOIC	D	8	2500	358.0	335.0	35.0

D (R–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
E. Reference JEDEC MS–012 variation AA.

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