Ordering number : ENN7740

SANYO Semiconductors
DATA SHEET

Monolithic Linear IC

LA6568 — Six-Channel Driver for Optical Disc Drives

Overview

The LA6568 is a six-channel driver for optical disc drives that includes built-in 3.3 V and 5 V regulators.

Functions

- Six power amplifier channels
- $I_O$max: 700 mA
- Built-in level shifter circuits (for the BTL amplifiers)
- Muting circuit (output on/off control) for one channel
- Built-in 3.3 V power supply ($I_O$max = 300 mA)
- Built-in 5 V power supply ($I_O$max = 5 mA)
- Thermal protection circuit (thermal shutdown circuit)

Specifications

Absolute Maximum Ratings at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Maximum supply voltage	V_{CC} max		14	V
Maximum output current	I_O max		0.7	A
Maximum input voltage	VINB max	Each channel for Ch.1 to Ch.6	13	V
Mute pin voltage	VMUTE		13	V
Allowable power dissipation	Pd max	Mounted on a board *1	2.00	W
		Independent IC	1.20	
Operating temperature	Topr		–30 to +85	°C
Storage temperature	Tstg		–55 to +150	°C

Note *1: Mounted on a board (76.1 × 114.3 × 1.66 mm) Material: glass epoxy

Recommended Operating Conditions at Ta = 25°C

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{CC}		6 to 13	V

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Electrical Characteristics

(Unless specified otherwise, the conditions are Ta = 25°C, S–V_{CC} = P–V_{CC} = 8 V, VREF = 1.65 V)

Parameter	Symbol	Conditions	Ratings			Unit
			min	typ	max	
[Overall]						
No load current drain - outputs on	I_{CC}-ON	All outputs on ∗1		30	50	mA
No load current drain - outputs off	I_{CC}-OFF	All outputs off ∗1		10	20	mA
VREF input voltage range	VREF-IN		0.5		V_{CC}-1.5	V
[BTL Amplifier Block]						
Output offset voltage	VOFF	The voltage difference between the output amplifier outputs, for each channel	–50		+50	mV
Input voltage range	V_{IN}		0		V_{CC}	V
Output voltage	V_O	The voltage between the V_O+ and V_O– outputs when R_L = 8 Ω ∗2	4	4.5		V
Closed circuit voltage gain 1	VG1	The gain between input and output for channels 1, 4, and 5	1.6	2	2.4	Multiplier
Closed circuit voltage gain 2	VG2	The gain between input and output for channel 2. Input resistance: 11 kΩ	3.5	4	4.5	Multiplier
Slew rate	SR	Twice the value between each output pair ∗3		1		V/μs
Muting on voltage	VMUTE-ON	For each of the muting functions ∗4			0.5	V
Muting off voltage	VMUTE-OFF	For each of the muting functions ∗4	2			V
[Loading Block]						
Voltage between outputs: F	VOF	V_{IN}+ = 2 V, V_{IN}–=0 V	2.5	2.9	3.3	V
Voltage between outputs: R	VOR	V_{IN}+ = 0 V, V_{IN}– = 2 V	–3.3	–2.9	–2.5	V
Output voltage range: F	VOMF	V_{IN}+ = 5 V, V_{IN}– = 0	4.5	5.0		V
Output voltage range: R	VOMR	V_{IN}+ = 0 V, V_{IN}– = 5 V		–5.0	–4.5	V
Output offset voltage	VOFF	Potential difference between the outputs when braking is applied	–50		+50	mV
Input current	I-IN	When V_{IN} = 3.3 V			500	μA
[3.3 V Regulator Block]						
Output voltage	V_O-REG1	I_O = 100 mA	3.15	3.3	3.45	V
Line regulation	ΔV-LIN1	When I_O = 100 mA, V_{CC} = 6 to 12 V	–100		+100	mV
Load regulation	ΔV-LOAD1	When I_O = 0 to 200 mA	–100		+100	mV
[5 V Regulator Block]						
Output voltage	V_O-REG2	When I_O = 3 mA	4.75	5	5.25	V
Line regulation	ΔV-LIN1	When I_O = 3 mA, V_{CC} = 6 to 12 V		100		mV
Load regulation	ΔV-LOAD	When I_O = 1 to 3 mA		100		mV
[0-$\overline{\text{RESET}}$ Block] (Operating for V_{REF})						
High-level reset output voltage	VORH	With a 10 kΩ resistor between V_{CC} and RESET	6.5			V
Low-level reset output voltage	VORL	With a 10 kΩ resistor between V_{CC} and RESET			0.5	V
0-$\overline{\text{RESET}}$ threshold voltage	VRT		0.5	0.7	0.9	V
0-$\overline{\text{RESET}}$ hysteresis	VHYS		50	100	200	mV

Note ∗1: The combined current drain for P-V_{CC} and S-V_{CC} with no load

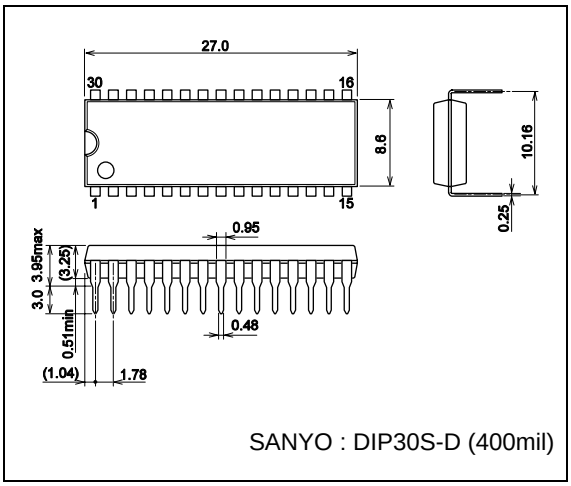
∗2: The voltage difference across the load (8Ω) terminals. With the outputs in the saturated state.

∗3: Design target value. Parameters are not tested.

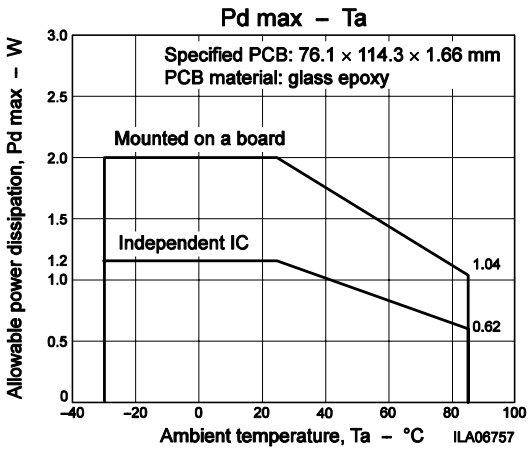
∗4: When IN-$\overline{\text{MUTE}}$ is high: output on, when IN-$\overline{\text{MUTE}}$ is low: output off (high-impedance state)

Package Dimensions

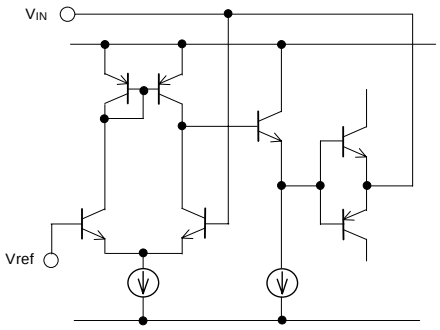
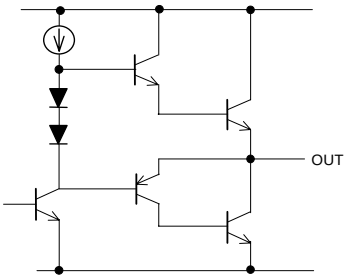
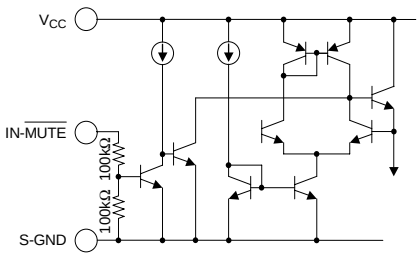
unit: mm
3196A



SANYO : DIP30S-D (400mil)



Pin Functions

Pin No.	Symbol	Pin name	Pin description	Equivalent circuit
20 19 12 13	$V_{IN}1$ $V_{IN}2$ $V_{IN}4$ $V_{IN}5$	Input	Inputs	
26 25 28 27 6 5 4 3 2 1 30 29	V_O1+ V_O1- V_O2+ V_O2- V_O4+ V_O4- V_O5+ V_O5- V_O3+ V_O3- V_O6+ V_O6-	Output	Outputs	
10	IN-$\overline{\text{MUTE}}$	Mute	Controls the on/off state of the outputs. IN-$\overline{\text{MUTE}}$ high: outputs on IN-$\overline{\text{MUTE}}$ low: outputs off	

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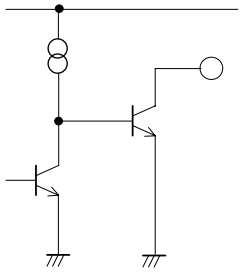
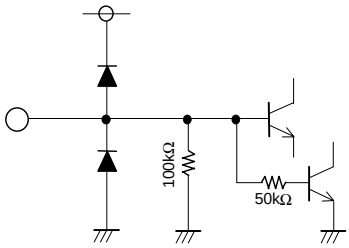
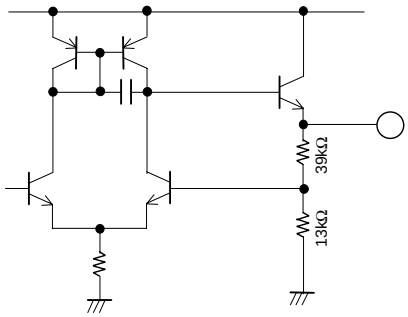
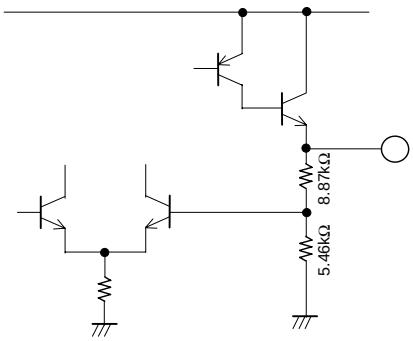
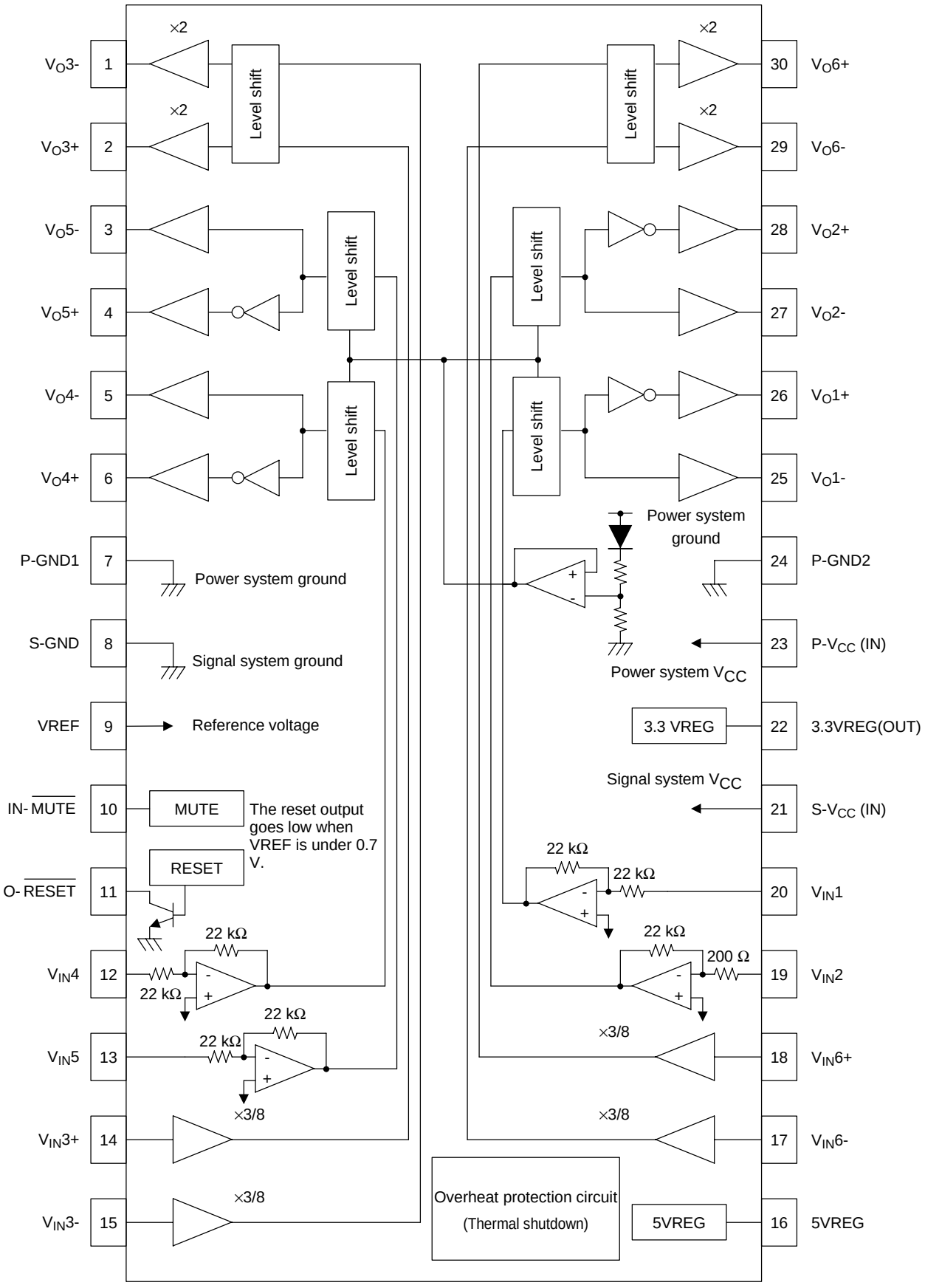
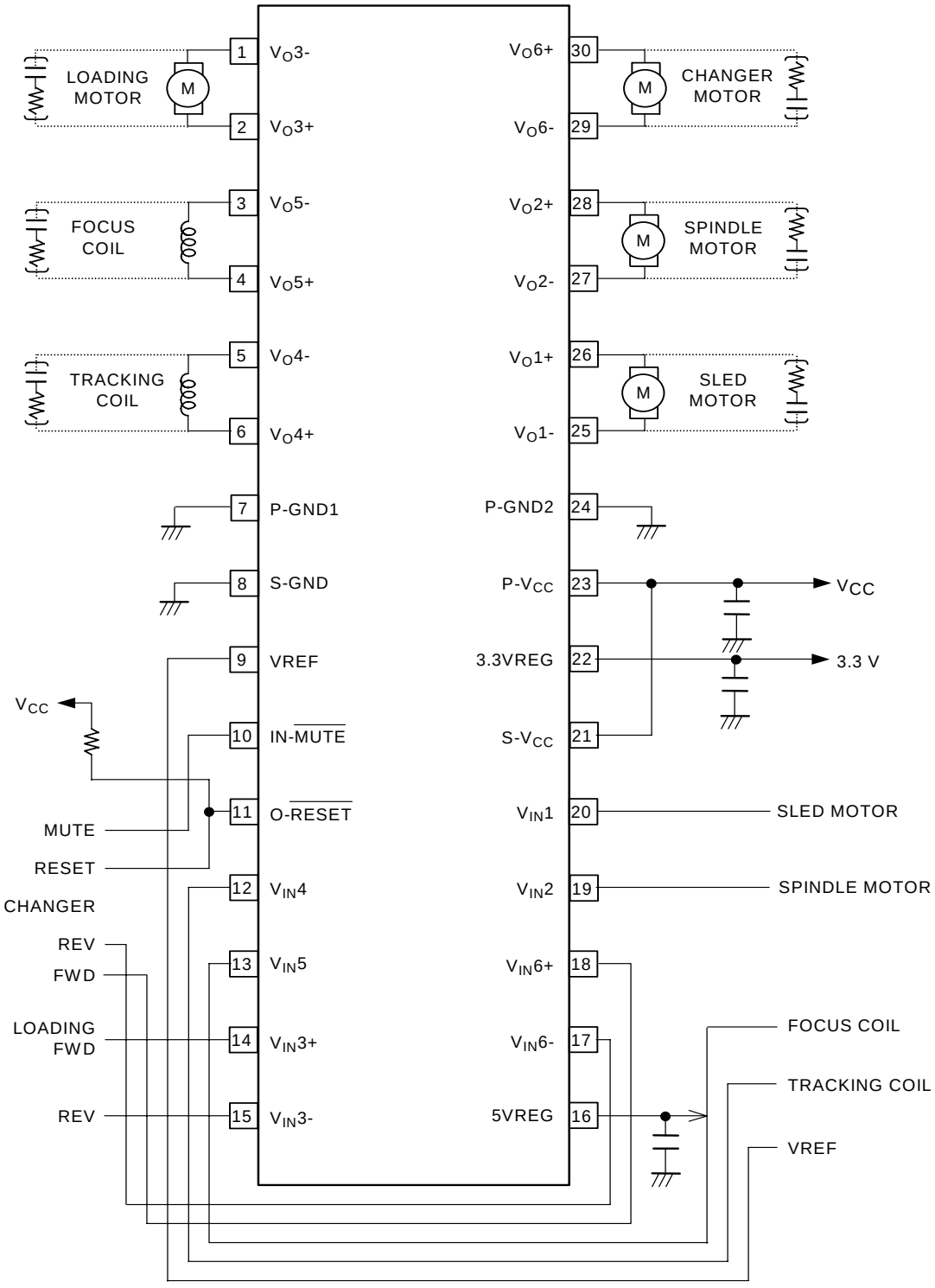
Pin No.	Symbol	Pin name	Pin description	Equivalent circuit
11	O-$\overline{\text{RESET}}$	Reset	Open-collector output	
15 14 17 18	$V_{IN}3-$ $V_{IN}3+$ $V_{IN}6-$ $V_{IN}6+$	Input (Loading block)	Inputs	
16	5VREG	5VREG	5 V regulator output	
22	3.3VREG	3.3VREG	3.3 V regulator output	

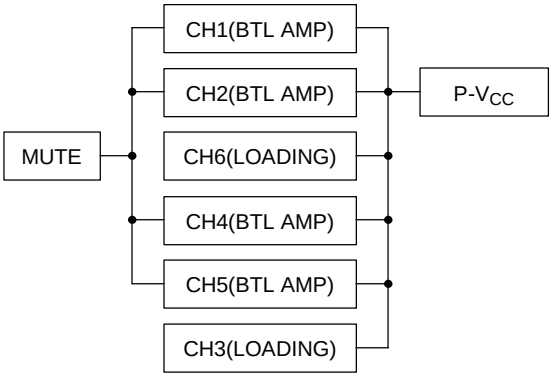
Block Diagram



Sample Application Circuit



Relationship Between Muting and the P-V_{CC} Power Supply



Note: • Connect both S-V_{CC} and P-V_{CC} to the power supply system externally.
• Connect both S-GND and P-GND to the ground system externally.

Muting Functions vs. Outputs and 3.3 V Regulator Operating States

	CH1, 2, 4, 5 (BTL-AMP)	CH3, 6 (LOADING)	3.3VREG 5VREG
When IN-$\overline{\text{MUTE}}$ is low	OFF	–	OFF
When the thermal shutdown circuit has operated	OFF	OFF	OFF
When VREF has fallen below 0.7 V	OFF	–	–

Note: • A dash (–) indicates no operation for functions to which muting, thermal shutdown, or VREF fall protection apply.
• The IN-$\overline{\text{MUTE}}$ pin applies to the BTL amplifiers (channels 1, 2, 4, and 5) and the 3.3 V and 5 V regulators.
• The VREF fall protection function only applies to the BTL amplifiers.

The muting function applies to the BTL amplifiers (channels 1, 2, 4, and 5) and the 3.3 V and 5 V regulators.

IN-$\overline{\text{MUTE}}$ state	BTL-AMP (CH1, 2, 4, 5)	3.3VREG 5 VREG
H	ON	
L	OFF	

The VREF fall protection function only applies to the BTL amplifiers.

VREF state	BTL-AMP (CH1, 2, 4, 5)
VREF > 0.7 (V)	ON
VREF < 0.7 (V)	OFF

Loading Block

V_{IN}*+ (FWD)	V_{IN}*– (REV)	Loading output
L	L	Brake
	H	Reverse (V_O = –1.5 × REV) *1
H	L	Forward (V_O = 1.5 × FWD) *1
	H	(V_O = 1.5 × (FWD – REV))

Note *1: FWD: V_{IN}6+, V_{IN}3+, REV: V_{IN}6–, V_{IN}3–

Note: • In brake mode, the + and - output voltages both go to V_{CC}/2.
• The "L" voltage level is any level less than VF (approximately 0.6 V).
• The loading circuit (channels 3 and 6) gain is 3.5 dB (typical).

Reset Function

IN-$\overline{\text{MUTE}}$	VREF	O-$\overline{\text{RESET}}$
L	VREF < 0.7 V	L
	VREF > 0.7 V	L
H	VREF < 0.7 V	L
	VREF > 0.7 V	H

Note: The O-$\overline{\text{RESET}}$ output is an open-collector output (NPN). The O-$\overline{\text{RESET}}$ low state is when the NPN transistor output is on, and the O-$\overline{\text{RESET}}$ high state is when the NPN transistor output is off.

Relationship Between the BTL Amplifier Inputs and Outputs