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LH51256

CMOS 256K (32K × 8) Static RAM

FEATURES

- 32,768 × 8 bit organization
- Access times:
  100/120 ns (MAX.)
- Power consumption:
  Operating: 248 mW (MAX.)
  (T_A = -40 to 85°C, minimum cycle)
  Standby: 16.5 µW (MAX.)
  (T_A = 0 to 60°C)
- Fully static operation
- TTL compatible I/O
- Three state outputs
- Single +5 V power supply
- Packages:
  28-pin, 600-mil DIP
  28-pin, 450-mil SOP

DESCRIPTION

The LH51256 is a 256K bit static RAM organized as 32,768×8 bits. It is fabricated using silicon-gate CMOS process technology.

PIN CONNECTIONS

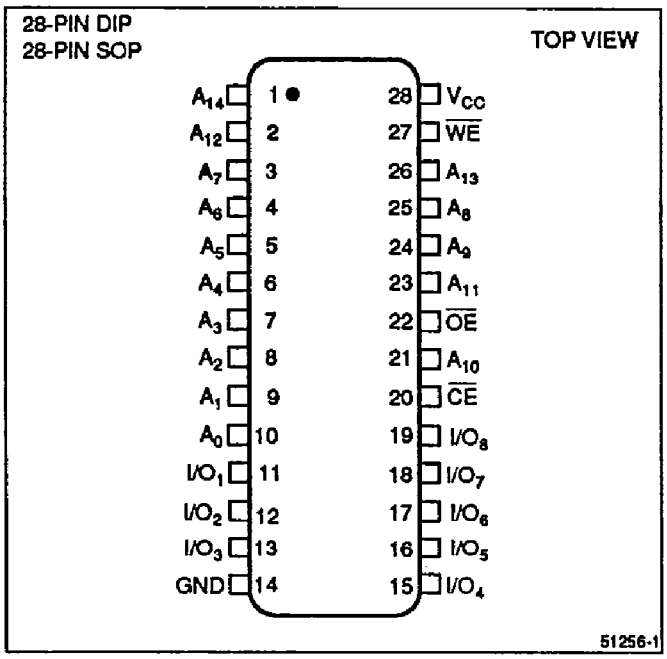

Figure 1. Pin Connections for DIP and SOP Packages

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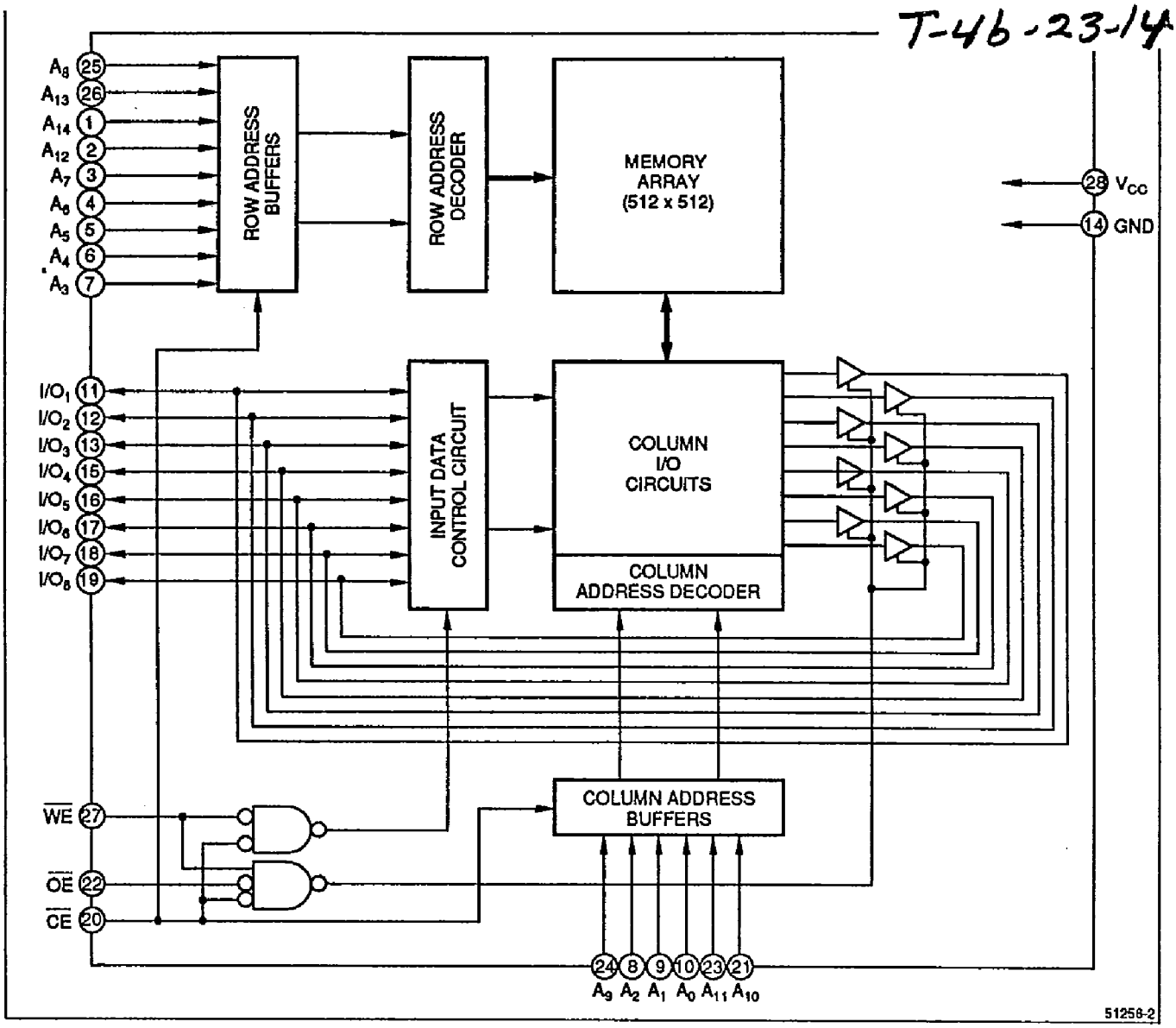

Figure 2. LH51256 Block Diagram

PIN DESCRIPTION

SIGNAL	PIN NAME
A_0 - A_{14}	Address input
$\overline{CE}$	Chip Enable input
$\overline{WE}$	Write Enable input
$\overline{OE}$	Output Enable input

SIGNAL	PIN NAME
I/O_1 - I/O_8	Data I/O
Vcc	Power supply
GND	Ground

TRUTH TABLE

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	MODE	I/O_1 - I/O_8	Icc	NOTE
H	X	X	Non selected	High-Z	Standby (I_{SB})	1
L	L	X	Write	Data in	Operating (Icc)	1
L	H	L	Read	Data out	Operating (Icc)	
L	H	H	Output disable	High-Z	Operating (Icc)	

NOTE:
1. X = H or L

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT	NOTE
Supply voltage	V_{CC}	-0.3 to +7.0	V	1
Input voltage	V_{IN}	-0.3 to +7.0	V	1
Operating temperature	Topr	-40 to +85	°C	
Storage temperature	Tstg	-55 to +150	°C	

NOTES:
1. The maximum applicable voltage on any pin with respect to GND.

RECOMMENDED OPERATING CONDITIONS (T_A = -40 to + 85°C)

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC} +0.3	V
	V_{IL}	-0.3		0.8	V

DC CHARACTERISTICS (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C unless otherwise noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input leakage current	$\lvert I_{LI} \rvert$	V_{CC} = 5.5V, V_{IN} = 0 to V_{CC}			1	µA
Output leakage current	$\lvert I_{LO} \rvert$	$\overline{CE}$ or $\overline{OE}$ = V_{IH}, $V_{I/O}$ = 0 to V_{CC}			1	µA
Operating current	I_{CC}	$\overline{CE}$ = V_{IL}, Outputs open			45	mA
Standby current	I_{SB1}	$\overline{CE}$ = V_{IH}			10	mA
	I_{SB}	$\overline{CE}$ ≥ V_{CC} - 0.2 V, T_A = 0 to +60°C			3	µA
		$\overline{CE}$ ≥ V_{CC} - 0.2 V, T_A = -40 to +85°C			10	µA
Output voltage	V_{OL}	I_{OL} = 2.1 mA			0.4	V
	V_{OH}	I_{OH} = -1.0 mA	2.4			V

AC CHARACTERISTICS

(1) READ CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

PARAMETER	SYMBOL	LH51256/N-10		LH51256/N-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Read cycle time	t_{RC}	100		120		ns	
Address access time	t_{AA}		100		120	ns	
$\overline{CE}$ access time	t_{ACE}		100		120	ns	
Output enable time	t_{OE}		50		60	ns	
Output hold time	t_{OH}	5		5		ns	
$\overline{CE}$ Low to output in Low-Z	t_{LZ}	5		5		ns	1
$\overline{OE}$ Low to output in Low-Z	t_{OLZ}	5		5		ns	1
$\overline{CE}$ High to output in High-Z	t_{HZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

NOTE:
1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

2) WRITE CYCLE (V_{CC} = 5 V ± 10%, T_A = -40 to +85°C)

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PARAMETER	SYMBOL	LH51256/N-10		LH51256/N-12		UNIT	NOTE
		MIN.	MAX.	MIN.	MAX.		
Write cycle time	t_{WC}	100		120		ns	
$\overline{CE}$ Low to end of write	t_{CW}	90		100		ns	
Address valid to end of write	t_{AW}	90		100		ns	
Address setup time	t_{AS}	5		5		ns	
Write recovery time	t_{WR}	15		15		ns	
Write pulse width	t_{WP}	50		50		ns	
Input data setup time	t_{DW}	30		30		ns	
Input data hold time	t_{DH}	10		10		ns	
$\overline{WE}$ High to output active	t_{OW}	0		0		ns	1
$\overline{WE}$ Low to output in High-Z	t_{WZ}	0	30	0	30	ns	1
$\overline{OE}$ High to output in High-Z	t_{OHZ}	0	30	0	30	ns	1

NOTE:

1. Active output to high-impedance and high-impedance to output active tests specified for a ±500 mV transition from steady state levels into the test load. C_{LOAD} = 5 pF.

AC TEST CONDITIONS

PARAMETER	MODE
Input voltage amplitude	0.6V to 2.4 V
Input rise/fall time	10 ns
Timing reference level	1.5 V
Output load conditions	1TTL + C_L = 100 pF (Includes scope and jig capacitance)

CAPACITANCE [1] (T_A = 25°C, f = 1MHz)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_{IN}	V_{IN} = 0 V			7	pF
Input/output capacitance	$C_{I/O}$	$V_{I/O}$ = 0 V			10	pF

NOTE:

1. This parameter is sampled and not production tested.

DATA RETENTION CHARACTERISTICS (T_A = -40 to +85°C except as noted)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Data retention voltage	V_{CCDR}	$\overline{CE} \geq V_{CCDR}$ - 0.2V	2.0			V	
Data retention current	I_{CCDR}	V_{CCDR} = 3 V $\overline{CE} \geq V_{CCDR}$ - 0.2V, T_A = 0 to +60°C, V_{IN} = 0 to V_{CCDR}			1	µA	
		V_{CCDR} = 3 V $\overline{CE} \geq V_{CCDR}$ - 0.2V, T_A = -40 to +85°C, V_{IN} = 0 to V_{CCDR}			6	µA	
$\overline{CE}$ setup time	t_{CDR}		0			ns	
$\overline{CE}$ hold time	t_R		t_{RC}			ns	1

NOTE:

1. t_{RC} = Read cycle time

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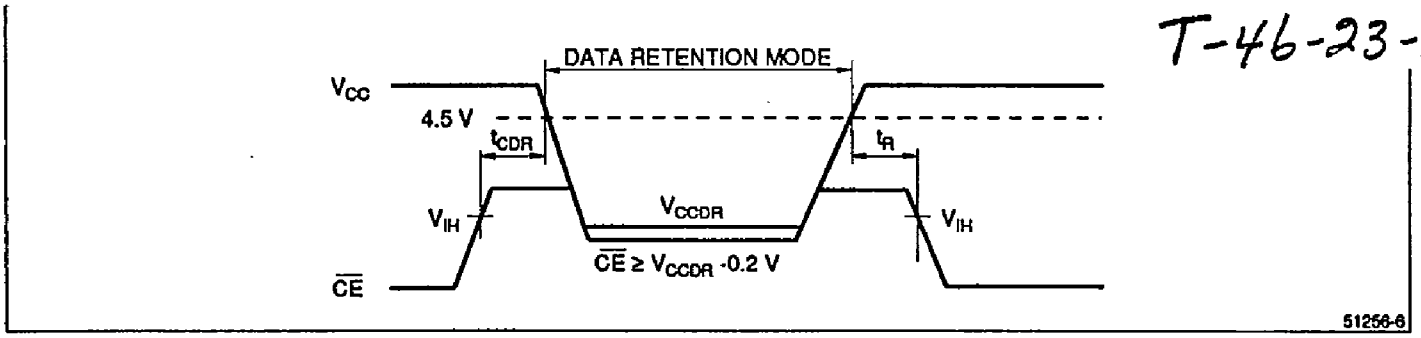


Figure 3. Low Voltage Data Retention

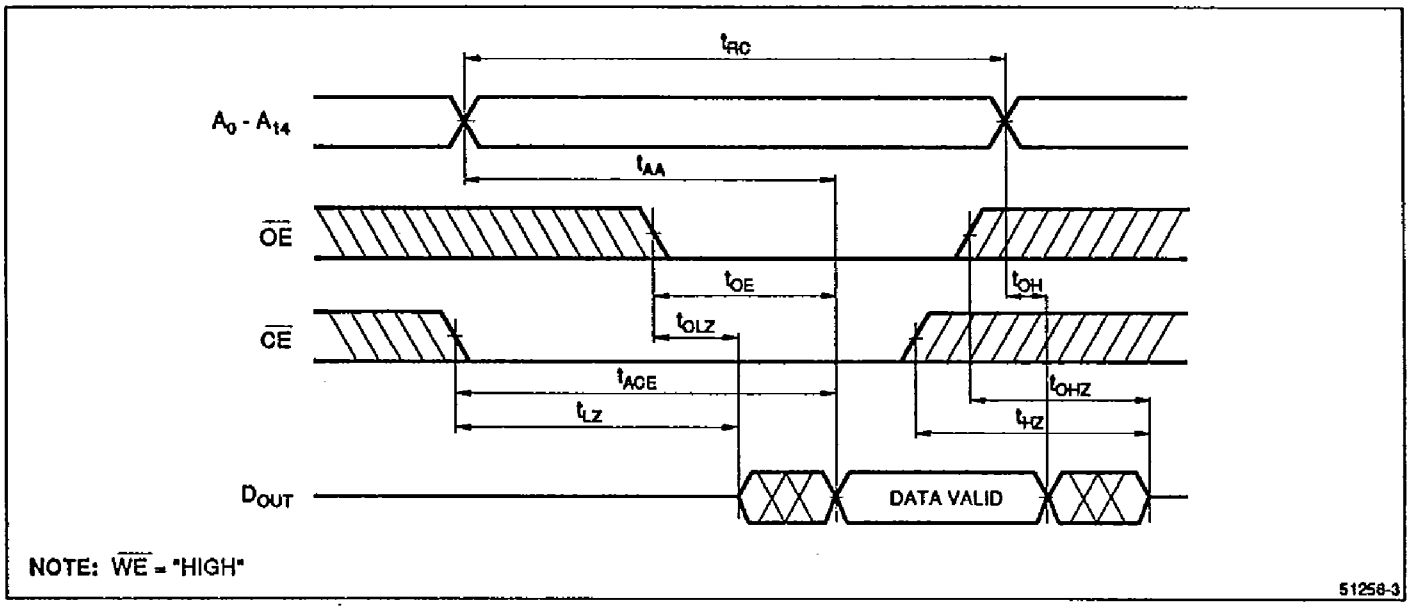
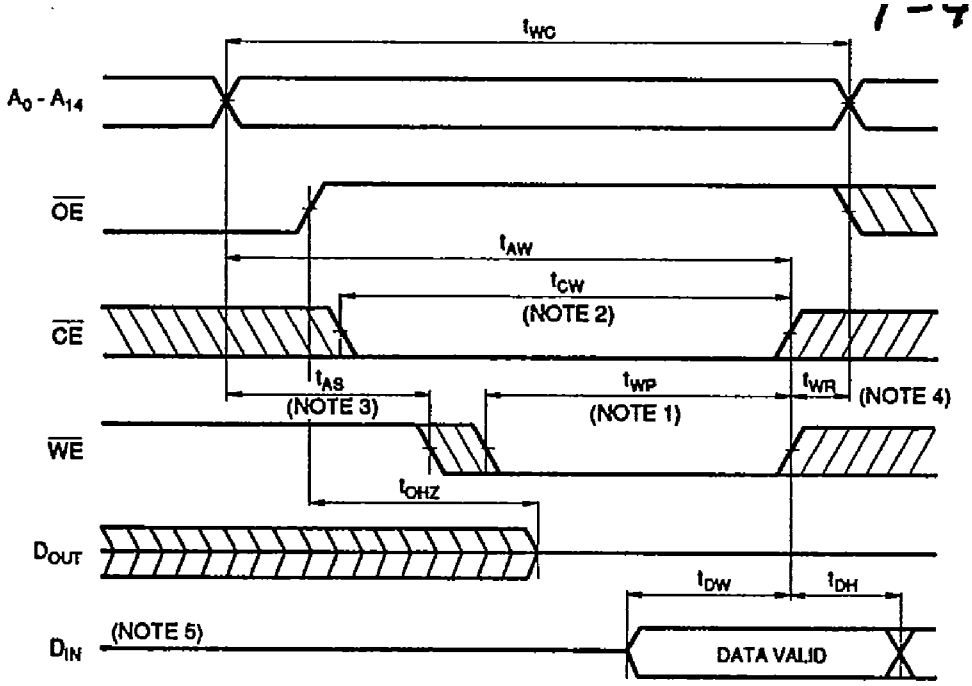


Figure 4. Read Cycle



NOTES:

1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from the $\overline{CE}$ low transition to the end of write.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.

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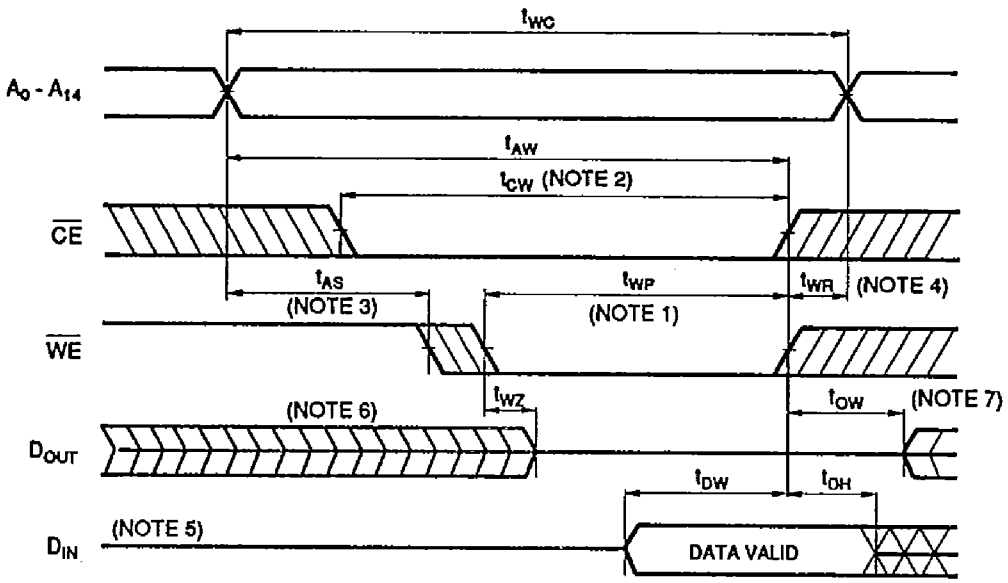
Figure 5. Write Cycle 1 ($\overline{OE}$ Clock)



NOTES:

1. The write pulse occurs during the overlap (t_{WP}) of $\overline{CE}$ = LOW and $\overline{WE}$ = LOW.
2. t_{CW} is defined as the time from the $\overline{CE}$ low transition to the end of write.
3. t_{AS} is defined as the time from address change to the start of writing.
4. t_{WR} is defined as the time from the end of writing to the address change.
5. When the I/O pins are in the output state, input signals with the opposite logic level must not be applied.
6. If $\overline{CE}$ LOW transition occurs at the same time or after $\overline{WE}$ LOW transition, the output will remain high-impedance.
7. If $\overline{CE}$ HIGH transition occurs at the same time or prior to the $\overline{WE}$ HIGH transition, the output will remain high-impedance.

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Figure 6. Write Cycle 2 ($\overline{OE}$ Low)

ORDERING INFORMATION

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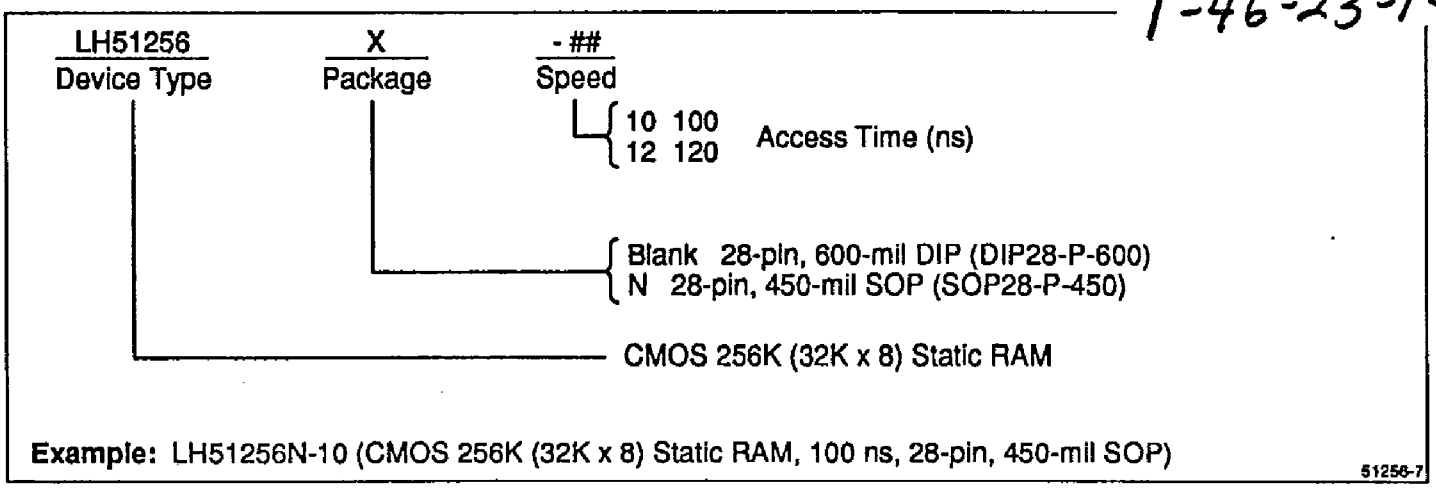

Example: LH51256N-10 (CMOS 256K (32K x 8) Static RAM, 100 ns, 28-pin, 450-mil SOP)

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