

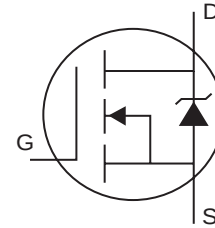
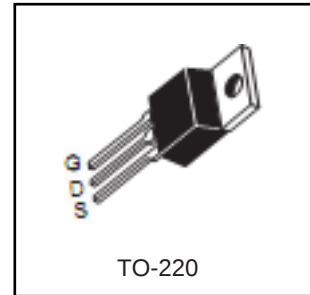
55V N-Channel Mode MOSFET

$V_{DS}=55V$

$R_{DS(ON)}, V_{GS}@10V, I_{DS}@25A = 17.5m\Omega$

- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

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Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	49	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	35	
I_{DM}	Pulsed Drain Current ①	160	
$P_D @ T_C = 25^\circ C$	Power Dissipation	94	W
	Linear Derating Factor	0.63	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
I_{AR}	Avalanche Current①	25	A
E_{AR}	Repetitive Avalanche Energy①	9.4	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw	10 lbf•in (1.1N•m)	

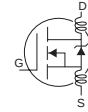
Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.5	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	62	

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Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.058	—	V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	—	17.5	m Ω	$V_{GS} = 10V, I_D = 25A$ ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance	19	—	—	S	$V_{DS} = 25V, I_D = 25A$ ④
I_{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	$V_{DS} = 55V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 44V, V_{GS} = 0V, T_J = 150^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-100		$V_{GS} = -20V$
Q_g	Total Gate Charge	—	—	63	nC	$I_D = 25A$
Q_{gs}	Gate-to-Source Charge	—	—	14		$V_{DS} = 44V$
Q_{gd}	Gate-to-Drain ("Miller") Charge	—	—	23		$V_{GS} = 10V$, See Fig. 6 and 13
$t_{d(on)}$	Turn-On Delay Time	—	12	—	ns	$V_{DD} = 28V$
t_r	Rise Time	—	60	—		$I_D = 25A$
$t_{d(off)}$	Turn-Off Delay Time	—	44	—		$R_G = 12\Omega$
t_f	Fall Time	—	45	—		$V_{GS} = 10V$, See Fig. 10 ④
L_D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	—	7.5	—		
C_{iss}	Input Capacitance	—	1470	—	pF	$V_{GS} = 0V$
C_{oss}	Output Capacitance	—	360	—		$V_{DS} = 25V$
C_{rss}	Reverse Transfer Capacitance	—	88	—		$f = 1.0MHz$, See Fig. 5
E_{AS}	Single Pulse Avalanche Energy②	—	530⑤	150⑥	mJ	$I_{AS} = 25A, L = 0.47mH$



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	—	—	49	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode)①	—	—	160		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 25A, V_{GS} = 0V$ ④
t_{rr}	Reverse Recovery Time	—	63	95	ns	$T_J = 25^\circ\text{C}, I_F = 25A$
Q_{rr}	Reverse Recovery Charge	—	170	260	nC	$di/dt = 100A/\mu s$ ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting $T_J = 25^\circ\text{C}$, $L = 0.48mH$
 $R_G = 25\Omega$, $I_{AS} = 25A$. (See Figure 12)

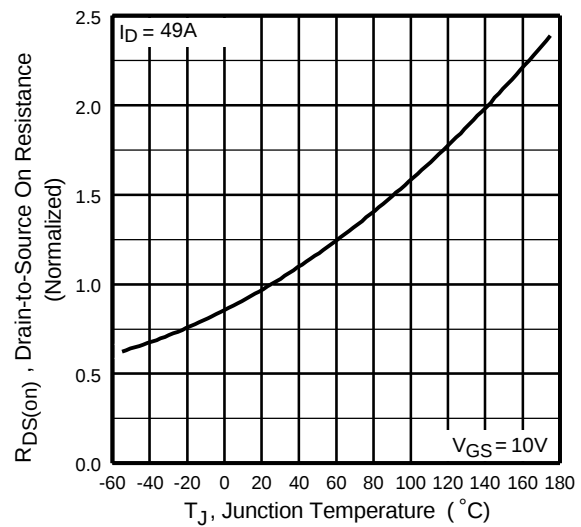
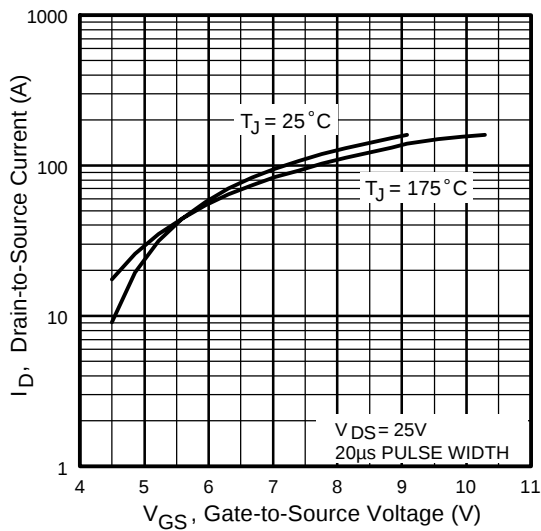
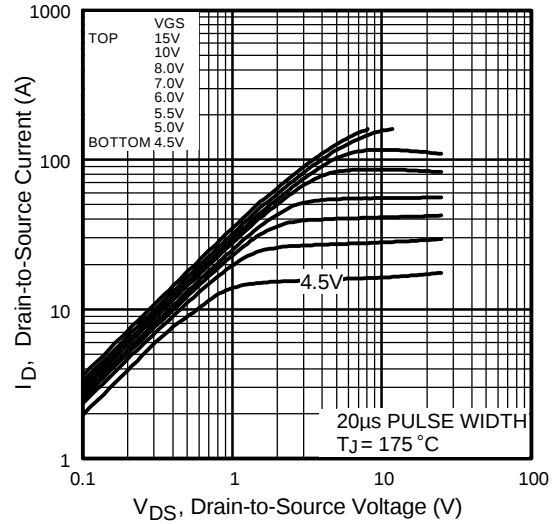
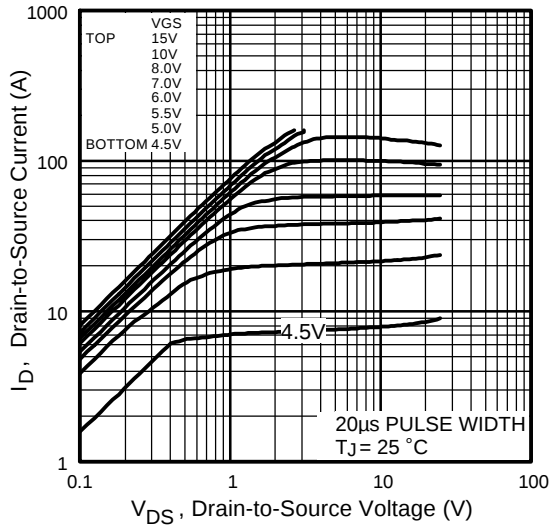
③ $I_{SD} \leq 25A$, $di/dt \leq 230A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$,
 $T_J \leq 175^\circ\text{C}$

④ Pulse width $\leq 400\mu s$; duty cycle $\leq 2\%$.

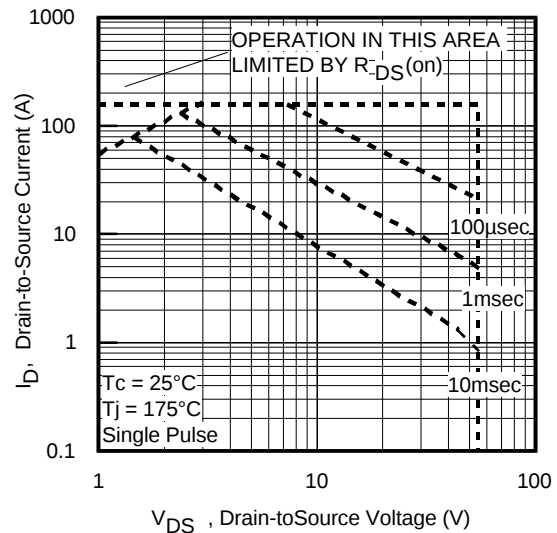
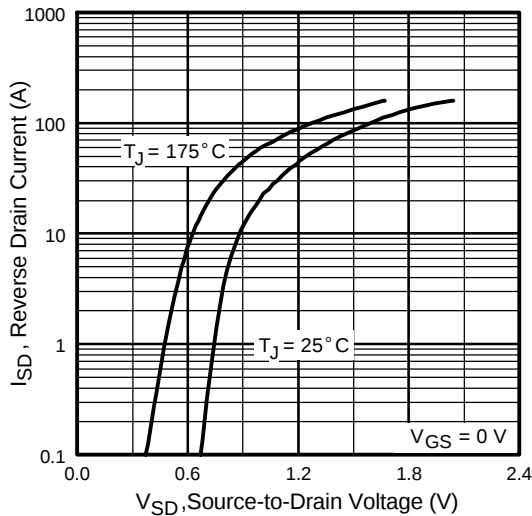
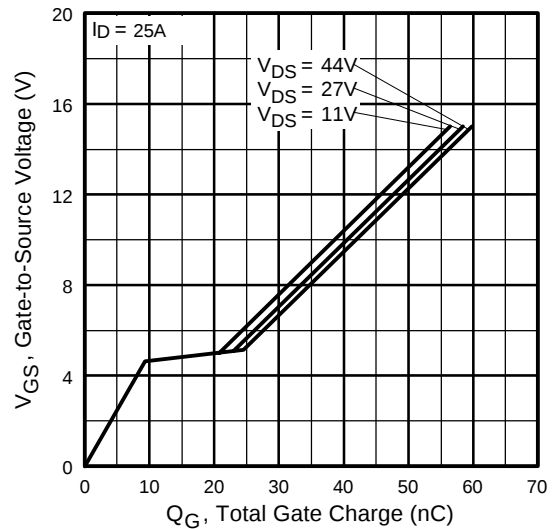
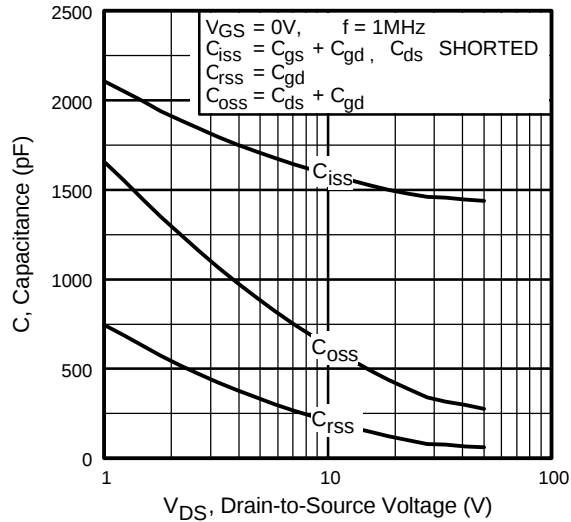
⑤ This is a typical value at device destruction and represents operation outside rated limits.

⑥ This is a calculated value limited to $T_J = 175^\circ\text{C}$.

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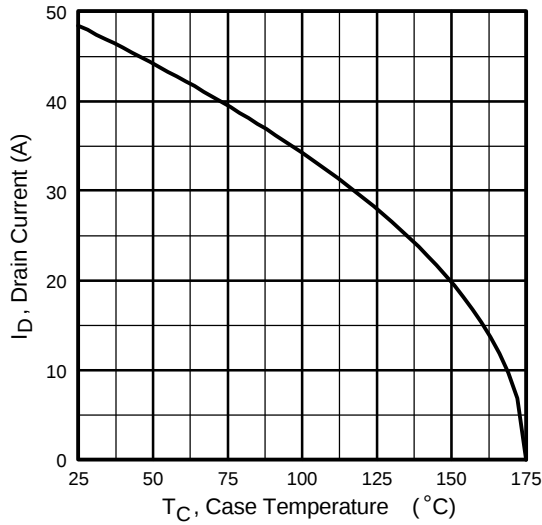


Fig 9. Maximum Drain Current Vs. Case Temperature

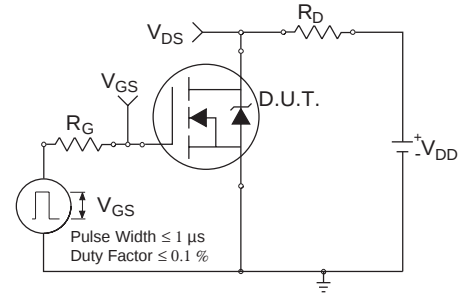


Fig 10a. Switching Time Test Circuit

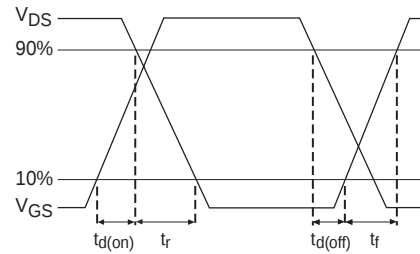


Fig 10b. Switching Time Waveforms

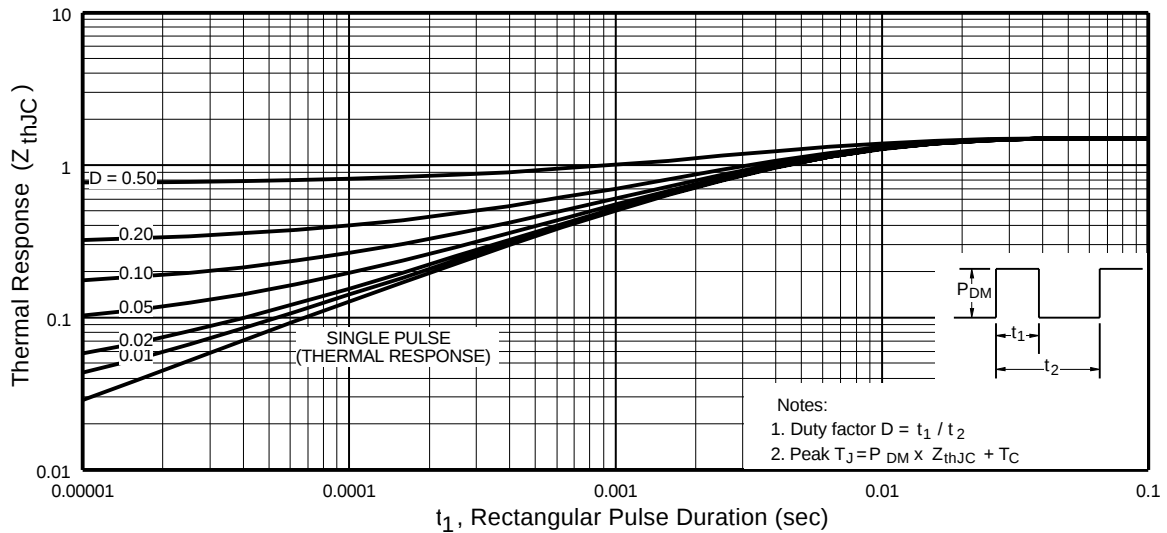


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

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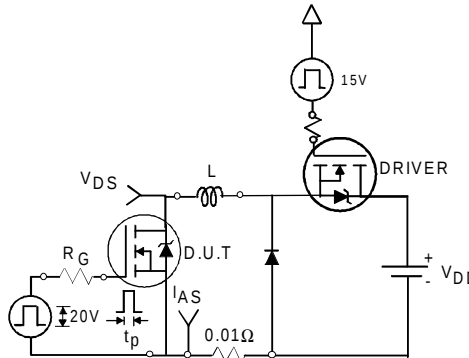


Fig 12a. Unclamped Inductive Test Circuit

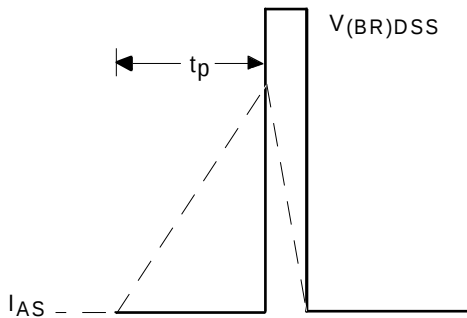


Fig 12b. Unclamped Inductive Waveforms

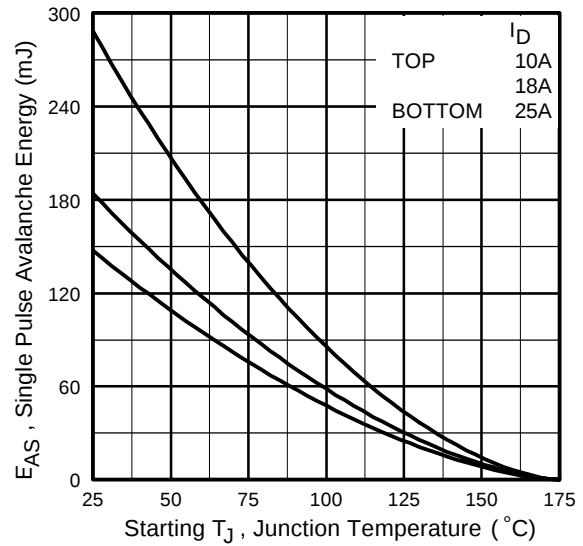


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

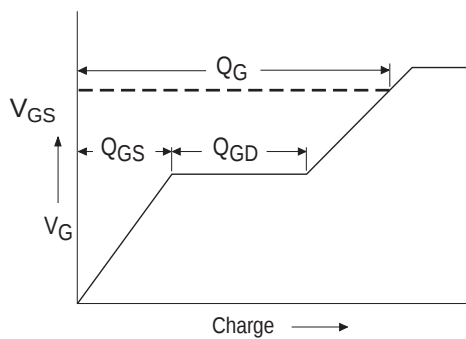


Fig 13a. Basic Gate Charge Waveform

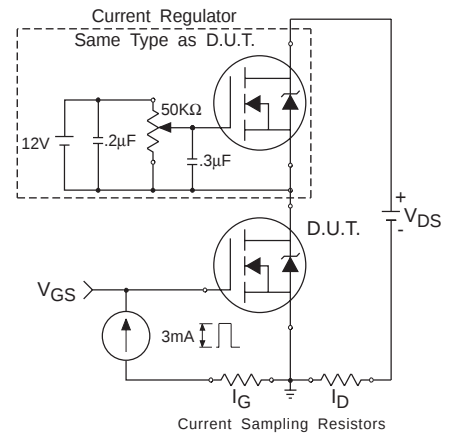
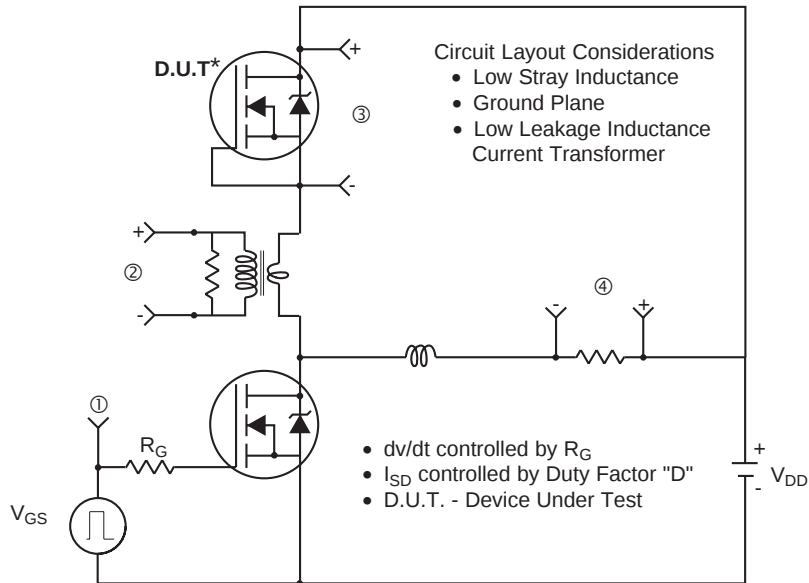


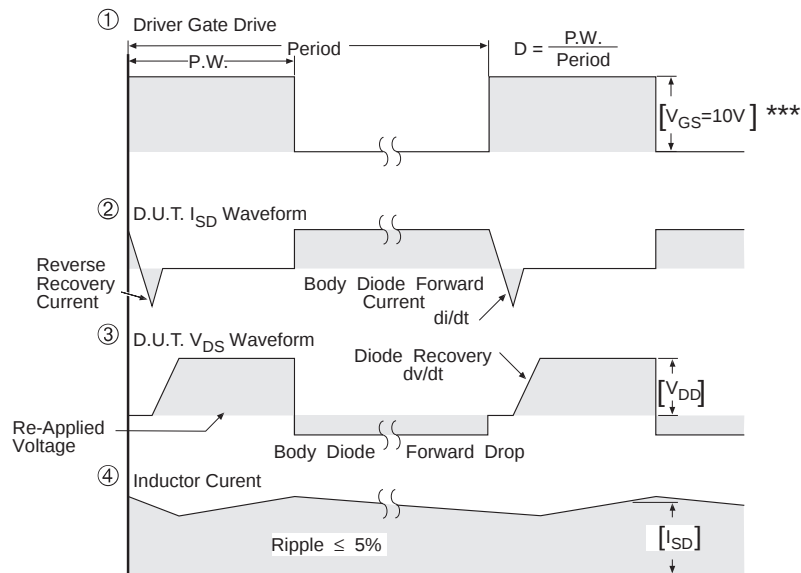
Fig 13b. Gate Charge Test Circuit

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Peak Diode Recovery dv/dt Test Circuit



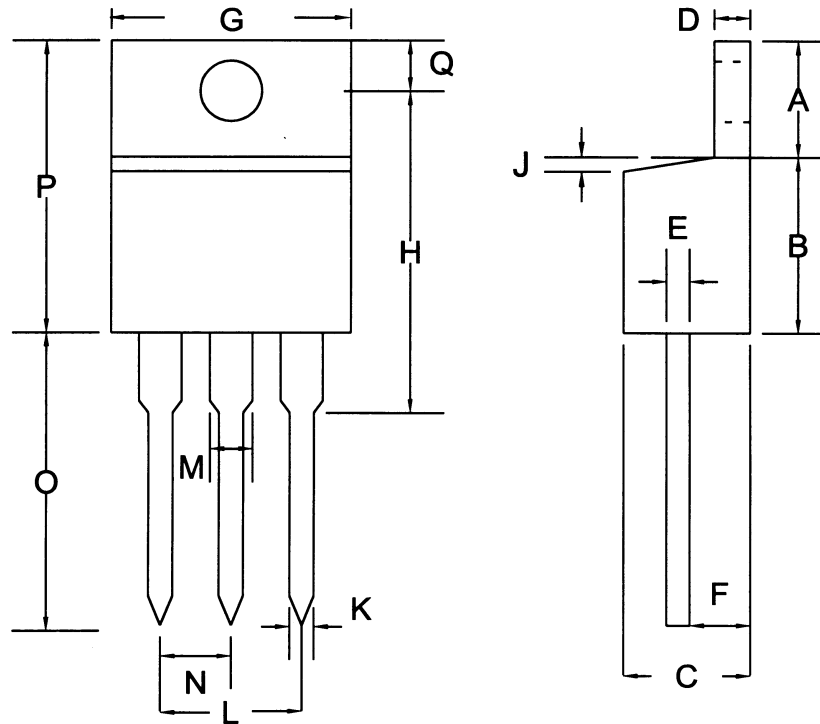
* Reverse Polarity of D.U.T for P-Channel



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

Fig 14. For N-channel power MOSFETs

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Symbol	Dimensions In Millimeters			Dimensions In Inches		
	Min	Nom	Max	Min	Nom	Max
A	5.58	6.54	7.49	0.220	0.257	0.295
B	8.38	8.64	8.90	0.330	0.340	0.350
C	4.07	4.45	4.82	0.160	0.175	0.190
D	1.15	1.27	1.39	0.045	0.050	0.055
E	0.35	0.45	0.60	0.014	0.018	0.024
F	2.04	2.42	2.79	0.080	0.095	0.110
G	9.66	9.97	10.28	0.380	0.393	0.405
H	—	16.25	—	—	0.640	—
I	3.68	3.83	3.98	0.145	0.151	0.157
J	—	—	1.27	—	—	0.050
K	0.75	0.85	0.95	0.030	0.033	0.037
L	4.83	5.08	5.33	0.190	0.200	0.210
M	1.15	1.33	1.52	0.045	0.052	0.060
N	2.42	2.54	2.66	0.095	0.100	0.105
O	12.70	13.48	14.27	0.500	0.531	0.562
P	14.48	15.17	15.87	0.570	0.597	0.625
Q	2.54	2.79	3.04	0.100	0.110	0.120