National Semiconductor

PRELIMINARY
November 10, 2008

LMH6517
Multi Standard, IF and Baseband, Dual, DVGA

General Description

The LMH6517 contains two high performance digitally controlled variable gain amplifiers (DVGA). It has been designed for use in narrowband and broadband IF sampling applications. Typically the LMH6517 drives a high performance ADC in a broad range of mixed signal and digital communication applications such as mobile radio and cellular base stations where automatic gain control (AGC) is required to increase system dynamic range.

Each channel of LMH6517 has an independent digitally controlled attenuator and a high linearity, differential output amplifier. Each block has been optimized for low distortion and maximum system design flexibility. Each channel can be individually disabled for power savings.

The LMH6517 digitally controlled attenuator provides precise 0.5 dB gain steps over a 31.5 dB range. On chip digital latches are provided for local storage of the gain setting. Both serial and parallel programming options are provided. A Pulse mode is also offered where simple up or down commands can change the gain one step at a time.

The output amplifier has a differential output allowing large signal swings on a single 5V supply. The low impedance output provides maximum flexibility when driving filters or analog to digital converters.

The LMH6517 operates over the industrial temperature range of −40°C to +85°C. The LMH6517 is available in a 32-Pin, thermally enhanced, LLP package.

Features

- Accurate, 0.5dB gain steps
- 200Ω Resistive, differential input
- Low impedance, differential output
- Disable function for each channel
- Parallel or serial gain control
- SPI compatible serial bus
- On chip register stores gain setting
- Low sensitivity of linearity and phase to gain setting
- Single 5V supply voltage
- Small footprint LLP package

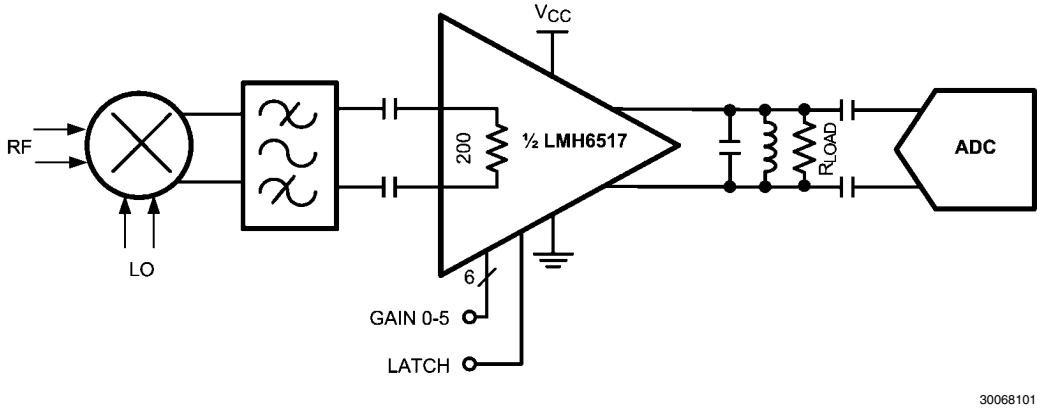
Key Specifications

- Gain step size of 0.5 dB
- Operating frequency Range of 1200 MHz
- OIP3: 47 dBm @ 100 MHz
- Noise figure 6 dB
- Gain step accuracy: 0.15 dB
- Supply current 80 mA per channel

Applications

- Cellular base stations
- IF sampling receivers
- Instrumentation
- Modems
- Imaging

Typical Application



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Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

ESD Tolerance (Note 2)	
Human Body Model	2 kV
Machine Model	200V
Positive Supply Voltage (Pin 3)	−0.6V to 5.5V
Output Voltage (Pin 14,15)	
Differential Voltage between Any Two Grounds	<200 mV
Analog Input Voltage Range	−0.6V to V_{CC}
Digital Input Voltage Range	−0.6V to 3.6V
Output Short Circuit Duration (one pin to ground)	Infinite
Junction Temperature	+150°C
Storage Temperature Range	−65°C to +150°C
Soldering Information	
Infrared or Convection (20 sec)	235°C
Wave Soldering (10 sec)	260°C

Operating Ratings (Note 1)

Supply Voltage (Pin 3)	3.15V to 5.25V
Output Voltage Range	
Differential Voltage Between Any Two Grounds	<10 mV
Analog Input Voltage Range, AC Coupled	
Temperature Range (Note 3)	−40°C to +85°C
Package Thermal Resistance (θ_{JA})	
32-Pin LLP	32°C/W

5V Electrical Characteristics (Note 4)

The following specifications apply for single supply with V_{CC} = 5V, Maximum Gain , R_L = 100Ω, V_{OUT} = 2 V_{PP}, fin = 150 MHz. Boldface limits apply at temperature extremes.

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
Dynamic Performance						
SSBW	Frequency Range			1200		MHz
	Maximum Gain		21.85 **21.8**	22	22.15 **22.2**	dB
	Input Noise Voltage	Maximum Gain, f > 1 MHz, R_{IN} = 0Ω		1.1		$nV/\sqrt{Hz}$
	Output Noise Voltage	Maximum Gain, f > 1 MHz		22		$nV/\sqrt{Hz}$
	Noise Figure	Maximum Gain		6		dB
OIP3	Output Third Order Intercept Point	f = 100 MHz, V_{OUT} = 1 dBm per tone	43	47		dBm
	Output Third Order Intercept Point	f = 200 MHz, V_{OUT} = 1 dBm per tone	40	45		
Analog I/O						
	Input Resistance	Differential	195	210	230	Ω
	Input Capacitance			2		pF
	Input Common Mode Voltage	Self Biased	2.48 **2.4**	2.5	2.52 **2.6**	V
	Input Common Mode Voltage Range	Externally Driven	1.5		3.5	V
	Maximum Input Voltage Swing	Volts peak to peak, differential		5.5		V
	Output Common Mode Voltage	Self Biased	2.4	2.5	2.6	V
	Maximum Output Voltage Swing			5		V
V_{OS}	Output Offset Voltage	All Gain Settings	−5 **−10**	0.5	5 **10**	mV
CMRR	Common Mode Rejection Ratio	Maximum Gain, f = 100 MHz		60		dB
PSRR	Power Supply Rejection Ratio	Maximum Gain, f = 100 MHz		60		dB
XTLK	Channel to Channel Crosstalk	Maximum Gain, f = 100 MHz		−60		dB
XTLK	Channel to Channel Crosstalk	Maximum Gain, f = 300 MHz		−50		dB
Gain Parameters						
	Maximum Gain	Gain Code 000000	21.85 **21.8**	22	22.15 **22.2**	dB
	Minimum Gain	Gain Code 111111	−9.3 **−9.2**	−9.5	−9.7 **−9.8**	dB

Symbol	Parameter	Conditions	Min (Note 6)	Typ (Note 5)	Max (Note 6)	Units
	Gain Adjust Range			31.5		dB
	Gain Step Size			0.5		dB
	Gain Step Error	Any two steps	−0.3	±0.05	0.3	dB
	Gain Step Error	Maximum Gain to Maximum Gain −12 dB	−0.2	±0.05	0.2	dB
	Gain Step Phase Shift	Between any two steps	−2	0.5	2	deg
	Gain Step Switching Time	Differential		15		ns
Digital Inputs/Timing						
	Logic Compatibility	TTL, 2.5V CMOS, 3.3V CMOS				
VIL	Logic Input Low Voltage		0		0.4	V
VIH	Logic Input High Voltage		2.0		3.6	V
IIH	Logic Input High Input Current	Digital Input Voltage = 3.3V	−100		100	µA
IIL	Logic Input Low Input Current	Digital Input Voltage = 0V	−100		100	
TSU	Setup Time			5		ns
THOLD	Hold Time			5		ns
TPW	Minimum Latch Pulse Width			10		ns
Power Requirements						
ICC	Supply Current	Each channel,	70	80	91	mA

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is intended to be functional, but specific performance is not guaranteed. For guaranteed specifications, see the Electrical Characteristics tables.

Note 2: Human Body Model, applicable std. MIL-STD-883, Method 3015.7. Machine Model, applicable std. JESD22-A115-A (ESD MM std. of JEDEC)

Field-Induced Charge-Device Model, applicable std. JESD22-C101-C (ESD FICDM std. of JEDEC).

Note 3: The maximum power dissipation is a function of $T_{J(MAX)}$, θ_{JA}. The maximum allowable power dissipation at any ambient temperature is $P_D = (T_{J(MAX)} - T_A)/ \theta_{JA}$. All numbers apply for packages soldered directly onto a PC Board.

Note 4: Electrical Table values apply only for factory testing conditions at the temperature indicated. No guarantee of parametric performance is indicated in the electrical tables under conditions different than those tested

Note 5: Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

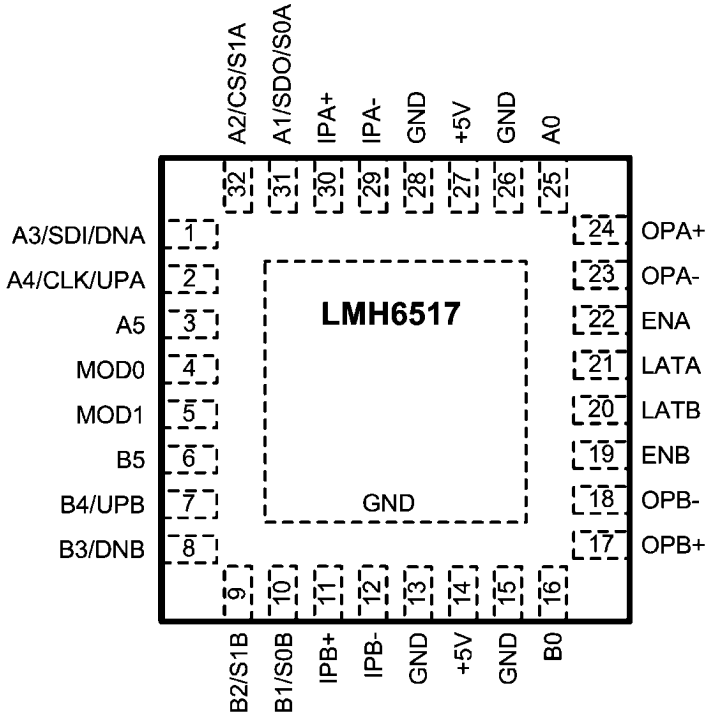
Note 6: Limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods.

Note 7: Negative input current implies current flowing out of the device.

Note 8: Drift determined by dividing the change in parameter at temperature extremes by the total temperature change.

Connection Diagram

32-Pin LLP



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Top View

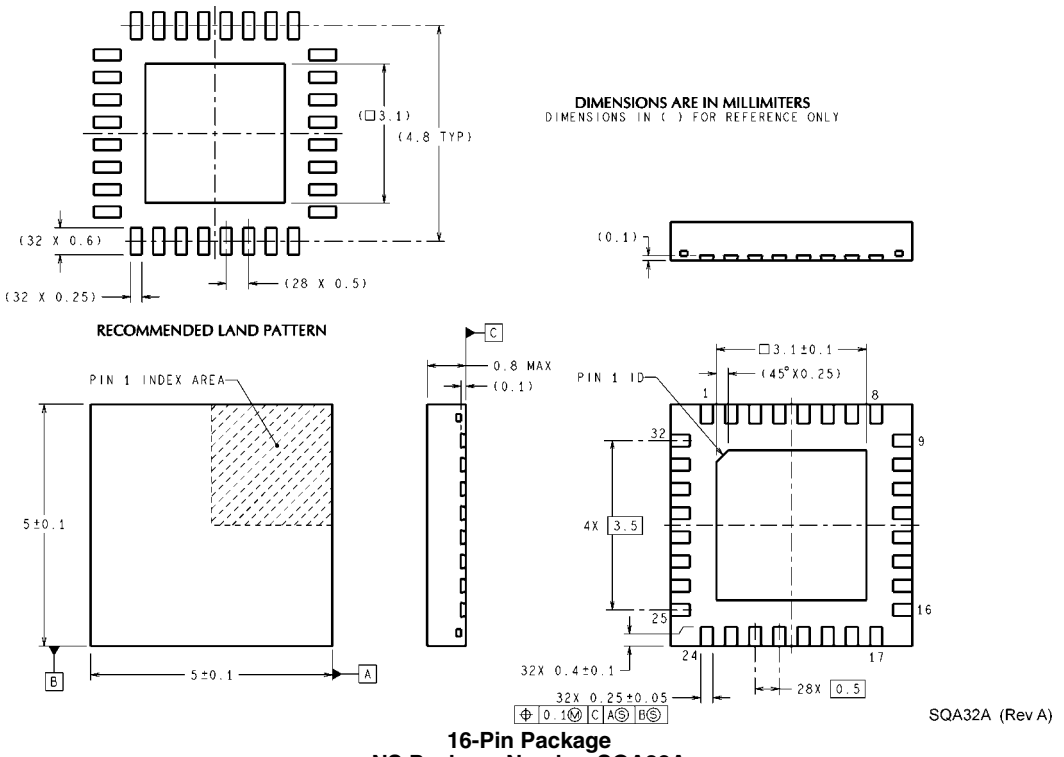
Ordering Information

Package	Part Number	Package Marking	Transport Media	NSC Drawing
32-Pin LLP	LMH6517SQ	L6517SQ	1k Units Tape and Reel	SQA32A
	LMH6517SQE		250 Units Tape and Reel	
	LMH6517SQX		4.5k Units Tape and Reel	

Pin Descriptions

Pin Number	Symbol	Description
Analog I/O		
30, 11	IPA+, IPB+	Amplifier non—inverting input. Internally biased to mid supply. Input voltage should not exceed V_{CC} or go below GND by more than 0.5V.
29, 12	IPA–, IPB–	Amplifier inverting input. Internally biased to mid supply. Input voltage should not exceed V_{CC} or go below GND by more than 0.5V.
24, 17	OPA+, OPB+	Amplifier non—inverting output. Internally biased to mid supply.
23, 18	OPA–, OPB–	Amplifier inverting output. Internally biased to mid supply.
Power		
13, 15, 26, 28, center pad	GND	Ground pins. Connect to low impedance ground plane. All pin voltages are specified with respect to the voltage on these pins. The exposed thermal pad is the primary ground connection.
14, 27	+5V	Power supply pins. Valid power supply range is 3V to 5.5V.
Common Control Pins		
4, 5	MOD0, MOD1	Digital Mode control pins. These pins float to the logic hi state if left unconnected. See below for Mode settings.
22, 19	ENA, ENB	Enable pins. Logic 1 = enabled state. See application section for operation in serial mode.
Digital Inputs Parallel Mode (MOD1 = 1, MOD0 = 1)		
25, 16	A0, B0	Gain bit zero = 0.5 dB step. Gain steps down from maximum gain (000000 = Maximum Gain)
31, 10	A1, B1	Gain bit one = 1 dB step
32, 9	A2, B2	Gain bit two = 2 dB step
1, 8	A3, B3	Gain bit three = 4 dB step
2, 7	A4, B4	Gain bit four = 8 dB step
3, 6	A5, B5	Gain bit five = 16 dB step
21, 20	LATA, LATB	Latch pins. Logic zero = active, logic 1 = latched. Gain will not change once latch is high. Connect to ground if the latch function is not desired.
Digital Inputs Serial Mode		
2	CLK	Serial Clock
1	SDI	Serial Data In (SPI Compatible) See application section for more details.
32	CS	Serial Chip Select (SPI compatible)
31	SDO	Serial Data Out (SPI compatible)
3, 4, 6 — 10, 15, 16, 20, 21, 25, 26	GND	Pins unused in Serial Mode, connect to DC ground.
Digital Inputs Pulse Mode		
2, 7	UPA, UPB	Up pulse pin. A logic 1 pulse will increase gain one step.
1, 8	DNA, DNB	Down pulse pin. A logic 1 pulse will decrease gain one step.
1 & 2 or 7 & 8		Pulsing both pins together will reset the gain to maximum gain.
31, 32	S0A, S1A	Step size zero and step size 1. (0,0) = 0.5 dB; (0, 1) = 1 dB; (1, 0) = 2 dB, and (1, 1) = 6 dB
10, 9	S0B, S1B	Step size zero and step size 1. (0,0) = 0.5 dB; (0, 1) = 1 dB; (1,0) = 2 dB, and (1, 1) = 6 dB
3, 5, 6, 13, 15, 16, 25, 26	GND	Pins unused in Pulse Mode, connect to DC ground.

Physical Dimensions inches (millimeters) unless otherwise noted



16-Pin Package
NS Package Number SQA32A

Notes

Notes

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