

## 300mA, Ultra-low noise, Small Package

### Ultra-Fast CMOS LDO Regulator

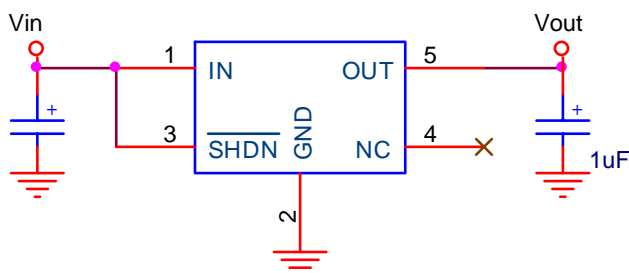
#### General Description

The LP3981 is designed for portable RF and wireless applications with demanding performance and space requirements. The LP3981 performance is optimized for battery-powered systems to deliver ultra low noise and low quiescent current. A noise bypass pin is available for further reduction of output noise. Regulator ground current increases only slightly in dropout, further prolonging the battery life. The LP3981 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices. The LP3981 consumes less than 0.01 $\mu$ A in shutdown mode and has fast turn-on time less than 50 $\mu$ s. The other features include ultra low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in the 5-lead of SOT23-5 packages.

#### Ordering Information

LP3981 -	□	□	□	□	□
	F: Pb-Free				
	Package Type				
	B5: SOT23-5				
	Output Voltage Type				
	12:	1.2V			
	15:	1.5V			
	18:	1.8V			
	25:	2.5V			
	28:	2.8V			
	30:	3.0V			
	33:	3.3V			
	50:	5.0V			

#### Typical Application Circuit



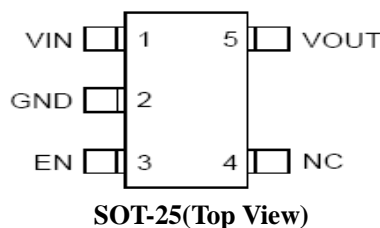
#### Features

- ◆ Ultra-Low-Noise for RF Application
- ◆ 2V- 6.5V Input Voltage Range
- ◆ Low Dropout : 220mV @ 300mA
- ◆ 1.2V, 1.5V, 1.8V, 2.5V, 2.8V 3.0V and 3.3V Fixed
- ◆ 300mA Output Current, 550mA Peak Current
- ◆ High PSSR:-73dB at 1KHz
- ◆ < 0.01 $\mu$ A Standby Current When Shutdown
- ◆ Available in SOT23-5 Package
- ◆ TTL-Logic-Controlled Shutdown Input
- ◆ Ultra-Fast Response in Line/Load transient
- ◆ Current Limiting and Thermal Shutdown Protection
- ◆ Quick start-up (typically 50 $\mu$ s)

#### Applications

- ✧ Portable Media Players/MP3 players
- ✧ Cellular and Smart mobile phone
- ✧ LCD
- ✧ DSC Sensor
- ✧ Wireless Card

#### Pin Configurations



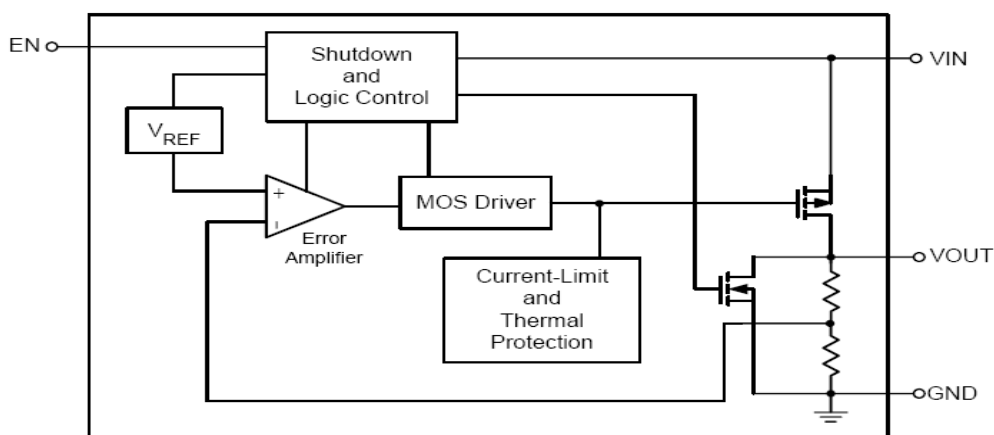
#### Marking Information

Please see website.

## Functional Pin Description

Pin Name	Pin Function
EN	Chip Enable (Active High). Note that this pin is high impedance. There should be a pull low 100kΩ resistor connected to GND when the control signal is floating.
NC	NC
GND	Ground
VOUT	Output Voltage
VIN	Power Input Voltage

## Function Block Diagram



## Absolute Maximum Ratings

Supply Input Voltage	-----6V
Power Dissipation, PD @ TA = 25° C	
SOT-25	-----400mW
Package Thermal Resistance	
SOT-25, θJA	-----250°C/W
Lead Temperature (Soldering, 10 sec.)	-----260°C
Storage Temperature Range	----- -65°C to 150°C
ESD Susceptibility	
HBM (Human Body Mode)	-----2kV
MM(Machine-Mode)	-----200V
Recommended Operating Conditions	
Supply Input Voltage	-----2.5V to 5.5V
EN Input Voltage	-----0V to 5.5V
Operation Junction Temperature Range	----- -40°C to 125°C
Operation Ambient TemperatureRange	----- -40°C to 85°C

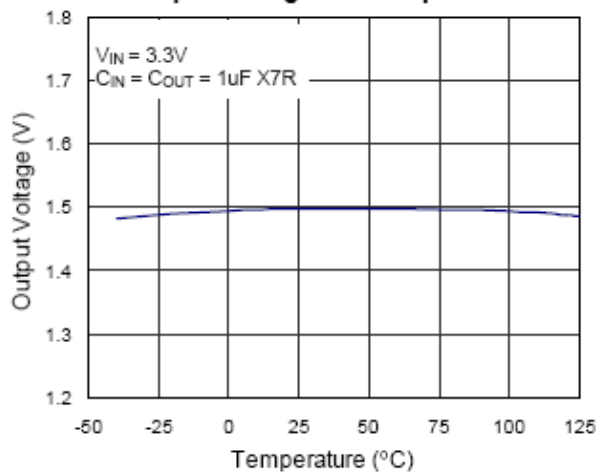
## Electrical Characteristics

(VIN = VOUT + 1V, CIN = COUT = 1μF, CBP = 22nF, TA = 25° C, unless otherwise specified)

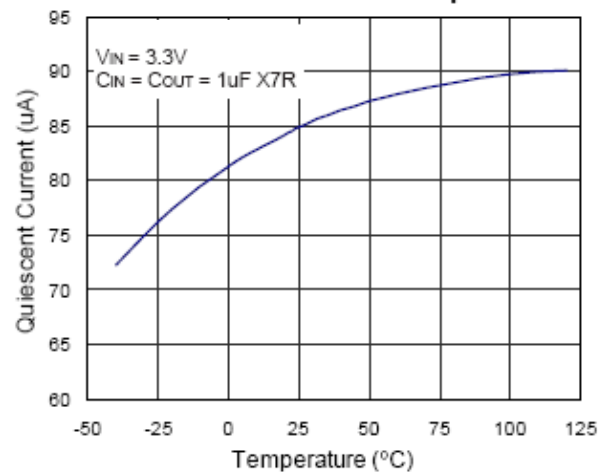
Parameter		Symbol	Test Conditions	Min	Typ	Max	Units
Output Voltage Accuracy		ΔVOUT	IOUT = 1mA	-2	--	+2	%
Output Current		IOUT	VEN=VIN, VIN>2.5V		300		mA
Current Limit		ILIM	RLOAD = 1Ω	360	400		mA
Quiescent Current		IQ	VEN ≥ 1.2V, IOUT = 0mA		75	120	μA
Dropout Voltage		VDROP	IOUT = 200mA, VOUT > 2.8V		170	200	mV
			IOUT = 300mA, VOUT > 2.8V		220	300	
Line Regulation		ΔVLINE	VIN = (VOUT + 1V) to 5.5V, IOUT = 1mA			0.3	%
Load Regulation		ΔLOAD	1mA < IOUT < 300mA			0.6	%
Standby Current		ISTBY	VEN = GND, Shutdown		0.01	1	μA
EN Input Bias Current		IIBSD	VEN = GND or VIN		0.01	100	nA
EN Threshold	Logic-Low Voltage	VIL	VIN = 3V to 5.5V, Shutdown			0.4	V
	Logic-High Voltage	VIH	VIN = 3V to 5.5V, Start-Up	1.2			
Output Noise Voltage			10Hz to 100kHz, IOUT = 200mA COUT = 1μF		100		μVRMS
Power Supply	f = 100Hz	PSRR	COUT = 1μF, IOUT = 10mA		-73		dB
Rejection Rate	f = 10kHz				-70		
Thermal Shutdown Temperature		TSD			165		°C

## Typical Operating Characteristics

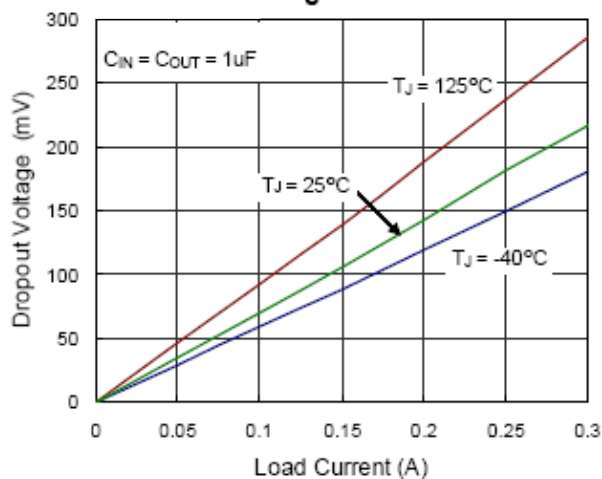
### Output Voltage vs. Temperature



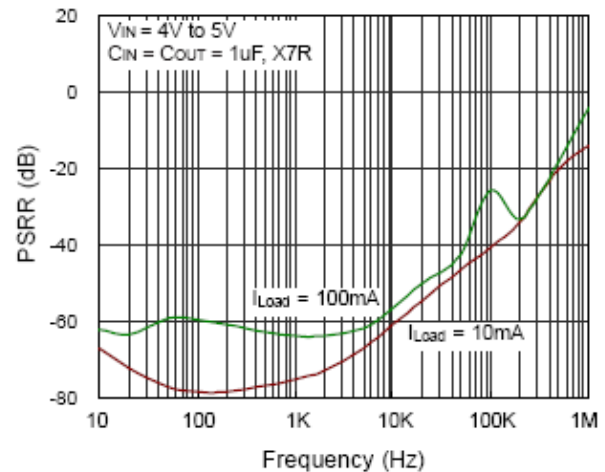
### Quiescent Current vs. Temperature



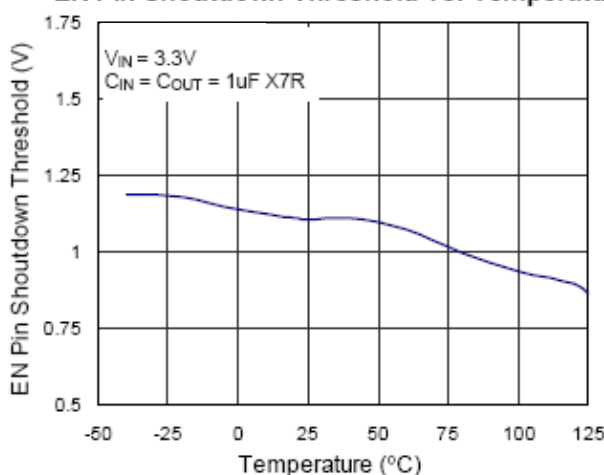
### Dropout Voltage vs. Load Current



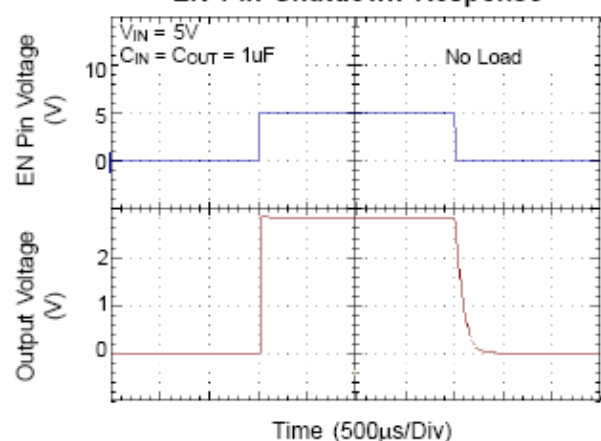
### PSRR



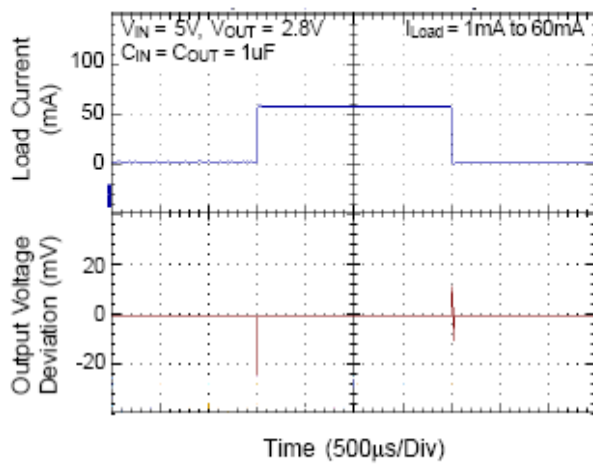
### EN Pin Shutdown Threshold vs. Temperature



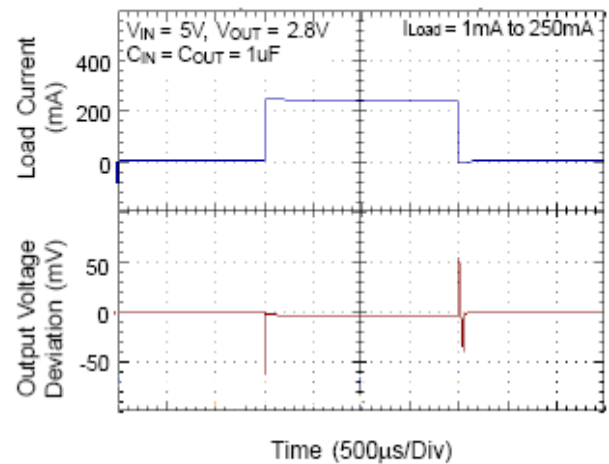
### EN Pin Shutdown Response



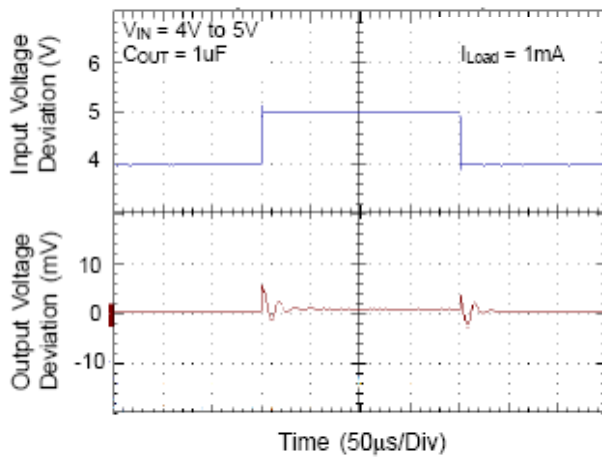
Load Transient Response



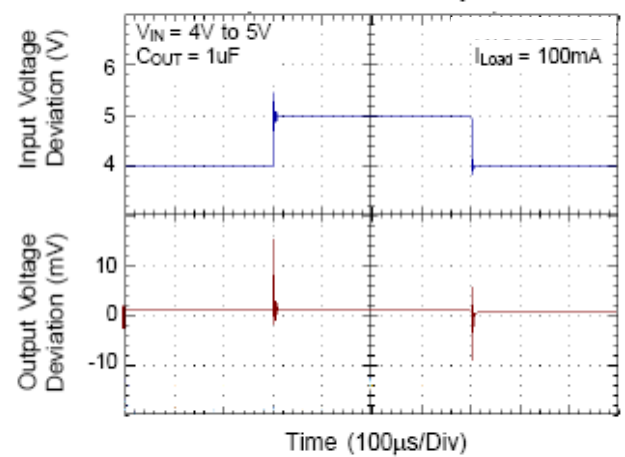
Load Transient Response



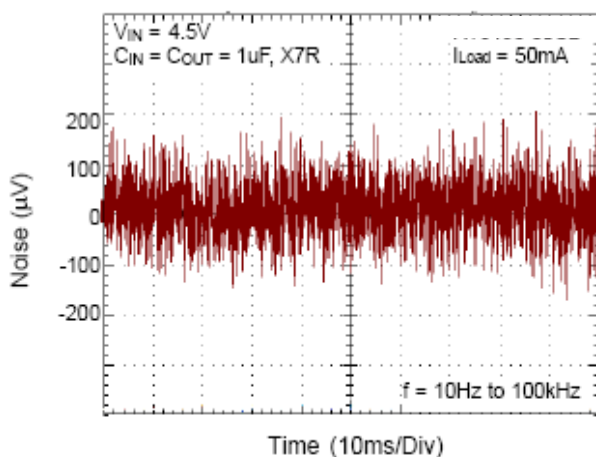
Line Transient Response



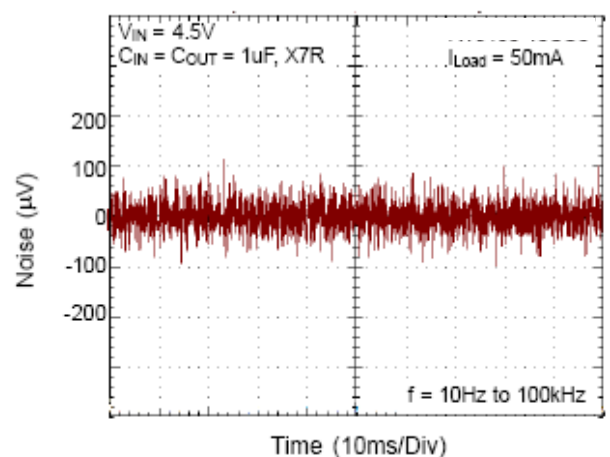
Line Transient Response



Noise



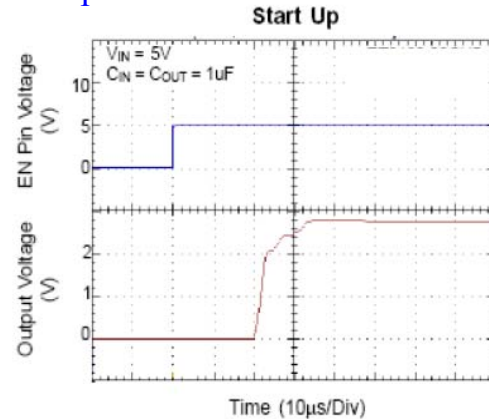
Noise



## Applications Information

Like any low-dropout regulator, the external capacitors used with the LP3981 must be carefully selected for regulator stability and performance. Using a capacitor whose value is  $> 1\mu\text{F}$  on the LP3981 input and the amount of capacitance can be increased without limit. The input capacitor must be located a distance of not more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. Any good quality ceramic or tantalum can be used for this capacitor. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response. The output capacitor must meet both requirements for minimum amount of capacitance and ESR in all LDOs application. The LP3981 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least  $1\mu\text{F}$  with ESR is  $> 25\text{m}\Omega$  on the LP3981 output ensures stability. The LP3981 still works well with output capacitor of other types due to the wide stable ESR range. Figure 1 shows the curves of allowable ESR range as a function of load current for various output capacitor values. Output capacitor of larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located not more than 0.5 inch from the VOUT pin of the LP3981 and returned to a clean analog ground.

## Start-up Function Enable Function



The LP3981 features an LDO regulator enable/disable function. To assure the LDO regulator will switch on, the EN turn on control level must be greater than 1.2 volts. The LDO regulator will go into the shutdown mode when the voltage on the EN pin falls below 0.4 volts. For protecting the system, the LP3981 have a quick-discharge function. If the enable function is not needed in a specific application, it may be tied to VIN to keep the LDO regulator in a continuously on state.

## Bypass Capacitor and Low Noise

Connecting a 22nF between the BP pin and GND pin significantly reduces noise on the regulator output, it is critical that the capacitor connection between the BP pin and GND pin be direct and PCB traces should be as short as possible. There is a relationship between the bypass capacitor value and the LDO regulator turn on time. DC leakage on this pin can affect the LDO regulator output noise and voltage regulation performance.

## Thermal Considerations

Thermal protection limits power dissipation in LP3981. When the operation junction temperature exceeds  $165^{\circ}\text{C}$ , the OTP circuit starts the thermal shutdown function turn the pass element off. The pass element turn on again after the junction temperature cools by  $30^{\circ}\text{C}$ . For continue operation, do not exceed absolute maximum operation junction temperature  $125^{\circ}\text{C}$ .

The power dissipation definition in device is :

$$PD = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient.

The maximum power dissipation can be calculated by following formula :

$$PD(MAX) = (T_J(MAX) - T_A) / \theta_{JA}$$

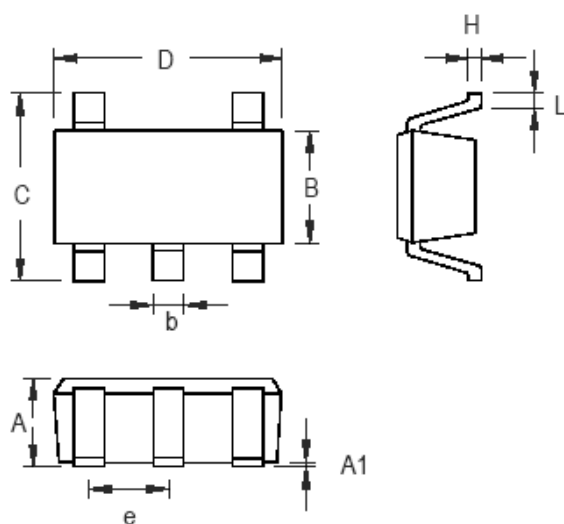
Where  $T_J(MAX)$  is the maximum operation junction temperature 125°C,  $T_A$  is the ambient temperature and the  $\theta_{JA}$  is the junction to ambient thermal resistance. For recommended operating conditions specification of LP3981, where  $T_J(MAX)$  is the maximum junction temperature of the die (125°C) and  $T_A$  is the maximum ambient temperature. The junction to ambient thermal resistance ( $\theta_{JA}$  is layout dependent) for Sot23-5 package is 250°C/W.

$$PD(MAX) = (125^{\circ}C - 25^{\circ}C) / 250 = 400mW \text{ (Sot23-5)}$$

$$PD(MAX) = (125^{\circ}C - 25^{\circ}C) / 165 = 606mW$$

The maximum power dissipation depends on operating ambient temperature for fixed  $T_J(MAX)$  and thermal resistance  $\theta_{JA}$ .

## Packaging Information



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.889	1.295	0.035	0.051
A1	0.000	0.152	0.000	0.006
B	1.397	1.803	0.055	0.071
b	0.356	0.559	0.014	0.022
C	2.591	2.997	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.838	1.041	0.033	0.041
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

### SOT- 25 Surface Mount Package