承永資訊科技
CYRUSTEK CO.

ES7

True RMS-to-DC Converters

Features

- True RMS-to-DC Conversion
- **Input level is specified up to 400mV$_{RMS}$**
- **Averaging capacitor is typically 2.2uF**
- **Positive output voltage**
- Computes RMS of AC and DC Signals
- Single or Dual Supply Operation
- Low Cost
- Power-Down Function
- **Low Power: 600 μA typically**
- **Wide power supply range : from ±2.5V to ±10V**
- **8-pin SOP package**

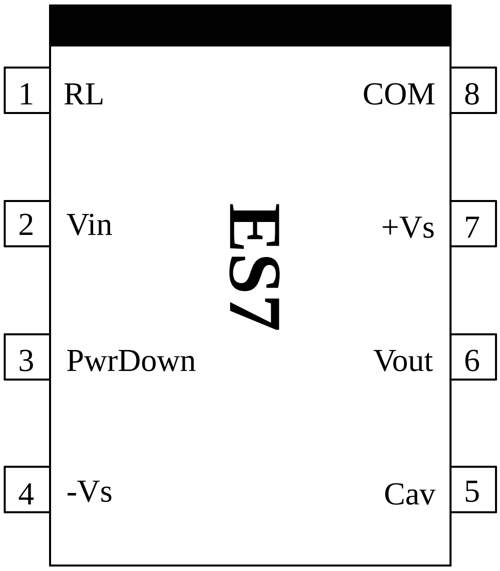
Description

The ES7 series are designed for the true RMS-to-DC conversion. ES7 accept low-level input signals from 0 to 400 mV $_{RMS}$ complex input waveforms. ES7 can be operated form either a single supply or dual supplies. The device draw less than 1 mA of quiescent supply current, furthermore, an enable pin is provided to turn-off the device, making it ideal for battery-powered applications.

Application

* Digital Multi-Meters
* Battery-Powered Instruments
* Panel Meter

Pin Assignment: ES7



SOP 8 Pin Package

Pin Description

Pin No	Symbol	Type	Description
1	RL	-	RL terminal. For zero-offset removing.
2	Vin	I	Measurement input.
3	PwrDown	I	Pull high (+Vs) to enable power-down function.
4	-Vs	P	Negative supply voltage.
5	Cav	I/O	Averaging capacitor
6	Vout	O	Measurement output.
7	+Vs	P	Positive supply voltage.
8	COM	P	Power ground

I: input, O: output, P: power

Absolute Maximum Ratings

Supply Voltage: Dual Supplies .... ±10V

Single Supply ....+20V

Input Voltage: .... ±10V

Power Dissipation (Package)

SOP...450mW

Operating Temperature Range ....0℃ to +70℃

Storage Temperature Range...-55℃ to +150℃

Lead Temperature (Soldering, 10sec)...300℃

Electrical Characteristics-ES7

(T_A= +25℃, Vs = +3V, -Vs = -3V, unless otherwise noted.)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Transfer Equation					$V_{OUT} = \sqrt{avg.[(V_{IN})^2]}$		
Averaging Time Constant					6		ms/μF C_{AV}
CONVERSION ACCURACY							
Total Error, Internal Trim **(Notes 1)**	ES7					±0.5 ± 1.0	mV ±% of Reading
Total Error vs. Temperature (0℃ to + 70℃)					±0.1 ±0.01		mV ±% of Reading/℃
Total Error vs. Supply					±0.1 ±0.01		mV ±% of Reading/V
Total Error vs. DC Reversal	VIN=±400mV					±2.0	±% of Reading
Additional Error **(Note 2)**	Cav=2.2μF	Crest Factor = 1	400mV		Specified Accuracy		±% of Reading
		Crest Factor = 2	200mV		1.00		
			400mV		1.10		
		Crest Factor = 3	200mV		1.25		
			400mV		1.50		
		Crest Factor = 4	200mV		1.50		
			400mV		2.00		
FREQUENCY RESPONSE							
Bandwidth for 1% Additional Error (0.09dB)	35mV				50		kHz
	100mV				200		
	200mV				200		
	400mV				200		
±3dB Bandwidth	35mV				1.0		MHz
	100mV				1.0		
	200mV				1.0		
	400mV				0.5		

Electrical Characteristics-ES7 (continued)

(T_A= +25℃, Vs = +3V, -Vs = -3V, unless otherwise noted.)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS						
Input Signal range	Continuous RMS, All Supplies			0 to 400		mV_{RMS}
	Peak Transient	±2.5V Supplies			1	V_{PK}
		±3V Supplies			1.5	
		±5V Supplies			2.8	
Input Resistance			6	8	10	MΩ
Input Offset Voltage **(Note3)**	ES7				±0.5	mV
OUTPUT CHARACTERISTICS						
Output Voltage Swing	+3V, -3V Supplies		1			V_{RMS}
	±5V to ±10V Supplies		1	1.5		
Output Resistance			8	10	12	kΩ
Power SUPPLY						
Rated Performance				±3		V
Dual Supplies			±2.5		±10	V
Single Supply			+5		+20	V
Supply Current	±3V Supply. Vin connects to COM			600	800	μA
Supply Current (Power Down)	Pin3 connects to V+			60	75	μA

Note 1: Accuracy is specified for 0 to 400mV, 1kHz sine-wave input. Accuracy is degraded at higher RMS signal levels.

Note 2: Error vs. crest factor is specified as an additional error for $200mV_{RMS}$ and $400mV_{RMS}$ rectangular pulse input, pulse width = 200μs

Note 3: The input offset voltage can be reduced or canceled by an external 500kohm variable resistor shown in Figure 3.

Detailed Description

Figure 1 shows the simplified schematic of ES7. It consists of four major sub-circuits: absolute value circuit (rectifier), square/divider, current mirror and buffer amplifier. The actual computation performed by the ES7 follows the equation:

$$V_{RMS} = \text{Avg.}\ [V_{IN}2 / V_{RMS}]$$

The input voltage, V_{IN}, applied to the ES7 is converted to a unipolar current I_1 (Figure 1) by the absolute-value/voltage. This current drives one input of the squarer/divider that produces a current I_4 , which has the transfer function:

$$I_4 = \frac{I_1^2}{I_3}$$

The current I_4 drives the internal current mirror through a low-pass filter formed by R1 and the external capacitor, C_{AV}. As long as the time constant of this filter is greater than the longest period of the input signal, I_4 is averaged. The current mirror returns a current, I_3, to the square/divider to complete the circuit. The current I_4 is then a function of the average of (I_1^2/ I_4), which is equal to I_{1RMS}.

The current mirror also produces a $2 \cdot I_4$ output current, I_{OUT}, that can be used directly or converted to a voltage using resistor R2 and the internal buffer to provide a low-impedance voltage output. The transfer function for the ES7 is:

$$V_{OUT} = 2 \cdot R2 \cdot I_{RMS} = V_{IN}$$

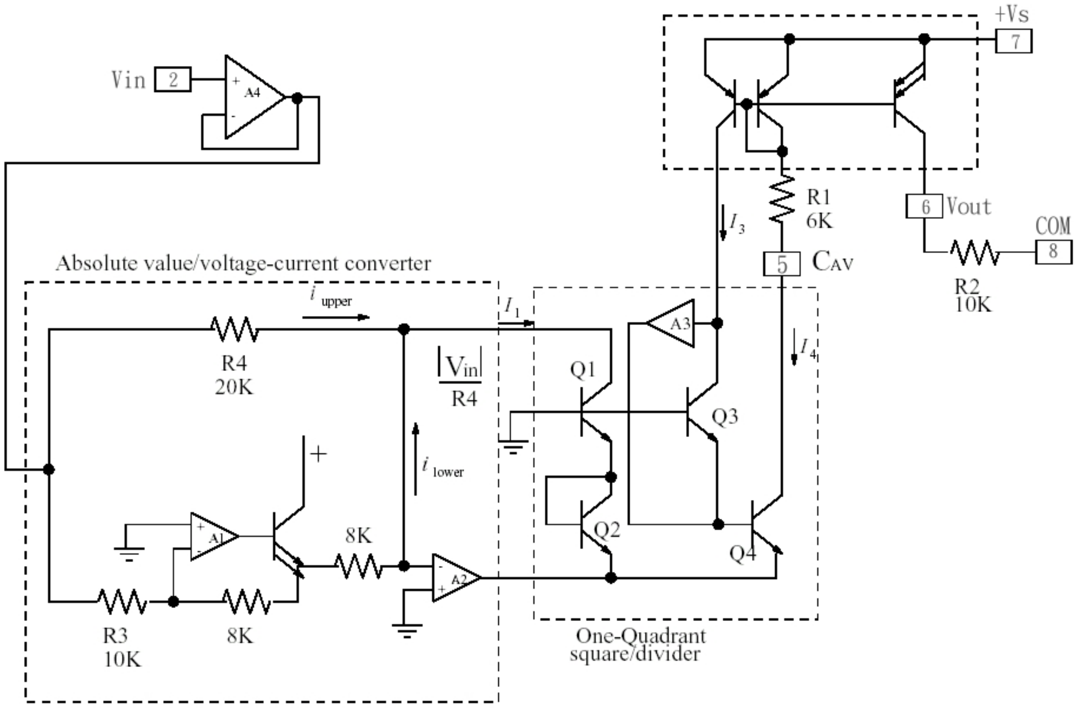


Figure 1. ES7 Simplified Schematic

Standard Connection for ES7 (Figure 2)

The standard RMS connection requires only two external components, Rin and C_{av}. Other components shown in figure 2 are optional. In this configuration, ES7 measure the RMS of the AC and DC levels present at the input, but shows an error for low-frequency inputs as a function of the C_{av} filter capacitor. Figure 4 gives practical values of C_{av} for various values of averaging error over frequency for the standard RMS connections (no post filtering). If a 3uF capacitor is chosen, the additional error at 30Hz will be 1%. If the DC error can be rejected, a capacitor Ccp should be connected in series with the input, as would typically be the case in single-supply operation.

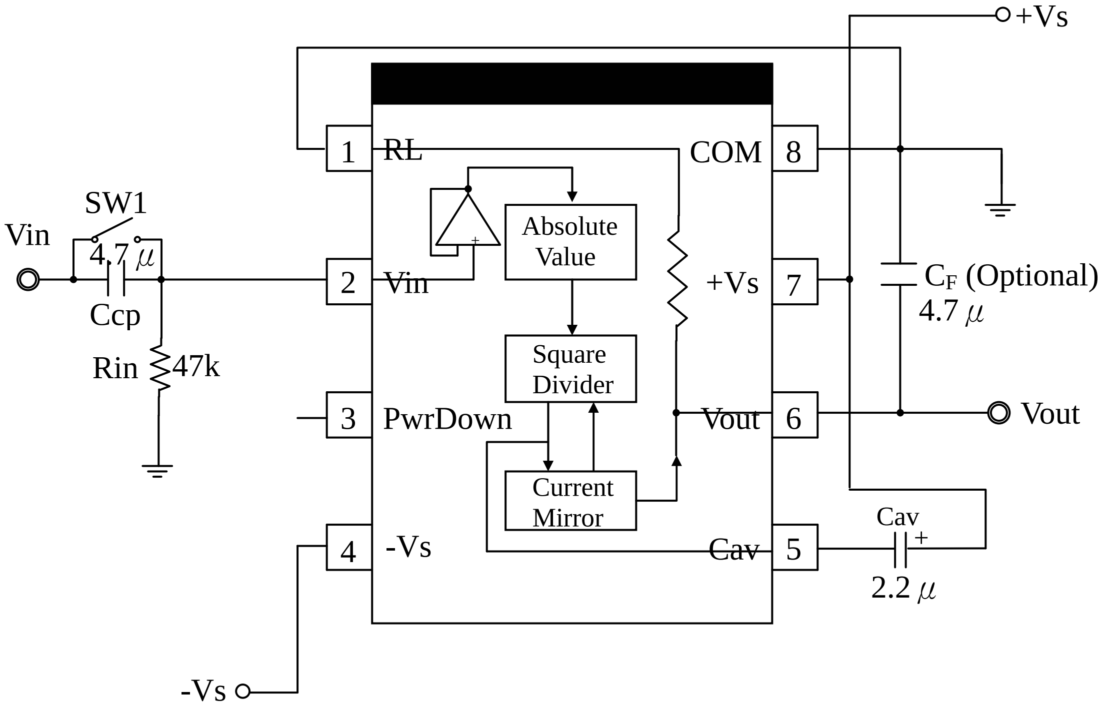


Figure 2. Standard connection for ES7.

Note:

1. SW1 is opened for AC-coupled operation, or closed for direct input.
2. PwrDown pin is pulled to –Vs or keeps floating for normal operation. Connect it to +Vs will force ES7 to enter power down mode.

To Adjust the zero-offset of ES7 (Figure 3)

The output of some ES7 ICs may have an offset voltage when the input is zero. The amount of this offset voltage might be different in every ES7. We provide pin1-RL to achieve the reduction of zero offset voltage. The test circuit is shown as below. The 500kohm VR, 1kohm and 10ohm resistors are used to reduce zero offset voltage. Adjusting the 500kohm VR can reduce the zero offset voltage. However it must be noted that the 10ohm resistor enlarge the output impedance. The voltage of pin6-Vout is equal to (output current)*(output impedance), so it would be enlarged too. This will cause an additional error for ES7. So we recommend that the value of resistor between pin1-RL and pin8-COM should not be too large.

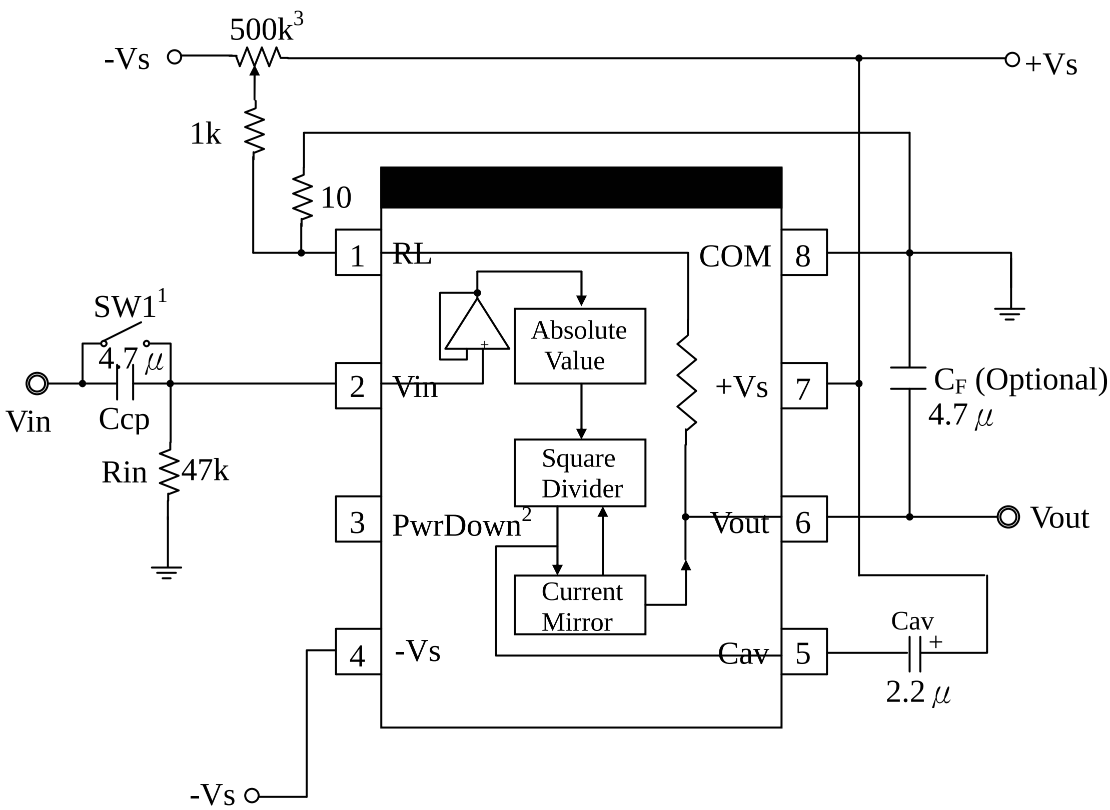


Figure 3. Adjust the zero-offset

Note:

1. SW1 is opened for AC-coupled operation, or closed for direct input.
2. PwrDown pin is pulled to –Vs or keeps floating for normal operation. Connect it to +Vs will force ES7 to enter power down mode.
3. The 500k ohm variable resistor can be used to adjust the zero-offset voltage.

Application notes

1. AC-coupled operation

Refer to the standard circuit of ES7 shown in Figure 2~3. ES7 will work in an AC-coupled operation when the SW1 is opened. In AC-coupled operation, an AC-coupled capacitor (Ccp) and bias resistors Rin must be required. For a low frequency input under 100Hz, the Ccp need a 1uF or even larger capacitor to prevent input signal from decaying.

Due to the architecture of ES7, a bias current is needed to activate the input buffer. The resistor Rin applied from Vin to GND supplies a bias current flow path in AC-coupled operation. The bias current flows from GND to Vin through Rin will cause a bias voltage at Vin pin. So the Rin resistance should not be too large (cause an additional zero offset) or too small (low input impedance).

2. Power Down Function

The ES7 provides a power-down enable pin (Pin 3). To enable the device, this pin must be connected to –Vs or keep floating. If it is connected to V+, the device will enter power-down mode.

3. Post Filter C_F

To reduce the output ripple of ES7, a post filter capacitor C_F is required. This capacitor should be connected as shown in figure 2. With post filter, the value of Cav should be just large enough to give the maximum dc error at the lowest frequency of interest. And the output ripple will be removed by the post filter.

Choosing the Averaging Time Constant

The ES7 computes the RMS value of AC and DC signals. At low frequencies and DC, the output tracks the input exactly; at higher frequencies, the average output approaches the RMS value of the input signal. The actual output differs from the ideal by an average (or DC) error plus some amount of ripple.

The DC error term is a function of the value of C_{av} and the input signal frequency. The output ripple is inversely proportional to the value of C_{av}. Waveforms with high crest factors, such as a pulse train with low duty cycle, should have an average time constant chosen to be at least ten times the signal period.

Using a large value of C_{av} to remove the output ripple increases the setting time for a step change in the input signal level. Figure 4 shows the relationship between C_{av} and 1 % settling time, where 110ms settling equals 4uF of C_{av}. The settling time, or time for the RMS converter to settle to within a given percent of the change in RMS level, is set by the averaging time constant, which varies approximately 2:1 between decreasing and increasing input signals. In addition, the settling time also varies with input signal levels, increasing as the input signal is reduced, and decreasing as the input is increased.

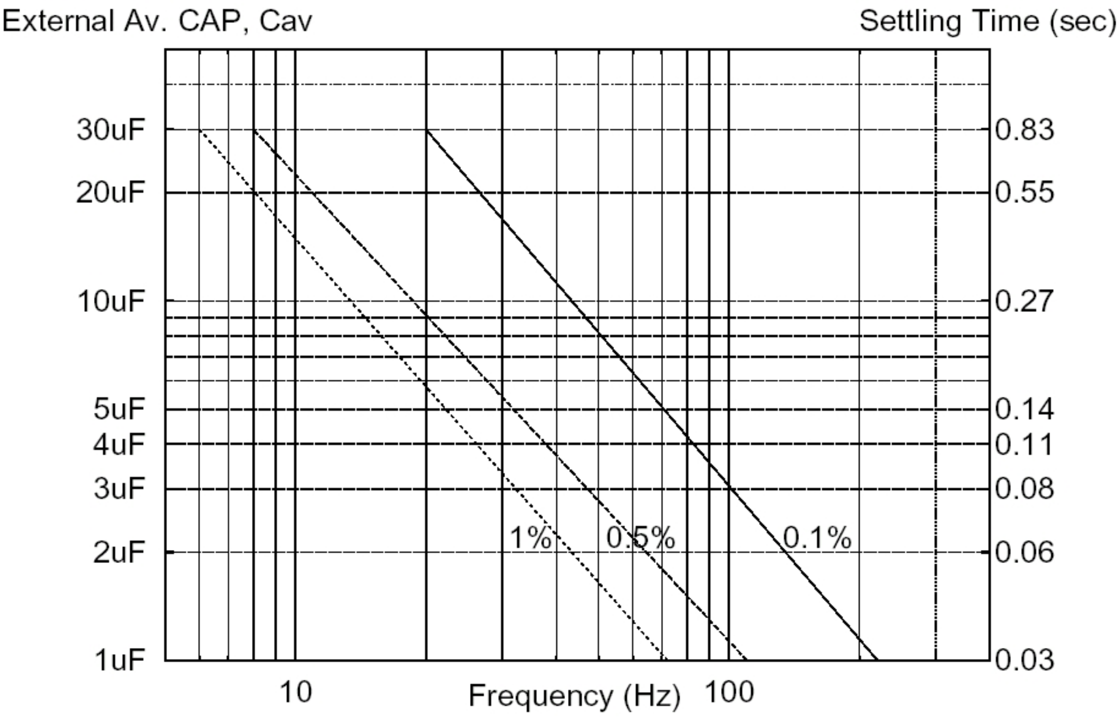
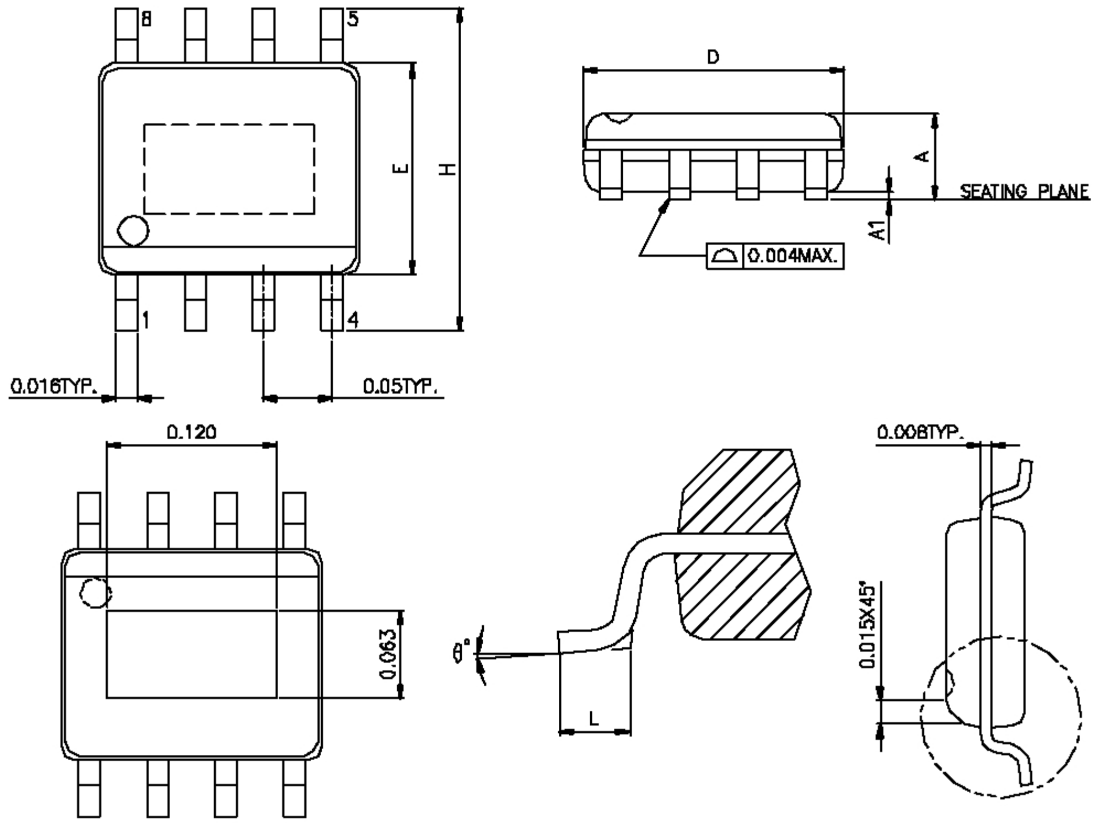


Figure 4. Errors/Settling Time Graph for Standard Connection

Packaging

8 Pin SOP Package



Dimension Parameters

SYMBOLS	MIN.	MAX.
A	0.053	0.069
A1	0.004	0.010
D	0.189	0.196
E	0.150	0.157
H	0.228	0.244
L	0.016	0.050
θ°	0	8

UNIT : INCH

NOTES:

1.JEDEC OUTLINE : MS-012 AA

2.DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED .15mm (.006in) PER SIDE.

3.DIMENSIONS "E" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED .25mm (.010in) PER SIDE.