

# Dual I<sup>2</sup>C Power Supply Monitor and Margining Controller

## FEATURES

- **Less Than  $\pm 0.5\%$  Total Unadjusted Error 14-Bit  $\Delta\Sigma$  ADC with On-Chip Reference**
- **Dual, 8-Bit IDACs with 1x Voltage Buffers**
- **Linear, Voltage Servo Adjusts Supply Voltages by Ramping IDAC Outputs Up/Down**
- **I<sup>2</sup>C™ Bus Interface (SMBus Compatible)**
- **Extensive, User Configurable Fault Monitoring**
- **On-Chip Temperature Sensor**
- **Available in 24-Lead 4mm × 5mm QFN Package**

## APPLICATIONS

- Dual Power Supply Voltage Servo
- Monitoring Supply Voltage and Current
- Programmable Power Supplies
- Programmable Reference

## DESCRIPTION

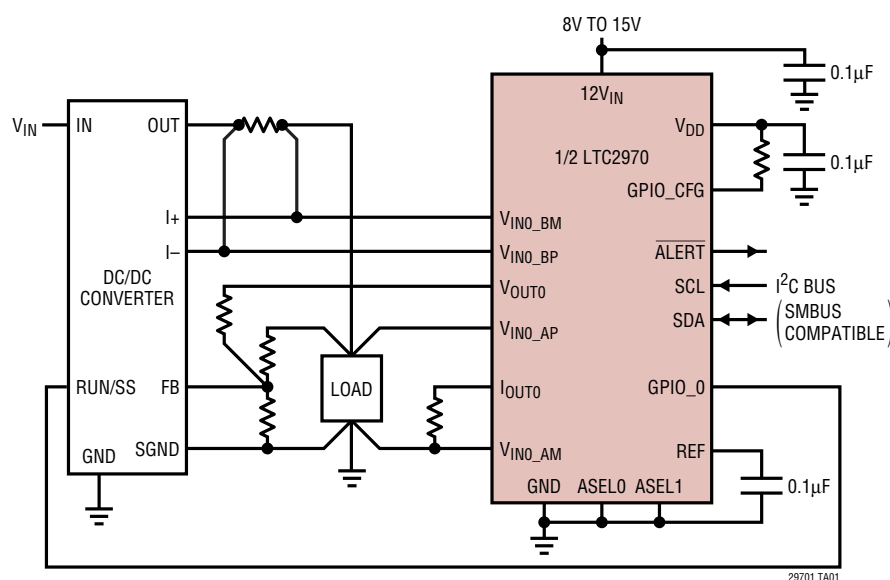
The LTC®2970 is a dual power supply monitor and margining controller with an SMBus compatible I<sup>2</sup>C bus interface. A low-drift, on-chip reference and 14-bit  $\Delta\Sigma$  A/D converter allow precise measurements of supply voltages, load currents or internal die temperature. Fault management allows  $\overline{\text{ALERT}}$  to be asserted for configurable over and under voltage fault conditions. Two voltage buffered, 8-bit IDACs allow highly accurate programming of DC/DC converter output voltages. The IDACs can be configured to automatically servo the power supplies to the desired voltages using the ADC. The LTC2970-1 adds a tracking feature that can be used to turn multiple power supplies on or off in a controlled manner.

The bus address is set to 1 of 9 possible combinations by pin strapping the ASELO and ASEL1 pins. The LTC2970/LTC2970-1 are packaged in the 24-lead, 4mm × 5mm QFN package.

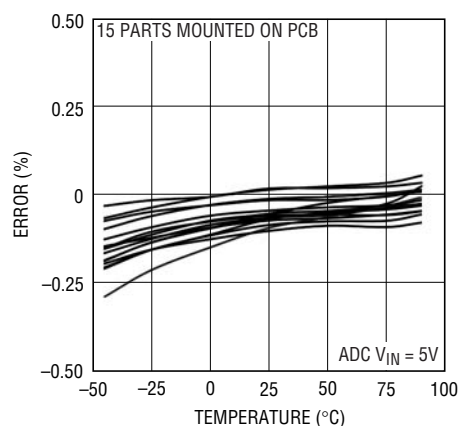
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## TYPICAL APPLICATION

### Dual Power Supply Monitor and Controller (One of Two Channels Shown)



### ADC Total Unadjusted Error vs Temperature



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# LTC2970/LTC2970-1

## ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltages:

$V_{DD}$  ..... -0.3V to 6V

$12V_{IN}$  ..... -0.3V to 15V

Digital Input/Output Voltages:

ASEL0, ASEL1 ..... -0.3V to  $V_{DD} + 0.3V$

SDA, SCL, GPIO\_CFG,

ALERT, GPIO\_0, GPIO\_1 ..... -0.3V to 6V

Analog Voltages:

$V_{INO\_AP}$ ,  $V_{INO\_AM}$ ,  $V_{INO\_BP}$ ,

$V_{INO\_BM}$ ,  $V_{IN1\_AP}$ ,  $V_{IN1\_AM}$ ,

$V_{IN1\_BP}$ ,  $V_{IN1\_BM}$ ,  $V_{OUT0}$ ,  $V_{OUT1}$  ..... -0.3V to 6V

$I_{OUT0}$ ,  $I_{OUT1}$ , REF ..... -0.3V to  $V_{DD} + 0.3V$

RGND ..... -0.3V to 0.3V

Operating Temperature Range:

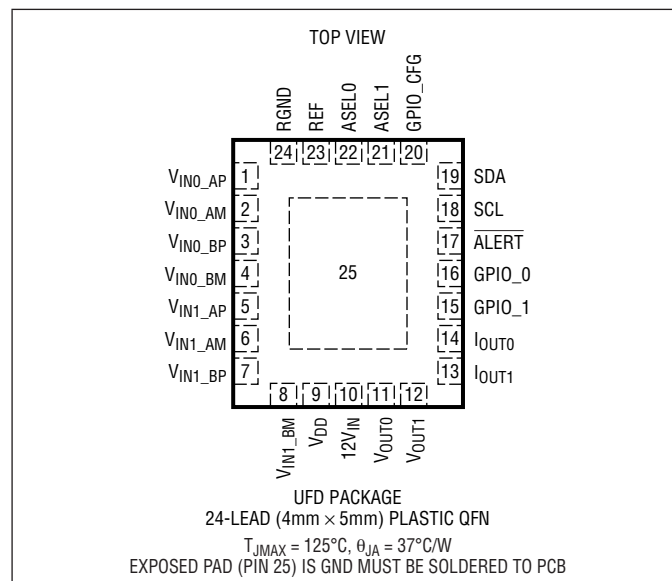
LTC2970C ..... 0°C to 70°C

LTC2970I ..... -40°C to 85°C

Storage Temperature Range ..... -65°C to 125°C

Lead Temperature (Soldering, 10 sec) ..... 300°C

## PIN CONFIGURATION



## ORDER INFORMATION

| LEAD FREE FINISH  | TAPE AND REEL       | PART MARKING* | PACKAGE DESCRIPTION             | TEMPERATURE RANGE |
|-------------------|---------------------|---------------|---------------------------------|-------------------|
| LTC2970CUFD#PBF   | LTC2970CUFD#TRPBF   | 2970          | 24-Lead (4mm × 5mm) Plastic DFN | 0°C to 70°C       |
| LTC2970CUFD-1#PBF | LTC2970CUFD-1#TRPBF | 29701         | 24-Lead (4mm × 5mm) Plastic DFN | 0°C to 70°C       |
| LTC2970IUFD#PBF   | LTC2970IUFD#TRPBF   | 2970          | 24-Lead (4mm × 5mm) Plastic DFN | -40°C to 85°C     |
| LTC2970IUFD-1#PBF | LTC2970IUFD-1#TRPBF | 29701         | 24-Lead (4mm × 5mm) Plastic DFN | -40°C to 85°C     |

Consult LTC Marketing for parts specified with wider operating temperature ranges. \*The temperature grade is identified by a label on the shipping container.

For more information on lead free part marking, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

**ELECTRICAL CHARACTERISTICS** The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .  $V_{12VIN} = 12\text{V}$ ,  $V_{DD}$  and REF pins floating unless otherwise indicated,  $C_{VDD} = 100\text{nF}$  and  $C_{REF} = 100\text{nF}$ .

| SYMBOL                                     | PARAMETER                                        | CONDITIONS                                                                     |   | MIN   | TYP   | MAX       | UNITS                        |
|--------------------------------------------|--------------------------------------------------|--------------------------------------------------------------------------------|---|-------|-------|-----------|------------------------------|
| <b>Power-Supply Characteristics</b>        |                                                  |                                                                                |   |       |       |           |                              |
| $I_{V12}$                                  | 12V <sub>IN</sub> Supply Current                 | $V_{12VIN} = 12\text{V}$ , $V_{DD}$ Floating                                   | ● |       | 4.24  | 7.5       | mA                           |
| $I_{DD}$                                   | $V_{DD}$ Supply Current                          | $V_{DD} = 5\text{V}$ , $V_{12VIN} = V_{DD}$                                    | ● |       | 3.7   | 5         | mA                           |
| $V_{LKO}$                                  | $V_{DD}$ Undervoltage Lockout                    | $V_{DD}$ Ramping-Down, $V_{12VIN} = V_{DD}$                                    | ● | 3.7   | 4.14  | 4.4       | V                            |
|                                            | $V_{DD}$ Undervoltage Lockout Hysteresis         |                                                                                |   |       | 118   |           | mV                           |
| $V_{DD}$                                   | Supply Input Operating Range                     |                                                                                | ● | 4.5   |       | 5.75      | V                            |
|                                            | Regulator Output Voltage                         | $8\text{V} \leq V_{12VIN} \leq 15\text{V}$ , $-1\text{mA} \leq I_{VDD} \leq 0$ | ● | 4.75  | 4.95  | 5.25      | V                            |
|                                            | Regulator Output Voltage Temperature Coefficient |                                                                                |   |       | 10    |           | ppm/ $^\circ\text{C}$        |
|                                            | Regulator Output Voltage Load Regulation         | $-1\text{mA} \leq I_{VDD} \leq 0$                                              |   |       | 160   |           | ppm/mA                       |
|                                            | Regulator Line Regulation                        | $8\text{V} \leq V_{12VIN} \leq 15\text{V}$ , $I_{VDD} = 0\text{mA}$            |   |       | 80    |           | ppm/V                        |
|                                            | Regulator Output Short-Circuit Current           | $V_{12VIN} = 12\text{V}$ , $V_{DD} = 0\text{V}$                                | ● | -5    | -34   | -63       | mA                           |
| $V_{12VIN}$                                | 12V <sub>IN</sub> Supply Operating Range         |                                                                                | ● | 8     |       | 15        | V                            |
| <b>Voltage Reference Characteristics</b>   |                                                  |                                                                                |   |       |       |           |                              |
| $V_{REF}$                                  | Reference Output Voltage                         |                                                                                |   |       | 1.229 |           | V                            |
|                                            | Reference Voltage Temperature Coefficient        |                                                                                |   |       | 2     |           | ppm/ $^\circ\text{C}$        |
|                                            | Reference Overdrive Voltage Input Range          |                                                                                | ● | 1     |       | 1.5       | V                            |
| <b>ADC Characteristics</b>                 |                                                  |                                                                                |   |       |       |           |                              |
| $N_{ADC}$                                  | Resolution                                       | $N_{ADC} = 8.192\text{V}/16384$                                                |   |       | 500   |           | $\mu\text{V}/\text{LSB}$     |
| $TUE_{ADC}$                                | Total Unadjusted Error                           | $V_{IN} = 3\text{V}$ , $V_{IN} = V_{INn\_xP} - V_{INn\_xM}$ (Note 3)           | ● |       |       | $\pm 0.5$ | %                            |
| $INL_{ADC}$                                | Integral Nonlinearity                            | (Note 4)                                                                       | ● | -4.5  | 2     | 4.5       | LSB                          |
| $DNL_{ADC}$                                | Differential Nonlinearity                        | (Note 7)                                                                       | ● |       |       | $\pm 0.5$ | LSB                          |
| $V_{IN\_ADC}$                              | Input Voltage Range                              |                                                                                | ● | 0     |       | 6         | V                            |
| $V_{OS\_ADC}$                              | Offset Error                                     |                                                                                | ● | -1000 | -316  | 1000      | $\mu\text{V}$                |
|                                            | Offset Error Drift                               |                                                                                |   |       | 0.19  |           | $\mu\text{V}/^\circ\text{C}$ |
| $GAIN_{ADC}$                               | Gain Error                                       | Full-Scale $V_{IN} = 6\text{V}$                                                | ● |       |       | $\pm 0.4$ | %                            |
|                                            | Gain Error Drift                                 |                                                                                |   |       | 3     |           | ppm/ $^\circ\text{C}$        |
| $T_{CONV\_ADC}$                            | Conversion Time                                  |                                                                                |   |       | 33.3  |           | ms                           |
| $C_{IN\_ADC}$                              | Input Sampling Capacitance                       |                                                                                |   |       | 3     |           | pF                           |
| $F_{IN\_ADC}$                              | Input Sampling Frequency                         |                                                                                |   |       | 61.4  |           | kHz                          |
| $I_{LEAK\_ADC}$                            | Input Leakage Current                            | $0\text{V} < V_{IN} < 6\text{V}$                                               | ● |       |       | $\pm 0.1$ | $\mu\text{A}$                |
| <b>IDAC Output Current Characteristics</b> |                                                  |                                                                                |   |       |       |           |                              |
| $N_{IOUT}$                                 | Resolution (Guaranteed Monotonic)                |                                                                                |   | 8     |       |           | Bits                         |
| $INL_{IOUT}$                               | Integral Nonlinearity                            | $V_{IOUTn} < V_{DD} - 1.5\text{V}$                                             | ● |       |       | $\pm 1$   | LSB                          |
| $DNL_{IOUT}$                               | Differential Nonlinearity                        | $V_{IOUTn} < V_{DD} - 1.5\text{V}$                                             | ● |       |       | $\pm 1$   | LSB                          |
| $I_{FS\_IOUT}$                             | Full-Scale Output Current                        | $V_{IOUTn} < V_{DD} - 1.5\text{V}$ , DAC Code = 'hff                           | ● | -236  | -255  | -276      | $\mu\text{A}$                |
| $I_{DRIFT\_IOUT}$                          | Output Current Drift                             | DAC Code = 'hff                                                                |   |       | 32    |           | ppm/ $^\circ\text{C}$        |
| $I_{OS\_IOUT}$                             | Offset Current                                   | DAC Code = 'h00                                                                | ● |       |       | $\pm 0.1$ | $\mu\text{A}$                |

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| SYMBOL                                                         | PARAMETER                    | CONDITIONS                                                                    |   | MIN   | TYP     | MAX            | UNITS                        |
|----------------------------------------------------------------|------------------------------|-------------------------------------------------------------------------------|---|-------|---------|----------------|------------------------------|
| <b>Voltage Buffered IDAC Output Characteristics</b>            |                              |                                                                               |   |       |         |                |                              |
| $INL_{V_{OUT}}$                                                | Integral Nonlinearity        | $R_{I_{OUTn}} = 10\text{k}\Omega$ , No Load on $V_{OUTn}$ (Note 5)            | ● |       |         | $\pm 1$        | LSB                          |
| $DNL_{V_{OUT}}$                                                | Differential Nonlinearity    | $R_{I_{OUTn}} = 10\text{k}\Omega$ , No Load on $V_{OUTn}$ (Note 5)            | ● |       |         | $\pm 1$        | LSB                          |
| $V_{OS-V_{OUT}}$                                               | Offset Voltage               | $V_{OS} = V_{OUTn} - V_{I_{OUTn}}$ , No Load on $V_{OUTn}$                    | ● |       | 1.6     | $\pm 10$       | mV                           |
|                                                                | Output Voltage Drift         | No Load on $V_{OUTn}$                                                         |   |       | 0.17    |                | $\mu\text{V}/^\circ\text{C}$ |
| $V_{OUT}$                                                      | Load Regulation              | $0.1\text{V} < V_{OUTn} < V_{DD} - 1.5\text{V}$ , $I_{V_{OUTn}}$ Source = 1mA |   |       | -57     |                | ppm/mA                       |
|                                                                |                              | $0.1\text{V} < V_{OUTn} < V_{DD} - 1.5\text{V}$ , $I_{V_{OUTn}}$ Sink = 1mA   |   |       | 100     |                | ppm/mA                       |
|                                                                | Leakage Current              | $V_{OUTn}$ High-Z, $0\text{V} \leq V_{OUTn} \leq V_{DD}$                      | ● |       | 1       | $\pm 100$      | nA                           |
|                                                                | Short-Circuit Current Low    | $V_{OUTn}$ Shorted to GND                                                     | ● |       |         | -50            | mA                           |
|                                                                | Short-Circuit Current High   | $V_{OUTn}$ Shorted to $V_{DD}$                                                | ● |       |         | 50             | mA                           |
| <b>Soft Connect Comparator Characteristics (CMP0, CMP1)</b>    |                              |                                                                               |   |       |         |                |                              |
| $V_{OS}$                                                       | Offset Voltage               |                                                                               |   |       | $\pm 3$ |                | mV                           |
| <b>Temperature Sensor Characteristics</b>                      |                              |                                                                               |   |       |         |                |                              |
| TMP                                                            | Gain                         |                                                                               |   |       | 0.25    |                | $^\circ\text{C}/\text{LSB}$  |
| <b>12VIN Voltage Divider Characteristics</b>                   |                              |                                                                               |   |       |         |                |                              |
| $GAIN_{12VIN}$                                                 | Gain                         |                                                                               | ● | 0.329 | 0.333   | 0.335          | V/V                          |
| <b>Digital Inputs SCL, SDA, GPIO_CFG, GPIO_0, GPIO_1</b>       |                              |                                                                               |   |       |         |                |                              |
| $V_{IH}$                                                       | Input High Threshold Voltage | SDA, SCL                                                                      | ● |       |         | 2.1            | V                            |
|                                                                |                              | GPIO_CFG, GPIO_0, GPIO_1                                                      | ● |       |         | 1.6            | V                            |
| $V_{IL}$                                                       | Input Low Threshold Voltage  | SDA, SCL                                                                      | ● |       | 1.5     |                | V                            |
|                                                                |                              | GPIO_CFG, GPIO_0, GPIO_1                                                      | ● |       | 1.0     |                | V                            |
| $V_{HYST}$                                                     | Input Hysteresis             |                                                                               |   |       | 0.08    |                | V                            |
| $I_{LEAK}$                                                     | Input Leakage Current        | $0\text{V} \leq V_{IN} \leq 6\text{V}$                                        | ● |       |         | $\pm 1$        | $\mu\text{A}$                |
| $C_{IN}$                                                       | Input Capacitance            |                                                                               |   |       | 10      |                | pF                           |
| <b>Three State Inputs ASEL[1:0]</b>                            |                              |                                                                               |   |       |         |                |                              |
| $V_{IH\_ASEL}$                                                 | Input High Threshold Voltage |                                                                               | ● |       |         | $V_{DD} - 0.5$ | V                            |
| $V_{IL\_ASEL}$                                                 | Input Low Threshold Voltage  |                                                                               | ● |       | 0.5     |                | V                            |
| $I_{IN,HL}$                                                    | High, Low Input Current      | $ASEL[1:0] = 0$ , $V_{DD}$                                                    | ● |       |         | $\pm 20$       | $\mu\text{A}$                |
| $I_{IN,Z}$                                                     | High Z Input Current         |                                                                               | ● |       | $\pm 2$ |                | $\mu\text{A}$                |
| <b>Open Drain Outputs SDA, GPIO_CFG, GPIO_0, GPIO_1, ALERT</b> |                              |                                                                               |   |       |         |                |                              |
| $V_{OL}$                                                       | Output Low Voltage           | $I_{SINK} = 3\text{mA}$                                                       | ● |       |         | 0.4            | V                            |
| $I_{OH}$                                                       | Input Leakage Current        | $0\text{V} \leq V_{IN} \leq 6\text{V}$                                        | ● |       |         | $\pm 1$        | $\mu\text{A}$                |

# ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

| SYMBOL                                                 | PARAMETER                                                                             | CONDITIONS                                                                                                                                                                                                              |   | MIN      | TYP | MAX | UNITS         |
|--------------------------------------------------------|---------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|---|----------|-----|-----|---------------|
| <b>I<sup>2</sup>C Interface Timing Characteristics</b> |                                                                                       |                                                                                                                                                                                                                         |   |          |     |     |               |
| $f_{\text{SCL}}$                                       | Serial Clock Frequency                                                                | (Note 6)                                                                                                                                                                                                                | ● | 10       |     | 400 | kHz           |
| $t_{\text{LOW}}$                                       | Serial Clock Low Period                                                               | (Note 6)                                                                                                                                                                                                                | ● | 1.3      |     |     | $\mu\text{s}$ |
| $t_{\text{HIGH}}$                                      | Serial Clock High Period                                                              | (Note 6)                                                                                                                                                                                                                | ● | 0.6      |     |     | $\mu\text{s}$ |
| $t_{\text{BUF}}$                                       | Bus Free Time Between Stop and Start                                                  | (Note 6)                                                                                                                                                                                                                | ● | 1.3      |     |     | $\mu\text{s}$ |
| $t_{\text{HD,STA}}$                                    | Start Condition Hold Time                                                             | (Note 6)                                                                                                                                                                                                                | ● | 600      |     |     | ns            |
| $t_{\text{SU,STA}}$                                    | Start Condition Setup Time                                                            | (Note 6)                                                                                                                                                                                                                | ● | 600      |     |     | ns            |
| $t_{\text{SU,STO}}$                                    | Stop Condition Setup Time                                                             | (Note 6)                                                                                                                                                                                                                | ● | 600      |     |     | ns            |
| $t_{\text{HD,DAT}}$                                    | Data Hold Time (LTC2970 Receiving Data)<br>Data Hold Time (LTC2970 Transmitting Data) | (Note 6)                                                                                                                                                                                                                | ● | 0<br>300 |     | 900 | ns<br>ns      |
| $t_{\text{SU,DAT}}$                                    | Data Setup Time (LTC2970 Receiving Data)                                              | (Note 6)                                                                                                                                                                                                                | ● | 100      |     |     | ns            |
| $t_{\text{SP}}$                                        | Pulse Width of Spike Suppressed                                                       | (Note 6)                                                                                                                                                                                                                | ● |          | 98  |     | ns            |
| $t_{\text{SETUP\_GPIO}}$                               | GPIO_0 and GPIO_1 Setup Time                                                          | GPIO_0 and GPIO_1 input setup time prior to the 26th rising SCL of an IO() I <sup>2</sup> C read. These inputs must be valid and stable by this time to be returned in the IO() read result. (Note 6)                   | ● | 2.5      |     |     | $\mu\text{s}$ |
| $t_{\text{HOLD\_GPIO}}$                                | GPIO_0 and GPIO_1 Hold Time                                                           | GPIO_0 and GPIO_1 input hold time after the 26th rising SCL of an IO() I <sup>2</sup> C read. These inputs must be held until this amount of time has elapsed to be returned in the IO() read result. (Note 6)          | ● | 2.5      |     |     | $\mu\text{s}$ |
| $t_{\text{OUT\_GPIO}}$                                 | GPIO_0 and GPIO_1 Output Time                                                         | GPIO_0 and GPIO_1 output delay after the 35th rising SCL of an I <sup>2</sup> C write. These outputs will become high impedance or begin driving low by this time. (Note 6)                                             | ● |          |     | 2.5 | $\mu\text{s}$ |
| <b>Internal Timers</b>                                 |                                                                                       |                                                                                                                                                                                                                         |   |          |     |     |               |
| $t_{\text{TIMEOUT\_SMB}}$                              | Stuck BUS Timer                                                                       | The LTC2970 will release the I <sup>2</sup> C bus and terminate the current command if the command is not completed before this amount of time has elapsed.                                                             |   | 24       | 32  | 39  | ms            |
| $t_{\text{SETUP\_ADC}}$                                | ADC Channel Setup Time                                                                | After selecting a new ADC channel, the LTC2970 will wait this amount of time to allow the analog input to settle before beginning an ADC conversion.                                                                    |   |          | 304 |     | $\mu\text{s}$ |
| $t_{\text{TIMEOUT\_SYNC}}$                             | Tracking SYNC Failure Timer                                                           | LTC2970-1 Only: The LTC2970-1 will abort a pending SYNC() command if a tracking command is not received before this amount of time has elapsed.                                                                         |   |          | 255 |     | ms            |
| $t_{\text{HOLD\_TRACK}}$                               | Tracking IDAC Disconnect Delay                                                        | LTC2970-1 Only: After the tracking algorithm asserts CPIO_CFG low, the LTC2970-1 will delay disconnecting the IDACs from the power supply feedback nodes by this amount of time. Used while tracking power supplies on. |   |          | 32  |     | ms            |

# LTC2970/LTC2970-1

## ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at  $T_A = 25^\circ\text{C}$ .

| SYMBOL                    | PARAMETER                      | CONDITIONS                                                                                                                                                                                                   | MIN | TYP | MAX | UNITS                    |
|---------------------------|--------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----|-----|-----|--------------------------|
| $t_{\text{SETUP\_TRACK}}$ | Tracking IDAC Disconnect Delay | LTC2970-1 Only: After the tracking algorithm asserts CPIO_CFG high, the LTC2970-1 will wait this amount of time before starting to decrement Chn_a_delay_track[9:0]. Used while tracking power supplies off. |     | 32  |     | ms                       |
| $t_{\text{DEC\_TRACK}}$   | Tracking IDAC Decrement Rate   | LTC2970-1 Only: The LTC2970-1 changes Chn_a_delay_track[9:0] at this rate.                                                                                                                                   |     | 88  |     | $\mu\text{s}/\text{LSB}$ |

**Note 1:** Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

**Note 2:** All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to ground unless otherwise specified.

**Note 3:** TUE (%) is defined as:

$$\% \text{ Gain Error} + \frac{(\text{INL} \cdot 500\mu\text{V}/\text{LSB} + V_{\text{OS}}) \cdot 100}{V_{\text{IN}}}$$

**Note 4:** Integral nonlinearity (INL) is defined as the deviation of a code from a straight line passing through the actual endpoints (0V and 6V) of the transfer curve. The deviation is measured from the center of the quantization band.

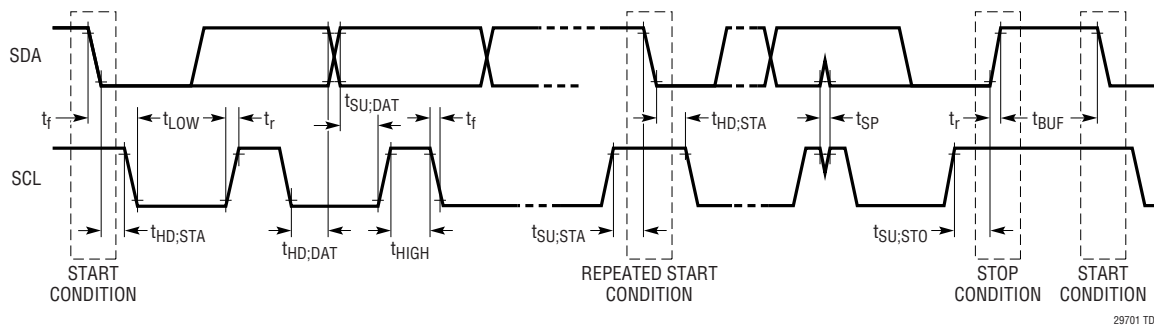
**Note 5:** Nonlinearity is defined from the first code that is greater than or equal to the maximum offset specification to code 255 (full-scale).

**Note 6:** Maximum capacitive load,  $C_B$ , for SCL and SDA is 400pF. Data and clock risetime ( $t_r$ ) and falltime ( $t_f$ ) are:  $(20 + 0.1 \cdot C_B)(\text{ns}) < t_r < 300\text{ns}$  and  $(20 + 0.1 \cdot C_B)(\text{ns}) < t_f < 300\text{ns}$ .  $C_B$  = capacitance of one bus line in pF. SCL and SDA external pull-up voltage,  $V_{\text{IO}}$ , is  $3\text{V} < V_{\text{IO}} < 5.5\text{V}$ .

**Note 7:** This specification is guaranteed by design.

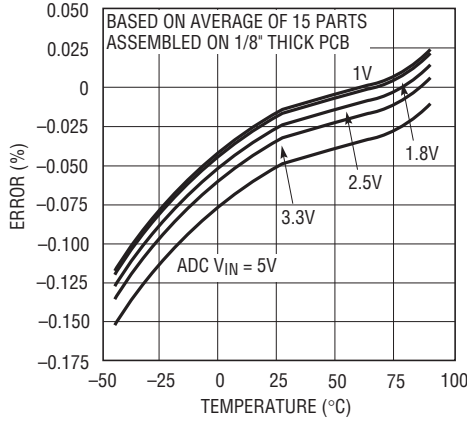
## TIMING DIAGRAM

The I<sup>2</sup>C Bus Specification



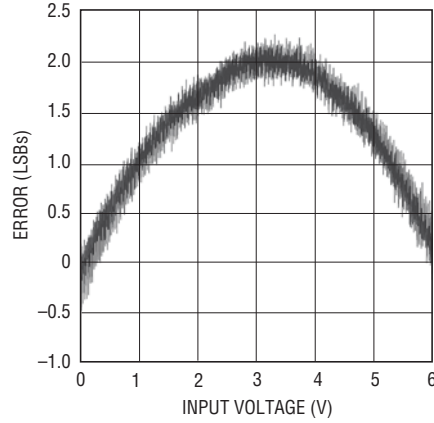
## TYPICAL PERFORMANCE CHARACTERISTICS

ADC Total Unadjusted Error vs Temperature



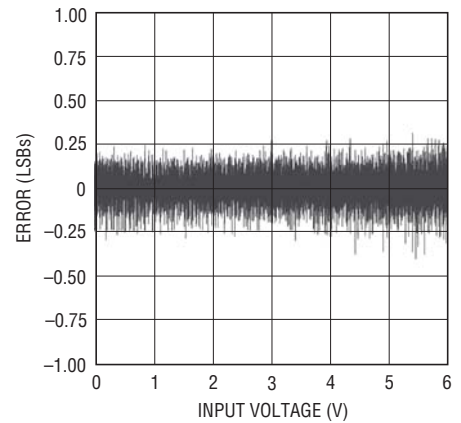
29701 G01

ADC INL



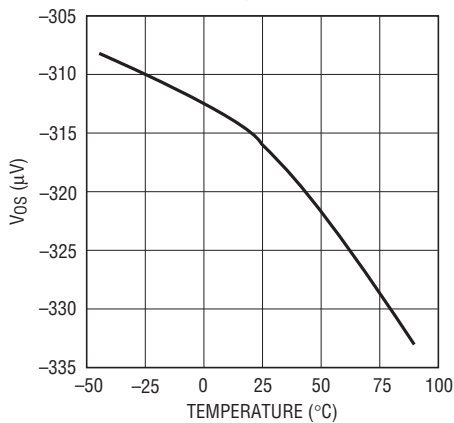
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ADC DNL

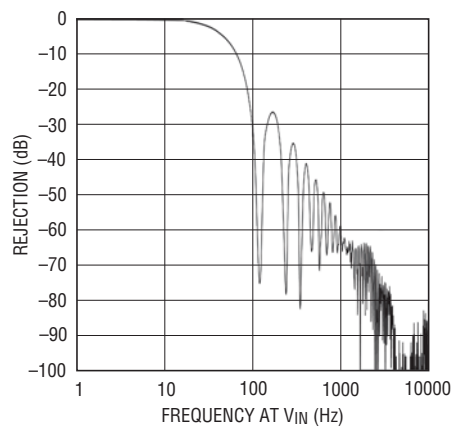


29701 G03

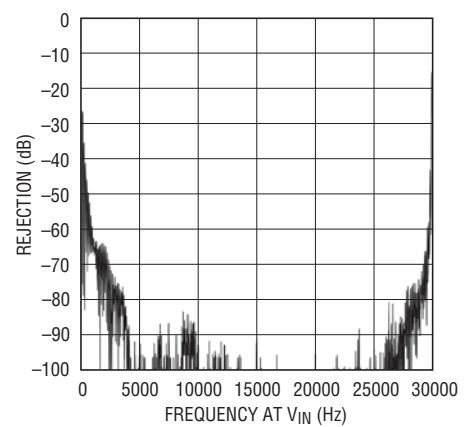
ADC Zero Code Center Offset Voltage vs Temperature



29701 G04

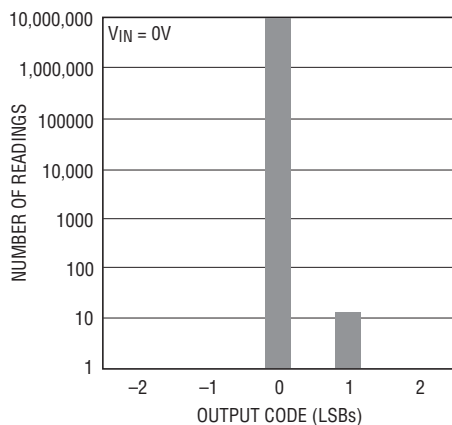
ADC Rejection vs Frequency at  $V_{IN}$ 

29701 G05

ADC Rejection vs Frequency at  $V_{IN}$ 

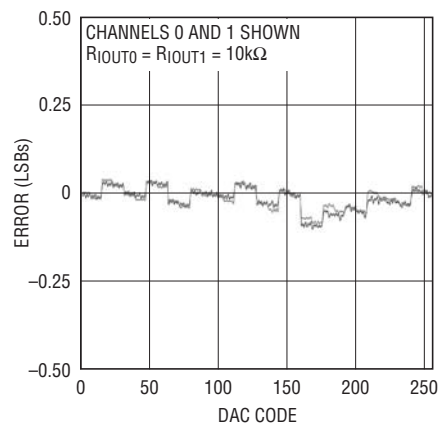
29701 G06

ADC Noise Histogram



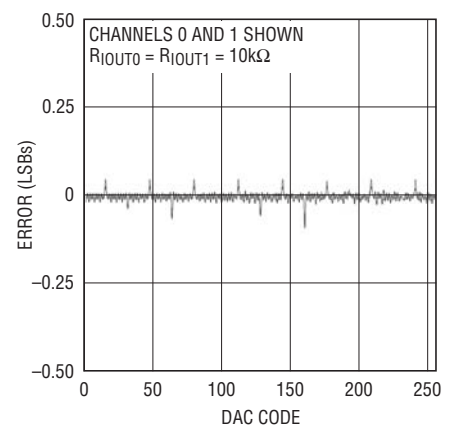
29701 G07

Voltage Buffered IDAC INL



29701 G08

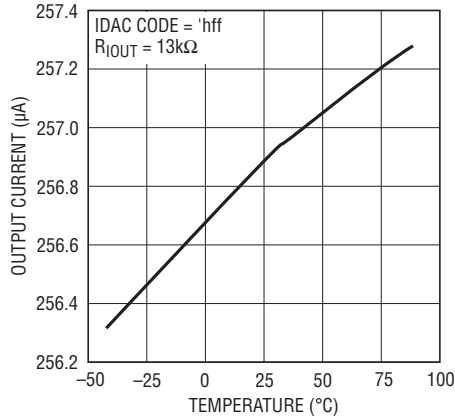
Voltage Buffered IDAC DNL



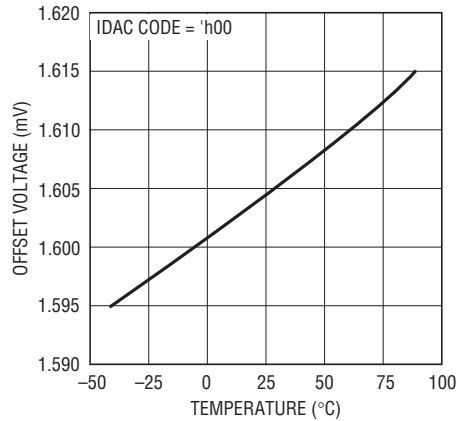
29701 G09

## TYPICAL PERFORMANCE CHARACTERISTICS

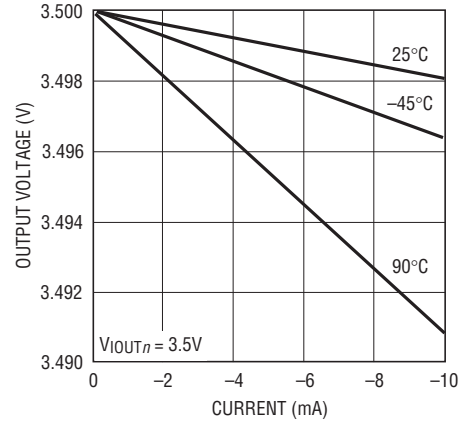
**IDAC Output Current vs Temperature**



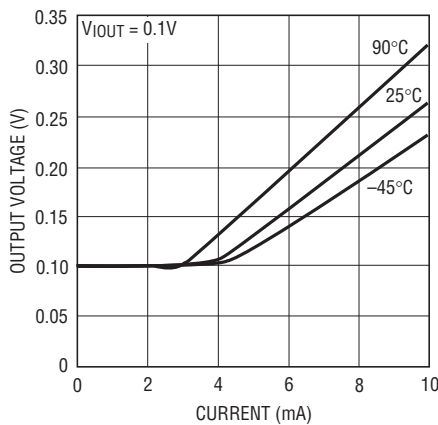
**V<sub>OUTn</sub> Offset Voltage vs Temperature**



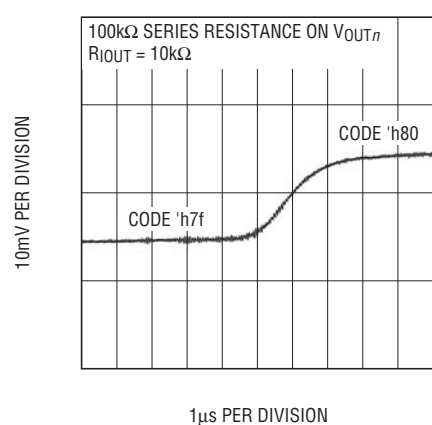
**Voltage Buffered IDAC Load Regulation Sourcing**



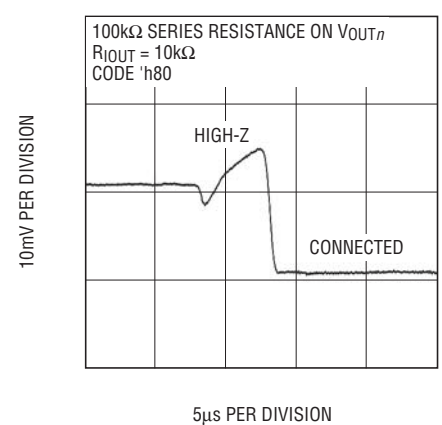
**Voltage Buffered IDAC Load Regulation Sinking**



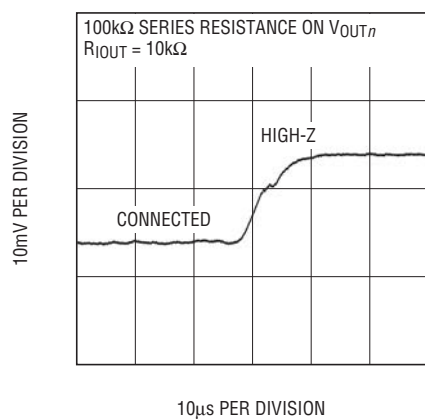
**Voltage Buffered IDAC Transient Response to 1LSB DAC Code Change**



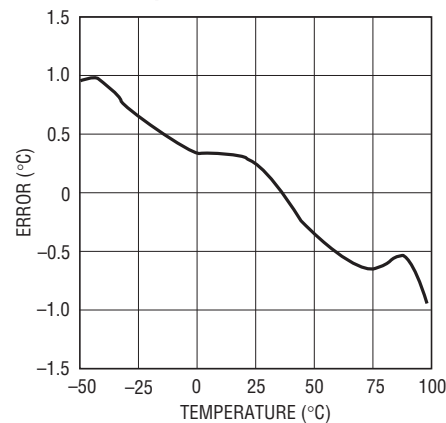
**Voltage Buffered IDAC Soft-Connect Transient Response**



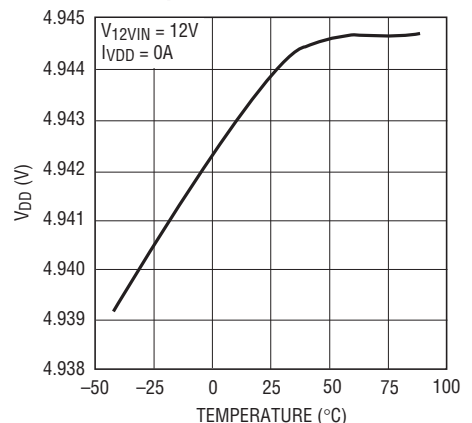
**Voltage Buffered IDAC Transient Response During Transition from On State to High-Z State**



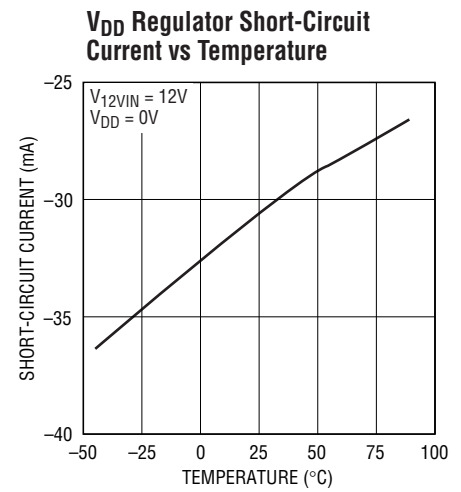
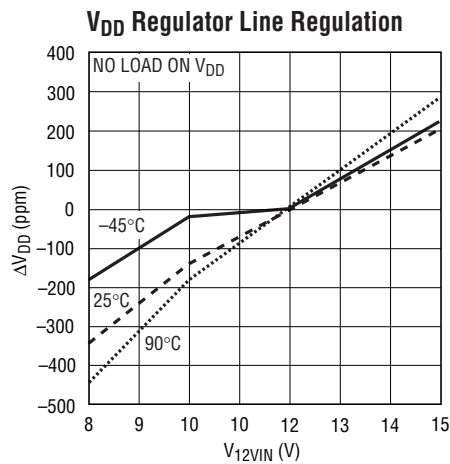
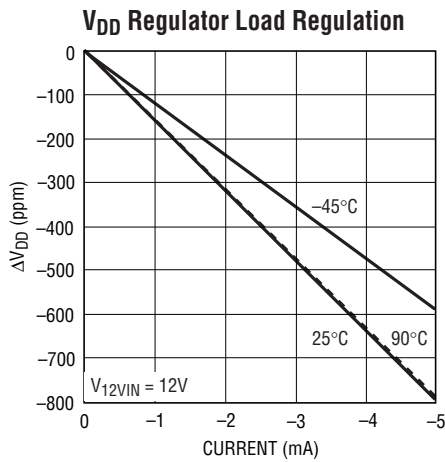
**Temperature Sensor Error vs Temperature**



**V<sub>DD</sub> Regulator Output Voltage vs Temperature**



## TYPICAL PERFORMANCE CHARACTERISTICS



## PIN FUNCTIONS

**V<sub>INO\_AP</sub> (Pin 1):** Positive CH0\_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0\_A can be configured to servo IDAC0.

**V<sub>INO\_AM</sub> (Pin 2):** Negative CH0\_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0\_A can be configured to servo IDAC0.

**V<sub>INO\_BP</sub> (Pin 3):** Positive CH0\_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0\_B is a voltage monitor input only.

**V<sub>INO\_BM</sub> (Pin 4):** Negative CH0\_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH0\_B is a voltage monitor input only.

**V<sub>IN1\_AP</sub> (Pin 5):** Positive CH1\_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1\_A can be configured to servo IDAC1.

**V<sub>IN1\_AM</sub> (Pin 6):** Negative CH1\_A ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1\_A can be configured to servo IDAC1.

**V<sub>IN1\_BP</sub> (Pin 7):** Positive CH1\_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1\_B is a voltage monitor input only.

**V<sub>IN1\_BM</sub> (Pin 8):** Negative CH1\_B ADC Multiplexer Input. The output of the differential, 7:1 multiplexer connects to the input of the ADC. CH1\_B is a voltage monitor input only.

**V<sub>DD</sub> (Pin 9):** V<sub>DD</sub> Power Supply, Voltage Monitor Input, and Internal 5V Regulator Output. The supply input range is 4.5V to 5.75V. The V<sub>DD</sub> pin voltage can be connected to the ADC through an internal mux. Bypass the V<sub>DD</sub> pin to device ground with a 100nF capacitor (C<sub>VDD</sub>). If no 5V input voltage supply is available, float the V<sub>DD</sub> pin and power the LTC2970 from the 12V<sub>IN</sub> pin.

**12V<sub>IN</sub> (Pin 10):** 12V Power Supply and Voltage Monitor Input. An internal regulator generates 5V from 12V<sub>IN</sub>. The input range for 12V<sub>IN</sub> is 8V to 15V. Bypass this pin with a 100nF capacitor. The regulator's output is connected to the V<sub>DD</sub> pin. The 12V<sub>IN</sub> pin voltage can also be monitored by the ADC through a 3:1 attenuator and the internal mux. If no 12V supply input is available, tie the 12V<sub>IN</sub> to the V<sub>DD</sub> pin and operate from 4.5V to 5.75V.

**V<sub>OUT0</sub> (Pin 11):** CH0 Voltage Output. Buffered version of IDAC0 output voltage.

## PIN FUNCTIONS

**V<sub>OUT1</sub> (Pin 12):** CH1 Voltage Output. Buffered version of IDAC1 output voltage.

**I<sub>OUT1</sub> (Pin 13):** IDAC1 Current Output. Connect a resistor between this pin and the point-of-load ground for channel 1. The IDAC sources between 0 and 255 $\mu$ A.

**I<sub>OUT0</sub> (Pin 14):** IDAC0 Current Output. Connect a resistor between this pin and the point-of-load ground for channel 0. The IDAC sources between 0 and 255 $\mu$ A.

**GPIO\_1 (Pin 15):** General Purpose Input or Open Drain Digital Output. GPIO\_1 can be configured as the IDAC Fault or Faults output, a digital input, or an open-drain digital output.

**GPIO\_0 (Pin 16):** General Purpose Input or Open Drain Digital Output. GPIO\_0 can be configured as the voltage monitor power-good or power-good bar output, a digital input, or a programmable open-drain output. Power good is the NOR of all instantaneous OV and UV faults; it does not include IDAC faults.

**$\overline{\text{ALERT}}$  (Pin 17):** Open Drain Digital Output. Connect the SMBALERT signal to this pin.  $\overline{\text{ALERT}}$  is asserted low when either IDAC0 or IDAC1 rails out (optional), or when one of the monitored voltages ventures outside its UV and OV thresholds (also optional).

**SCL (Pin 18):** Serial Bus Clock Input.

**SDA (Pin 19):** Serial Bus Data Input and Output.

**GPIO\_CFG (Pin 20):** GPIO Configuration Digital Input and Open Drain Output. Pulling GPIO\_CFG high will cause the GPIO\_0 and GPIO\_1 open-drain outputs to automatically assert low after a power-on reset. If GPIO\_CFG is pulled low, then GPIO\_0 and GPIO\_1 do not assert low after power-up.

**ASEL1 (Pin 21):** Slave Address Select Bit 1. Tie this pin to the V<sub>DD</sub> pin, ground, or float in order to select the address location (see Table 2).

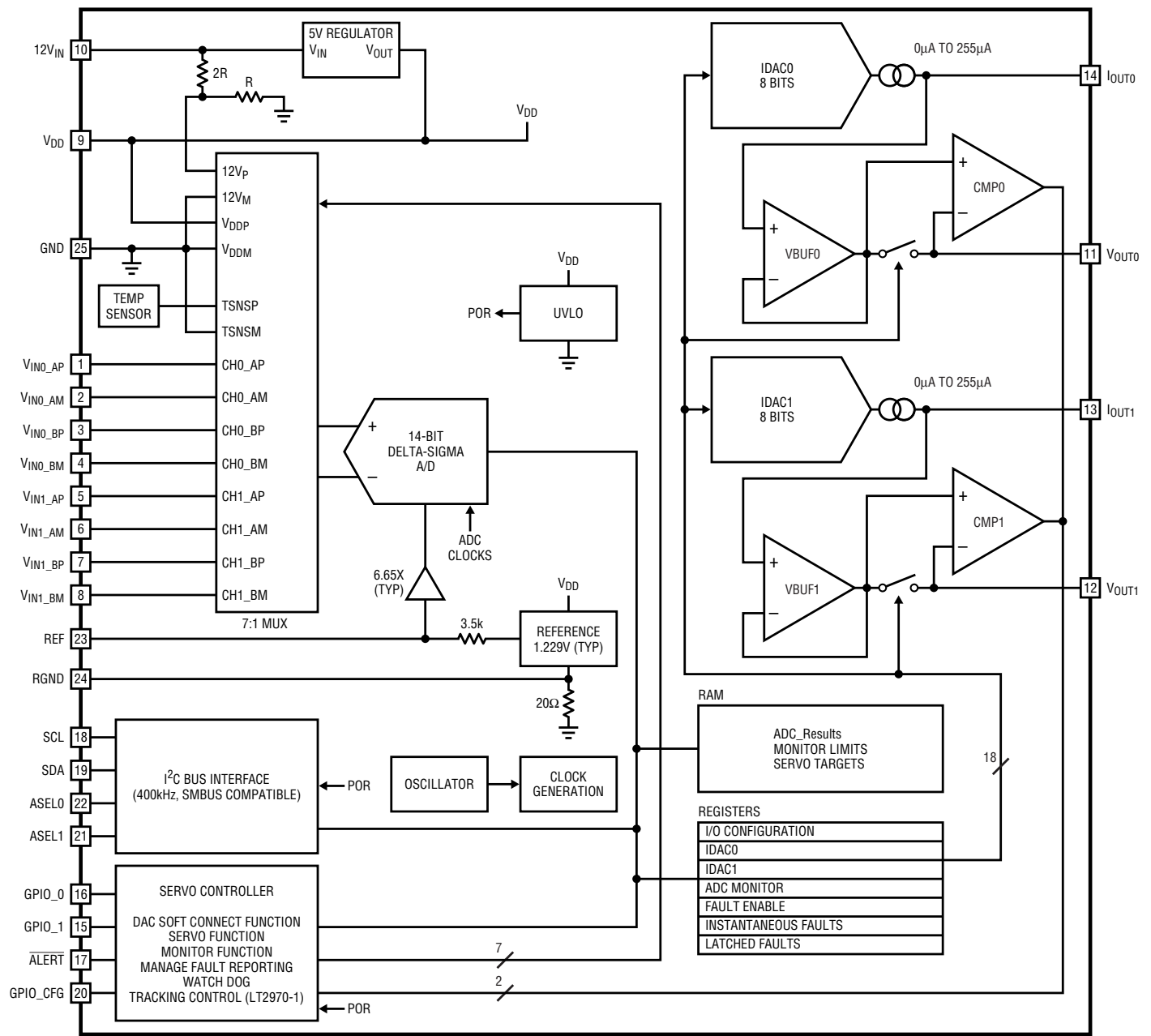
**ASEL0 (Pin 22):** Slave Address Select Bit 0. Tie this pin to the V<sub>DD</sub> pin, ground, or float in order to select the address location (see Table 2).

**REF (Pin 23):** Internal Reference Output or ADC Reference Overdrive Input. The voltage at this pin determines the full-scale input voltage of the delta-sigma ADC ( $V_{\text{FULL-SCALE}} = 6.65 \cdot V_{\text{REF}}$ , typically). An internal 3.5k resistor decouples the reference output from this pin. Bypass this pin to RGND with a 100nF capacitor ( $C_{\text{REF}}$ ).

**RGND (Pin 24):** Reference Ground. Connect to device ground.

**GND (Pin 25):** Device Ground. Must be soldered to ground.

## BLOCK DIAGRAM



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## OPERATION

### 1. LTC2970 Operation Overview

The LTC2970 is designed to control and monitor two power supplies. The LTC2970's superior accuracy allows it to precisely servo each supply's output voltage over a wide range of operating conditions; increasing accuracy, reducing power requirements and component costs. Margining may be performed with equal ease and precision. The monitoring functions allow for increased reliability by alerting a system host about incipient failures before they occur. The seven channel ADC may also be used to monitor current, temperature, and the 5V or optional 12V supply.

The LTC2970's unique architecture and control algorithm have been especially tailored for power supply management. The soft connect feature allows the LTC2970 to begin controlling a power supply without perturbing its initial value. The delta-sigma ADC architecture was specifically chosen to average out power-supply noise and allow the LTC2970 to ignore fast transients. Unlike discrete time DACs, the LTC2970's continuous time, voltage buffered IDAC is ideal for noise sensitive applications. The servo algorithm limits the IDAC step size to one LSB per iteration in order to minimize power supply transients. The point of load ground reference for the IDAC outputs minimize errors that would otherwise occur in a power system that experiences ground bounce. By selecting two resistor values, the user can choose the appropriate resolution while providing an important hardware range limit beyond which the supply may not be driven. The servo on fault option allows the LTC2970 to further reduce output voltage disturbances by only stepping the IDAC when the output voltage drifts outside of a user programmable window. The LTC2970 powers up in a high impedance state and will not interfere with default power supply operation. Similarly, powering down the LTC2970 will restore its high impedance state.

All communication with the LTC2970 is performed over an industry standard I<sup>2</sup>C bus. The LTC2970 I<sup>2</sup>C interface also meets all SMBus setup times, hold times, and timeout requirements. The ALERT pin may be used to signal that one or more of the fourteen configurable fault limits have been reached. Each fault may be individually masked. The I<sup>2</sup>C interface supports word reads, word writes and the SMBus Alert Response Address protocol. Two general purpose IO pins may be used to provide additional fault information or user defined system control. Powering down the LTC2970 will not interfere with I<sup>2</sup>C operation.

The LTC2970-1 enables power supply tracking and sequencing with the addition of a few external components. A special global address and synchronization command allow multiple LTC2970-1's to track and sequence multiple pairs of power supplies.

The LTC2970 can perform the following operations:

- Accept all programming commands and report status over the I<sup>2</sup>C or SMBus bus.
- Command each voltage buffered IDAC to connect to the corresponding power supply's feedback node through an external resistor using the IDAC code that most closely approximates the feedback node's regulation voltage (Soft Connect).
- Command each voltage buffered IDAC output to connect to the corresponding power supply's feedback node through an external resistor with a user-selected IDAC code (Hard Connect).
- Change the code of a previously connected IDAC.
- Disconnect each voltage buffered IDAC output from the power supply's feedback node.
- *LTC2970-1 Only:* Track two power supplies up or down. Multiple LTC2970-1's can be configured to track simultaneously or in a sequence.

## OPERATION

- Continuously servo one or both supplies to a programmed voltage.
- Perform a one-time servo of one or both supplies to a programmed voltage and hold the servo codes in the controlling IDAC.
- Perform a one time servo of one or both supplies to a programmed voltage and hold the code(s) in the controlling IDAC(s) until over/under voltage monitoring detects a fault, at which point a control bit may be used to allow the LTC2970 to servo back to the initial voltage target.
- Select any combination of seven possible ADC channels to be monitored by the ADC.
- Generate instantaneous faults based on user programmable over-voltage and under-voltage limits and fixed IDAC limits. The status of OR'd voltage limit faults and IDAC faults may be output over GPIO\_0 and GPIO\_1, respectively.
- Enable instantaneous faults to set associated latched faults using the FAULT\_EN register. The status of OR'd latched faults may be signalled using ALERT.
- Configure the GPIO\_0 and GPIO\_1 pins to act as inputs or outputs.

### 2. I<sup>2</sup>C Serial Digital Interface

The LTC2970 communicates with a host (master) using the 2-wire, I<sup>2</sup>C serial bus interface. The Timing Diagram shows the timing relationship of the signals on the bus.

The two bus lines, SDA and SCL, must be high when the bus is not in use. External pull-up resistors or current sources are required on these lines.

The LTC2970 I<sup>2</sup>C interface is SMBus compatible; it meets all SMBus setup times, hold times and timeout requirements.

The LTC2970 is a receive-only (slave) device. The LTC2970 can signal the host through the SMBALERT protocol that it wants to talk by asserting  $\overline{\text{ALERT}}$  low. The LTC2970 supports the three I<sup>2</sup>C protocols summarized in Table 1.

#### Slave Address

The LTC2970 can respond to one of nine 7-bit addresses. The two slave address select pins (ASEL1 and ASEL0) are programmed by the user and determine the slave address, as shown in Table 2.

The LTC2970 also supports the ARA address and a global address that allows multiple LTC2970s to be programmed with the same data simultaneously, as shown in Table 3.

**Table 1. Supported I<sup>2</sup>C Command Types**

#### READ DATA WORD:

S:ADR:W:A:CMD:A:Sr:ADR:R:A:DATA:A:DATA:NACK:P

#### WRITE DATA WORD:

S:ADR:W:A:CMD:A:DATA:A:DATA:A:P

#### ALERT RESPONSE

S:ARA:R:A:ADR:NACK:P:

## OPERATION

Table 2. LTC2970 Address Table

| ADDRESS[7:0]<br>(R/W = 0) | ADDRESS[7:1] | ASEL1 | ASEL0 |
|---------------------------|--------------|-------|-------|
| 8'hB8                     | 7'h5C        | L     | L     |
| 8'hBA                     | 7'h5D        | L     | F     |
| 8'hBC                     | 7'h5E        | L     | H     |
| 8'hBE                     | 7'h5F        | F     | L     |
| 8'hD6                     | 7'h6B        | F     | F     |
| 8'hD8                     | 7'h6C        | F     | H     |
| 8'hDA                     | 7'h6D        | H     | L     |
| 8'hDC                     | 7'h6E        | H     | F     |
| 8'hDE                     | 7'h6F        | H     | H     |

L:  $V_{ASEL1} < V_{IL\_ASEL}$  F: ASEL1 Floating H:  $V_{ASEL1} > V_{IH\_ASEL}$

Table 3. Special LTC2970 Addresses

|        | ADDRESS[7:0]<br>(R/W = 0) | ADDRESS[7:1] | FUNCTION                                                                                                                                 |
|--------|---------------------------|--------------|------------------------------------------------------------------------------------------------------------------------------------------|
| ARA    | 8'h18                     | 7'h0C        | This is the standard Alert Response Address for all SMBus devices. This address is independent of the value of the ASEL1 and ASEL0 pins. |
| Global | 8'hB6                     | 7'h5B        | This a global address to which all LTC2970s will respond. This address is independent of the value of the ASEL1 and ASEL0 pins.          |

### 3. Register Command Set

| COMMAND FUNCTION     | DESCRIPTION                                                         | R/W        | DATA LENGTH | COMMAND BYTE VALUE |
|----------------------|---------------------------------------------------------------------|------------|-------------|--------------------|
| FAULT()              | Instantaneous Fault Status For All Channels                         | Read Only  | 16 Bits     | 'h00               |
| FAULT_EN()           | Enable For All Latched Faults and Servo On Fault                    | Read/Write | 16 Bits     | 'h08               |
| FAULT_LA_INDEX()     | Index to All Latched Faults                                         | Read Only  | 16 Bits     | 'h10               |
| FAULT_LA()           | Latched Fault Status For All Channels                               | Read Only  | 16 Bits     | 'h11               |
| IO()                 | IO Control and Status Register                                      | Read/Write | 16 Bits     | 'h17               |
| ADC_MON()            | Control Register For Selecting ADC Channels to Monitor              | Read/Write | 16 Bits     | 'h18               |
| *SYNC()              | Control Register For Synchronizing Tracking Across Multiple Devices | Read/Write | 16 Bits     | 'h1F               |
| VDD_ADC()            | $V_{DDIN}$ ADC Conversion Result Register                           | Read Only  | 16 Bits     | 'h28               |
| VDD_OV()             | $V_{DDIN}$ Over-Voltage Monitor Control Register                    | Read/Write | 16 Bits     | 'h29               |
| VDD_UV()             | $V_{DDIN}$ Under-Voltage Monitor Control Register                   | Read/Write | 16 Bits     | 'h2A               |
| V12_ADC()            | $12V_{IN}$ ADC Conversion Result Register                           | Read Only  | 16 Bits     | 'h38               |
| V12_OV()             | $12V_{IN}$ Over-Voltage Monitor Control Register                    | Read/Write | 16 Bits     | 'h39               |
| V12_UV()             | $12V_{IN}$ Under-Voltage Monitor Control Register                   | Read/Write | 16 Bits     | 'h3A               |
| CH0_A_ADC()          | CH0_A ADC Conversion Result Register                                | Read Only  | 16 Bits     | 'h40               |
| CH0_A_OV()           | CH0_A Over-Voltage Monitor Control Register                         | Read/Write | 16 Bits     | 'h41               |
| CH0_A_UV()           | CH0_A Under-Voltage Monitor Control Register                        | Read/Write | 16 Bits     | 'h42               |
| CH0_A_SERVO()        | CH0_A Voltage Servo Control Register                                | Read/Write | 16 Bits     | 'h43               |
| CH0_A_IDAC()         | CH0_A IDAC Control Register                                         | Read/Write | 16 Bits     | 'h44               |
| *CH0_A_IDAC_TRACK()  | CH0_A IDAC Track Final Value Register                               | Read/Write | 16 Bits     | 'h45               |
| *CH0_A_DELAY_TRACK() | CH0_A IDAC Track Delay Register                                     | Read/Write | 16 Bits     | 'h46               |
| CH0_B_ADC()          | CH0_B ADC Conversion Result Register                                | Read Only  | 16 Bits     | 'h48               |
| CH0_B_OV()           | CH0_B Over-Voltage Monitor Control Register                         | Read/Write | 16 Bits     | 'h49               |
| CH0_B_UV()           | CH0_B Under-Voltage Monitor Control Register                        | Read/Write | 16 Bits     | 'h4A               |
| CH1_A_ADC()          | CH1_A ADC Conversion Result Register                                | Read Only  | 16 Bits     | 'h50               |
| CH1_A_OV()           | CH1_A Over-Voltage Monitor Control Register                         | Read/Write | 16 Bits     | 'h51               |
| CH1_A_UV()           | CH1_A Under-Voltage Monitor Control Register                        | Read/Write | 16 Bits     | 'h52               |

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## OPERATION

### 3. Register Command Set (Cont.)

| COMMAND FUNCTION     | DESCRIPTION                                                                             | R/W        | DATA LENGTH | COMMAND BYTE VALUE |
|----------------------|-----------------------------------------------------------------------------------------|------------|-------------|--------------------|
| CH1_A_SERVO()        | CH1_A Voltage Servo Control Register                                                    | Read/Write | 16 Bits     | 'h53               |
| CH1_A_IDAC()         | CH1_A IDAC Control Register                                                             | Read/Write | 16 Bits     | 'h54               |
| *CH1_A_IDAC_TRACK()  | CH1_A IDAC Track Control Register                                                       | Read/Write | 16 Bits     | 'h55               |
| *CH1_A_DELAY_TRACK() | CH1_A IDAC Track Delay Register                                                         | Read/Write | 16 Bits     | 'h56               |
| CH1_B_ADC()          | CH1_B ADC Conversion Result Register                                                    | Read Only  | 16 Bits     | 'h58               |
| CH1_B_OV()           | CH1_B Over-Voltage Monitor Control Register                                             | Read/Write | 16 Bits     | 'h59               |
| CH1_B_UV()           | CH1_B Under-Voltage Monitor Control Register                                            | Read/Write | 16 Bits     | 'h5A               |
| TEMP_ADC()           | Temperature ADC Conversion Result Register                                              | Read/Write | 16 Bits     | 'h68               |
| RESERVED()           | All other commands are reserved for future expansion and should not be written or read. | Read/Write | 16 Bits     | 'hXX               |

\*LTC2970-1 Only. LTC2970 will not acknowledge these commands.

### 4. Detailed I<sup>2</sup>C Command Register Descriptions

#### FAULT: Instantaneous Fault Register – Read

| BIT(s)   | SYMBOL           | OPERATION                                                                                                                                                  |
|----------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[0]     | Fault_ch0_a_ov   | 0 = The associated channel is clear of instantaneous faults.                                                                                               |
| b[1]     | Fault_ch0_a_uv   |                                                                                                                                                            |
| b[2]     | Fault_ch0_a_idac | 1 = The associated channel has an instantaneous fault.                                                                                                     |
| b[3]     | Fault_ch0_b_ov   |                                                                                                                                                            |
| b[4]     | Fault_ch0_b_uv   | The reported faults are instantaneous and not latched. When used in conjunction with latched faults they may indicate faults that are transient in nature. |
| b[5]     | Fault_ch1_a_ov   |                                                                                                                                                            |
| b[6]     | Fault_ch1_a_uv   |                                                                                                                                                            |
| b[7]     | Fault_ch1_a_idac |                                                                                                                                                            |
| b[8]     | Fault_ch1_b_ov   |                                                                                                                                                            |
| b[9]     | Fault_ch1_b_uv   |                                                                                                                                                            |
| b[10]    | Fault_vdd_ov     |                                                                                                                                                            |
| b[11]    | Fault_vdd_uv     |                                                                                                                                                            |
| b[12]    | Fault_v12_ov     |                                                                                                                                                            |
| b[13]    | Fault_v12_uv     |                                                                                                                                                            |
| b[15:14] | Reserved         | Always Returns 0                                                                                                                                           |

#### FAULT\_EN: Fault Enabling Register – Read/Write

| BIT(s) | SYMBOL               | OPERATION                                                                                                                                                                                                                                                                 |
|--------|----------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[0]   | Fault_en_ch0_a_ov    | 0 = The associated bit in the FAULT_LA register will always be 0. (default)<br><br>1 = Instantaneous faults reported in the FAULT register will set associated bit in the FAULT_LA register.                                                                              |
| b[1]   | Fault_en_ch0_a_uv    |                                                                                                                                                                                                                                                                           |
| b[2]   | Fault_en_ch0_a_idac  |                                                                                                                                                                                                                                                                           |
| b[3]   | Fault_en_ch0_b_ov    |                                                                                                                                                                                                                                                                           |
| b[4]   | Fault_en_ch0_b_uv    |                                                                                                                                                                                                                                                                           |
| b[5]   | Fault_en_ch1_a_ov    |                                                                                                                                                                                                                                                                           |
| b[6]   | Fault_en_ch1_a_uv    |                                                                                                                                                                                                                                                                           |
| b[7]   | Fault_en_ch1_a_idac  |                                                                                                                                                                                                                                                                           |
| b[8]   | Fault_en_ch1_b_ov    |                                                                                                                                                                                                                                                                           |
| b[9]   | Fault_en_ch1_b_uv    |                                                                                                                                                                                                                                                                           |
| b[10]  | Fault_en_vdd_ov      |                                                                                                                                                                                                                                                                           |
| b[11]  | Fault_en_vdd_uv      |                                                                                                                                                                                                                                                                           |
| b[12]  | Fault_en_v12_ov      |                                                                                                                                                                                                                                                                           |
| b[13]  | Fault_en_v12_uv      |                                                                                                                                                                                                                                                                           |
| b[14]  | Fault_en_ch0_a_servo | 0 = Do not re-servo CH0_A in response to instantaneous OV or UV fault.<br><br>1 = Repeat a one time servo of CH0_A in response to instantaneous OV or UV fault. CH0_A must have servo operation enabled with Ch0_a_idac_servo_repeat set low, and Adc_mon_ch0_a set high. |
| b[15]  | Fault_en_ch1_a_servo |                                                                                                                                                                                                                                                                           |

## OPERATION

### 4. Detailed I<sup>2</sup>C Command Register Descriptions (Cont.)

#### FAULT\_INDEX: Latched Fault Index Register – Read

| BITS(s) | SYMBOL         | OPERATION                                                                                                                                                                                                                            |
|---------|----------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[0]    | Fault_la_index | 0 = All faults indicated by FAULT_LA are clear.<br>1 = One or more faults indicated by FAULT_LA are set.<br><br>This register allows a summary of all latched faults to be viewed in a single read without resetting latched faults. |
| b[15:1] | Reserved       | Always Returns 0                                                                                                                                                                                                                     |

#### FAULT\_LA: Latched Fault Register – Read

| BITS(s)  | SYMBOL              | OPERATION                                                                                                                                                                                                                                          |
|----------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[0]     | Fault_la_ch0_a_ov   | 0 = The associated channel is clear of faults.<br>1 = The associated channel has faulted and is enabled.                                                                                                                                           |
| b[1]     | Fault_la_ch0_a_uv   |                                                                                                                                                                                                                                                    |
| b[2]     | Fault_la_ch0_a_idac | The latched faults are set and held when the associated channel's instantaneous fault has occurred with faults enabled. Clearing the enable bit for the associated channel in FAULT_EN will immediately clear its corresponding latched fault bit. |
| b[3]     | Fault_la_ch0_b_ov   |                                                                                                                                                                                                                                                    |
| b[4]     | Fault_la_ch0_b_uv   | All latched channel faults are cleared when this register is read. They may be set again if the instantaneous fault condition and fault_en have not changed.                                                                                       |
| b[5]     | Fault_la_ch1_a_ov   |                                                                                                                                                                                                                                                    |
| b[6]     | Fault_la_ch1_a_uv   |                                                                                                                                                                                                                                                    |
| b[7]     | Fault_la_ch1_a_idac |                                                                                                                                                                                                                                                    |
| b[8]     | Fault_la_ch1_b_ov   |                                                                                                                                                                                                                                                    |
| b[9]     | Fault_la_ch1_b_uv   |                                                                                                                                                                                                                                                    |
| b[10]    | Fault_la_vdd_ov     |                                                                                                                                                                                                                                                    |
| b[11]    | Fault_la_vdd_uv     |                                                                                                                                                                                                                                                    |
| b[12]    | Fault_la_v12_ov     |                                                                                                                                                                                                                                                    |
| b[13]    | Fault_la_v12_uv     |                                                                                                                                                                                                                                                    |
| b[15:14] | Reserved            | Always Returns 0                                                                                                                                                                                                                                   |

#### IO: Input/Output Data and General Purpose Control Register – Read/Write unless specified otherwise.

| BITS(s)  | SYMBOL         | OPERATION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
|----------|----------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[1:0]   | lo_cfg_0[1:0]  | lo_cfg_0[1:0] is used to configure the function of the GPIO_0 pin and IO(lo_gpio_0).<br>00: lo_gpio_0 = GPIO_0 = Power_good. Power_good asserts high if there are no instantaneous over-voltage or under-voltage faults.<br>01: lo_gpio_0 = GPIO_0 = Power_good_bar. Power_good_bar is the complement of Power_good.<br>10: GPIO_0 is a general-purpose open-drain output and mirrors the value written to lo_gpio_0 (default).<br>11: GPIO_0 is a general-purpose digital input with lo_gpio_0 = GPIO_0 |
| b[3:2]   | lo_cfg_1[1:0]  | lo_cfg_1[1:0] is used to configure the function of the GPIO_1 pin and IO(lo_gpio_1).<br>00: lo_gpio_1 = GPIO_1 = Idac_fault. Idac_fault asserts if either IDAC value is faulted (Chn_idac[7:0] = 8'h00 or 8'hff)<br>01: lo_gpio_1 = GPIO_1 = Idac_fault_bar. Idac_fault_bar is the complement of Idac_fault.<br>10 = GPIO_1 is a general-purpose open-drain output and mirrors the value written to lo_gpio_1 (default).<br>11 = GPIO_1 is a general-purpose digital input with lo_gpio_1 = GPIO_1       |
| b[4]     | lo_gpio_0      | See lo_cfg_0.<br>If the GPIO_CFG pin is pulled-high during a power on reset, lo_gpio_0 is cleared and the GPIO_0 open-drain output will assert low.                                                                                                                                                                                                                                                                                                                                                      |
| b[5]     | lo_gpio_1      | See lo_cfg_1.<br>If the GPIO_CFG pin is pulled-high during a power on reset, lo_gpio_1 is cleared and the GPIO_1 open-drain output will assert low.                                                                                                                                                                                                                                                                                                                                                      |
| b[6]     | lo_alertb      | Mirrors the value of the ALERT pin.<br>Read only.                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| b[7]     | lo_alertb_enb  | 1 = ALERT pin never asserts (default).<br>0 = ALERT pin asserts low when one or more FAULT_LA bits are set.                                                                                                                                                                                                                                                                                                                                                                                              |
| b[8]     | lo_i2c_adc_wen | 1 = Special test mode that inhibits ADC from writing to ADC result register and allows user to update registers over the I <sup>2</sup> C serial interface.<br>0 = Normal operation (default).                                                                                                                                                                                                                                                                                                           |
| b[9]     | lo_gpio_cfg    | Read only. GPIO_CFG digital input and open-drain output. Reading this bit returns the current state of the GPIO_CFG pin voltage.                                                                                                                                                                                                                                                                                                                                                                         |
| b[10]    | lo_track_start | Writing a 1 to this bit will start tracking all enabled channels. Returns a 1 when tracking is pending (LTC2970-1). Reserved on LTC2970 and always returns 0.                                                                                                                                                                                                                                                                                                                                            |
| b[15:11] | Reserved       | Always Returns 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |

## OPERATION

### 4. Detailed I<sup>2</sup>C Command Register Descriptions (Cont.)

#### ADC\_MON: ADC Monitoring Mux Control Register – Read/Write

| BIT(s)  | SYMBOL        | OPERATION                                                                                                       |
|---------|---------------|-----------------------------------------------------------------------------------------------------------------|
| b[0]    | Adc_mon_vdd   | 0 = ADC will not convert associated channel. (Default)<br>1 = ADC will continuously convert associated channel. |
| b[1]    | Adc_mon_v12   |                                                                                                                 |
| b[2]    | Adc_mon_ch0_a |                                                                                                                 |
| b[3]    | Adc_mon_ch0_b |                                                                                                                 |
| b[4]    | Adc_mon_ch1_a |                                                                                                                 |
| b[5]    | Adc_mon_ch1_b |                                                                                                                 |
| b[6]    | Adc_mon_temp  |                                                                                                                 |
| b[15:7] | Reserved      | Always Returns 0                                                                                                |

#### SYNC: Tracking Synchronization Control Register – Read/Write LTC2970-1 Only

| BIT(s)  | SYMBOL     | OPERATION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
|---------|------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[0]    | Sync_track | Write<br>0 = Do not synchronize.<br>1 = Synchronize all tracking enabled registers to the same starting point.<br><br>Read<br>0 = The LTC2970-1 is not synchronized for tracking (default).<br>1 = The LTC2970-1 is synchronized for tracking.<br><br>Use of the global address will allow the synchronization status of multiple LTC2970-1s to be verified in a single read; since a one can only be returned if all LTC2970-1s are synchronized. The IO_track_start command may then be issued with the same global address to begin synchronized tracking across multiple ICs. |
| b[15:1] | Reserved   | Always Returns 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  |

#### VDD\_ADC, V12\_ADC, CH0\_A\_ADC, CH0\_B\_ADC, CH1\_A\_ADC, CH1\_B\_ADC, and TEMP\_ADC: ADC Conversion Result Registers – Read Only Unless Specified Otherwise

| BIT(s)  | SYMBOL                                                                                                                       | OPERATION                                                                                                                                                                                                                                                                                    |
|---------|------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[14:0] | Vdd_adc[14:0]<br>V12_adc[14:0]<br>Ch0_a_adc[14:0]<br>Ch0_b_adc[14:0]<br>Ch1_a_adc[14:0]<br>Ch1_b_adc[14:0]<br>Temp_adc[14:0] | Measured data from ADC conversion.<br>'h4000 corresponds to negative full-scale input voltage.<br>'h0000 corresponds to 0V.<br>'h3fff corresponds to full-scale input voltage.<br>2's complement format, b[14] = sign.<br>Read/Write when lo_i2c_adc_wen = 1.<br>Default value is undefined. |
| b[15]   | Vdd_adc_new<br>V12_adc_new<br>Ch0_a_adc_new<br>Ch0_b_adc_new<br>Ch1_a_adc_new<br>Ch1_b_adc_new<br>Temp_adc_new               | 1 = The ADC has updated the associated result register since the last time the data was read.<br>0 = Previously read data. (Default)                                                                                                                                                         |

#### VDD\_OV, V12\_OV, CH0\_A\_OV, CH0\_B\_OV, CH1\_A\_OV, CH1\_B\_OV: Over Voltage Limit Registers – Read/Write

| BIT(s)  | SYMBOL                                                                                               | OPERATION                                                                                                                                                                                                                                                                                             |
|---------|------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[14:0] | Vdd_ov[14:0]<br>V12_ov[14:0]<br>Ch0_a_ov[14:0]<br>Ch0_b_ov[14:0]<br>Ch1_a_ov[14:0]<br>Ch1_b_ov[14:0] | ADC over-voltage threshold limit.<br>The associated instantaneous over voltage fault is asserted if the channel's ADC result is greater than this limit.<br>Code 'h3fff disables OV threshold detect feature for that channel.<br>2's complement format, b[14] = sign.<br>Default value is undefined. |
| b[15]   | Reserved                                                                                             | Always Returns 0                                                                                                                                                                                                                                                                                      |

#### VDD\_UV, V12\_UV, CH0\_A\_UV, CH0\_B\_UV, CH1\_A\_UV, CH1\_B\_UV: Under Voltage Limit Registers – Read/Write

| BIT(s)  | SYMBOL                                                                                               | OPERATION                                                                                                                                                                                                                                                                                               |
|---------|------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[14:0] | Vdd_uv[14:0]<br>V12_uv[14:0]<br>Ch0_a_uv[14:0]<br>Ch0_b_uv[14:0]<br>Ch1_a_uv[14:0]<br>Ch1_b_uv[14:0] | ADC under-voltage threshold limit.<br>The associated instantaneous under voltage fault is asserted if the channel's ADC result is greater than this limit.<br>Code 'h4000 disables UV threshold detect feature for that channel.<br>2's complement format, b[14] = sign.<br>Default value is undefined. |
| b[15]   | Reserved                                                                                             | Always Returns 0                                                                                                                                                                                                                                                                                        |

## OPERATION

### 4. Detailed I<sup>2</sup>C Command Register Descriptions (Cont.)

#### CH0\_A\_SERVO, CH1\_A\_SERVO: Voltage Servo Control Registers – Read/Write

| BIT(s)  | SYMBOL                                 | OPERATION                                                                                                                                                                                                                     |
|---------|----------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[14:0] | Ch0_a_servo[14:0]<br>Ch1_a_servo[14:0] | During servo operation<br>Chn_a_idac[7:0] output current is stepped to force Chn_a_adc[14:0] code to equal target code stored in Chn_a_servo[14:0].<br><br>2's complement format, b[14] = sign<br>Default value is undefined. |
| b[15]   | Ch0_a_servo_en<br>Ch1_a_servo_en       | 0 = Chn_a servo disabled (default).<br>1 = Chn_a servo enabled.                                                                                                                                                               |

#### CH0\_A\_IDAC, CH1\_A\_IDAC: IDAC Control/Data Registers – Read/Write

| BIT(s) | SYMBOL                             | OPERATION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      |
|--------|------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[7:0] | Ch0_a_idac[7:0]<br>Ch1_a_idac[7:0] | Chn_a IDAC data value.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| b[8]   | Ch0_a_idac_en<br>Ch1_a_idac_en     | 0 = V <sub>OUTn</sub> output tri-stated.<br>1 = V <sub>OUTn</sub> output enabled.<br>There are two ways to enable V <sub>OUTn</sub> .<br>1) When Chn_a_idac_en is set high with Chn_a_idac_con low, the LTC2970 will perform a soft connect. During a soft connect, the V <sub>OUTn</sub> voltage buffer output will not be connected to the V <sub>OUTn</sub> pin until the internal algorithm has servo'd the voltage at the IDACn pin to match the V <sub>OUTn</sub> pin voltage. Resolution is one Chn_a_idac LSB.<br>2) When Chn_a_idac_en is enabled with Chn_a_idac_con high, the LTC2970 will perform a hard connect. The V <sub>OUTn</sub> voltage buffer will be immediately connected to the V <sub>OUTn</sub> pin. |
| b[9]   | Ch0_a_idac_con<br>Ch1_a_idac_con   | 0 = V <sub>OUTn</sub> is not enabled or has been enabled but is not yet connected to the output of the CHn voltage buffer. (Default)<br>1 = V <sub>OUTn</sub> is enabled and has been connected to the output of the CHn voltage buffer.<br>See Chn_a_idac_en for additional information.                                                                                                                                                                                                                                                                                                                                                                                                                                      |

|          |                                                    |                                                                                                                                                                                                                                                                                                                                                                                                             |
|----------|----------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| b[10]    | Ch0_a_idac_pol<br>Ch1_a_idac_pol                   | 0 = Use this setting when increasing V <sub>OUTn</sub> causes (VIN <sub>n</sub> _AP-VIN <sub>n</sub> _AM) to decrease. Inverting configuration common to DC/DC converters with external feedback networks.<br>1 = Use this setting when increasing V <sub>OUTn</sub> causes (VIN <sub>n</sub> _AP-VIN <sub>n</sub> _AM) to increase. Non-inverting configuration common to DC/DC converters with trim pins. |
| b[11]    | Ch0_a_idac_servo_repeat<br>Ch1_a_idac_servo_repeat | 0 = During servo operation, servo Chn_a until the measured result is stable and matches the target code.<br>1 = During servo operation, continuously servo Chn_a to the target code.                                                                                                                                                                                                                        |
| b[15:12] | Reserved                                           | Always Returns 0                                                                                                                                                                                                                                                                                                                                                                                            |

#### CH0\_A\_IDAC\_TRACK and CH1\_A\_IDAC\_TRACK: IDAC Tracking data and control registers – Read/Write LTC2970-1 Only

| BIT(s)  | SYMBOL                                         | OPERATION                                                                                                                                    |
|---------|------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------|
| b[7:0]  | Ch0_a_idac_track[7:0]<br>Ch1_a_idac_track[7:0] | Final target value for of Chn_a_idac[7:0]. During tracking, Chn_a_idac[7:0] is incremented/decremented by 1 until it is equal to this value. |
| b[8]    | Ch0_a_idac_track_en<br>Ch1_a_idac_track_en     | 0 = inhibit tracking of Chn_a_idac[7:0].<br>1 = enable tracking of Chn_a_idac[7:0]                                                           |
| b[15:9] | Reserved                                       | Always Returns 0                                                                                                                             |

#### CH0\_A\_DELAY\_TRACK and CH1\_A\_DELAY\_TRACK: IDAC Tracking delay register – Read/Write LTC2970-1 Only

| BIT(s)   | SYMBOL                                           | OPERATION                                            |
|----------|--------------------------------------------------|------------------------------------------------------|
| b[9:0]   | Ch0_a_delay_track[9:0]<br>Ch1_a_delay_track[9:0] | Delay used to synchronize or offset tracking events. |
| b[15:10] | Reserved                                         | Always Returns 0                                     |

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### 5. Soft Connecting the LTC2970 to the Power Supply Feedback Node

The soft connect feature allows the LTC2970 to connect to the power supply's feedback node with minimal disturbance to the supply's output voltage. This is accomplished by comparing the buffered voltage of  $I_{OUTn}$  to the voltage at  $V_{OUTn}$  and incrementing or decrementing  $Chn\_a\_idac[7:0]$  until the comparator output ( $COMPn$ ) changes. The value of  $Chn\_a\_idac[7:0]$  when the comparator transitions is the appropriate value for a soft connect. The voltage buffer output is only connected to  $V_{OUTn}$  if the IDAC reaches this soft connect value without generating an instantaneous IDAC fault ( $Fault\_chn\_a\_idac$ ).

#### *Soft-Connect Procedure:*

Determine the appropriate polarity for  $Chn\_a\_idac\_pol$ . Select  $Chn\_a\_idac\_pol = 1$  if incrementing  $V_{OUTn}$  causes differential voltage ( $V_{INn\_AP} - V_{INn\_AM}$ ) to increase. When properly programmed, lowering the value in  $Chn\_a\_idac[7:0]$  will always cause the output of the controlled power supply to decrease.

Ensure that the channel's IDAC is not currently enabled for connection, i.e., the  $Chn\_a\_idac\_en$  bit must be 0.

Update  $CHn\_A\_IDAC()$  with  $Chn\_a\_idac\_pol$ ,  $Chn\_a\_idac\_con = 0$ ,  $Chn\_a\_idac\_en = 1$ , and  $Chn\_a\_idac[7:0] = 0x80$ . The value programmed into  $Chn\_a\_idac[7:0]$  is ignored and  $Chn\_a\_idac[7:0]$  is initially set to  $8'h80$ .

The LTC2970 will now ramp  $Chn\_a\_idac[7:0]$  while monitoring the output of the soft connect comparator. If the soft connect comparator trips, the LTC2970 will connect the output of  $V_{BUFn}$  to  $V_{OUTn}$  and set  $Chn\_a\_idac\_con$  high. If the soft connect comparator does not trip before the IDAC value reaches 'h00 or 'hFF, then the soft connection will fail, an IDAC fault will be indicated ( $Fault\_chn\_a\_idac$ ), and  $Chn\_a\_idac\_con$  will remain low.

#### *Soft-Connect Rules:*

When both channels are requesting a soft connect, channel 0 has priority.

Soft connect requests will be ignored and the user will not be able to change  $Chn\_a\_idac\_pol$  or  $Chn\_a\_idac[7:0]$  if the LTC2970 is servicing a previously issued soft connect

on that channel or the previously issued soft connect failed with an IDAC fault ( $Fault\_chn\_a\_idac = 1$ ). Recall that the  $Chn\_a\_idac\_en$  bit must initially have been set to 0.

*LTC2970-1 Only:* Soft connect requests will be ignored and the user will not be able to change  $Chn\_a\_idac\_pol$  or  $Chn\_a\_idac[7:0]$  if  $GPIO\_CFG$  is high and either  $GPIO\_0$  or  $GPIO\_1$  are high.

*LTC2970-1 Only:* Soft connect requests will be ignored and the user will not be able to change the  $Chn\_a\_idac\_pol$  bit if there is a pending tracking operation.

### 6. Hard Connecting the LTC2970 to the Power Supply Trim Pin

The hard connect feature allows the LTC2970 to bypass the soft connect algorithm and connect directly to the power supply's feedback node using the value programmed into  $Chn\_a\_idac[7:0]$ . This feature is useful for systems that have calculated or measured an acceptable voltage at which to connect the IDAC's buffered voltage  $V_{BUFn}$  to  $V_{OUTn}$ .

#### *Hard Connect Procedure:*

Determine the appropriate polarity for  $Chn\_a\_idac\_pol$ . Select  $Chn\_a\_idac\_pol = 1$  if incrementing  $V_{OUTn}$  causes ( $V_{INn\_AP} - V_{INn\_AP}$ ) to increase. When properly programmed, lowering the value in the IDAC will always cause the output of the controlled power supply to decrease.

Determine the value for  $Chn\_a\_idac[7:0]$ . The values 'h00 or 'hff are allowed, but they will trip the IDAC's fault bit ( $Fault\_chn\_a\_idac = 1$ ).

When the IDAC is already connected, the value  $Chn\_a\_idac[7:0]$  and  $Chn\_a\_idac\_pol$  will be programmed into the IDAC provided all other conditions are met. See "Programming a Previously Connected Current DAC" for details

Update  $CHn\_A\_IDAC()$  with  $Chn\_a\_idac\_pol$ ,  $Chn\_a\_idac\_con = 1$ ,  $Chn\_a\_idac\_en = 1$ , and  $Chn\_a\_idac[7:0]$ .

#### *Hard Connect Rules:*

Hard connect requests will be ignored and the user will not be able to change  $Chn\_a\_idac\_pol$ ,  $Chn\_a\_idac\_con$  or  $Chn\_a\_idac[7:0]$  if the LTC2970 is servicing a previously issued soft connect on that channel or the previously issued

## OPERATION

soft connect failed with an IDAC fault (Fault\_chn\_a\_idac = 1). Recall that a new hard connection requires the previous value of Chn\_a\_idac\_en = 0.

*LTC2970-1 Only:* Hard connect requests will be ignored and the user will not be able to change Chn\_a\_idac\_pol, Chn\_a\_idac\_con or Chn\_a\_idac[7:0] if GPIO\_CFG is high and either GPIO\_0 or GPIO\_1 are high.

*LTC2970-1 Only:* Hard connect requests will be ignored and the user will not be able to change Chn\_a\_idac\_pol, Chn\_a\_idac\_con or Chn\_a\_idac[7:0] if there is a pending tracking operation.

### 7. Programming a Previously Connected IDAC

The LTC2970 IDAC's may be programmed after they have been connected with a soft connect or a hard connect provided a servo operation is not enabled on the associated channel.

#### *Procedure:*

Determine the value for Chn\_a\_idac[7:0]. The values 'h00 or 'hff are allowed, but will trip the IDAC's fault bit (Fault\_chn\_a\_idac = 1).

Verify that the IDAC is already connected, and that Chn\_a\_idac\_con is high.

Ensure that servo mode is not enabled for the channel being programmed. Chn\_a\_servo\_en must be low. This requirement prevents the user from interfering with a previously requested servo operation.

Update the CHn\_A\_IDAC() register with Chn\_a\_idac\_pol, Chn\_a\_idac\_con = 1, Chn\_a\_idac\_en = 1, and Chn\_a\_idac[7:0].

*Note:* Care should be taken to preserve the current value of the Chn\_a\_idac\_pol bit, since the LTC2970 does not prevent the user from changing this value when writing to the IDAC control registers.

#### *Rules:*

Setting Chn\_a\_idac\_con to zero will not disconnect the DAC unless Chn\_a\_idac\_en is also set low.

All Hard Connect rules apply.

### 8. Disconnecting the LTC2970 from the Power Supply Trim Pin

V<sub>OUTn</sub> can be placed in a high impedance state simply by clearing the Chn\_a\_idac\_en bit. In order to minimize the resulting disturbance to the power supply voltage, the IDAC code should not be changed from its current value when clearing the Chn\_a\_idac\_en bit. This is not an issue if the channel's associated servo\_en bit is high.

#### *Disconnect Procedure:*

Update CHn\_IDAC() with Chn\_a\_idac\_en set low.

The LTC2970 will immediately disconnect the buffered I<sub>OUTn</sub> from V<sub>OUTn</sub>.

#### *Disconnect Rules:*

Clearing Chn\_a\_idac\_con with Chn\_a\_idac\_en high will not disconnect the IDAC. Only setting Chn\_a\_idac\_en low will clear Chn\_a\_idac\_con.

*LTC2970-1 Only:* Chn\_a\_idac\_en may not be changed if the feedback node connection is configured for tracking. Tracking is enabled when GPIO\_CFG is high and either GPIO\_0 or GPIO\_1 are high.

### 9. Tracking Power Supplies Overview (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I<sup>2</sup>C interface to initiate a controlled power up or power down of two or more supplies (Figure 2 shows a typical LTC2970-1 application circuit). Multiple LTC2970-1's with different addresses may be simultaneously programmed using the LTC2970 group address and the SYNC() command. Tracking is enabled when GPIO\_CFG is pulled high and either GPIO\_0 or GPIO\_1 are high.

### 10. Tracking Power Supplies On (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I<sup>2</sup>C to initiate a controlled power up of two or more supplies.

*Procedure:* This procedure describes all the steps necessary to track up two or more power supplies. Steps that require I<sup>2</sup>C interaction are prefixed with the required I<sup>2</sup>C command function.

Power-up the LTC2970-1 with GPIO\_CFG pulled high.

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This causes open-drain outputs GPIO\_1 and GPIO\_0 to automatically pull the power supplies' run/soft-start pins to ground.

**CH<sub>n</sub>\_A\_IDAC():** Hard connect CH<sub>n</sub>\_a\_idac[7:0] with a value that forces the power supplies off when GPIO\_CFG = 1. Verify that CH<sub>n</sub>\_a\_idac\_pol is at the appropriate value.

**CH<sub>n</sub>\_A\_IDAC\_TRACK():** Set CH<sub>n</sub>\_a\_idac\_track\_en = 1, and set the CH<sub>n</sub>\_a\_idac\_track[7:0] target value to the code that causes V<sub>OUT<sub>n</sub></sub> to most closely approximate the corresponding power supply's feedback node voltage when it is in regulation.

**CH<sub>n</sub>\_A\_DELAY\_TRACK():** Set the value by which the incrementing of IDAC<sub>n</sub> should be delayed with respect to the start of tracking event. This controls whether the power supplies track up coincidentally or sequentially.

**IO():** Release the run/soft-start pins by programming io\_gpio\_n = 1. This will enable the power supplies without allowing their outputs to move since these are held low by CH<sub>n</sub>\_a\_idac[7:0]. Wait until power supplies have had sufficient time to start running before starting tracking.

**SYNC():** Optional command that allows multiple LTC2970-1's to be synchronized for tracking. Writing Sync\_track = 1 will allow the LTC2970-1 to finish its current ADC conversion before having it wait to receive io\_track\_start = 1. The LTC2970-1 will timeout this wait command after t<sub>TIMEOUT\_SYNC</sub>. Reading back Sync\_track = 1 using the global address will ensure all LTC2970-1's are synchronized before proceeding with the tracking operation.

**IO():** Set io\_track\_start = 1 and keep the run/soft-start pins enabled. Use the global I<sup>2</sup>C address to simultaneously track up power supplies across multiple LTC2970-1's.

**LTC2970-1 response:** For each tracking enabled channel, the LTC2970-1 will decrement the CH<sub>n</sub>\_A\_delay\_track counter at a rate of t<sub>DEC\_TRACK</sub>. As soon as a channel's tracking counter reaches zero, the LTC2970-1 will begin stepping the value of CH<sub>n</sub>\_a\_idac[7:0] by one count until the final value of CH<sub>n</sub>\_a\_idac\_track[7:0] is reached, at which point CH<sub>n</sub>\_a\_idac\_track\_en is de-asserted. When the final value is reached for all channels, GPIO\_CFG is asserted low. After a time delay of t<sub>HOLD\_TRACK</sub>, CH<sub>n</sub>\_a\_idac\_en is de-asserted.

### Power-Up Tracking Rules:

Tracking cannot begin if CH<sub>n</sub>\_a\_idac\_con is not connected. This condition is met when the previous procedure is followed.

CH<sub>n</sub>\_a\_idac\_track\_pol, CH<sub>n</sub>\_a\_idac\_track\_en, and ch0\_idac[7:0] updates will be ignored after IO(io\_track\_start) is asserted until tracking is complete or whenever tracking is pending, i.e., GPIO\_CFG pulled high with either GPIO\_0 or GPIO\_1 asserted pulled high.

## 11. Tracking Power Supplies Off (LTC2970-1 Only)

The LTC2970-1 tracking feature allows the I<sup>2</sup>C to initiate a controlled power down of two or more supplies.

**Procedure:** This procedure describes all steps necessary to track down two or more power supplies. Steps that require I<sup>2</sup>C interaction are prefixed with the required I<sup>2</sup>C command function.

**CH<sub>n</sub>\_IDAC():** Disable the IDAC's for each tracking enabled channel (CH<sub>n</sub>\_a\_idac\_en = 0). Ensure CH<sub>n</sub>\_a\_idac\_pol is at the appropriate value.

**CH<sub>n</sub>\_IDAC\_TRACK():** Select the channels to be tracked by setting CH<sub>n</sub>\_a\_idac\_track\_en = 1, and set the target value for each CH<sub>n</sub>\_a\_idac\_track[7:0] to that which forces the supply off.

**CH<sub>n</sub>\_A\_DELAY\_TRACK():** Set the value by which the decrementing of that channel's DAC should be delayed with respect to the start of the tracking event. This controls whether the supplies track down coincidentally or sequentially.

**SYNC():** Optional command that allows multiple LTC2970-1's to be synchronized for tracking. Writing Sync\_track = 1 will allow the LTC2970-1 to finish its current ADC conversion before having it wait to receive io\_track\_start = 1. The LTC2970-1 will timeout this wait command after t<sub>TIMEOUT\_SYNC</sub>. Reading back Sync\_track = 1 using the global address will ensure all LTC2970's are synchronized before proceeding with the tracking operation.

**IO():** Set io\_track\_start = 1. Use the global I<sup>2</sup>C address to simultaneously track down power supplies across multiple LTC2970's.

## OPERATION

LTC2970-1 response: Each tracking enabled channel is soft connected. The GPIO\_CFG pin is released allowing it to be pulled high. The LTC2970-1 waits  $t_{\text{SETUP\_TRACK}}$  to allow GPIO\_CFG to settle. For each tracking enabled channel, the  $\text{Chn\_a\_delay\_track}$  counter is decremented at a rate of  $t_{\text{DEC\_TRACK}}$ . As soon as a channel's tracking counter reaches zero, the LTC2970-1 will begin stepping the value of  $\text{Chn\_a\_idac}[7:0]$  by one count until the final value of  $\text{Chn\_a\_idac\_track}[7:0]$  is reached. The tracking enable bit is then cleared for both channels ( $\text{Chn\_a\_idac\_track\_en} = 0$ ).

IO(): The I<sup>2</sup>C interface may then be used to set GPIO\_1 and GPIO\_0 low, disabling the power supplies.

### *Power Down Tracking Rules:*

Power down tracking requests will be ignored until the user has disabled the IDAC's by setting  $\text{Chn\_a\_idac\_en} = 0$  for each tracking enabled channel.

$\text{Chn\_a\_idac\_track\_pol}$ ,  $\text{Chn\_a\_idac\_track\_en}$ , and  $\text{ch0\_idac}[7:0]$  updates will be ignored after IO(IO\_track\_start) is asserted until tracking is complete and whenever tracking range is configured; (GPIO\_CFG high with either GPIO\_0 or GPIO\_1 asserted high).

## 12. Continuous Power Supply Voltage Servo

The continuous voltage servo feature allows the LTC2970 to servo an external power supply to a programmed value. The voltage of the external supply is monitored over  $\text{Chn\_A\_ADC}$  and compared to a target value stored in  $\text{Chn\_a\_servo}$ . After each conversion,  $\text{Chn\_A\_IDAC}$  is incremented by 1, decremented by 1, or held; whichever brings or keeps the measured voltage closer to the targeted servo value.

### *Procedure:*

Follow procedure for hard connecting or soft connecting the LTC2970 to power supply trim pin; when updating  $\text{CHn\_A\_IDAC}()$ ,  $\text{Chn\_a\_idac\_servo\_repeat}$  should be asserted high. The servo channel's IDAC must be enabled before  $\text{Chn\_A\_servo\_en}$  can be set high.

Determine the target servo voltage,  $\text{Chn\_a\_servo}[14:0]$ .

Update  $\text{CHn\_A\_SERVO}()$  with  $\text{Chn\_a\_servo\_en} = 1$ , and  $\text{Chn\_a\_servo}[14:0]$ .

Update  $\text{CHn\_A\_IDAC}()$  with  $\text{Chn\_a\_idac\_servo\_repeat} = 1$ . This step may be skipped if  $\text{Chn\_a\_idac\_servo\_repeat}$  was set high during the soft or hard connect procedure.

LTC2970 response: The LTC2970 will continuously increment, decrement or hold  $\text{Chn\_a\_idac}[7:0]$  in order to match the measured value of ( $\text{VINn\_AP-VINn\_AM}$ ) to  $\text{Chn\_a\_servo}[14:0]$ .

Whenever the  $\text{CHn\_A\_SERVO}()$  register is updated an internal flag is cleared indicating that a successful servo has not been completed. This internal flag,  $\text{Chn\_a\_servo\_done}$ , initially causes the ADC to operate in an accelerated 12-bit mode. Once the channel reaches the servo target, the ADC switches back to 14-bit mode for two conversions before asserting  $\text{Chn\_a\_servo\_done}$  high.

In continuous voltage servo mode the  $\text{Chn\_a\_servo\_done}$  flags allow the initial servo target to be reached quickly. During this time, ADC conversions for all non-servo channels are temporarily inhibited.

### *Rules:*

The IDAC associated with the servo channel must be enabled. If  $\text{Chn\_a\_idac\_en}$  is low the servo enable bit  $\text{Chn\_a\_servo\_en}$  is always forced low.

The IDAC associated with the servo channel must be connected ( $\text{Chn\_a\_idac\_con} = 1$ ).

An IDAC fault may be generated during a continuous servo operation. The LTC2970 will report the fault and continue trying to servo that channel.

*LTC2970-1 Only:* There must be no pending tracking commands. A pending tracking command will clear  $\text{Chn\_a\_servo\_en}$ .

*LTC2970-1 Only:* The tracking range must not be enabled; (GPIO\_CFG high with either GPIO\_0 or GPIO\_1 asserted high). An enabled tracking range will clear  $\text{Chn\_a\_servo\_en}$  low.

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### 13. One Time Power Supply Voltage Servo

The one time voltage servo feature allows the LTC2970 to servo an external power supply to a programmed value and then stop updating the IDAC once the target value has been reached.

#### *Procedure:*

Follow procedure for hard connecting or soft connecting the LTC2970 to power supply trim pin; when updating `CHn_A_IDAC()`, `Chn_a_idac_servo_repeat` should be de-asserted low. The servo channel's IDAC must be enabled before `Chn_a_servo_en` may be set high.

Update `CHn_A_IDAC()` with `Chn_a_idac_servo_repeat = 0`. This step may be skipped if `Chn_a_idac_servo_repeat` was cleared low during the soft or hard connect procedure.

Update `FAULT_EN()` with `Fault_en_chn_a_servo = 0`. This prevents the LTC2970 from reinitiating a servo after an over-voltage or under-voltage fault.

Determine the target servo voltage, `Chn_a_servo[14:0]`.

Update `CHn_A_SERVO()` register with `Chn_a_servo_en = 1`, and `Chn_a_servo[14:0]`.

**LTC2970 response:** The LTC2970 will increment, decrement or hold `Chn_a_idac[7:0]` in order to match the measured value of `(VINn_AP-VINn_AM)` to `Chn_a_servo[14:0]`. The servo procedure will end when the internal `Chn_a_servo_done` flag is set (see "Continuous Power Supply Voltage Servo"). At this point the IDAC is either programmed to the appropriate servo value or faulted.

#### *Rules:*

All "Continuous Power Supply Voltage Servo" rules apply.

### 14. One Time Power Supply Voltage Servo with Repeat On Fault

The LTC2970 one time voltage servo feature may be modified to allow the LTC2970 to perform an additional power supply servo operation after an under-voltage or over-voltage fault is detected on the servo channel.

#### *Procedure:*

Follow procedure outlined for "One Time Power Supply Voltage Servo".

Update `FAULT_EN()` with `Fault_en_chn_a_servo = 1`.

Enable detection of the appropriate instantaneous faults for all servo channels; see "Generating and Monitoring Instantaneous Faults".

**LTC2970 response:** Any time an instantaneous under-voltage or over-voltage fault is detected on the servo channel (`Fault_ov_a_chn` or `Fault_uv_a_chn`), the internal `Chn_a_servo_done` flag for that channel is cleared, and the LTC2970 will perform a complete one time servo. This allows the LTC2970 to precisely restore the power supply to the target servo value, after it has drifted beyond a user defined operating window.

#### *Rules:*

All "Continuous Power Supply Voltage Servo" rules apply.

During a permanent under-voltage or over-voltage fault the LTC2970 will continuously try to correct the faulted channel, after each failed attempt all other channels that need monitoring by the ADC will be serviced.

### 15. Configuring ADC to Monitor Input Channels and Internal Temperature Sensor

The LTC2970 is able to perform ADC conversions on any combination of seven different input channels. A channel is converted if its associated `ADC_MON()` bit is set high. Refer to Table 7 for details.

#### *Procedure:*

Update `ADC_MON()` with the control bit of each channel that is to be monitored set high.

**LTC2970 response:** All enabled channels will be sequentially converted. The result of the most recent conversion may be read from the ADC result register. Each time a conversion is completed the new data bit associated with the result register is asserted high. The new data bit is

## OPERATION

**Table 7. LTC2970 ADC Conversion and Fault Limit Registers**

| INPUT CHANNEL   | ADC_MON()<br>CONTROL BIT | ADC RESULT REGISTER<br>(2s COMPLEMENT) | OV FAULT REGISTER<br>(2s COMPLEMENT) | UV FAULT REGISTER<br>(2s COMPLEMENT) |
|-----------------|--------------------------|----------------------------------------|--------------------------------------|--------------------------------------|
| TEMPERATURE     | Adc_mon_temp             | Temp_adc[14:0]                         | -                                    | -                                    |
| VIN1_BP-VIN1_BM | Adc_mon_b_ch1            | Ch1_b_adc[14:0]                        | Ch1_b_ov[14:0]                       | Ch1_b_uv[14:0]                       |
| VIN1_AP-VIN1_AM | Adc_mon_a_ch1            | Ch1_a_adc[14:0]                        | Ch1_a_ov[14:0]                       | Ch1_a_uv[14:0]                       |
| VINO_BP-VINO_BM | Adc_mon_b_ch0            | Ch0_b_adc[14:0]                        | Ch0_b_ov[14:0]                       | Ch0_b_uv[14:0]                       |
| VINO_AP-VINO_AM | Adc_mon_a_ch0            | Ch0_a_adc[14:0]                        | Ch0_a_ov[14:0]                       | Ch0_a_uv[14:0]                       |
| 12VIN           | Adc_mon_v12              | V12_adc[14:0]                          | V12_ov[14:0]                         | V12_uv[14:0]                         |
| VDD             | Adc_mon_vdd              | Vdd_adc[14:0]                          | Vdd_ov[14:0]                         | Vdd_uv[14:0]                         |

reset each time the result register is read. This provides a simple mechanism for supervisory software to determine if a new conversion has been completed since data was last read.

### Rules:

The LTC2970 assigns priority to ADC conversions of CH1\_A\_ADC and CH0\_A\_ADC when these channels are in their initial fast servo mode.

The IO() register control bit lo\_i2c\_adc\_wen must be low in order for ADC conversions to be performed.

*LTC2970-1 Only:* ADC conversions are suspended during any pending tracking requests.

## 16. Generating and Monitoring Instantaneous Faults

The LTC2970 supports fourteen different types of instantaneous faults. These faults together with the conditions that trigger them are defined in Table 8. There are six under-voltage faults, six over-voltage faults and two IDAC limit faults. The FAULT() command may be used to read the status of all instantaneous fault bits. The IO() command may be used to configure GPIO\_0 and GPIO\_1 to view voltage limit and IDAC faults respectively. The state of GPIO\_0 and GPIO\_1 may be read using IO().

**Table 8. LTC2970 Fault Reporting Bits and Conditions**

| CONDITION THAT GENERATES AN INSTANTANEOUS FAULT | FAULT()<br>INSTANTANEOUS FAULT REPORTING | FAULT_EN()<br>ENABLE FOR LATCHED FAULT REPORTING | FAULT_LA()<br>LATCHED FAULT REPORTING |
|-------------------------------------------------|------------------------------------------|--------------------------------------------------|---------------------------------------|
| V12_adc[14:0] < V12_uv[14:0]                    | Fault_v12_uv                             | Fault_en_v12_uv                                  | Fault_la_v12_uv                       |
| V12_adc[14:0] > V12_ov[14:0]                    | Fault_v12_ov                             | Fault_en_v12_ov                                  | Fault_la_v12_ov                       |
| Vdd_adc[14:0] < Vdd_uv[14:0]                    | Fault_vdd_uv                             | Fault_en_vdd_uv                                  | Fault_la_vdd_uv                       |
| Vdd_adc[14:0] > Vdd_ov[14:0]                    | Fault_vdd_ov                             | Fault_en_vdd_ov                                  | Fault_la_vdd_ov                       |
| Ch1_b_adc[14:0] < Ch1_b_uv[14:0]                | Fault_ch1_b_uv                           | Fault_en_ch1_b_uv                                | Fault_la_ch1_b_uv                     |
| Ch1_b_adc[14:0] > Ch1_b_ov[14:0]                | Fault_ch1_b_ov                           | Fault_en_ch1_b_ov                                | Fault_la_ch1_b_ov                     |
| Idac_a_ch1[7:0] = 8'ff or 8'h00                 | Fault_ch1_a_idac                         | Fault_en_ch1_a_idac                              | Fault_la_ch1_a_idac                   |
| Ch1_a_adc[14:0] < Ch1_a_uv[14:0]                | Fault_ch1_a_uv                           | Fault_en_ch1_a_uv                                | Fault_la_ch1_a_uv                     |
| Ch1_a_adc[14:0] > Ch1_a_ov[14:0]                | Fault_ch1_a_ov                           | Fault_en_ch1_a_ov                                | Fault_la_ch1_a_ov                     |
| Ch0_b_adc[14:0] < Ch0_b_uv[14:0]                | Fault_ch0_b_uv                           | Fault_en_ch0_b_uv                                | Fault_la_ch0_b_uv                     |
| Ch0_b_adc[14:0] > Ch0_b_ov[14:0]                | Fault_ch0_b_ov                           | Fault_en_ch0_b_ov                                | Fault_la_ch0_b_ov                     |
| Idac_a_ch0[7:0] = 8'ff or 8'h00                 | Fault_ch0_a_idac                         | Fault_en_ch0_a_idac                              | Fault_la_ch0_a_idac                   |
| Ch0_a_adc[14:0] < Ch0_a_uv[14:0]                | Fault_ch0_a_uv                           | Fault_en_ch0_a_uv                                | Fault_la_ch0_a_uv                     |
| Ch0_a_adc[14:0] > Ch0_a_ov[14:0]                | Fault_ch0_a_ov                           | Fault_en_ch0_a_ov                                | Fault_la_ch0_a_ov                     |

## OPERATION

### Procedure:

Update the over-voltage limit register with the value above which the ADC result should generate an over-voltage fault. Instantaneous over-voltage faults are updated after each ADC conversion. They are asserted high when the ADC result is greater than the over-voltage limit. They are cleared if the ADC result is less than or equal to the over-voltage limit. Setting the over-voltage limit to 14'h3fff inhibits instantaneous faults for the associated channel.

Update the under-voltage limit register with the value below which the ADC result should generate an under-voltage fault. Instantaneous under-voltage faults are updated after each ADC conversion. They are asserted high when the ADC result is less than the under-voltage limit. They are cleared if the ADC result is greater than or equal to the under-voltage limit. Setting the over-voltage limit to 14'h4000 inhibits instantaneous faults for the associated channel.

Update ADC\_MON() control bits to allow ADC conversions on all channels that are to be monitored for over and under voltage limits. Instantaneous IDAC faults are polled after all ADC conversions are completed and set when the associated IDAC registers are at 'h00 or 'hff.

Read FAULT() to view the value of all instantaneous faults.

The IO(io\_cfg\_0) command may be used to configure the GPIO\_0 pin to output the internal Power\_good flag. Power\_good is asserted high if there are no instantaneous over-voltage or under-voltage faults. IO() may be used to read the value of Power\_good through io\_gpio\_0.

The IO(io\_cfg\_1) command may be used to configure the GPIO\_1 pin to output the internal Idac\_fault flag. Idac\_fault is asserted high if either IDAC value is faulted. IO() may be used to read the value of Idac\_fault through io\_gpio\_1.

### Rules:

The over-voltage and under-voltage limits must be initialized; they do not have a default value.

All over-voltage limits, under-voltage limits and ADC results use 2's complement notation with bit position [14] of register [14:0] being used for the sign.

Instantaneous Ch0\_a and Ch1\_a faults may be used to trigger a servo on fault event.

Over-voltage and under-voltage faults require that the associated ADC\_MON control bit be asserted high for instantaneous fault detection to be updated.

## 17. Generating and Monitoring Latched Faults

The LTC2970 is able to selectively latch instantaneous faults in the latched fault register FAULT\_LA. Each instantaneous fault has an associated latched fault bit in FAULT\_LA and a fault enable bit in FAULT\_EN; (see Table 8) for details. When an instantaneous fault enable bit is high, any event that sets the instantaneous fault will simultaneously set the latched fault. The latched fault will remain set even if conditions permit the instantaneous fault to be cleared. The latched faults are immediately cleared whenever the associated fault enable bit is cleared. All latched faults are also cleared when the latched fault register is read over FAULT\_LA().

The FAULT\_INDEX() command may be read to determine if any latched faults are asserted. Reading FAULT\_INDEX() does not clear latched faults. The  $\overline{\text{ALERT}}$  output may also be configured to view whether any latched faults are asserted.

### Procedure:

Follow procedure for generating instantaneous faults.

Write FAULT\_EN() to enable any combination of latched faults.

Read FAULT\_INDEX() to determine if any latched faults are asserted without clearing latched faults.

Read FAULT\_LA() to monitor all latched faults. Reading FAULT\_LA() will clear all latched faults. These will remain clear until the next time the LTC2970 polls and sets an associated instantaneous fault.

Setting IO(io\_alert\_enb) low will cause  $\overline{\text{ALERT}}$  to be asserted low whenever any one of the fourteen latched faults is asserted high. The value of the  $\overline{\text{ALERT}}$  pin may also be read through IO(Alertb).

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### Rules:

See “Generating and Monitoring Instantaneous Faults”.

### 18. General Purpose Input/Output Pins

The GPIO\_0 and GPIO\_1 may be used to: (1) monitor instantaneous faults (see “Generating and Monitoring Instantaneous faults”); (2) control switcher run/start pins during tracking (see “Tracking Power Supplies Overview”); or (3) provide general purpose input/output pins.

### Procedure:

To program GPIO\_0 as an open drain output set  $lo\_cfg\_0 = 2'b10$ . The value written to  $lo\_gpio\_0$  will be output over GPIO\_0.

To program GPIO\_0 as an input set  $lo\_cfg\_0 = 2'b11$ . The value of GPIO\_0 may now be read through  $lo\_gpio\_0$ .

### Rules:

The power on reset configurations for GPIO\_0 and GPIO\_1 are output pins with a value equal to the complement of the GPIO\_CFG level.

### 19. Advanced Development Features

The internal ADC may be disabled with the ADC result registers accepting written I<sup>2</sup>C data. This feature allows faults to be generated for diagnostic purposes, without having to generate an actual overvoltage or undervoltage event.

### Procedure:

Set IO( $lo\_i2c\_adc\_wen$ ) high to enable ADC result register writes and disable internal ADC updates.

### Rules:

$lo\_i2c\_adc\_wen$  must be clear for normal operation.

## APPLICATIONS INFORMATION

### Margining DC/DC Converters with External Feedback Resistors

Figure 1 shows a typical application circuit for margining a power supply with an external feedback network. The  $V_{IN0\_AP}$  and  $V_{IN0\_AM}$  differential inputs sense the load voltage directly, and differential inputs  $V_{IN0\_BP}$  and  $V_{IN0\_BM}$  are connected across load current sense resistor R50. A correction voltage is developed at the  $I_{OUT0}$  pin by sourcing IDAC0's current into resistor R40. R40 is Kelvin connected to the point-of-load GND in order to isolate  $V_{IOUT0}$  from ground bounce due to load current changes.  $V_{IOUT0}$  is replicated at  $V_{OUT0}$  by an on-chip, unity-gain voltage buffer.  $V_{OUT0}$  is then connected to the feedback node of the power supply through resistor R30. The feedback node can be isolated from the DAC's correction voltage by placing the  $V_{OUT0}$  pin in high-impedance mode. Since the GPIO\_CFG pin is pulled-up to  $V_{DD}$ , the LTC2970's GPIO\_0 pin will automatically hold the power supply's RUN/SS pin low after power-up until the I<sup>2</sup>C interface releases it.

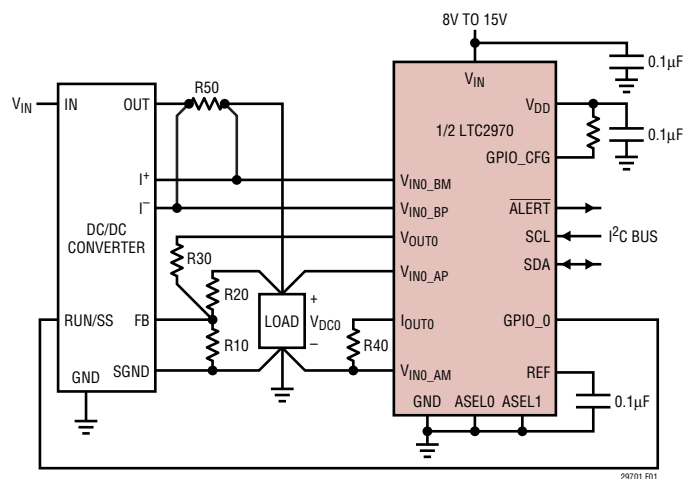


Figure 1. Typical LTC2970 Application Circuit for DC/DC Converters with External Feedback Resistors

## APPLICATIONS INFORMATION

### 4-Step Resistor Selection Procedure for DC/DC Converters with External Feedback Resistors

The following 4-step procedure should be used to quickly calculate the resistor values shown for the Typical Application Circuit shown in Figure 1.

1. Assume values for feedback resistor R20 and the nominal DC/DC converter output voltage  $V_{DC0,NOM}$ , and solve for R10.

$V_{DC0,NOM}$  is the desired output voltage of the DC/DC converter when the LTC2970's  $V_{OUT0}$  pin is in a high impedance state.  $V_{FB0}$  is the voltage at the converter's feedback node when the loop is in regulation, and  $I_{FB0}$  is the feedback node's input current.

$$R10 = \frac{R20 \cdot V_{FB0}}{V_{DC,NOM} - I_{FB0} \cdot R20 - V_{FB0}} \quad (1)$$

2. Solve for the maximum value of R30 that yields the maximum required DC/DC converter output voltage  $V_{DC0,max}$ .

When  $V_{OUT0}$  is at 0V, the output of the DC/DC converter is at its maximum voltage. Note that the 10mV term corresponds to the maximum offset voltage of the IDAC 1X voltage buffer.

$$R30 \leq \frac{R20 \cdot (V_{FB} - 10mV)}{V_{DC,MAX} - V_{DC,NOM}} \quad (2)$$

3. Solve for the minimum value of R40 that's needed to yield the minimum required DC/DC converter output voltage  $V_{DC0,MIN}$ .

The DC/DC converter output voltage will be a minimum when IDAC0 is at its full-scale current. In order to guarantee that R40 is large enough, assume that IDAC0's full-scale current is at the datasheet minimum of 236μA.

$$R40 \geq \frac{(V_{DC,NOM} - V_{DC,MIN}) \cdot \frac{R30}{R20} + V_{FB} + 10mV}{236\mu A} \quad (3)$$

4. Re-calculate the minimum, nominal, and maximum DC/DC converter output voltages and the resulting margining resolution.

$$V_{DC0,NOM} = V_{FB} \cdot \left(1 + \frac{R20}{R10}\right) + I_{FB} \cdot R20 \quad (4)$$

$$V_{DC0,MIN} \leq V_{DC0,NOM} - \frac{R20}{R30} \cdot (R40 \cdot 236\mu A - V_{FB0} - 10mV) \quad (5)$$

$$V_{DC0,MAX} \geq V_{DC0,NOM} + \frac{R20}{R30} \cdot (V_{FB0} - 10mV) \quad (6)$$

The margining resolution is bounded by:

$$V_{RES} \leq \frac{\frac{R20}{R30} \cdot R40 \cdot 276\mu A}{256} \text{ volts/DAC LSB} \quad (7)$$

### Margining DC/DC Converters with a TRIM Pin

Figure 2 illustrates a typical application circuit for margining the output voltage of a DC/DC converter with a TRIM Pin. The LTC2970's  $V_{OUT0}$  pin connects directly to the TRIM pin through resistor R30 and the  $I_{OUT0}$  pin is terminated at the converter's point-of-load ground through R40. Resistors R30 and R40 give this application circuit two degrees of freedom so that the margin-up and margin-down percentages can be specified independently.

Following power-up, the LTC2970's  $V_{OUT0}$  pin defaults to a high-impedance state. If the soft-connect feature is used,

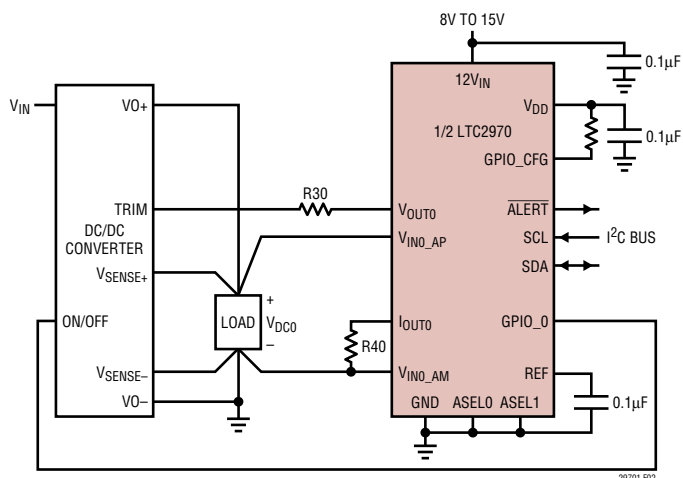


Figure 2. LTC2970 Application Circuit for DC/DC Converters with a TRIM Pin

## APPLICATIONS INFORMATION

the LTC2970 will automatically find the IDAC code that most closely approximates the TRIM pin's open-circuit voltage before enabling  $V_{OUT0}$ . Note: The relationship between  $V_{TRIM}$  and the converter's output is typically non-inverting, so be sure to set the LTC2970's CHO\_a\_idac\_pol bit to 1 in order to allow the voltage servo feature to function properly.

DC/DC converters with a TRIM pin are usually margined high or low by connecting an external resistor between the TRIM pin and either the  $V_{\text{SENSE}+}$  or  $V_{\text{SENSE}-}$  pin. The relationships between these resistors and the  $\Delta\%$  change in the output voltage of the DC/DC converter are typically expressed as:

$$R_{\text{TRIM\_DOWN}} = \frac{R_{\text{TRIM}} \cdot 50}{\Delta_{\text{DOWN}}\%} - R_{\text{TRIM}} \quad (8)$$

$$R_{\text{TRIM-UP}} = \left[ \frac{R_{\text{TRIM}} \cdot V_{\text{DC}} \cdot (100 + \Delta_{\text{UP}}\%)}{2 \cdot V_{\text{REF}} \cdot \Delta_{\text{UP}}\%} - \frac{R_{\text{TRIM}} \cdot 50}{\Delta_{\text{UP}}\%} - R_{\text{TRIM}} \right] \quad (9)$$

where  $R_{\text{TRIM}}$  is the resistance looking into the TRIM pin,  $V_{\text{REF}}$  is the TRIM pin's open-circuit output voltage and  $V_{\text{DC}}$  is the DC/DC converter's nominal output voltage.  $\Delta_{\text{UP}}\%$  and  $\Delta_{\text{DOWN}}\%$  denote the percentage change in the converter's output voltage when margining up or down respectively.

## 2-Step Resistor Selection Procedure for DC/DC Converters with a TRIM Pin

The following two-step procedure should be used to calculate values for resistors R30 and R40 shown in Figure 2.

1. Solve for R30:

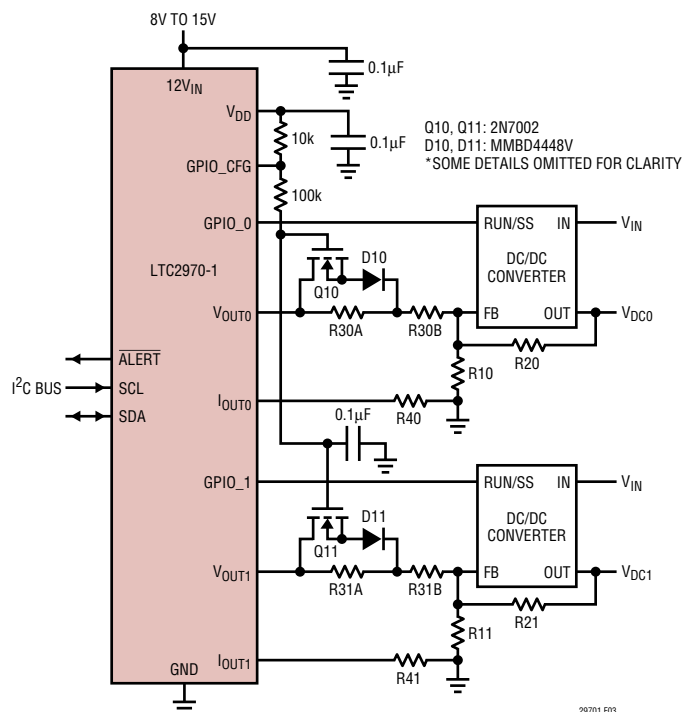
$$R_{30} \leq R_{\text{TRIM}} \cdot \left( \frac{50 - \Delta_{\text{DOWN}\%}}{\Delta_{\text{DOWN}\%}} \right) \quad (10)$$

2. Solve for R40:

$$R_{40} \geq \left(1 + \frac{\Delta_{UP\%}}{\Delta_{DOWN\%}}\right) \cdot \frac{V_{REF}}{236\mu A} \quad (11)$$

## Tracking with the LTC2970-1

A typical LTC2970-1 tracking application circuit is shown in Figure 3 (the sequence of events for tracking are described in sections 9 and 10 of the Operation section). The GPIO\_0 and GPIO\_1 pins are tied directly to their respective DC/DC converter RUN/SS pins. Since GPIO\_CFG is pulled-up to  $V_{DD}$ , the LTC2970-1 will automatically hold off the DC/DC converters after power-up by asserting open drain outputs GPIO\_0 and GPIO\_1 low. N-channel FETs Q10/11 and diodes D10/11 form unidirectional range switches around resistors R30A/31A while GPIO\_CFG is high. These range switches allow the LTC2970-1's  $V_{OUT0}$  and  $V_{OUT1}$  pins to drive the converter outputs all the way to/from ground through resistors R30B/31B. When GPIO\_CFG pulls low, N-channel FETs Q10 and Q11 will turn off. R30A/31A and R30B/31B then combine in series for normal margin operation. The 100k/0.1 $\mu$ F low-pass filter in series with the gates of Q10/11 minimizes charge injection into the feedback nodes of the DC/DC converters when GPIO\_CFG pulls low.



### Figure 3. LTC2970-1 Tracking Application Circuit

## APPLICATIONS INFORMATION

### 7-Step Procedure for Calculating Tracking Application Circuit Resistor Values, Counter Delay Values, and Terminal IDAC Codes

The following 7-step procedure should be used to calculate the resistor values, tracking counter delays, and terminal IDAC codes for the Tracking Application Circuit shown in Figure 3.

1. Assume a value for R20 and solve for R21.

$V_{DCn,NOM}$  is the output voltage of the DC/DC converter when the LTC2970's  $V_{OUTn}$  pin is in a high impedance state.

$$R21 = R20 \cdot \frac{V_{DC1,NOM}}{V_{DC0,NOM}} \quad (12)$$

2. Solve for R10 and R11.

$$R1n = \frac{R2n}{\left( \frac{V_{DCn,NOM}}{V_{FBn}} - 1 \right)} \quad (13)$$

3. Solve for R40 and R41.

For simplicity, this procedure assumes that  $R40 = R41$ .  $V_{DCn,MAX}$  and  $V_{DCn,MIN}$  are the maximum and minimum converter output margin voltages, respectively.

The value of  $R40 = R41$  is constrained by:

$$R40 = R41 \geq \frac{V_{FBn} \cdot \left( \left( \frac{V_{DCn,NOM} - V_{DCn,MIN}}{V_{DCn,MAX} - V_{DCn,NOM}} \right) + 1 \right) + 10mV}{236\mu A} \quad (14)$$

Due to the forward drop of diodes D10 and D11 (0.8V max), the minimum value for  $R40 = R41$  from expression (14) may result in small or even negative values of R30 and R31 in Step 4. If this is the case, assume a minimum allowable value for  $R3nB$ , and use the following expression to calculate the minimum value  $R40 = R41$ :

$$R40 = R41 \geq \frac{V_{FBn} \cdot \left( 1 + \frac{R3nB}{R1n} + \frac{R3nB}{R2n} \right) + 0.8V + 10mV}{236\mu A} \quad (15)$$

Note: Use the channel whose parameters yield the maximum value for  $R40 = R41$ .

4. Solve for R30B and R31B.

Solve for the upper limits of R30B and R31B and then determine which resistor value constrains the maximum value of the other resistor using Equation 17.

$$R3nB \leq \frac{(R4n \cdot 236\mu A - V_{FBn} - 0.8V - 10mV)}{V_{FBn} \cdot \left( \frac{1}{R1n} + \frac{1}{R2n} \right)} \quad (16)$$

$$\frac{R30B}{R20} = \frac{R31B}{R21} \quad (17)$$

5. Solve for R30A and R31A.

R30A and R31A are constrained by:

$$R3nA \leq \frac{R2n}{\left( 1 + \frac{R2n}{R1n} \right) \cdot \left( \frac{V_{DCn,MAX} - V_{DCn,NOM}}{V_{DCn,NOM}} \right)} - R3nB \quad (18)$$

## APPLICATIONS INFORMATION

6. Solve for Channel 1's tracking counter delay relative to Channel 0, CH1\_A\_DELAY\_TRACK().

$$\text{CH1\_A\_DELAY\_TRACK()} = \frac{\left(V_{\text{DC1,NOM}}' - V_{\text{DC0,NOM}}'\right) \cdot \frac{R31B}{R21}}{1\mu\text{A} / \text{count} \cdot R41} \quad (\text{counts}) \quad (19)$$

Note:  $V_{\text{DCn,NOM}}'$  is based on the final values of  $R2n$  and  $R1n$ . If the result for CH1\_A\_DELAY\_TRACK() is less than 0, apply the unsigned result to the CH0\_A\_DELAY\_TRACK() register.

7. Solve for the IDAC0 and IDAC1 terminal tracking codes, Chn\_a\_idac\_track[7:0].

$$\text{Chn\_a\_idac\_track}[7:0] = 255 - \frac{V_{\text{FBn}}}{1\mu\text{A} / \text{LSB} \cdot R4n} \quad (\text{LSB's}) \quad (20)$$

Note: This formula assumes that the Chn\_a\_idac\_pol bit is set to 0.

## Margining Application Circuit Design Example

Consider the LTC2970 application circuit shown in Figure 1. Channel 0 is a DC/DC converter whose output needs to be varied between 3.63V and 1.62V.  $V_{\text{FB0}} = 0.8\text{V}$  and assume that  $I_{\text{FB0}} = 0\text{A}$ .

1. Assume values for feedback resistor  $R20$  and the nominal DC/DC converter output voltage  $V_{\text{DC0,NOM}}$ , and solve for  $R10$ .

Let  $V_{\text{DC0,NOM}} = 2.625\text{V}$  (the average of 3.63V and 1.62V) and assume that  $R20 = 10\text{k}\Omega$ . From Equation 1:

$$R10 = \frac{R20 \cdot V_{\text{FB0}}}{V_{\text{DC,NOM}} - I_{\text{FB0}} \cdot R20 - V_{\text{FB0}}} = \frac{10\text{k}\Omega \cdot 0.8\text{V}}{2.625\text{V} - 0.8\text{V}} = 4,384\Omega$$

Let  $R10 = 4.37\text{k}\Omega$  (the nearest E192 series resistor value).

2. Solve for the value of  $R30$  that yields the maximum required DC/DC converter output voltage  $V_{\text{DC0,MAX}}$

From Equation 2:

$$R30 \leq \frac{R20 \cdot (V_{\text{FB}} - 10\text{mV})}{V_{\text{DC,MAX}} - V_{\text{DC,NOM}}} = \frac{10.0\text{k}\Omega \cdot (0.8\text{V} - 10\text{mV})}{3.63\text{V} - 2.625\text{V}} = 7,861\Omega$$

Let  $R30 = 7.68\text{k}\Omega$ .

3. Solve for the value of  $R40$  that's needed to yield the minimum required DC/DC converter output voltage  $V_{\text{DC0,MIN}}$ .

From Equation 3:

$$R40 \geq \frac{(V_{\text{DC,NOM}} - V_{\text{DC,MIN}}) \cdot \frac{R30}{R20} + V_{\text{FB}}}{236\mu\text{A}} = \frac{(2.625\text{V} - 1.62\text{V}) \cdot \frac{7.96\text{k}\Omega}{10\text{k}\Omega} + 0.8\text{V}}{236\mu\text{A}} = 6,780\Omega$$

Let  $R40 = 6.81\text{k}\Omega$ .

4. Re-calculate the minimum, nominal, and maximum DC/DC converter output voltages and the resulting margining resolution.

From Equations 4, 5, and 6:

$$V_{\text{DC0,NOM}} = V_{\text{FB}} \cdot \left(1 + \frac{R20}{R10}\right) + I_{\text{FB}} \cdot R20 =$$

$$0.8\text{V} \cdot \left(1 + \frac{10\text{k}\Omega}{4.37\text{k}\Omega}\right) = 2.631\text{V}$$

$$V_{\text{DC0,MIN}} < V_{\text{DC0,NOM}} - \frac{R20}{R30} \cdot (236\mu\text{A} \cdot R40 - V_{\text{FB0}})$$

$$\rightarrow V_{\text{DC0,MIN}} < 2.631\text{V} - \frac{10\text{k}\Omega}{7.68\text{k}\Omega} \cdot (236\mu\text{A} \cdot 6.81\text{k}\Omega - 0.8\text{V} - 10\text{mV}) = 1.59\text{V}$$

## APPLICATIONS INFORMATION

$$V_{DC0,MAX} > V_{DC0,NOM} + \frac{R20}{R30} \cdot (V_{FB0} - 10mV)$$

$$\rightarrow V_{DC0,MAX} > 2.631V + \frac{10k\Omega}{7.68k\Omega} \cdot$$

$$(0.8V - 10mV) = 3.660V$$

From Equation 7, the margining resolution will be less than:

$$V_{RES} < \frac{\frac{R20}{R30} \cdot R40 \cdot 276\mu A}{256} = \frac{\frac{10k\Omega}{7.68k\Omega} \cdot 6.65k\Omega \cdot 276\mu A}{256} = 9.33mV/LSB$$

### Margining DC/DC Converter with TRIM Pin Design Example

The output voltage of the DC/DC converter in Figure 2 needs to be margined  $\pm 10\%$  about its nominal value. Assume that  $R_{TRIM} = 10.22k\Omega$  and  $V_{REF} = 1.225V$ .

1. Solve for R30 using Equation 10:

$$R30 \leq R_{TRIM} \cdot \left( \frac{50 - \Delta_{DOWN}\%}{\Delta_{DOWN}\%} \right) = 10.22k\Omega \cdot \left( \frac{50 - 10}{10} \right) = 40,880\Omega$$

Let  $R30 = 39.2k\Omega$ .

2. Solve for R40 using Equations 11:

$$R40 \geq \left( 1 + \frac{\Delta_{UP}\%}{\Delta_{DOWN}\%} \right) \cdot \frac{V_{REF}}{236\mu A} = \left( 1 + \frac{10}{10} \right) \cdot \frac{1.225V}{236\mu A} = 10,381\Omega$$

Let  $R40 = 10.5k\Omega$ .

### Tracking Application Circuit Design Example

Consider the LTC2970-1 application circuit shown in Figure 3. Channel 0 is a 1.8V DC/DC converter while channel 1 is a 2.5V switching power supply. Both converters have a feedback node voltage of 0.8V and need to track on and off coincidentally. In addition, a margin range of +5% and -10% is required for each supply.

1. Assume a value for R20 and solve for R21.

Let  $R20 = 5,970\Omega$ . From Equation 12:

$$R21 = R20 \cdot \frac{V_{DC1,NOM}}{V_{DC0,NOM}} = 5,970\Omega \cdot \frac{2.5V}{1.8V} = 8,292\Omega$$

Let  $R21 = 8,250\Omega$  (the nearest E192 Series resistor value).

2. Solve for R10 and R11.

From Equation 13:

$$R10 = \frac{R20}{\left( \frac{V_{DC0,NOM}}{V_{FB0}} - 1 \right)} = \frac{5,970\Omega}{\left( \frac{1.8V}{0.8V} - 1 \right)} = 4,776\Omega$$

$$R11 = \frac{R21}{\left( \frac{V_{DC1,NOM}}{V_{FB1}} - 1 \right)} = \frac{8,250\Omega}{\left( \frac{2.5V}{0.8V} - 1 \right)} = 3,882\Omega$$

Let  $R10 = 4,750\Omega$  and  $R11 = 3,880\Omega$ .

3. Solve for R40 and R41.

Assume that  $R40 = R41$ .

$$R40 = R41 \geq \frac{V_{FBn} \cdot \left( \left( \frac{V_{DCn,NOM} - V_{DCn,MIN}}{V_{DCn,MAX} - V_{DCn,NOM}} \right) + 1 \right) + 10mV}{236\mu A} = \frac{0.8V \cdot \left( \left( \frac{(1-0.9)}{(1.05-1)} \right) + 1 \right) + 10mV}{236\mu A} = 10,212\Omega$$

Let  $R40 = R41 = 10.5k\Omega$

## APPLICATIONS INFORMATION

4. Solve for R30B and R31B.

$$R30B \leq \frac{(R40 \cdot 236\mu A - V_{FB0} - 0.8V - 10mV)}{V_{FB0} \cdot \left(\frac{1}{R10} + \frac{1}{R20}\right)} = \frac{(10.5k\Omega \cdot 236\mu A - 0.8V - 0.8V - 10mV)}{0.8V \cdot \left(\frac{1}{4,750\Omega} + \frac{1}{5,970\Omega}\right)} = 2,870\Omega$$

$$R31B \leq \frac{(R41 \cdot 236\mu A - V_{FB1} - 0.8V - 10mV)}{V_{FB1} \cdot \left(\frac{1}{R11} + \frac{1}{R21}\right)} = \frac{(10.5k\Omega \cdot 236\mu A - 0.8V - 0.8V - 10mV)}{0.8V \cdot \left(\frac{1}{3,880\Omega} + \frac{1}{8,250\Omega}\right)} = 2,863\Omega$$

For coincident tracking to occur Equation 17 also must be satisfied:

$$\frac{R30B}{R20} = \frac{R31B}{R21}$$

$$\rightarrow R30B = \frac{R31B}{R21} \cdot R20 = \frac{2,863\Omega}{8,250\Omega} \cdot 5,970\Omega = 2,078\Omega$$

$$\rightarrow R31B = \frac{R30B}{R20} \cdot R21 = \frac{2,870\Omega}{5,970\Omega} \cdot 8,250\Omega = 3,957\Omega$$

Let R30B = 2,100Ω and R31B = 2,890Ω.

5. Solve for R30A and R31A.

Referring to Equation 18:

$$R30A \leq \frac{R20}{\left(1 + \frac{R20}{R10}\right) \cdot \left(\frac{V_{DC0,MAX} - V_{DC0,NOM}}{V_{DC0,NOM}}\right)} - R30B = \frac{5,970\Omega}{\left(1 + \frac{5,970\Omega}{4,750\Omega}\right) \cdot \left(\frac{1.05 - 1}{1}\right)} - 2,100\Omega = 50,806\Omega$$

$$R31A \leq \frac{R21}{\left(1 + \frac{R21}{R11}\right) \cdot \left(\frac{V_{DC1,MAX} - V_{DC1,NOM}}{V_{DC1,NOM}}\right)} - R31B = \frac{8,250\Omega}{\left(1 + \frac{8,250\Omega}{3,880\Omega}\right) \cdot \left(\frac{1.05 - 1}{1}\right)} - 2,890\Omega = 49,888\Omega$$

Let R30A = 49.9kΩ and R31A = 48.7kΩ.

6. Solve for Channel 1's tracking counter delay relative to Channel 0, CH1\_A\_DELAY\_TRACK().

First, recalculate the values of  $V_{DCn,NOM}$  based on the final values of R1n and R2n:

$$V_{DC0,NOM}' = V_{FB} \cdot \left(1 + \frac{R20}{R10}\right) + I_{FB} \cdot R20 = 0.8V \cdot \left(1 + \frac{5,970\Omega}{4,750\Omega}\right) + 0 = 1.805V$$

$$V_{DC1,NOM}' = 0.8V \cdot \left(1 + \frac{8,250\Omega}{3,880\Omega}\right) + 0 = 2.501V$$

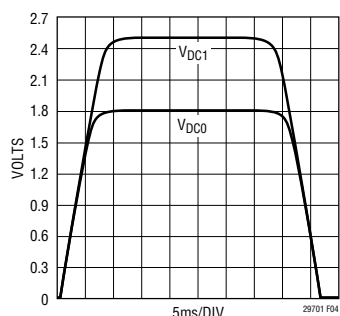
Next, apply Equation 19:

$$CH1\_A\_DELAY\_TRACK() = \frac{(V_{DC1,NOM}' - V_{DC0,NOM}') \cdot \frac{R31B}{R21}}{1\mu A / \text{count} \cdot R41} = \frac{(2.501V - 1.805V) \cdot \frac{2,890\Omega}{8,250\Omega}}{1\mu A / \text{count} \cdot 10.5k\Omega} = 23 \text{ counts}$$

7. Solve for the IDAC0 and IDAC1 terminal tracking codes, Chn\_a\_idac\_track[7:0].

$$Ch0\_a\_idac[7:0] = Ch1\_a\_idac[7:0] = 255 - \frac{0.8V}{1\mu A / \text{LSB} \cdot 10.5k\Omega} = 179$$

## APPLICATIONS INFORMATION



**Figure 4. Tracking Design Example DC/DC Converter Output Waveforms**

Figure 4 shows the DC/DC converter output voltages for this design example tracking-up and tracking-down.

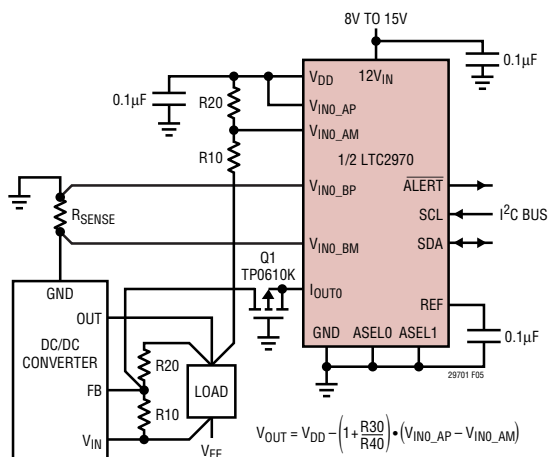
### Temperature Sensor Conversion

The LTC2970's internal temperature sensor output is proportional to absolute temperature (PTAT). In order to convert the ADC reading to degrees Celsius, apply the following formula:

$$\text{result}(^{\circ}\text{C}) = \frac{\text{ADC\_temp\_sensor\_reading}}{4} - 273.15 \quad (21)$$

### Negative Power Supply Application Circuit

Figure 5 shows the LTC2970 controlling a negative power supply. The R30/R40 resistor divider translates the point of load voltage to the LTC2970's  $V_{\text{INO\_A}}$  inputs while the  $V_{\text{INO\_B}}$  inputs monitor the converter's input current  $I \cdot R$



**Figure 5. Negative Power Supply Application Circuit**

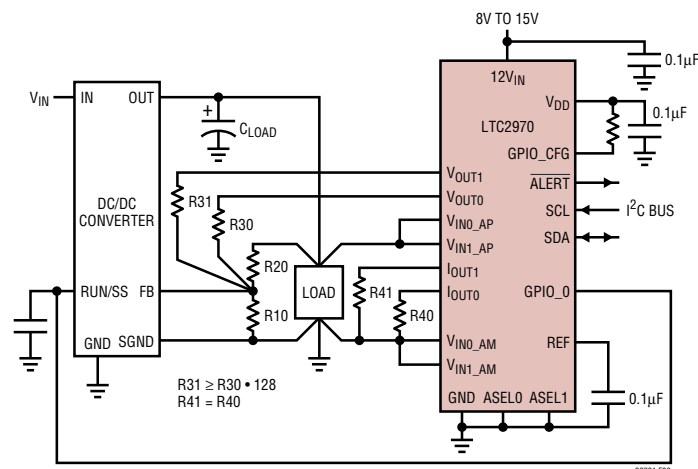
drop across resistor  $R_{\text{SENSE}}$ . Since the  $V_{\text{DD}}$  pin voltage is monitored by the LTC2970, its tolerance can be accounted for when calculating the point of load voltage. Transistor Q1 allows the  $I_{\text{OUT0}}$  pin to force current into the converter's feedback node without forward biasing the LTC2970's  $I_{\text{OUT0}}$  body diode. Note that  $I_{\text{OUT0}}$ 's output current defaults to 128 $\mu\text{A}$  after the LTC2970 comes out of power-on reset.

### 15-Bit Programmable Power Supply Application Circuit

Figure 6 illustrates how both servo channels of the LTC2970 can be configured to adjust a single DC/DC converter over a 15-bit dynamic range. R30 and R31 are sized to force 1 bit of overlap between the coarse (channel 0) and fine (channel 1) servo loops. One coarse servo iteration should be performed first on channel 0 with IDAC1 programmed to mid-scale, and then channel 1 can be programmed to servo to the desired voltage.

### Programmable Reference Application Circuit

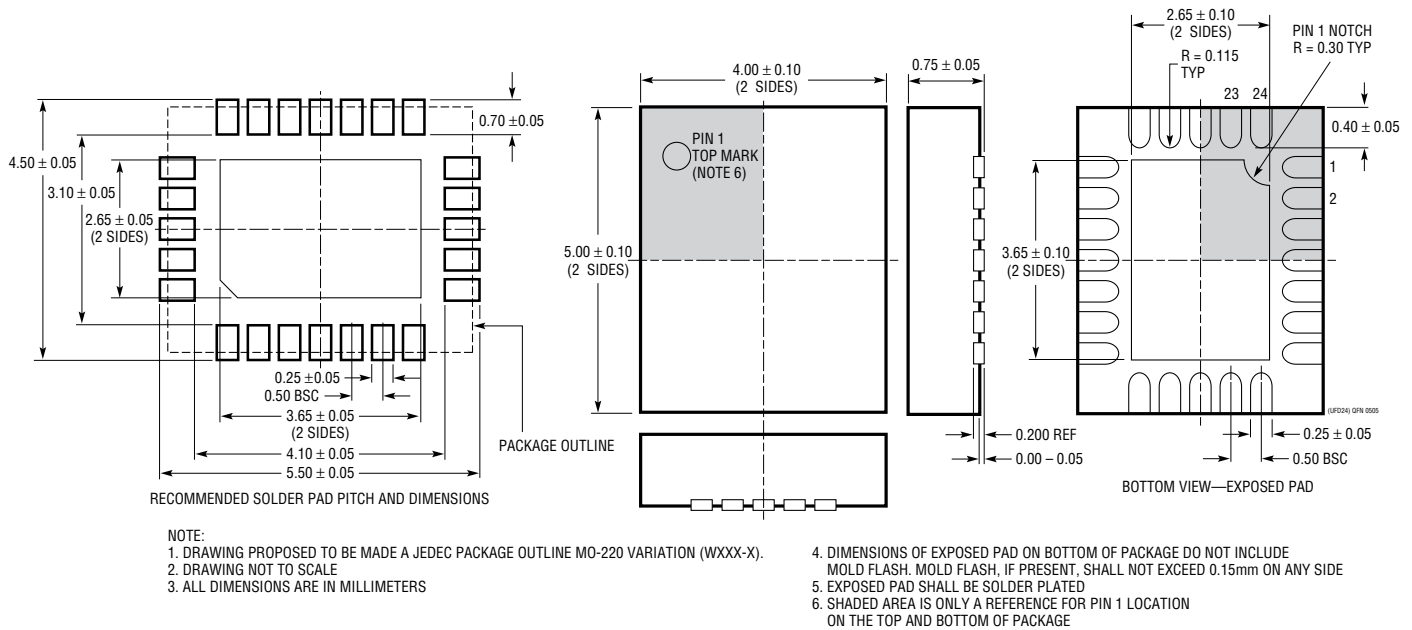
Figure 7 shows a LTC2970 configured as a programmable reference that can span a 0V to 3.5V range with a resolution of 100 $\mu\text{V}$  and an absolute accuracy of less than  $\pm 0.5\%$ . The two IDAC's are paralleled by terminating IDAC1's output resistor in the  $V_{\text{OUT0}}$  output and taking the output of the composite DAC from  $V_{\text{OUT1}}$ . IDAC0 should servo once with IDAC1 set to mid-scale, and then IDAC1 can servo once, continuously, or trigger on drift to the desired target voltage.



**Figure 6. Programmable Power Supply Application Circuit**

## PACKAGE DESCRIPTION

### UFD Package 24-Lead Plastic QFN (4mm × 5mm) (Reference LTC DWG # 05-08-1696)



## TYPICAL APPLICATION

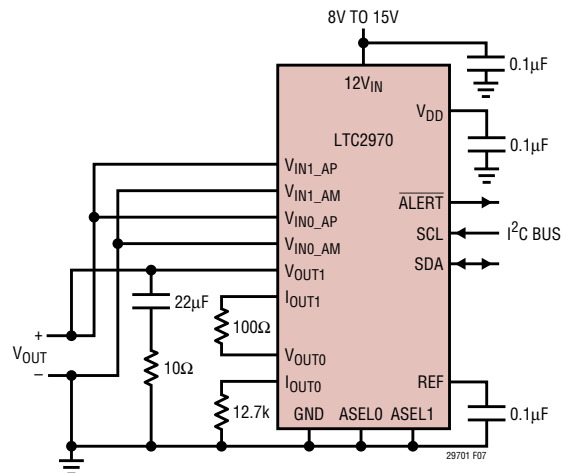


Figure 7. Programmable Reference Application Circuit

## TYPICAL APPLICATION

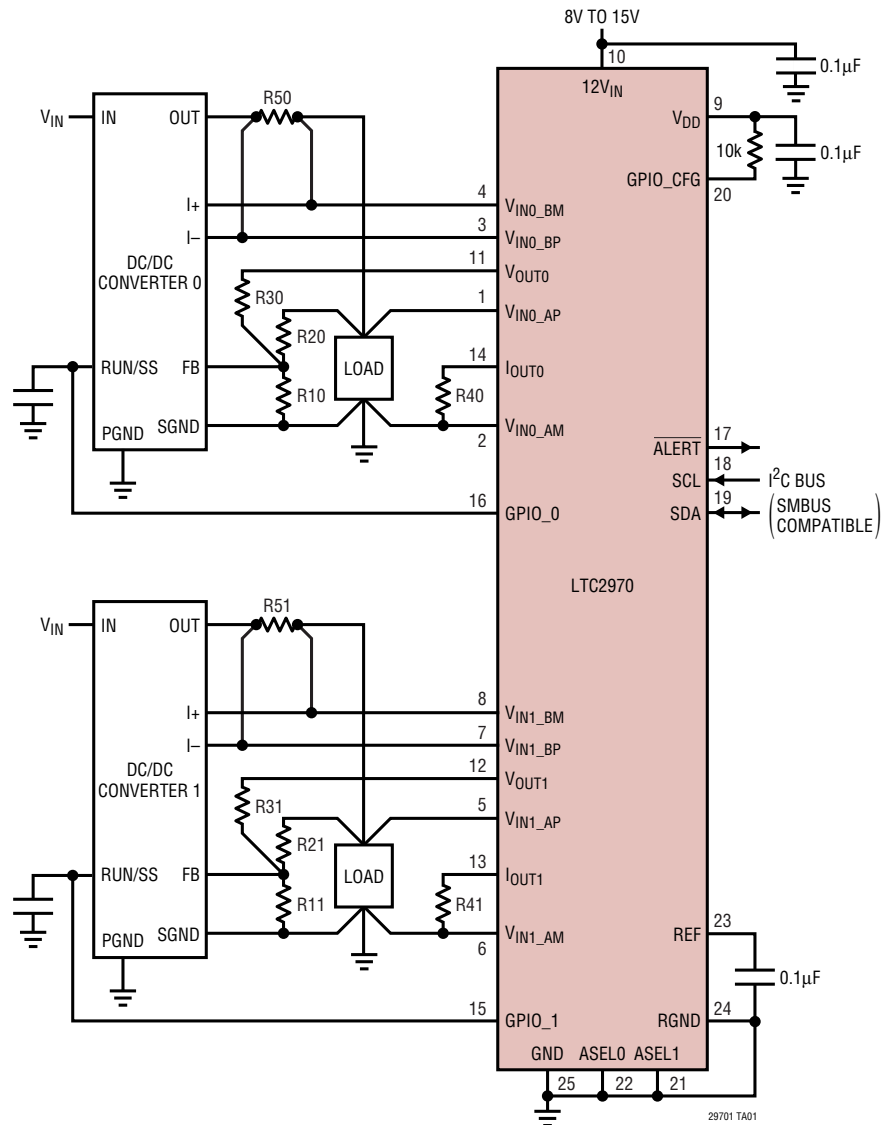


Figure 8. Typical LTC2970 Application Circuit for DC/DC Converters with External Feedback Resistors

## RELATED PARTS

| PART NUMBER         | DESCRIPTION                                    | COMMENTS                                                      |
|---------------------|------------------------------------------------|---------------------------------------------------------------|
| LTC2920-1/LTC2920-2 | Single/Dual Power Supply Margining Controllers | Symmetric/Asymmetric High and Low Voltage Margining           |
| LTC2921/LTC2922     | Power Supply Trackers with Input Monitors      | 3 (LTC2921) or 5 (LTC2922) Remote Sense Switches              |
| LTC2923             | Power Supply Tracking Controller               | Up to 3 Supplies                                              |
| LTC2924             | Quad Power Supply Sequencer                    | Voltage Monitoring and Sequence Error Detection and Reporting |
| LTC2925             | Multiple Power Supply Tracking Controller      | Power Good Timer, Remote Sense Switch                         |
| LTC2926             | MOSFET Controller Power Supply Tracker         | Up to 3 Modules                                               |
| LTC2927             | Single Power Supply Tracker                    | Point of Load Applications                                    |

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