LTC4253A-ADJ

–48V Hot Swap Controller with Sequencer

FEATURES

- **Allows Safe Board Insertion and Removal from a Live –48V Backplane**
- **Floating Topology Permits Very High Voltage Operation**
- **Adjustable Analog Current Limit with Breaker Timer**
- **Fast Response Time Limits Peak Fault Current**
- **Adjustable Undervoltage/Overvoltage Protection with ±1% Threshold Accuracy**
- **Three Sequenced Power Good Outputs**
- Adjustable Soft-Start Current Limit
- Adjustable Timer with Drain Voltage Accelerated Response
- Latchoff After Fault
- Available in 20-Pin SSOP and 20-Pin (4mm × 4mm) QFN Packages

APPLICATIONS

- –48V Distributed Power Systems
- Negative Power Supply Control
- Central Office Switching
- High Availability Servers
- Disk Arrays

DESCRIPTION

The LTC®4253A-ADJ negative voltage Hot Swap™ controller allows a board to be safely inserted and removed from a live backplane. Output current is controlled by three stages of current-limiting: a timed circuit breaker, active current limiting and a fast feedforward path that limits peak current under worst-case catastrophic fault conditions. The LTC4253A-ADJ latches off after a circuit fault.

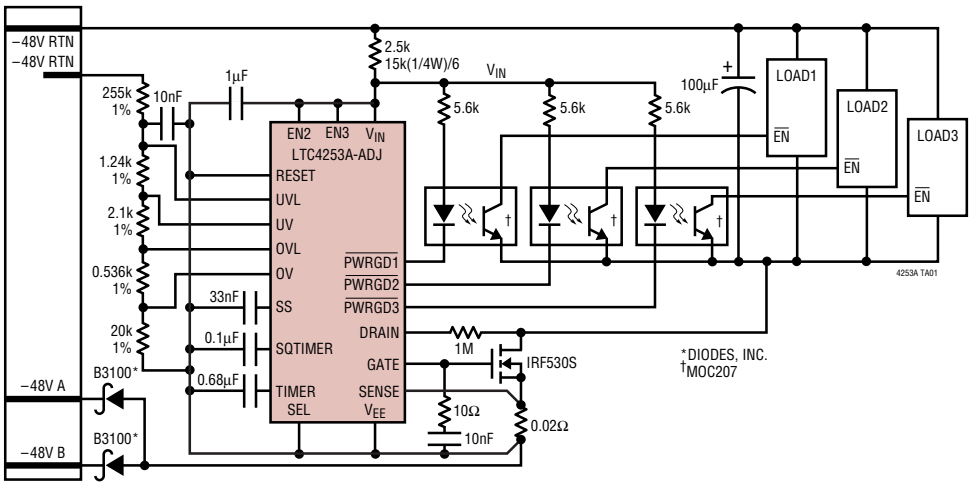
Undervoltage and overvoltage detectors with adjustable thresholds and hystereses disconnect the load whenever the input supply exceeds the desired operating range. The LTC4253A-ADJ's supply input is shunt-regulated, allowing safe operation with very high supply voltages. A multifunction timer delays initial start-up and controls the circuit breaker's response time. The circuit breaker's response time can be accelerated by sensing excessive MOSFET drain voltage. An adjustable soft-start circuit controls MOSFET inrush current at start-up.

Three power good outputs can be sequenced to enable external power modules at start-up or disable them if the circuit breaker trips. The LTC4253A-ADJ is available in 20-pin SSOP and 20-pin (4mm × 4mm) QFN packages.

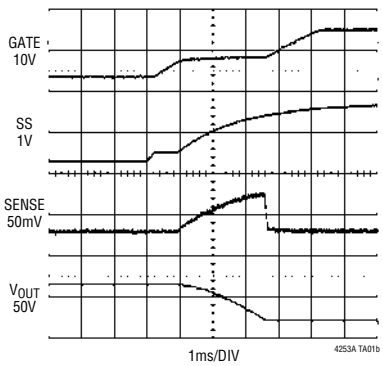
LT, LTC and LT are registered trademarks of Linear Technology Corporation.
Hot Swap is a trademark of Linear Technology Corporation. All other trademarks are the property of their respective owners. Patent pending.

TYPICAL APPLICATION

–48V/2.5A Hot Swap Controller



Start-Up Behavior



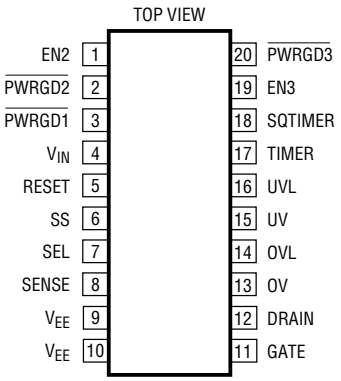
4253a-adjf

ABSOLUTE MAXIMUM RATINGS (Note 1) All voltages referred to V_{EE}

Current into V_{IN} (100µs Pulse) 100mA
Current into DRAIN (100µs Pulse) 20mA
V_{IN}, DRAIN Minimum Voltage ..... –0.3V
Input/Output (Except SENSE and DRAIN) Voltage ..... –0.3V to 16V
SENSE Voltage ..... –0.6V to 16V
Current Out of SENSE (20µs Pulse) ..... –200mA
Maximum Junction Temperature ..... 125°C

Operating Temperature Range
LTC4253A-ADJC ..... 0°C to 70°C
LTC4253A-ADJI ..... –40°C to 85°C
Storage Temperature Range
SSOP ..... –65°C to 150°C
QFN ..... –65°C to 125°C
Lead Temperature (Soldering, 10 sec)
SSOP ..... 300°C

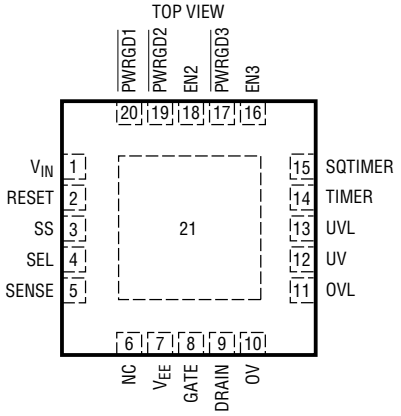
PACKAGE/ORDER INFORMATION



GN PACKAGE
20-LEAD PLASTIC SSOP
T_{JMAX} = 125°C, θ_{JA} = 95°C/W

ORDER PART NUMBER

LTC4253ACGN-ADJ
LTC4253AIGN-ADJ



UF PACKAGE
20-LEAD (4mm × 4mm) PLASTIC QFN
T_{JMAX} = 125°C, θ_{JA} = 37°C/W
EXPOSED PAD (PIN 21) IS V_{EE} MUST BE SOLDERED TO PCB

ORDER PART NUMBER

LTC4253ACUF-ADJ
LTC4253AIUF-ADJ

UF PART MARKING*

253AJ

Order Options Tape and Reel: Add #TR, Lead Free: Add #PBF, Lead Free Tape and Reel: Add #TRPBF, Lead Free Part Marking: http://www.linear.com/leadfree/

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.

ELECTRICAL CHARACTERISTICS The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_Z	V_{IN} – V_{EE} Zener Voltage	I_{IN} = 2mA	●	11.5	13	14.5	V
R_Z	V_{IN} – V_{EE} Zener Dynamic Impedance	I_{IN} = (2mA to 30mA)			5		Ω
I_{IN}	V_{IN} Supply Current	UV = UVL = OV = OVL = 4V, V_{IN} = (V_Z – 0.3V)	●		1.1	2	mA
V_{LKO}	V_{IN} Undervoltage Lockout	Coming Out of UVLO (Rising V_{IN})	●		9	10	V
V_{LKH}	V_{IN} Undervoltage Lockout Hysteresis		●	0.25	0.5	0.75	V
V_{IH}	TTL Input High Voltage		●	2			V
V_{IL}	TTL Input Low Voltage		●			0.8	V
V_{HYST}	TTL Input Buffer Hysteresis				600		mV
I_{RESET}	RESET Input Current	$V_{EE} \le V_{RESET} \le V_{IN}$	●		±0.1	±10	µA
I_{EN}	EN2, EN3 Input Current	V_{EN} = 4V (Sinking) V_{EN} = 0V	● ●	60	120 ±0.1	180 ±10	µA µA

4253a-adjf

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SEL}	SEL Input Current	V_{SEL} = 0V (Sourcing) V_{SEL} = V_{IN}	● ●	10	20 ±0.1	40 ±10	µA µA
V_{CB}	Circuit Breaker Current Limit Voltage	V_{CB} = (V_{SENSE} – V_{EE})	●	45	50	55	mV
$\frac{V_{ACL}}{V_{CB}}$	$\frac{\text{Analog Current Limit Voltage x\%}}{\text{Circuit Breaker Current Limit Voltage}}$	V_{ACL} = (V_{SENSE} – V_{EE}), SS = Open or 1.4V	●	105	120	138	%
V_{FCL}	Fast Current Limit Voltage	V_{FCL} = (V_{SENSE} – V_{EE})	●	150	200	300	mV
V_{SS}	SS Voltage	After End of SS Timing Cycle	●	1.25	1.4	1.55	V
I_{SS}	SS Pin Current	UV = UVL = OV = OVL = 4V, V_{SENSE} = V_{EE}, V_{SS} = 0V (Sourcing)	●	16	28	40	µA
		UV = UVL = OV = OVL = 0V, V_{SENSE} = V_{EE}, V_{SS} = 1V (Sinking)			28		mA
R_{SS}	SS Output Impedance				50		kΩ
V_{OS}	Analog Current Limit Offset Voltage				10		mV
$\frac{V_{ACL} + V_{OS}}{V_{SS}}$	Ratio (V_{ACL} + V_{OS}) to SS Voltage				0.05		V/V
I_{GATE}	GATE Pin Output Current	UV = UVL = OV = OVL = 4V, V_{SENSE} = V_{EE}, V_{GATE} = 0V (Sourcing)	●	30	50	70	µA
		UV = UVL = OV = OVL = 4V, V_{SENSE} – V_{EE} = 0.15V, V_{GATE} = 3V (Sinking)			17		mA
		UV = UVL = OV = OVL = 4V, V_{SENSE} – V_{EE} = 0.3V, V_{GATE} = 1V (Sinking)			190		mA
V_{GATE}	External MOSFET Gate Drive	V_{GATE} – V_{EE}, I_{IN} = 2mA	●	10	12	V_Z	V
V_{GATEL}	Gate Low Threshold	(Before Gate Ramp Up)			0.5		V
V_{GATEH}	Gate High Threshold	V_{GATEH} = V_{IN} – V_{GATE}, For $\overline{PWRGD1}$, $\overline{PWRGD2}$, $\overline{PWRGD3}$ Status			2.8		V
V_{UVHI}	UV Pin Threshold	UV Low to High	●	3.05	3.08	3.11	V
V_{UVLO}	UVL Pin Threshold	UVL High to Low	●	3.05	3.08	3.11	V
V_{OVHI}	OV Pin Threshold	OV Low to High	●	5.04	5.09	5.14	V
V_{OVLO}	OVL Pin Threshold	OVL High to Low	●	5.025	5.08	5.135	V
I_{SENSE}	SENSE Pin Input Current	UV = UVL = OV = OVL = 4V, V_{SENSE} = 50mV (Sourcing)	●		15	30	µA
I_{INP}	UV, UVL, OV, OVL Pin Input Current	UV = UVL = OV = OVL = 4V	●		±0.1	±1	µA
V_{TMRH}	TIMER Pin Voltage High Threshold		●	3.5	4	4.5	V
V_{TMRL}	TIMER Pin Voltage Low Threshold		●	0.8	1	1.2	V
I_{TMR}	TIMER Pin Current	Timer On (Initial Cycle/Latchoff, Sourcing), V_{TMR} = 2V	●	3	5	7	µA
		Timer Off (Initial Cycle, Sinking), V_{TMR} = 2V			28		mA
		Timer On (Circuit Breaker, Sourcing, I_{DRN} = 0µA), V_{TMR} = 2V	●	120	200	280	µA
		Timer On (Circuit Breaker, Sourcing, I_{DRN} = 50µA), V_{TMR} = 2V			600		µA
		Timer Off (Circuit Breaker, Sinking), V_{TMR} = 2V	●	3	5	7	µA
$\frac{\Delta I_{TMRACC}}{\Delta I_{DRN}}$	$\frac{(I_{TMR} \text{ at } I_{DRN} = 50\mu A - I_{TMR} \text{ at } I_{DRN} = 0\mu A)}{50\mu A}$	Timer On (Circuit Breaker with I_{DRN} = 50µA)	●	7	8	9	µA/µA
V_{SQTMRH}	SQTIMER Pin Voltage High Threshold		●	3.5	4	4.5	V
V_{SQTMRL}	SQTIMER Pin Voltage Low Threshold				0.33		V

4253a-adjf

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 2)

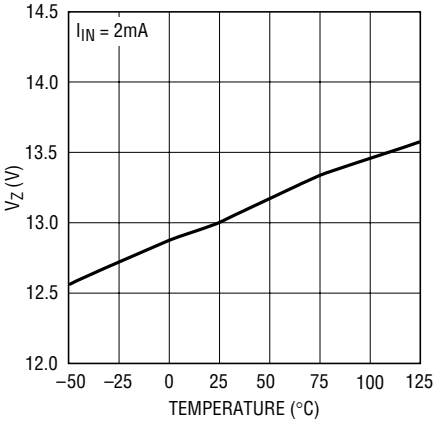
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
I_{SQTMR}	SQTIMER Pin Current	SQTIMER On (Power Good Sequence, Sourcing), V_{SQTMR} = 2V	●	3	5	7	µA
		SQTIMER On (Power Good Sequence, Sinking), V_{SQTMR} = 2V			28		mA
V_{DRNL}	DRAIN Pin Voltage Low Threshold	For $\overline{PWRGD1}$, $\overline{PWRGD2}$, $\overline{PWRGD3}$ Status	●	2	2.39	3	V
I_{DRNL}	DRAIN Leakage Current	V_{DRAIN} = 4V			±0.1	±1	µA
V_{DRNCL}	DRAIN Pin Clamp Voltage	I_{DRN} = 50µA	●	5	6	7.5	V
V_{PGL}	$\overline{PWRGD1}$, $\overline{PWRGD2}$, $\overline{PWRGD3}$ Signals Output Low Voltage	I_{PG} = 1.6mA I_{PG} = 5mA	● ●		0.25	0.4 1.2	V V
I_{PGH}	$\overline{PWRGD1}$, $\overline{PWRGD2}$, $\overline{PWRGD3}$ Output High Current	V_{PG} = 0V (Sourcing)	●	30	50	70	µA
t_{SQ}	SQ Timer Default Ramp Period	SQTIMER Pin Floating, V_{SQTMR} Ramps from 0.5V to 3.5V			250		µs
t_{SS}	SS Default Ramp Period	SS Pin Floating, V_{SS} Ramps from 0.2V to 1.25V			140		µs
t_{PLLUG}	UV Low to GATE Low		●		1	5	µs
t_{PHLOG}	OV High to GATE Low		●		1	5	µs

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to V_{EE} unless otherwise specified.

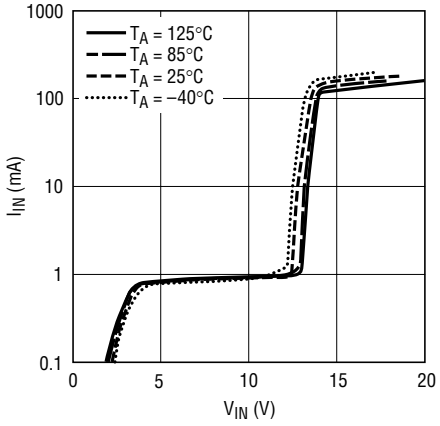
TYPICAL PERFORMANCE CHARACTERISTICS

V_Z vs Temperature



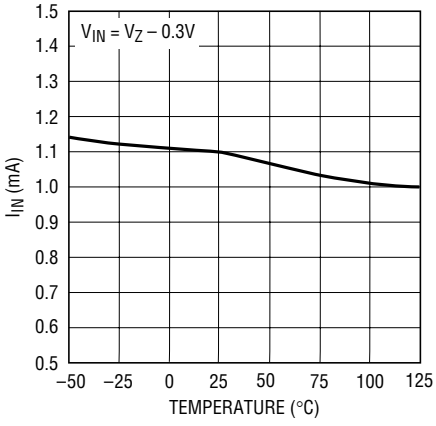
4253A G01

I_{IN} vs V_{IN}



4253A G02

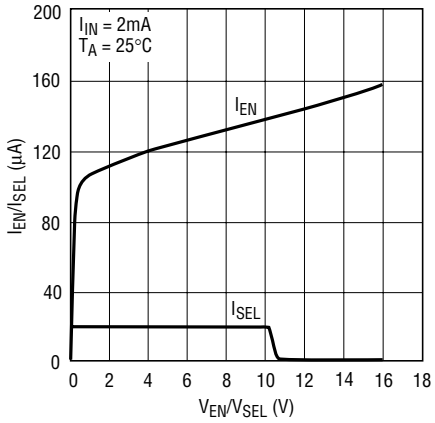
I_{IN} vs Temperature



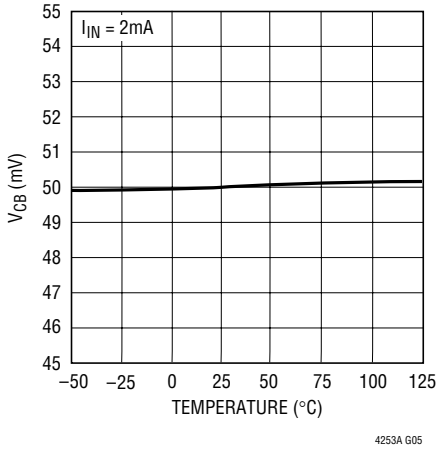
4253A G03

TYPICAL PERFORMANCE CHARACTERISTICS

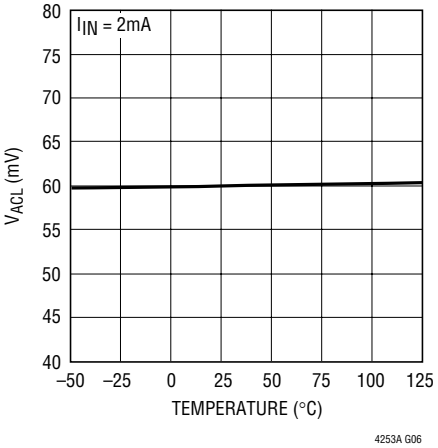
I_{EN} vs V_{EN} and I_{SEL} vs V_{SEL}



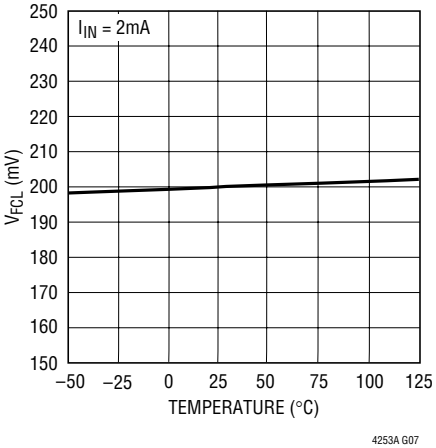
Circuit Breaker Current Limit Voltage V_{CB} vs Temperature



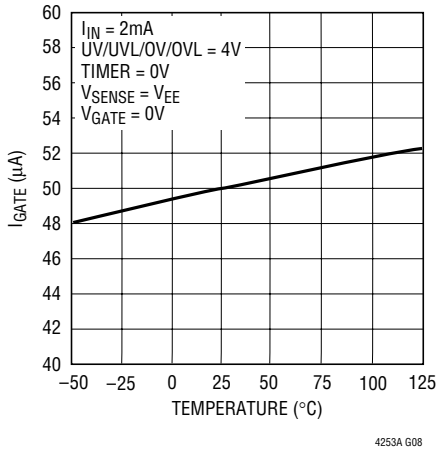
Analog Current Limit Voltage V_{ACL} vs Temperature



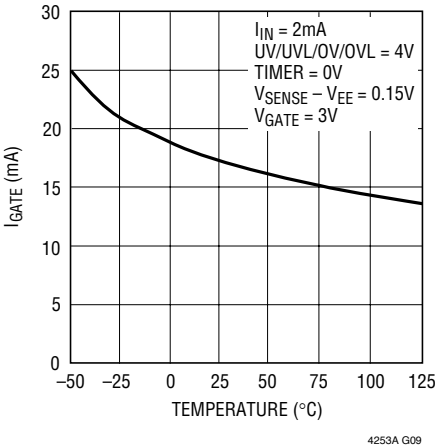
Fast Current Limit Voltage V_{FCL} vs Temperature



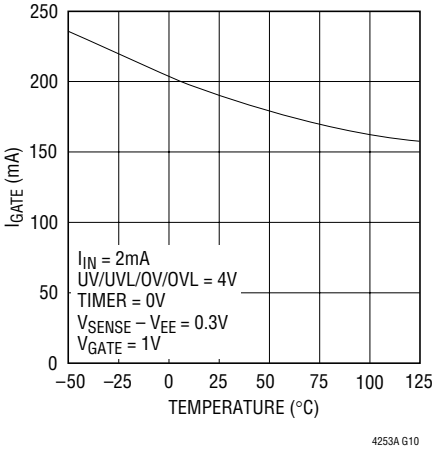
I_{GATE} (Source) vs Temperature



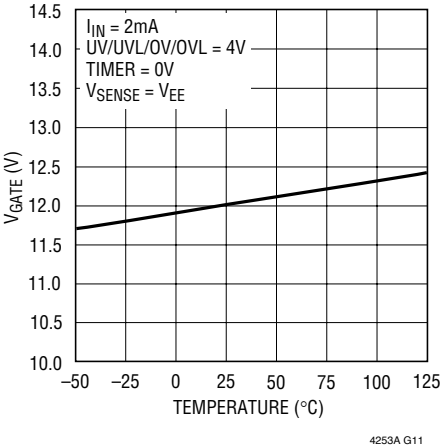
I_{GATE} (ACL, Sink) vs Temperature



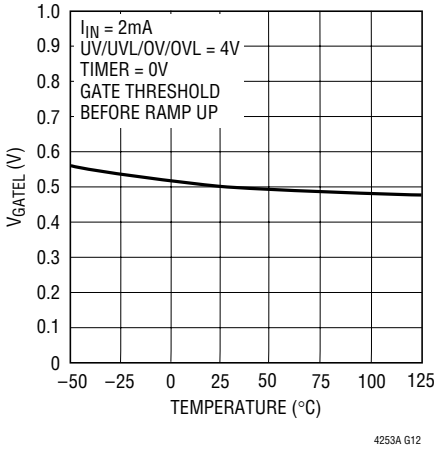
I_{GATE} (FCL, Sink) vs Temperature



V_{GATE} vs Temperature

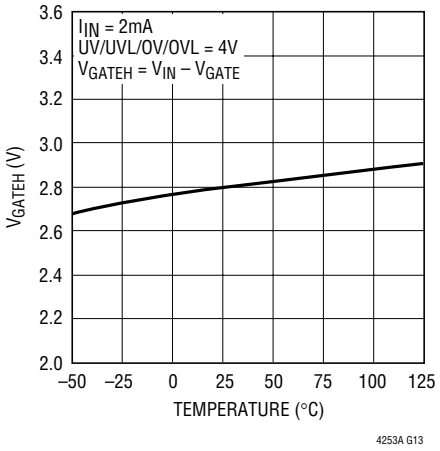


V_{GATEL} vs Temperature

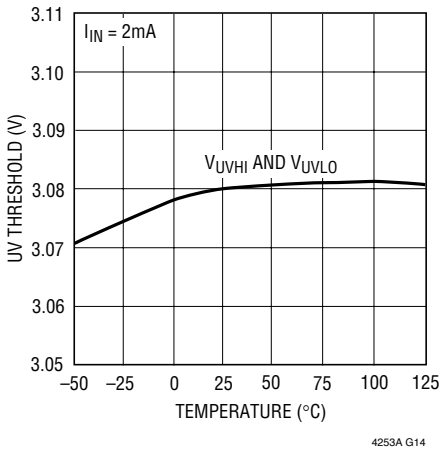


TYPICAL PERFORMANCE CHARACTERISTICS

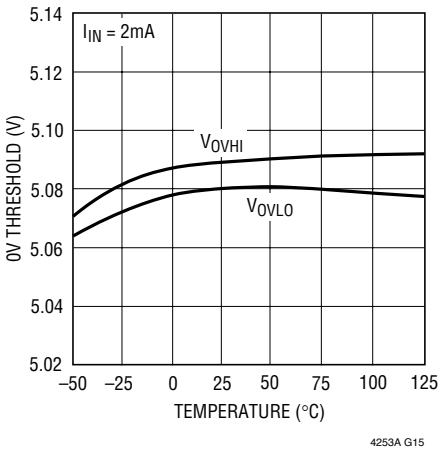
V_{GATEH} vs Temperature



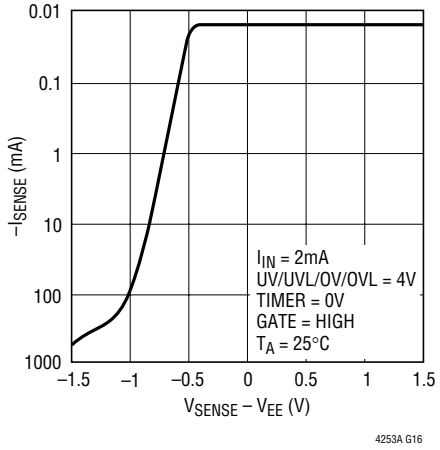
UV Threshold vs Temperature



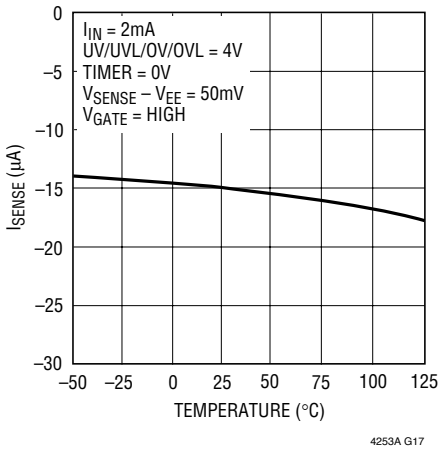
OV Threshold vs Temperature



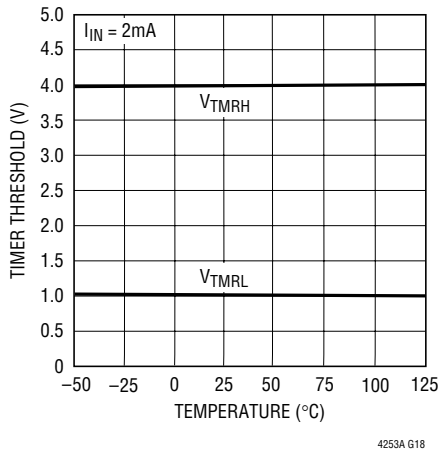
I_{SENSE} vs ($V_{SENSE} - V_{EE}$)



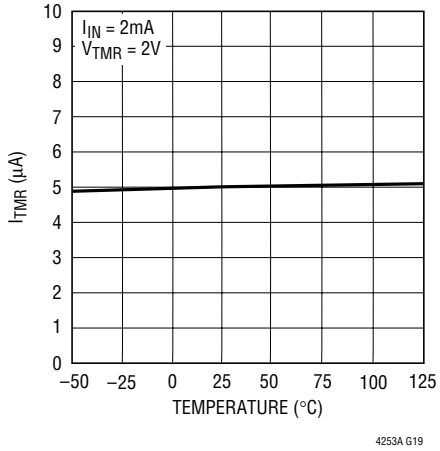
I_{SENSE} vs Temperature



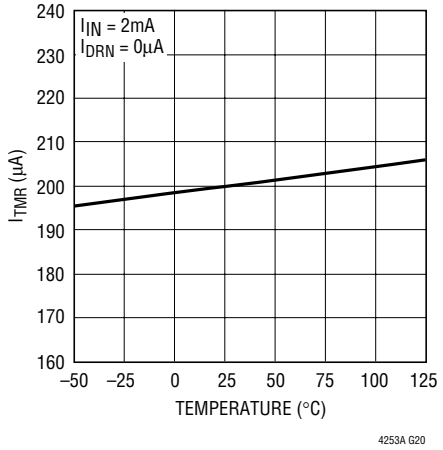
TIMER Threshold vs Temperature



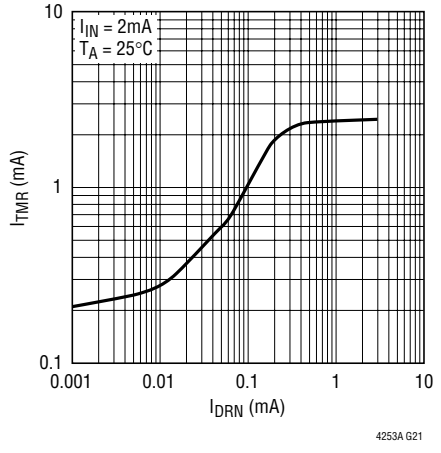
I_{TMR} (Initial Cycle, Sourcing) vs Temperature



I_{TMR} (Circuit Breaker, Sourcing) vs Temperature

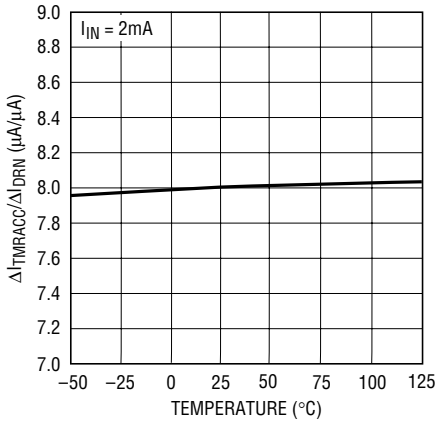


I_{TMR} vs I_{DRN}

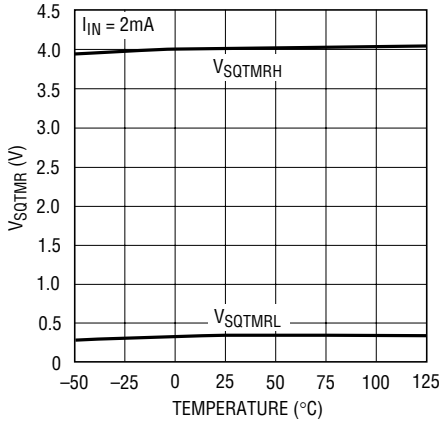


TYPICAL PERFORMANCE CHARACTERISTICS

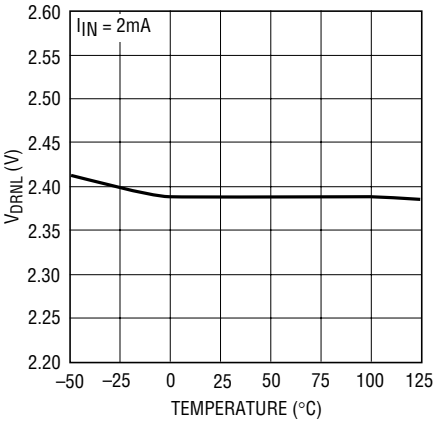
$\Delta I_{TMRACC}/\Delta I_{DRN}$ vs Temperature



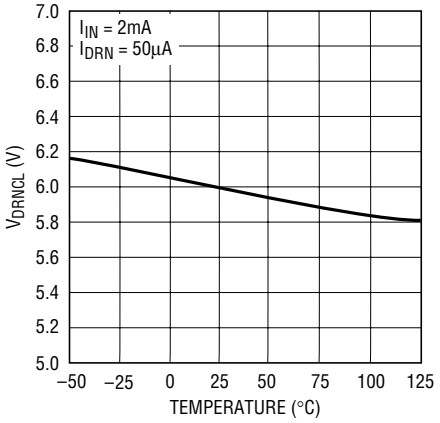
SQTIMER Threshold vs Temperature



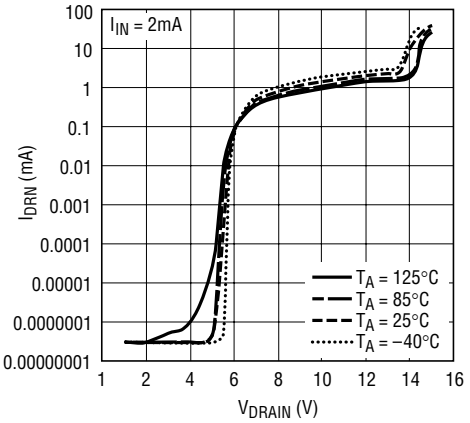
V_{DRNL} vs Temperature



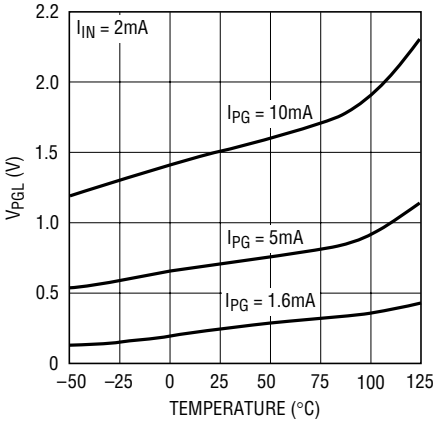
V_{DRNCL} vs Temperature



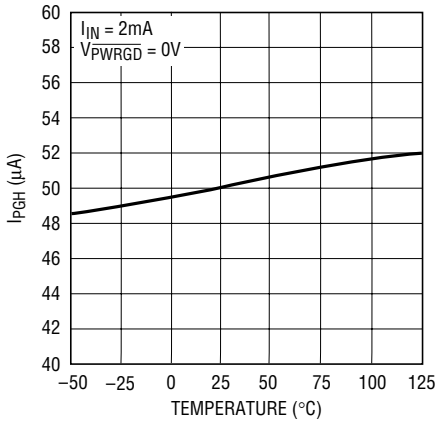
I_{DRN} vs V_{DRAIN}



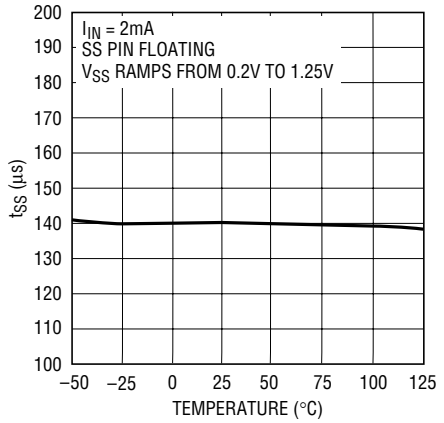
V_{PGL} vs Temperature



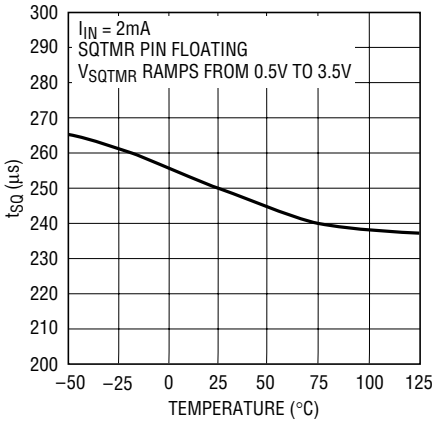
I_{PGH} vs Temperature



t_{SS} vs Temperature



t_{SQ} vs Temperature



PIN FUNCTIONS (SSOP/QFN)

EN2 (Pin 1/Pin 18): Power Good Status Output Two Enable. This is a TTL compatible input that is used to control $\overline{PWRGD2}$ and $\overline{PWRGD3}$ outputs. When EN2 is driven low, both $\overline{PWRGD2}$ and $\overline{PWRGD3}$ will go high. When EN2 is driven high, $\overline{PWRGD2}$ will go low provided $\overline{PWRGD1}$ has been active for more than one power good sequence delay (t_{SQT}) provided by the sequencing timer. EN2 can be used to control the power good sequence. This pin is internally pulled low by a 120µA current source.

$\overline{PWRGD2}$ (Pin 2/Pin 19): Power Good Status Output Two. Power good sequence starts with DRAIN going below 2.39V and GATE is within 2.8V on V_{IN}. $\overline{PWRGD2}$ will latch active low after EN2 goes high and after one power good sequence delay t_{SQT} provided by the sequencing timer from the time $\overline{PWRGD1}$ goes low, whichever comes later. $\overline{PWRGD2}$ is reset by $\overline{PWRGD1}$ going high or EN2 going low. This pin is internally pulled high by a 50µA current source.

$\overline{PWRGD1}$ (Pin 3/Pin 20): Power Good Status Output One. At start-up, $\overline{PWRGD1}$ latches active low one t_{SQT} after both DRAIN is below 2.39V and GATE is within 2.8V of V_{IN}. $\overline{PWRGD1}$ status is reset by undervoltage, V_{IN} (UVLO), RESET going high or circuit breaker fault time-out. This pin is internally pulled high by a 50µA current source.

V_{IN} (Pin 4/Pin 1): Positive Supply Input. Connect this pin to the positive side of the supply through a dropping resistor. A shunt regulator clamps V_{IN} at 13V above V_{EE}. An internal undervoltage lockout (UVLO) circuit holds GATE low until the V_{IN} pin is greater than V_{LKO} (9V), overriding undervoltage and overvoltage events. If there is no undervoltage, no overvoltage and V_{IN} comes out of UVLO, TIMER starts an initial timing cycle before initiating GATE ramp up. If V_{IN} drops below approximately 8.5V, GATE pulls low immediately.

RESET (Pin 5/Pin 2): Circuit Breaker Reset Pin. This is an asynchronous TTL compatible input. RESET going high will pull GATE, SS, TIMER, SQTIMER low and the $\overline{PWRGD}$ outputs high. The RESET pin has an internal glitch filter that rejects any pulse < 20µs. After the reset of a latched fault, the chip waits for the interlock conditions before recovering as described in Interlock Conditions in the Operation section.

SS (Pin 6/Pin 3): Soft-Start Pin. This pin is used to ramp inrush current during start up, thereby effecting control over di/dt. A 20X attenuated version of the SS pin voltage is presented to the current limit amplifier. This attenuated voltage limits the MOSFET's drain current through the sense resistor during the soft-start current limiting. At the beginning of the start-up cycle, the SS capacitor (C_{SS}) is ramped by a 28µA current source. The GATE pin is held low until SS exceeds 20 • V_{OS} = 0.2V. SS is internally shunted by a 50k R_{SS} which limits the SS pin voltage to 1.4V. This corresponds to an analog current limit SENSE voltage of 60mV.

SEL (Pin 7/Pin 4): Soft-Start Mode Select. This is an asynchronous TTL compatible input. SEL has an internal pull-up of 20µA that will pull it high if it is floated. SEL selects between two modes of SS ramp-up (see Applications Information, Soft-Start section).

SENSE (Pin 8/Pin 5): Circuit Breaker/Current Limit Sense Pin. Load current is monitored by a sense resistor R_S connected between SENSE and V_{EE}, and controlled in three steps. If SENSE exceeds V_{CB} (50mV), the circuit breaker comparator activates a (200µA + 8 • I_{DRN}) TIMER pull-up current. If SENSE exceeds V_{ACL} (60mV), the analog current-limit amplifier pulls GATE down to regulate the MOSFET current at V_{ACL}/R_S. In the event of a catastrophic short-circuit, SENSE may overshoot V_{ACL}. If SENSE reaches V_{FCL} (200mV), the fast current-limit comparator pulls GATE low with a strong pull-down. To disable the circuit breaker and current limit functions, connect SENSE to V_{EE}.

V_{EE} (Pins 9, 10/Pin 7): Negative Supply Voltage Input. Connect this pin to the negative side of the power supply.

GATE (Pin 11/Pin 8): N-channel MOSFET Gate Drive Output. This pin is pulled high by a 50µA current source. GATE is pulled low by invalid conditions at V_{IN} (UVLO), undervoltage, overvoltage, during the initial timing cycle, a circuit breaker fault time-out or the RESET pin going high. GATE is actively servoed to control the fault current as measured at SENSE. Compensation capacitor, C_C, at GATE stabilizes this loop. A comparator monitors GATE to ensure that it is low before allowing an initial timing cycle, then the GATE ramps up after an overvoltage event or

PIN FUNCTIONS (SSOP/QFN)

restart after a current limit fault. During GATE start-up, a second comparator detects GATE within 2.8V of V_{IN} before power good sequencing starts.

DRAIN (Pin 12/Pin 9): Drain Sense Input. Connecting an external resistor, R_D between this pin and the MOSFET's drain (V_{OUT}) allows voltage sensing below 5V and current feedback to TIMER. A comparator detects if DRAIN is below 2.39V and together with the GATE high comparator, starts the power good sequencing. If V_{OUT} is above V_{DRNCL}, the DRAIN pin is clamped at approximately V_{DRNCL}. R_D current is internally multiplied by 8 and added to TIMER's 200μA during a circuit breaker fault cycle. This reduces the fault time and MOSFET heating.

OV/OVL (Pins 13, 14/Pins 10, 11): Overvoltage and Overvoltage Low Inputs. The OV and OVL pins work together to implement the overvoltage function. OVL and OV must be tapped from an external resistive string across the input supply such that $V_{OVL} \geq V_{OV}$ under all circumstances. As the input supply ramps up, the OV pin input is multiplexed to the internal overvoltage comparator input. If OV > 5.09V, GATE pulls low and the overvoltage comparator input is switched to OVL. When OVL returns below 5.08V, GATE start-up begins without an initial timing cycle and the overvoltage comparator input is switched to OV. In this way, an external resistor between OVL and OV can set a low to high and high to low overvoltage threshold hysteresis that will add to the internal 10mV hysteresis. A 1nF to 10nF capacitor at OVL prevents transients and switching noise at both OVL and OV from causing glitches at the GATE.

UV/UVL (Pins 15, 16/Pins 12, 13): Undervoltage and Undervoltage Low Inputs. The UV and UVL pins work together to implement the undervoltage function. UVL and UV must be tapped from an external resistive string across the input supply such that $V_{UVL} \geq V_{UV}$ under all circumstances. As the input supply ramps up, the UV pin input is multiplexed to the internal undervoltage comparator input. If UV > 3.08V, an initial timing cycle is initiated followed by GATE start-up and input to the undervoltage comparator input is switched to UVL. When UVL returns below 3.08V, $\overline{\text{PWRGD1}}$ pulls high, both GATE and TIMER pull low and input to the undervoltage comparator input is switched to UV. In this way, an external resistor between UVL and UV can set the low to high and high to low undervoltage threshold hysteresis. A 1nF to 10nF capacitor at UVL prevents transients and switching noise at both UVL and UV from causing glitches at the GATE pin.

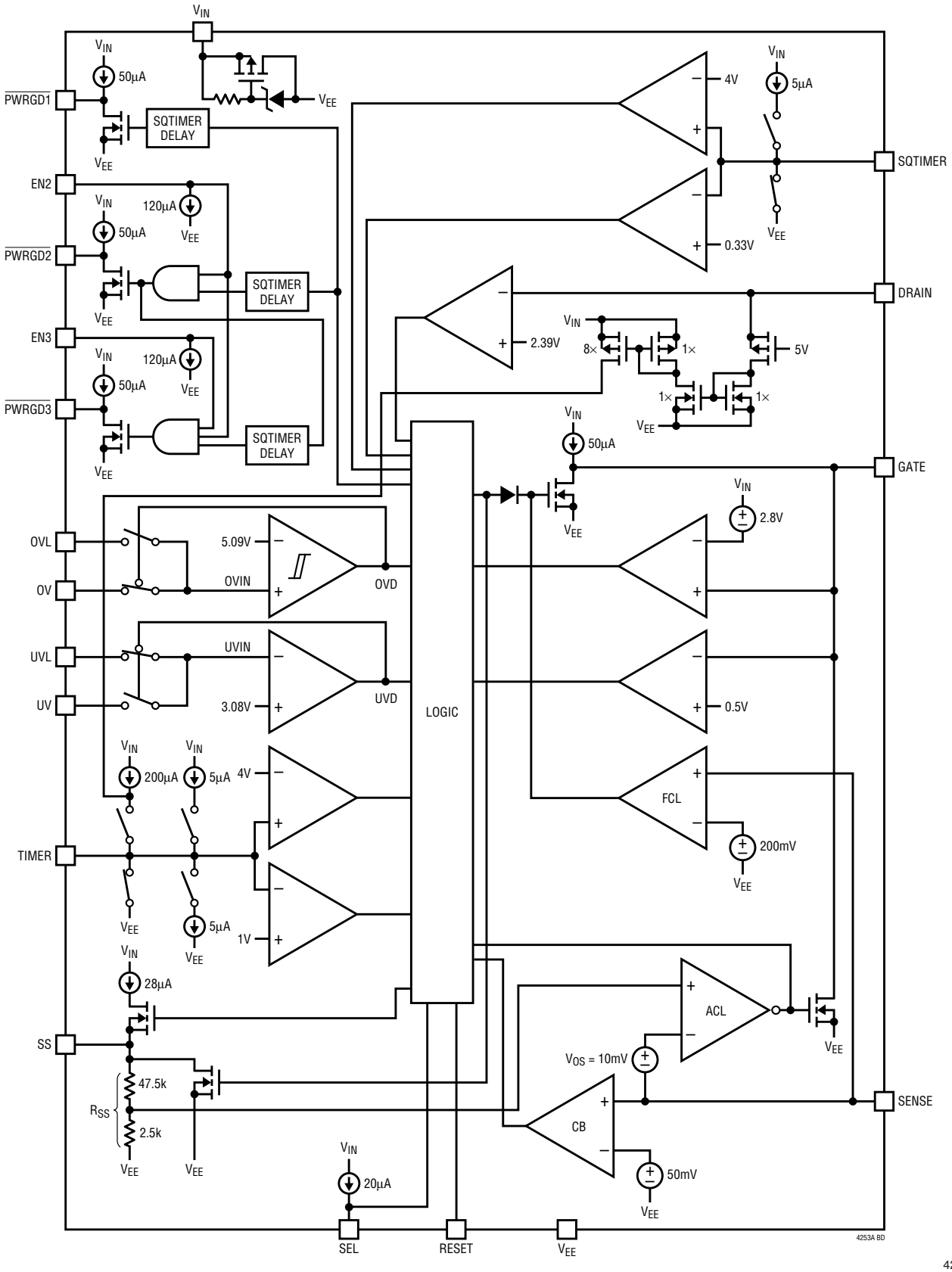
TIMER (Pin 17/Pin 14): Timer Input. Timer is used to generate an initial timing delay at start-up, and to delay shutdown in the event of an output overload (circuit breaker fault). These delays are adjustable by connecting an appropriate capacitor to this pin.

SQTIMER (Pin 18/Pin 15): Sequencing Timer Input. The sequencing timer provides a delay t_{SQT} for the power good sequencing. This delay is adjusted by connecting an appropriate capacitor to this pin. If the SQTIMER capacitor is omitted, the SQTIMER pin ramps from 0V to 4V in about 300μs.

EN3 (Pin 19/Pin 16): Power Good Status Output Three Enable. This is a TTL compatible input that is used to control the $\overline{\text{PWRGD3}}$ output. When EN3 is driven low, $\overline{\text{PWRGD3}}$ will go high. When EN3 is driven high, $\overline{\text{PWRGD3}}$ will go low provided $\overline{\text{PWRGD2}}$ has been active for for more than one power good sequence delay (t_{SQT}). EN3 can be used to control the power good sequence. This pin is internally pulled low by a 120μA current source.

$\overline{\text{PWRGD3}}$ (Pin 20/Pin 17): Power Good Status Output Three. Power good sequence starts with DRAIN going below 2.39V and GATE is within 2.8V of V_{IN}. $\overline{\text{PWRGD3}}$ will latch active low after EN3 goes high and after one power good sequence delay t_{SQT} provided by the sequencing timer from the time $\overline{\text{PWRGD2}}$ goes low, whichever comes later. $\overline{\text{PWRGD3}}$ is reset by $\overline{\text{PWRGD1}}$ going high or EN3 going low. This pin is internally pulled high by a 50μA current source.

BLOCK DIAGRAM



4253a-adjf

OPERATION

Hot Circuit Insertion

When circuit boards are inserted into a live backplane, the supply bypass capacitors can draw huge transient currents from the power bus as they charge. The flow of current damages the connector pins and glitches the power bus, causing other boards in the system to reset. The LTC4253A-ADJ is designed to turn on a circuit board supply in a controlled manner, allowing insertion or removal without glitches or connector damage.

Initial Start-Up

The LTC4253A-ADJ resides on a removable circuit board and controls the path between the connector and load or power conversion circuitry with an external MOSFET switch. Both inrush control and short-circuit protection are provided by the MOSFET.

A detailed schematic is shown in Figure 1. –48V and –48RTN receive power through the longest connector pins and are the first to connect when the board is inserted. The GATE pin holds the MOSFET off during this time. UV/UVL/OV/OVL determines whether or not the MOSFET should be turned on based upon internal high accuracy thresholds and an external divider. UV/UVL/OV/OVL does double duty by also monitoring whether or not the connector is seated. The top of the divider detects –48RTN by way of a short connector pin that is the last to mate during the insertion sequence.

Interlock Conditions

A start-up sequence commences once these "interlock" conditions are met:

1. The input voltage V_{IN} exceeds V_{LKO} (UVLO)
2. The voltage at UV > V_{UVHI}
3. The voltage at OVL < V_{OVLO}
4. The input voltage at RESET < 0.8V
5. The (SENSE – V_{EE}) voltage < 50mV (V_{CB})
6. The voltage at SS is < 0.2V (20 • V_{OS})
7. The voltage on the TIMER capacitor (C_T) is < 1V (V_{TMRL})
8. The voltage at GATE is < 0.5V (V_{GATEL})

The first four conditions are continuously monitored and the latter four are checked prior to initial timing or GATE ramp-up. Upon exiting an overvoltage condition, the TIMER pin voltage requirement is inhibited. Details are described in the Applications Information, Timing Waveforms section.

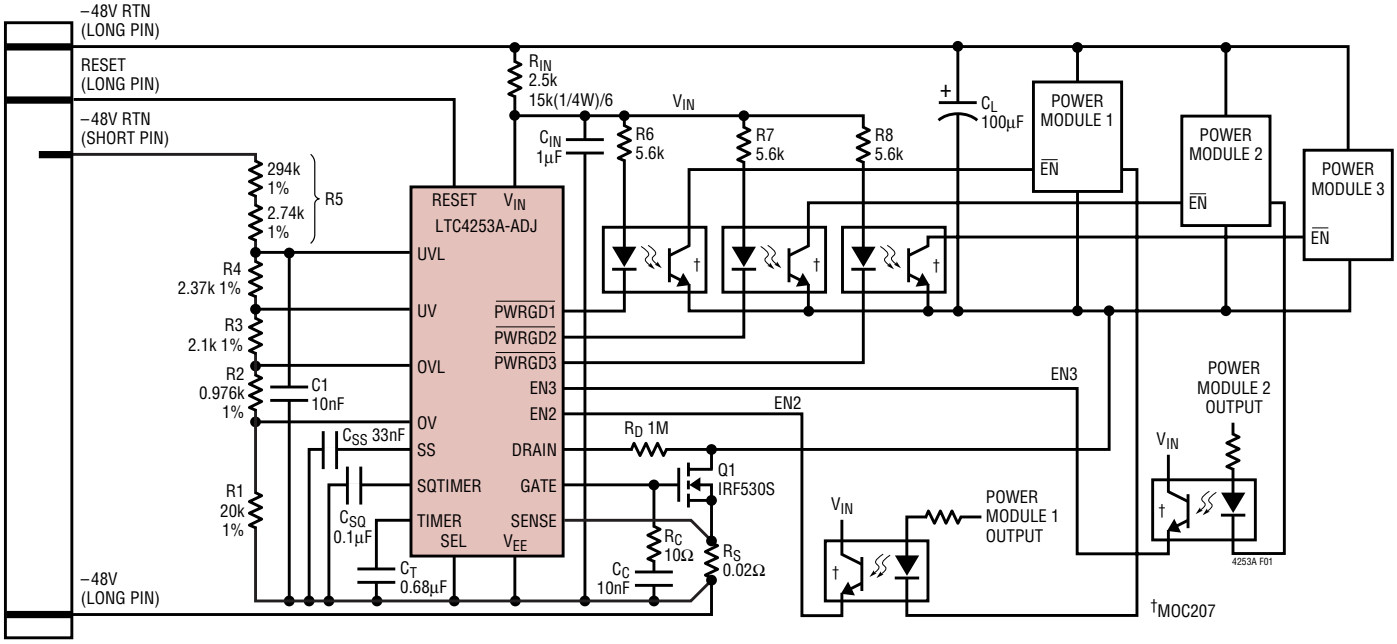


Figure 1. –48V/2.5A Application with Operating Range from 43V to 82V

4253a-adjf

OPERATION

If RESET < 0.8V occurs after the LTC4253A-ADJ comes out of UVLO (interlock condition 1) and undervoltage (interlock condition 2), GATE and SS are released without an initial TIMER cycle once the other interlock conditions are met (see Figure 13a). If not, TIMER begins the start-up sequence by sourcing 5μA into C_T. If V_{IN}, UVL/UV or OVL/OV falls out of range or RESET asserts, the start-up cycle stops and TIMER discharges C_T to less than 1V, then waits until the aforementioned conditions are once again met. If C_T successfully charges to 4V, TIMER pulls low and both SS and GATE pins are released. GATE sources 50μA (I_{GATE}), charging the MOSFET gate and associated capacitance. The SS voltage ramp limits V_{SENSE} to control the inrush current. The SEL pin selects between two different modes of SS ramp-up (refer to Applications Information, Soft-Start section). SQTIMER starts its ramp-up when GATE is within 2.8V of V_{IN} and DRAIN is lower than V_{DRNL}. This sets off the power good sequence in which $\overline{PWRGD1}$, $\overline{PWRGD2}$ and then $\overline{PWRGD3}$ is subsequently pulled low after a delay, adjustable through the SQTIMER capacitor C_{SQ} or by external control inputs EN2 and EN3. In this way, external loads or power modules controlled by the three $\overline{PWRGD}$ signals are turned on in a controlled manner without overloading the power bus.

Two modes of operation are possible during the time the MOSFET is first turned on, depending on the values of external components, MOSFET characteristics and nominal design current. One possibility is that the MOSFET will turn on gradually so that the inrush into the load capacitance remains a low value. The output will simply ramp to –48V and the LTC4253A-ADJ will fully enhance the MOSFET. A second possibility is that the load current exceeds the soft-start current limit threshold of $[V_{SS}(t)/20 – V_{OS}]/R_S$. In this case the LTC4253A-ADJ will ramp the output by sourcing soft-start limited current into the load capacitance. If the soft-start voltage is below 1.2V, the circuit breaker TIMER is held low. Above 1.2V, TIMER ramps up. It is important to set the timer delay so that, regardless of which start-up mode is used, the TIMER ramp is less than one circuit breaker delay time. If this condition is not met, the LTC4253A-ADJ may shut down after one circuit breaker delay time.

Board Removal

When the board is withdrawn from the card cage, the UVL/UV/OVL/OV divider is the first to lose connection. This shuts off the MOSFET and commutates the flow of current in the connector. When the power pins subsequently separate there is no arcing.

Current Control

Three levels of protection handle short-circuit and overload conditions. Load current is monitored by SENSE and resistor R_S. There are three distinct thresholds at SENSE: 50mV for a timed circuit breaker function; 60mV for an analog current limit loop; and 200mV for a fast, feedforward comparator which limits peak current in the event of a catastrophic short-circuit.

If, due to an output overload, the voltage drop across R_S exceeds 50mV, TIMER sources 200μA into C_T. C_T eventually charges to a 4V threshold and the LTC4253A-ADJ shuts off. If the overload goes away before C_T reaches 4V and SENSE measures less than 50mV, C_T slowly discharges (5μA). In this way the LTC4253A-ADJ's circuit breaker function responds to low duty cycle overloads, and accounts for the fast heating and slow cooling characteristic of the MOSFET.

Higher overloads are handled by an analog current limit loop. If the drop across R_S reaches V_{ACL}, the current limiting loop servos the MOSFET gate and maintains a constant output current of V_{ACL}/R_S. In current limit mode, V_{OUT} (MOSFET drain-source voltage drop) typically rises and this increases MOSFET heating. If $V_{OUT} > V_{DRNCL}$, connecting an external resistor, R_D between V_{OUT} and DRAIN allows the fault timing cycle to be shortened by accelerating the charging of the TIMER capacitor. The TIMER pull-up current is increased by $8 \bullet I_{DRN}$. Note that because SENSE > 50mV, TIMER charges C_T during this time, and the LTC4253A-ADJ will eventually shut down.

Low impedance failures on the load side of the LTC4253A-ADJ coupled with 48V or more driving potential can produce current slew rates well in excess of 50A/μs. Under these conditions, overshoot is inevitable. A fast SENSE

OPERATION

comparator with a threshold of 200mV detects overshoot and pulls GATE low much harder and hence much faster than the weaker current limit loop. The V_{ACL}/R_S current limit loop then takes over, and servos the current as previously described. As before, TIMER runs and shuts down LTC4253A-ADJ when C_T reaches 4V.

If C_T reaches 4V, the LTC4253A-ADJ latches off with a 5μA pull-up current source. The LTC4253A-ADJ circuit breaker latch is reset by either pulling the RESET pin active high for >20μs, pulling UVL/UV momentarily low, dropping the input voltage V_{IN} below the internal UVLO threshold or pulsing TIMER momentarily low with a switch.

Although short-circuits are the most obvious fault type, several operating conditions may invoke overcurrent protection. Noise spikes from the backplane or load, input steps caused by the connection of a second, higher voltage supply, transient currents caused by faults on adjacent circuit boards sharing the same power bus or the insertion of non-hot swappable products could cause higher than anticipated input current and temporary detection of an overcurrent condition. The action of TIMER and C_T rejects these events allowing the LTC4253A-ADJ to “ride out” temporary overloads and disturbances that could trip a simple current comparator and, in some cases, blow a fuse.

APPLICATIONS INFORMATION (Refer to Block Diagram)

SHUNT REGULATOR

A fast responding regulator shunts the LTC4253A-ADJ V_{IN} pin. Power is derived from –48RTN by an external current limiting resistor. The shunt regulator clamps V_{IN} to 13V (V_Z). A 1µF decoupling capacitor at V_{IN} filters supply transients and contributes a short delay at start-up. R_{IN} should be chosen to accommodate both V_{IN} supply current and the drive required for three optocouplers used by the $\overline{PWRGD}$ signals. Higher current through R_{IN} results in higher dissipation for R_{IN} and LTC4253A-ADJ as well as higher V_{IN} noise. Alternative circuits are V_{IN} with an NPN buffer as in Figure 16, V_{IN} driving base resistors of NPN cascodes as in Figure 17 or V_{IN} driving the gates of MOSFET cascodes replacing the NPNs in Figure 17. An alternative is a separate NPN buffer driving the optocoupler as shown in Figure 16. Multiple 1/4W resistors can replace a single higher power R_{IN} resistor.

INTERNAL UNDERVOLTAGE LOCKOUT (UVLO)

A hysteretic comparator, UVLO, monitors V_{IN} for undervoltage. The thresholds are defined by V_{LKO} and its hysteresis V_{LKH}. When V_{IN} rises above V_{LKO} the chip is enabled; below ($V_{LKO} – V_{LKH}$) it is disabled and GATE is pulled low. The UVLO function at V_{IN} should not be confused with the UVL/UV and OVL/OV pins. These are completely separate functions.

UNDERVOLTAGE AND OVERVOLTAGE COMPARATORS

The undervoltage comparator has inputs multiplexed from UVL and UV. When comparator output UVD is high, UV is multiplexed to the comparator input UVIN. When UVD is low, UVL is multiplexed to UVIN. By tapping UVL and UV off a resistive string across the supply such as in the Typical Application, the undervoltage function is implemented as shown in Figure 2a. During UVLO, UVD is forced high so UV is multiplexed to UVIN. At time point 1, V_{IN} ramps past V_{LKO} and the undervoltage comparator is enabled. UVIN = UV is less than V_{UVHI} (3.08V), so UVD is high and the part is in undervoltage shutdown. At time point 2, UV ramps past V_{UVHI} (3.08V) and UVD goes low, bringing the part out of undervoltage and switching UVL to UVIN. UVL is tied to UVIN until time point 3 when UVL ramps past V_{UVLO} (3.08V) and UVD goes high, bringing the part into undervoltage shutdown and switching UV to UVIN.

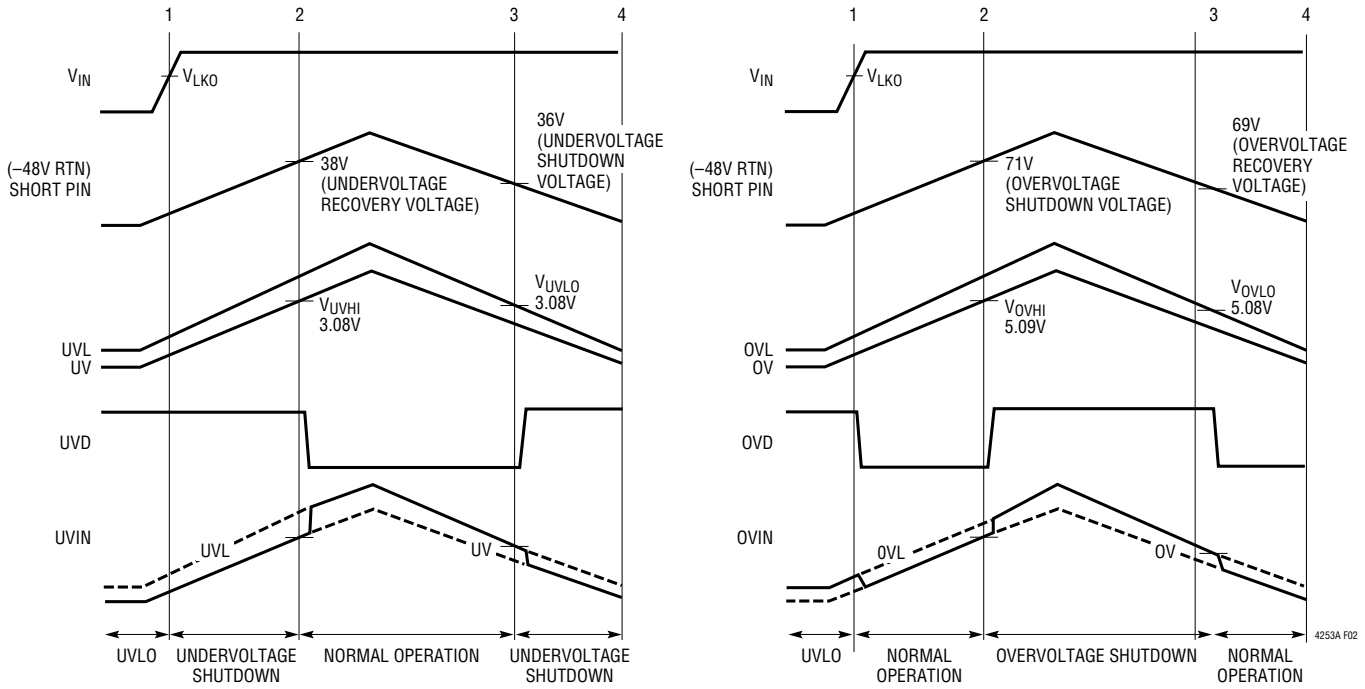


Figure 2. Undervoltage/Overvoltage Recovery and Shutdown (All Waveforms are Referenced to V_{EE})

4253a-adjf

APPLICATIONS INFORMATION

Figure 2b shows the implementation of the overvoltage function of the Typical Application. During UVLO, OVD is forced high so OVL is multiplexed to OVIN. At time point 1, the part exits UVLO and the overvoltage comparator is enabled. OVIN = OVL is less than V_{OVLO} (5.08V) so OVD goes low, switching OV to OVIN and bringing the part to Normal mode. At time point 2, OV ramps past V_{OVHI} (5.09V) and OVD goes high, switching OVL to OVIN as well as turning on the internal 10mV hysteresis as the part goes into overvoltage. OVL is tied to OVIN until time point 3 when OVL ramps past V_{OVLO} (5.09V – 10mV = 5.08V) and OVD goes low, bringing the part into Normal mode and switching OV to OVIN.

The undervoltage (UV) comparator has no internal hysteresis to preserve the accuracy of the hysteresis set across UVL/UV while the overvoltage (OV) comparator has an internal low to high hysteresis of 10mV. This will add to the hysteresis set across OVL/OV and provide some noise immunity if OVL/OV is shorted together. Any implementation must ensure that $V_{UVL} \geq V_{UV}$ and $V_{OVL} \geq V_{OV}$ under all conditions.

The various thresholds to note are:

UV low-to-high (V_{UVHI}) = 3.08V

UVL high-to-low (V_{UVLO}) = 3.08V

OV low-to-high (V_{OVHI}) = 5.09V

OVL high-to-low (V_{OVLO}) = 5.08V

Using these thresholds and an external resistive divider, any required supply operating range can be implemented. An example is shown in Figure 1 where the required typical operating range is:

Undervoltage low-to-high (V_{48UVHI}) = 43V

Undervoltage high-to-low (V_{48UVLO}) = 39V

Overvoltage low-to-high (V_{48OVHI}) = 82V

Overvoltage high-to-low (V_{48OVLO}) = 78V

A quick check of the resistive divider ratios required at UVL, UV, OVL and OV confirms that UVL is tapped between R5/R4, UV is tapped between R4/R3, OVL is tapped between R3/R2 and OV is tapped between R2/R1.

From Figure 1, by looking at the voltages at OV, OVL, UV and UVL, the following equations are obtained:

$$\frac{R_{TOTAL}}{R1} = \frac{V_{48OVHI}}{V_{OVHI}}$$

where:

$$R_{TOTAL} = (R1 + R2 + R3 + R4 + R5)$$

$$R_{TOTAL} = \frac{R1 \bullet V_{48OVHI}}{V_{OVHI}} \quad (1a)$$

$$\frac{R_{TOTAL}}{R1 + R2} = \frac{V_{48OVLO}}{V_{OVLO}}$$

$$R2 = R1\left(\frac{V_{OVLO}}{V_{48OVLO}} \bullet \frac{V_{48OVHI}}{V_{OVHI}}\right) - R1 \quad (1b)$$

$$\frac{R_{TOTAL}}{R1 + R2 + R3} = \frac{V_{48UVHI}}{V_{UVHI}}$$

$$R3 = R1\left(\frac{V_{UVHI}}{V_{48UVHI}} \bullet \frac{V_{48OVHI}}{V_{OVHI}}\right) - R1 - R2 \quad (1c)$$

$$\frac{R_{TOTAL}}{R1 + R2 + R3 + R4} = \frac{V_{48UVLO}}{V_{UVLO}}$$

$$R4 = R1\left(\frac{V_{UVLO}}{V_{48UVLO}} \bullet \frac{V_{48OVHI}}{V_{OVHI}}\right) - R1 - R2 - R3 \quad (1d)$$

Starting with a value of 20k for R1, Equation 1b gives R2 = 0.984k (use closest 1% standard value of 0.976k). Using R1 = 20k and R2 = 0.976k, Equation 1c gives R3 = 2.103k (use the closest 1% standard value of 2.1k). Using R1 = 20k, R2 = 0.976k and R3 = 2.1k, Equation 1d gives R4 = 2.37k (use closest 1% standard value of 2.37k). Using R1 = 20k, R2 = 0.976k, R3 = 2.1k and R4 = 2.37k in Equation 1a, R5 = 296.754k (use 1% standard values of 294k in series with 2.74k).

The divider values shown set a standing current of slightly more than 150μA and define an impedance at UVL/UV/OVL/OV of approximately 20k. This impedance will work with the hysteresis set across UVL/UV and OVL/OV to provide noise immunity to the UV and OV comparators. If

APPLICATIONS INFORMATION

more noise immunity is desired, add a 1nF to 10nF filter capacitor from UVL to V_{EE}.

UV/OV OPERATION

An undervoltage condition detected by the UV comparator immediately shuts down the LTC4253A-ADJ, pulls GATE, SS and TIMER low and resets the three latched PWRGD signals high. Recovery from an undervoltage will initiate an initial timing sequence if the other interlock conditions are met.

An overvoltage condition is detected by the OV comparator and pulls GATE low, thereby shutting down the load, but it will not reset the circuit breaker TIMER and PWRGD flags. Returning from the overvoltage condition will restart the GATE pin if all the interlock conditions except TIMER are met. Only during the initial timing cycle does an overvoltage condition have an effect of resetting TIMER. The internal UVLO at V_{IN} always overrides an overvoltage or undervoltage.

DRAIN

Connecting an external resistor, R_D, to this dual function DRAIN pin allows V_{OUT} (MOSFET drain-source voltage drop) sensing without it being damaged by large voltage transients. Below 5V, negligible pin leakage allows a DRAIN low comparator to detect V_{OUT} less than 2.39V (V_{DRNL}). This, together with the GATE low comparator, starts the power good sequencing.

When $V_{OUT} > V_{DRNCL}$, the DRAIN pin is clamped at V_{DRNCL} and the current flowing in R_D is given by:

$$I_{DRN} \approx \frac{V_{OUT} - V_{DRNCL}}{R_D} \quad (2)$$

This current is scaled up 8 times during a circuit breaker fault before being added to the nominal 200μA. This accelerates the fault TIMER pull-up when the MOSFET's drain-source voltage exceeds V_{DRNCL} and effectively shortens the MOSFET heating duration.

TIMER

The operation of the TIMER pin is somewhat complex as it handles several key functions. A capacitor C_T is used at TIMER to provide timing for the LTC4253A-ADJ. Four different charging and discharging modes are available at TIMER:

1. 5μA slow charge; initial timing delay.
2. (200μA + 8 • I_{DRN}) fast charge; circuit breaker delay.
3. 5μA slow discharge; circuit breaker "cool-off."
4. Low impedance switch; resets the TIMER capacitor after an initial timing delay, in UVLO, in UV and in OV during initial timing and when RESET is high.

For initial timing delay, the 5μA pull-up is used. The low impedance switch is turned off and the 5μA current source is enabled when the interlock conditions are met. C_T charges to 4V in a time period given by:

$$t = \frac{4V \bullet C_T}{5\mu A} \quad (3)$$

When C_T reaches V_{TMRH} (4V), the low impedance switch turns on and discharges C_T. A GATE start-up cycle begins and both SS and GATE outputs are released.

CIRCUIT BREAKER TIMER OPERATION

If the SENSE pin detects more than 50mV drop across R_S, the TIMER pin charges C_T with (200μA + 8 • I_{DRN}). If C_T charges to 4V, the GATE pin pulls low and the LTC4253A-ADJ latches off. The LTC4253A-ADJ remains latched off until the RESET pin is momentarily pulsed high, the UVL/UV pin is momentarily pulsed low, the TIMER pin is momentarily discharged low by an external switch or V_{IN} dips below UVLO and is then restored. The circuit breaker timeout period is given by:

$$t = \frac{4V \bullet C_T}{200\mu A + 8 \bullet I_{DRN}} \quad (4)$$

If $V_{OUT} < 5V$, an internal PMOS isolates DRAIN pin leakage current and this makes $I_{DRN} = 0$ in Equation 4. If V_{OUT} is above V_{DRNCL} during the circuit breaker fault period, the charging of C_T is accelerated by 8 • I_{DRN} of Equation 2.

Intermittent overloads may exceed the 50mV threshold at SENSE but, if their duration is sufficiently short, TIMER will not reach 4V and the LTC4253A-ADJ will not shut the

APPLICATIONS INFORMATION

external MOSFET off. To handle this situation, the TIMER discharges C_T slowly with a 5μA pull-down whenever the SENSE voltage is less than 50mV. Therefore any intermittent overload with $V_{OUT} < 5V$ and an aggregate duty cycle of more than 2.5% will eventually trip the circuit breaker and shut down the LTC4253A-ADJ. Figure 3 shows the circuit breaker response time in seconds normalized to 1μF. The asymmetric charging and discharging of C_T is a fair gauge of MOSFET heating.

The normalized circuit response time is estimated by:

$$\frac{t}{C_T(\mu F)} = \frac{4}{\left[\left(205 + 8 \bullet I_{DRN}\right) \bullet D - 5\right]} \text{ for } D > 2.5\% \quad (5)$$

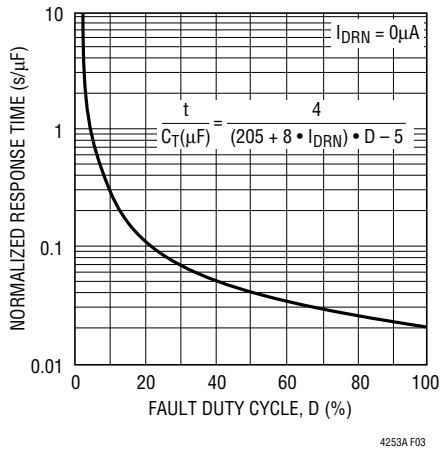


Figure 3. Circuit Breaker Response Time

POWER GOOD SEQUENCING

After the initial TIMER cycle, GATE ramps up to turn on the external MOSFET which in turn pulls DRAIN low. When GATE is within 2.8V of V_{IN} and DRAIN is lower than V_{DRNL}, the power good sequence starts off a 5μA pull-up on the SQTIMER pin which ramps up until it reaches the 4V threshold then pulls low. When the SQTIMER pin floats, this delay t_{SQT} is about 300μs. Connecting an external capacitor C_{SQ} from SQTIMER to V_{EE} modifies the delay to:

$$t_{SQT} = \frac{4V \bullet C_{SQ}}{5\mu A} \quad (6)$$

$\overline{PWRGD1}$ asserts low after one t_{SQT} and SQTIMER ramps up on another delay cycle. $\overline{PWRGD2}$ asserts when EN2 goes high and $\overline{PWRGD1}$ has asserted for more than one t_{SQT}. When $\overline{PWRGD2}$ successfully pulls low, SQTIMER ramps up on another delay cycle. $\overline{PWRGD3}$ asserts when EN2 and EN3 go high and $\overline{PWRGD2}$ has asserted for more than one t_{SQT}.

All three $\overline{PWRGD}$ signals are reset in UVLO, in UV condition, if RESET is high or when C_T charges up to 4V. In addition, $\overline{PWRGD2}$ is reset by EN2 going low. $\overline{PWRGD3}$ is reset by EN2 or EN3 going low. An overvoltage condition has no effect on the $\overline{PWRGD}$ flags. A 50μA current pulls each $\overline{PWRGD}$ pin high when reset. As power modules signal common are different from $\overline{PWRGD}$, optoisolation is recommended. These three pins can sink an optodiode current. Figure 17 shows an NPN configuration for the $\overline{PWRGD}$ interface. A limiting base resistor should be used for each NPN and the module enable input should have protection from negative bias current. Figure 17 also shows how the LTC4253A-ADJ can be used to sequence four power modules.

SOFT-START

Soft-start is effective in limiting the inrush current during GATE start-up. From the Block Diagram, the internal SS circuit consists of a current I_{SS} (28μA) feeding into a resistive divider. The resistive divider (47.5k/2.5k) scales V_{SS} (t) down by 20 times to give the analog current limit threshold:

$$V_{ACL}(t) = \frac{V_{SS}(t)}{20} - V_{OS} \quad (7)$$

After the initial timing cycle, SS ramps up from 0V to 1.4V (28μA • 50k), ramping V_{ACL} (t) from –10mV to 60mV. The ACL amplifier will then limit the inrush current to V_{ACL} (t)/R_S. The offset voltage, V_{OS} (10mV) ensures C_{SS} is sufficiently discharged and the ACL amplifier is in current limit mode before GATE start-up.

There are two modes of SS ramp up. If SEL is set high and the SS pin floats, an internal current source ramps SS from 0V to 1.4V in about 200μs. Connecting an external capacitor, C_{SS}, from SS to ground modifies the ramp to approximate an RC response of:

$$V_{SS}(t) \approx V_{SS}\left(1 - e^{\frac{-t}{R_{SS}C_{SS}}}\right) \quad (8)$$

APPLICATIONS INFORMATION

When V_{ACL} (t) exceeds V_{SENSE}, the ACL amplifier exits current limit mode and releases its pull-down on GATE. V_{SS} (t) = 20 • (V_{OS} + V_{SENSE}) from Equation 7. So when V_{SS} (t) > 20 • V_{OS} = 0.2V (since V_{SENSE} = 0V), GATE starts to ramp up and SS continues to ramp up. When GATE clears the threshold of the external FET and inrush current starts flowing, V_{ACL} (t) = (V_{SS} (t)/20 – V_{OS}) will have a positive offset from zero. V_{SENSE} will show an initial jump to clear this offset before going into analog current limit (Figure 4a).

If SEL is set low during SS ramp-up, V_{SS} is servoed when it exceeds 20 • V_{OS} = 0.2V and GATE starts its ramp-up. V_{SS} is servoed at a voltage that is just above 20 • V_{OS} to keep the ACL amplifier off and GATE ramping up freely. Once GATE clears the threshold of the external FET, inrush current starts flowing and V_{SENSE} will jump above V_{ACL} (t). This will engage the ACL amplifier and mask off V_{SS} servo so V_{SS} continues its RC ramp-up. In this way, the LTC4253A-ADJ enters analog current limit with V_{ACL} (t) = (V_{SS} (t)/20 – V_{OS}) ramping up from close to zero. The resultant inrush current profile presents a smooth ramp up from zero (Figure 4b). If there is little inrush current so the LTC4253A-ADJ does not enter current limit, V_{SS} servo will be masked off when DRAIN goes below 2.39V (V_{DRNL}) and latched off when GATE goes within 2.8V of V_{IN} (V_{GATEH}). A minimum C_{SS} of 5nF is required for the stability of the V_{SS} servo loop.

SS is discharged low during UVLO, UV, OV, during the initial timing cycle, a latched circuit breaker fault or the RESET pin going high.

GATE

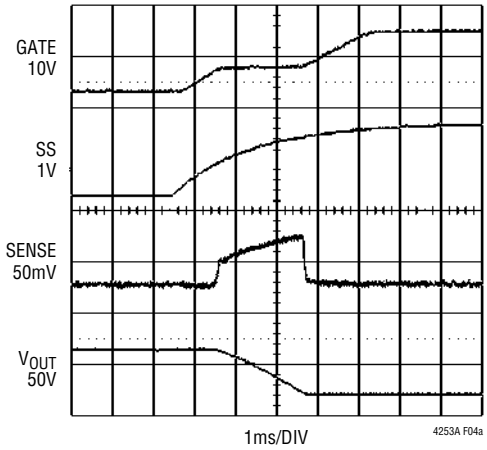
GATE is pulled low to V_{EE} under any of the following conditions: in UVLO, when RESET pulls high, in an undervoltage condition, in an overvoltage condition, during the initial timing cycle or a latched circuit breaker fault. When GATE turns on, a 50µA current source charges the MOSFET gate and any associated external capacitance. V_{IN} limits the gate drive to no more than 14.5V.

Gate-drain capacitance (C_{GD}) feedthrough at the first abrupt application of power can cause a gate-source voltage sufficient to turn on the MOSFET. A unique circuit pulls GATE low with practically no usable voltage at V_{IN}, and eliminates current spikes at insertion. A large external gate-source capacitor is thus unnecessary for the purpose of compensating C_{GD}. Instead, a smaller value (≥10nF) capacitor C_C is adequate. C_C also provides compensation for the analog current limit loop.

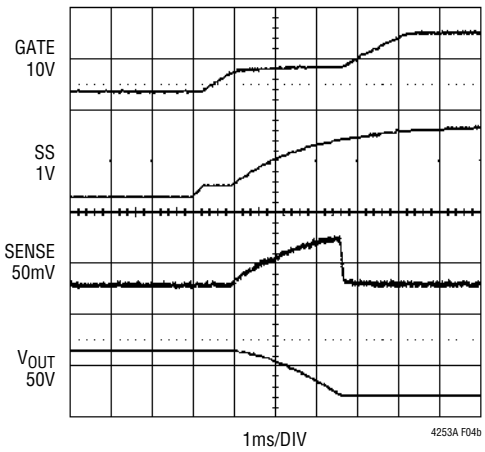
GATE has two comparators: the GATE low comparator looks for <0.5V threshold prior to initial timing; the GATE high comparator looks for <2.8V relative to V_{IN} and, together with DRAIN low comparator, starts power good sequencing during GATE start-up.

SENSE

The SENSE pin is monitored by the circuit breaker (CB) comparator, the analog current limit (ACL) amplifier, and the fast current limit (FCL) comparator. Each of these three measures the potential of SENSE relative to V_{EE}. When



(4a) SEL Set High



(4b) SEL Set Low

Figure 4. Two Modes of SS Ramp Up

APPLICATIONS INFORMATION

SENSE exceeds 50mV, the CB comparator activates the 200μA TIMER pull-up. At 60mV the ACL amplifier servos the MOSFET current, and at 200mV the FCL comparator abruptly pulls GATE low in an attempt to bring the MOSFET current under control. If any of these conditions persists long enough for TIMER to charge C_T to 4V (see Equation 4), the LTC4253A-ADJ shuts down and pulls GATE low.

If the SENSE pin encounters a voltage greater than V_{ACL}, the ACL amplifier will servo GATE downwards in an attempt to control the MOSFET current. Since GATE overdrives the MOSFET in normal operation, the ACL amplifier needs time to discharge GATE to the threshold of the MOSFET. For a mild overload the ACL amplifier can control the MOSFET current, but in the event of a severe overload the current may overshoot. At SENSE = 200mV the FCL comparator takes over, quickly discharging the GATE pin to near V_{EE} potential. FCL then releases, and the ACL amplifier takes over. All the while TIMER is running. The effect of FCL is to add a nonlinear response to the control loop in favor of reducing MOSFET current.

Owing to inductive effects in the system, FCL typically overcorrects the current limit loop, and GATE undershoots. A zero in the loop (resistor R_C in series with the gate capacitor) helps the ACL amplifier to recover.

SHORT-CIRCUIT OPERATION

Circuit behavior arising from a load side low impedance short is shown in Figure 5. Initially the current overshoots the analog current limit level of V_{SENSE} = 200mV (trace 2) as the GATE pin works to bring V_{GS} under control (trace 3). The overshoot glitches the backplane in the negative direction and when the current is reduced to 60mV/R_S, the backplane responds by glitching in the positive direction.

TIMER commences charging C_T (trace 4) while the analog current limit loop maintains the fault current at 60mV/R_S, which in this case is 5A (trace 2). Note that the backplane voltage (trace 1) sags under load. Timer pull-up is accelerated by V_{OUT}. When C_T reaches 4V, GATE turns off, the PWRGD signals pull high, the load current drops to zero and the backplane rings up to over 100V. The transient associated with the GATE turn-off can be controlled with a snubber to reduce ringing and a transient voltage suppressor (such as Diodes Inc. SMAT70A), to clip off large spikes. The choice of RC for the snubber is usually done experimentally. The value of the snubber capacitor is usually chosen between 10 to 100 times the MOSFET C_{OSS}. The value of the snubber resistor is typically between 3Ω to 100Ω.

A low impedance short on one card may influence the behavior of others sharing the same backplane. The initial glitch and backplane sag as seen in Figure 5 trace 1, can rob charge from output capacitors on the adjacent card. When the faulty card shuts down, current flows in to refresh the capacitors. If LTC4253A-ADJs are used by the other cards, they respond by limiting the inrush current to a value of V_{ACL}/R_S. If C_T is sized correctly, the capacitors will recharge long before C_T times out.

MOSFET SELECTION

The external MOSFET switch must have adequate safe operating area (SOA) to handle short-circuit conditions until TIMER times out. These considerations take precedence over DC current ratings. A MOSFET with adequate SOA for a given application can always handle the required current but the opposite may not be true. Consult the manufacturer's MOSFET datasheet for safe operating area and effective transient thermal impedance curves.

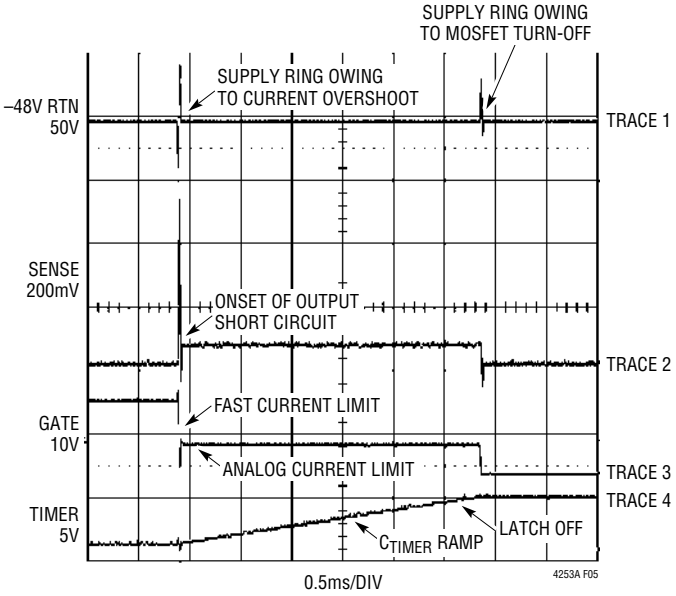


Figure 5. Output Short-Circuit Behavior of LTC4253A-ADJ

APPLICATIONS INFORMATION

MOSFET selection is a 3-step process by assuming the absense of soft-start capacitor. First, R_S is calculated and then the time required to charge the load capacitance is determined. This timing, along with the maximum short-circuit current and maximum input voltage, defines an operating point that is checked against the MOSFET's SOA curve.

To begin a design, first specify the required load current and load capacitance, I_L and C_L. The circuit breaker current trip point (V_{CB}/R_S) should be set to accommodate the maximum load current. Note that maximum input current to a DC/DC converter is expected at $V_{SUPPLY(MIN)}$. R_S is given by:

$$R_S = \frac{V_{CB(MIN)}}{I_{L(MAX)}} \quad (9)$$

where $V_{CB(MIN)}$ = 45mV represents the guaranteed minimum circuit breaker threshold.

During the initial charging process, the LTC4253A-ADJ may operate the MOSFET in current limit, forcing (V_{ACL}) between 54mV to 66mV across R_S. The minimum inrush current is given by:

$$I_{INRUSH(MIN)} = \frac{V_{ACL(MIN)}}{R_S} \quad (10)$$

Maximum short-circuit current limit is calculated using the maximum V_{SENSE}. This gives

$$I_{SHORTCIRCUIT(MAX)} = \frac{V_{ACL(MAX)}}{R_S} \quad (11)$$

The TIMER capacitor, C_T, must be selected based on the slowest expected charging rate; otherwise TIMER might time out before the load capacitor is fully charged. A value for C_T is calculated based on the maximum time it takes the load capacitor to charge. That time is given by:

$$t_{CL(CHARGE)} = \frac{C \bullet V}{I} = \frac{C_L \bullet V_{SUPPLY(MAX)}}{I_{INRUSH(MIN)}} \quad (12)$$

The maximum current flowing in the DRAIN pin is given by:

$$I_{DRN(MAX)} = \frac{V_{SUPPLY(MAX)} - V_{DRNCL}}{R_D} \quad (13)$$

Approximating a linear charging rate, I_{DRN} drops from $I_{DRN(MAX)}$ to zero, the I_{DRN} component in Equation 4 can be approximated with 0.5 • $I_{DRN(MAX)}$. Rearranging the equation, TIMER capacitor C_T is given by:

$$C_T = \frac{t_{CL(CHARGE)} \bullet (200\mu A + 4 \bullet I_{DRN(MAX)})}{4V} \quad (14)$$

Returning to Equation 4, the TIMER period is calculated and used in conjunction with $V_{SUPPLY(MAX)}$ and $I_{SHORTCIRCUIT(MAX)}$ to check the SOA curves of a prospective MOSFET.

As a numerical design example, consider a 30W load, which requires 1A input current at 36V. If $V_{SUPPLY(MAX)}$ = 72V and C_L = 100µF, R_D = 1MΩ, Equation 9 gives R_S = 45mΩ; use R_S = 40mΩ for more margin. Equation 14 gives C_T = 619nF. To account for errors in R_S, C_T, TIMER current (200µA), TIMER threshold (4V), R_D, DRAIN current multiplier and DRAIN voltage clamp (V_{DRNCL}), the calculated value should be multiplied by 1.5, giving the nearest standard value of C_T = 1µF.

If a short-circuit occurs, a current of up to 66mV/45mΩ = 1.65A will flow in the MOSFET for 9.1ms as dictated by C_T = 1µF in Equation 4. The MOSFET must be selected based on this criterion. The IRF530S can handle 100V and 2A for 22.5ms and is safe to use in this application.

Computing the maximum soft-start capacitor value during soft-start to a load short is complicated by the nonlinear MOSFET's SOA characteristics and the $R_{SS}C_{SS}$ response. An overconservative but simple approach begins with the maximum circuit breaker current, given by:

$$I_{CB(MAX)} = \frac{V_{CB(MAX)}}{R_S} \quad (15)$$

From the SOA curves of a prospective MOSFET, determine the time allowed, $t_{SOA(MAX)}$. C_{SS} is given by:

$$C_{SS} = \frac{t_{SOA(MAX)}}{2.48 \bullet R_{SS}} \quad (16)$$

In the above example, 55mV/40mΩ gives 1.375A. t_{SOA} for the IRF530S is 47.6ms. From Equation 16, C_{SS} = 384nF.

APPLICATIONS INFORMATION

Actual board evaluation showed that C_{SS} = 100nF was appropriate. The ratio ($R_{SS} \bullet C_{SS}$) to $t_{CL(CHARGE)}$ is a good gauge as large ratios may result in the time-out period expiring prematurely. This gauge is determined empirically with board level evaluation.

SUMMARY OF DESIGN FLOW

To summarize the design flow, consider the application shown in Figure 1. It was designed for 80W and C_L = 100µF.

Calculate maximum load current: 80W/43V = 1.86A; allowing for 83% converter efficiency, $I_{IN(MAX)}$ = 2.2A.

Calculate R_S: from Equation 9 R_S = 20mΩ.

Calculate $I_{SHORT\text{-}CIRCUIT(MAX)}$: from Equation 11 $I_{SHORTCIRCUIT(MAX)}$ = 3.3A.

Select a MOSFET that can handle 3.3A at 71V: IRF530S.

Calculate C_T: from Equation 14 C_T = 383nF. Select C_T = 680nF, which gives the circuit breaker time-out period t_{MAX} = 5.9ms.

Consult MOSFET SOA curves: the IRF530S can handle 3.3A at 100V for 8.3ms, so it is safe to use in this application.

Calculate C_{SS}: using Equations 15 and 16 select C_{SS} = 33nF.

FREQUENCY COMPENSATION

The LTC4253A-ADJ typical frequency compensation network for the analog current limit loop is a series R_C (10Ω) and C_C connected from GATE to V_{EE}. Figure 6 depicts the relationship between the compensation capacitor C_C and the MOSFET's C_{ISS}. The line in Figure 6 is used to select a starting value for C_C based upon the MOSFET's C_{ISS} specification. Optimized values for C_C are shown for several popular MOSFETs. Differences in the optimized value of C_C versus the starting value are small. Nevertheless, compensation values should be verified by board level short-circuit testing.

As seen in Figure 5, at the onset of a short-circuit event, the input supply voltage can ring dramatically due to series inductance. If this voltage avalanches the MOSFET, current continues to flow through the MOSFET to the output. The analog current limit loop cannot control this current flow and therefore the loop undershoots. This effect cannot be eliminated by frequency compensation. A zener diode is required to clamp the input supply voltage and prevent MOSFET avalanche.

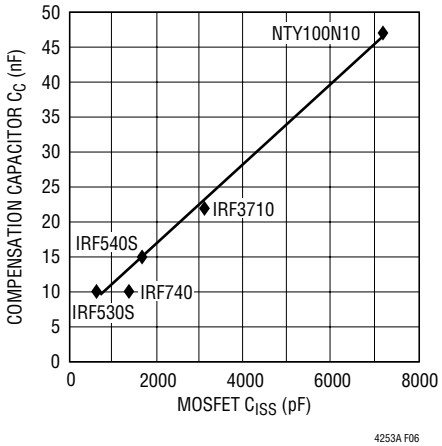


Figure 6. Recommended Compensation Capacitor C_C vs MOSFET C_{ISS}

SENSE RESISTOR CONSIDERATIONS

For proper circuit breaker operation, Kelvin-sense PCB connections between the sense resistor and the LTC4253A-ADJ's V_{EE} and SENSE pins are strongly recommended. The drawing in Figure 7 illustrates the correct way of making connections between the LTC4253A-ADJ and the sense resistor. PCB layout should be balanced and symmetrical to minimize wiring errors. In addition, the PCB layout for the sense resistor should include good thermal management techniques for optimal sense resistor power dissipation.

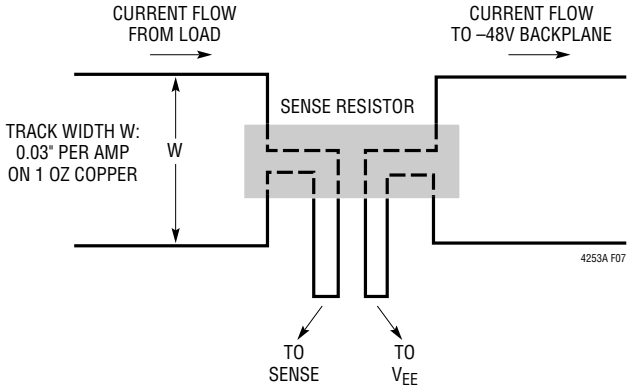


Figure 7. Making PCB Connections to the Sense Resistor

APPLICATIONS INFORMATION

TIMING WAVEFORMS

System Power-Up

Figure 8 details the timing waveforms for a typical power-up sequence in the case where a board is already installed in the backplane and system power is applied abruptly. At time point 1, the supply ramps up, together with UV/OV, V_{OUT} and DRAIN. V_{IN} and the $\overline{PWRGD}$ signals follow at a slower rate as set by the V_{IN} bypass capacitor. At time point 2, V_{IN} exceeds V_{LKO} and the internal logic checks for UV > V_{UVHI}, OVL < V_{OVLO}, RESET < 0.8V, GATE < V_{GATEL}, SENSE < V_{CB}, SS < 20 • V_{OS}, and TIMER < V_{TMRL}. When

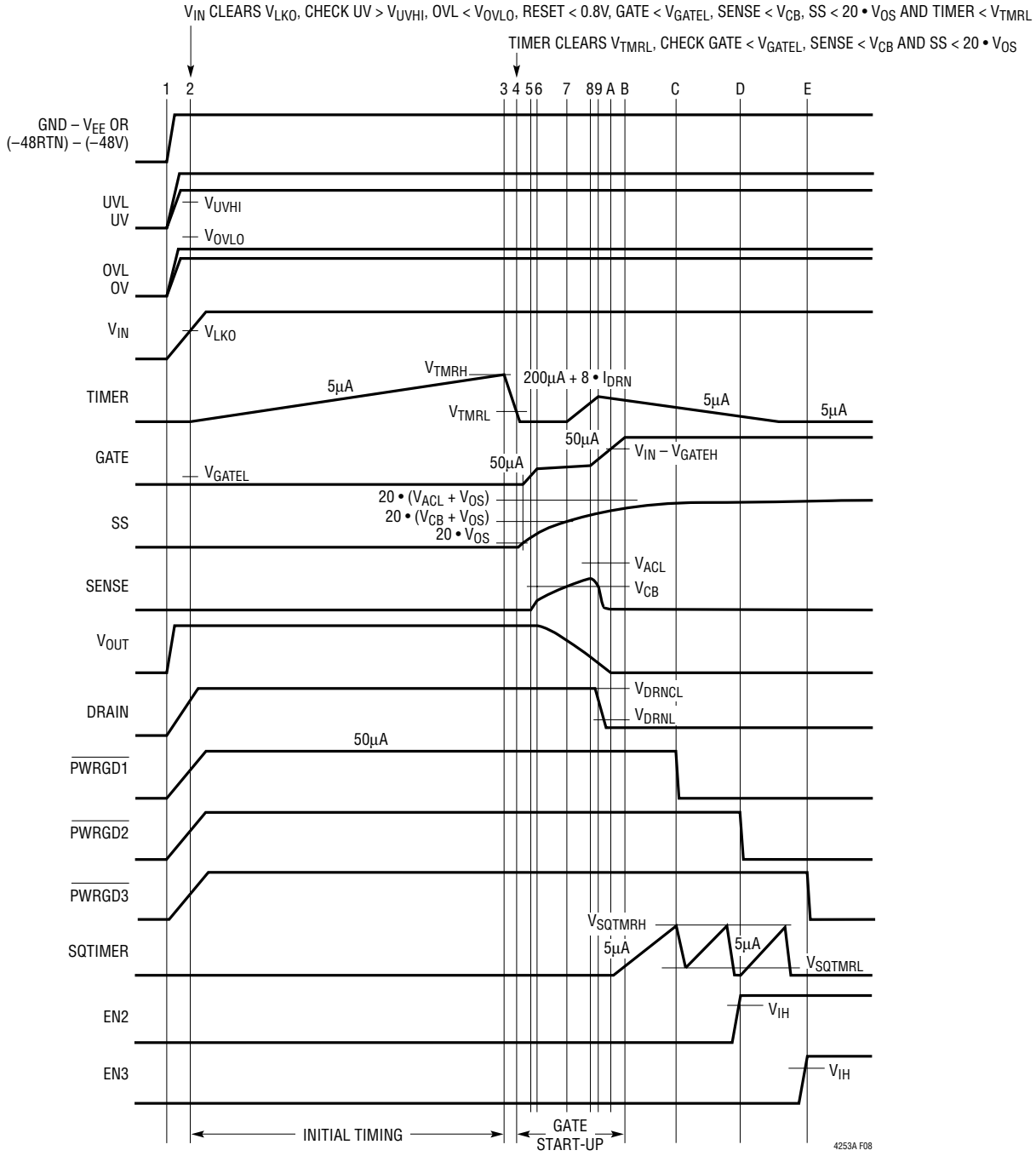


Figure 8. System Power-Up Timing (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

all conditions are met, initial timing starts and the TIMER capacitor is charged by a 5μA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL}, SENSE < V_{CB} and SS < 20 • V_{OS} must be satisfied before the GATE start-up cycle begins. SS ramps up as dictated by R_{SS} • C_{SS} (as in Equation 8); GATE is held low by the analog current limit (ACL) amplifier until SS crosses 20 • V_{OS}. Upon releasing GATE, 50μA sources into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current flows into the load capacitor at time point 5. At time point 6, load current reaches SS control level and the analog current limit loop activates. Between time points 6 and 8, the GATE voltage is servoed, the SENSE voltage is regulated at $V_{ACL}(t)$ (Equation 7) and soft-start limits the slew rate of the load current. If the SENSE voltage ($V_{SENSE} – V_{EE}$) reaches the V_{CB} threshold at time point 7, circuit breaker TIMER activates. The TIMER capacitor, C_T is charged by a (200μA + 8 • I_{DRN}) current pull-up. As the load capacitor nears full charge, load current begins to decline. At time point 8, the load current falls and the SENSE voltage drops below $V_{ACL}(t)$. The analog current limit loop shuts off and the GATE pin ramps further. At time point 9, the SENSE voltage drops below V_{CB}, the fault TIMER ends, followed by a 5μA discharge cycle (cool-off). The duration between time points 7 and 9 must be shorter than one circuit breaker delay to avoid fault time-out during GATE ramp-up. At time point B, GATE reaches its maximum voltage as determined by V_{IN}. At time point A, GATE ramps past V_{GATEH} and SQTIMER starts its ramp-up to 4V. $\overline{PWRGD1}$ pulls low at time point C after one t_{SQT} from time point A, setting off the second SQTIMER ramp up. Having satisfied the requirement that $\overline{PWRGD1}$ is low for more than one t_{SQT}, $\overline{PWRGD2}$ pulls low after EN2 pulls high above the V_{IH} threshold at time point D. This sets off the third SQTIMER ramp-up. Having satisfied the requirement that $\overline{PWRGD2}$ is low for more than one t_{SQT}, $\overline{PWRGD3}$ pulls low after EN3 pulls high at time point E.

Live Insertion with Short Pin Control of UV/OV

In the example shown in Figure 9, power is delivered through long connector pins whereas the UV/OV divider makes contact through a short pin. This ensures the power connections are firmly established before the LTC4253A-ADJ is activated. At time point 1, the power pins make contact and V_{IN} ramps through V_{LKO}. At time point 2, the UV/OV divider makes contact and UV > V_{UVHI}. In addition, the internal logic checks for OV < V_{OVHI}, RESET < 0.8V, GATE < V_{GATEL}, SENSE < V_{CB}, SS < 20 • V_{OS} and TIMER < V_{TMRL}. When all conditions are met, initial timing starts and the TIMER capacitor is charged by a 5μA current source pull-up. At time point 3, TIMER reaches the V_{TMRH} threshold and the initial timing cycle terminates. The TIMER capacitor is quickly discharged. At time point 4, the V_{TMRL} threshold is reached and the conditions of GATE < V_{GATEL}, SENSE < V_{CB} and SS < 20 • V_{OS} must be satisfied before the GATE start-up cycle begins. SS ramps up as dictated by R_{SS} • C_{SS}; GATE is held low by the analog current limit amplifier until SS crosses 20 • V_{OS}. Upon releasing GATE, 50μA sources into the external MOSFET gate and compensation network. When the GATE voltage reaches the MOSFET's threshold, current begins flowing into the load capacitor at time point 5. At time point 6, load current reaches SS control level and the analog current limit loop activates. Between time points 6 and 8, the GATE voltage is servoed and the SENSE voltage is regulated at $V_{ACL}(t)$ and soft-start limits the slew rate of the load current. If the SENSE voltage ($V_{SENSE} – V_{EE}$) reaches the V_{CB} threshold at time point 7, the circuit breaker TIMER activates. The TIMER capacitor, C_T is charged by a (200μA + 8 • I_{DRN}) current pull-up. As the load capacitor nears full charge, load current begins to decline. At point 8, the load current falls and the SENSE voltage drops below $V_{ACL}(t)$. The analog current limit loop shuts off and the GATE pin ramps further. At time point 9, the SENSE voltage drops below V_{CB} and the fault TIMER ends, followed by a 5μA discharge current source (cool-off). When GATE ramps past V_{GATEH} threshold at time point A, SQTIMER starts its ramp-up. $\overline{PWRGD1}$ pulls low at time point C after one t_{SQT} from time

APPLICATIONS INFORMATION

point A, setting off the second SQTIMER ramp-up. $\overline{PWRGD2}$ pulls low at time point D when EN2 is high and $\overline{PWRGD1}$ is low for more than one t_{SQT}. $\overline{PWRGD3}$ pulls low at time point E when EN2 and EN3 is high and $\overline{PWRGD2}$ is low for more than one t_{SQT}. At time point B, GATE reaches its maximum voltage as determined by V_{IN}.

Undervoltage Timing

In Figure 10 when the UVL pin drops below V_{UVLO} (time point 1), the LTC4253A-ADJ shuts down with TIMER, SS and GATE pulled low. If current has been flowing, the SENSE pin voltage decreases to zero as GATE collapses. When UV recovers and clears V_{UVHI} (time point 2), an initial time cycle begins followed by a start-up cycle.

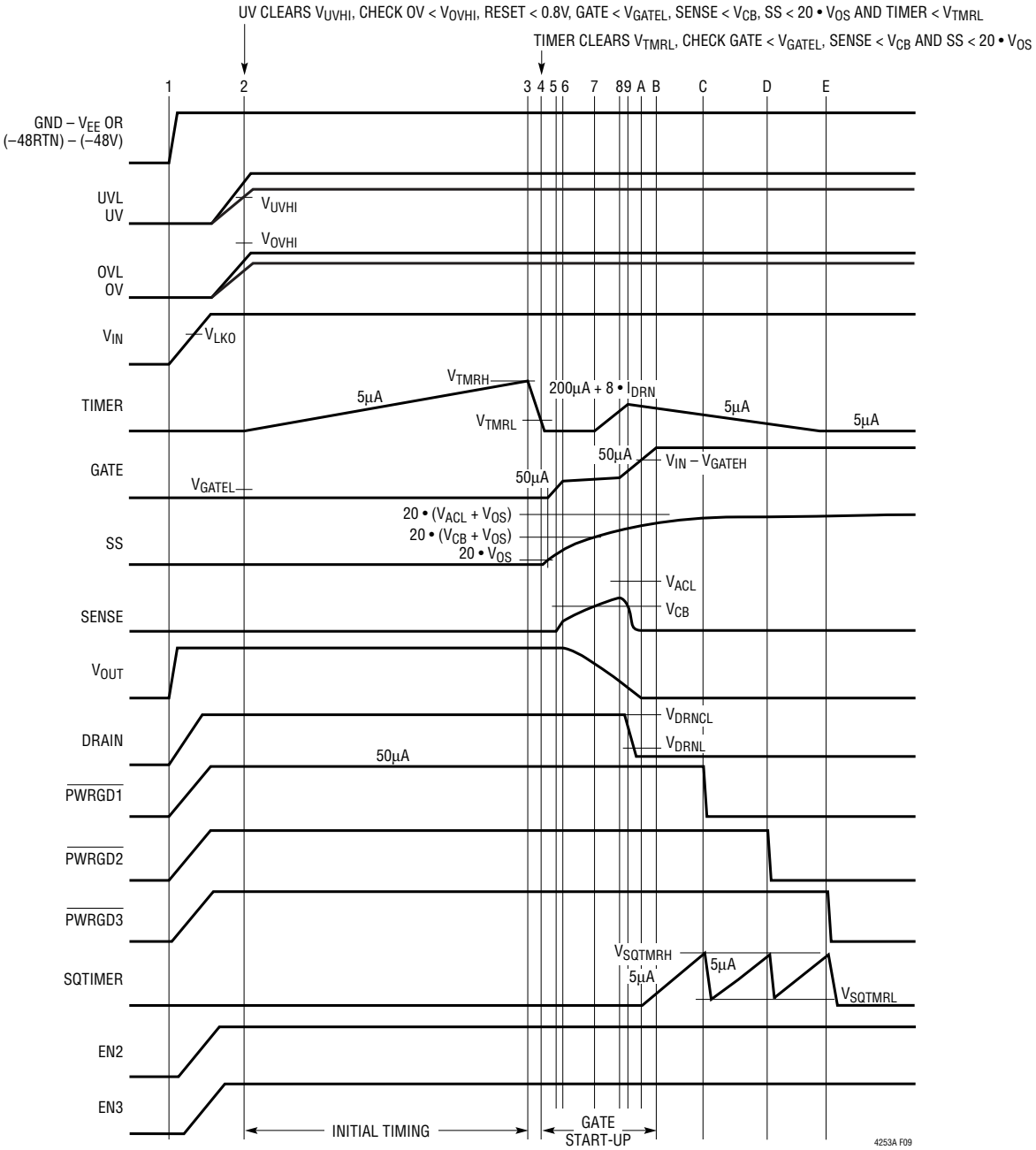


Figure 9. Power-Up Timing with a Short Pin (All Waveforms are Referenced to V_{EE})

APPLICATIONS INFORMATION

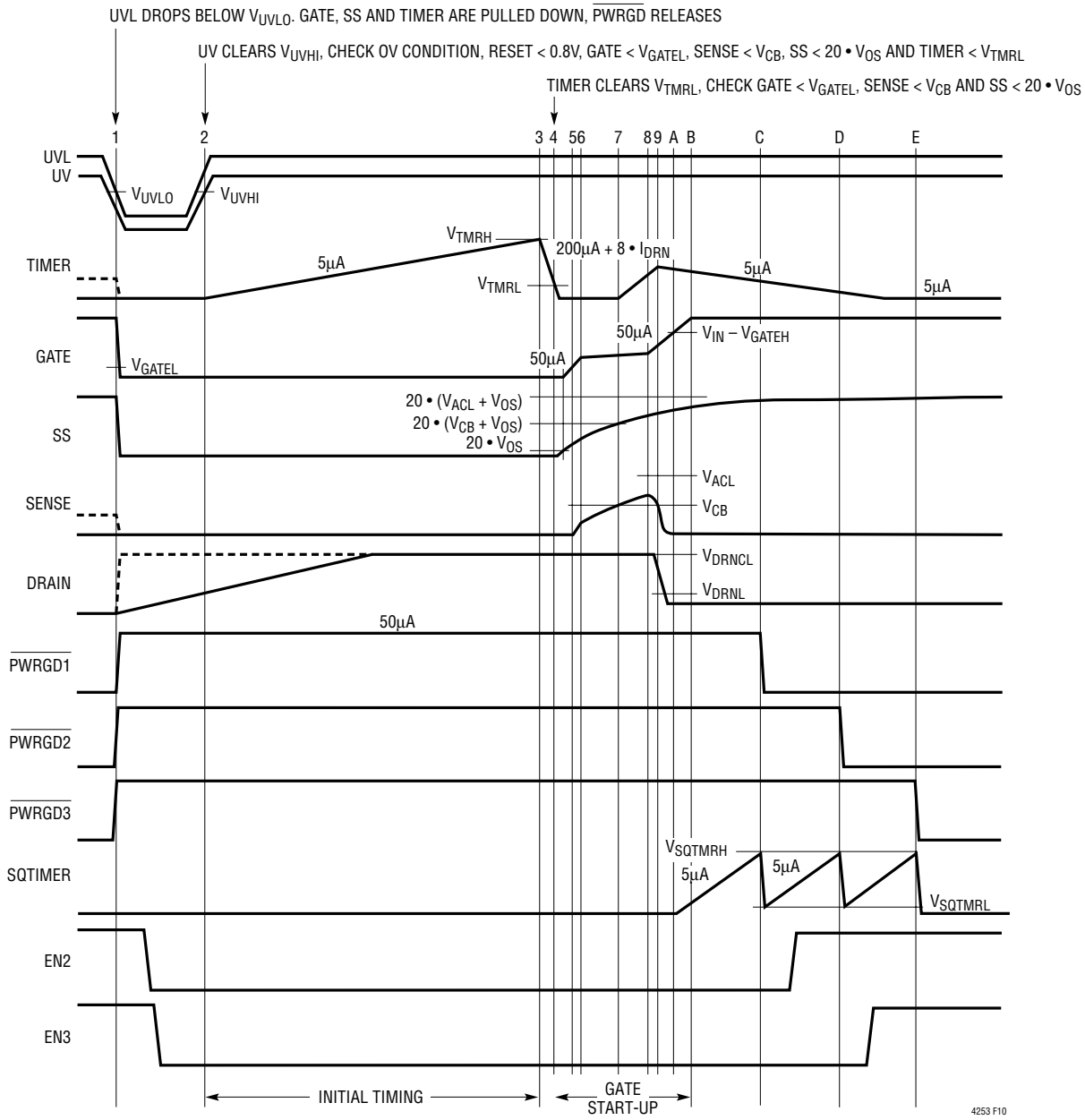


Figure 10. Undervoltage Timing (All Waveforms are Referenced to V_{EE})

V_{IN} Undervoltage Lockout Timing

V_{IN} undervoltage lockout comparator, UVLO has a similar timing behavior as the UV pin timing except it looks at $V_{IN} < (V_{LKO} – V_{LKH})$ to shut down and $V_{IN} > V_{LKO}$ to start. In an undervoltage lockout condition, both UV and OV comparators are held off. When V_{IN} exits undervotlage lockout, the UV and OV comparators are enabled.

Overvoltage Timing

During normal operation, if the OV pin exceeds V_{OVHI} as shown at time point 1 of Figure 11, the TIMER and $\overline{PWRGD}$ status are unaffected; SS and GATE pull down; load disconnects. At time point 2, OVL recovers and drops below the V_{OVLO} threshold; GATE start-up begins. If the overvoltage glitch is long enough to deplete the load capacitor, time points 4 through 7 may occur.

APPLICATIONS INFORMATION

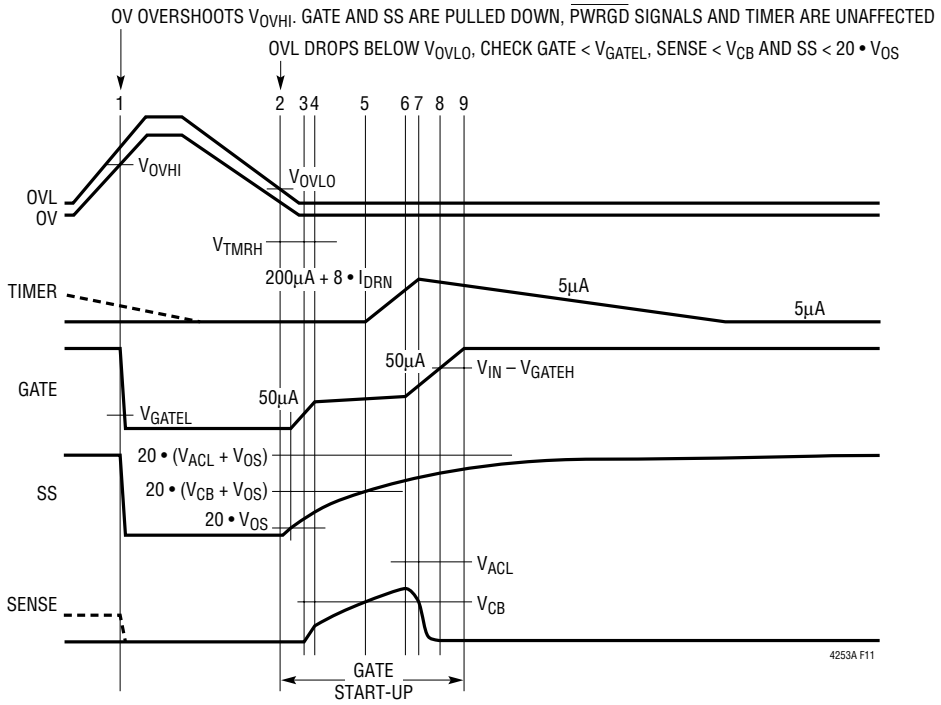


Figure 11. Overvoltage Timing (All Waveforms are Referenced to V_{EE})

Circuit Breaker Timing

In Figure 12a, the TIMER capacitor charges at 200µA if the SENSE pin exceeds V_{CB} but V_{DRN} is less than 5V. If the SENSE pin returns below V_{CB} before TIMER reaches the V_{TMRH} threshold, TIMER is discharged by 5µA. In Figure 12b, when TIMER exceeds V_{TMRH}, GATE pulls down immediately and the chip shuts down. In Figure 12c, multiple momentary faults cause the TIMER capacitor to integrate and reach V_{TMRH} followed by GATE pull down and the chip shuts down. During chip shutdown, LTC4253A-ADJ latches TIMER high with a 5µA pull-up current source.

Resetting a Fault Latch

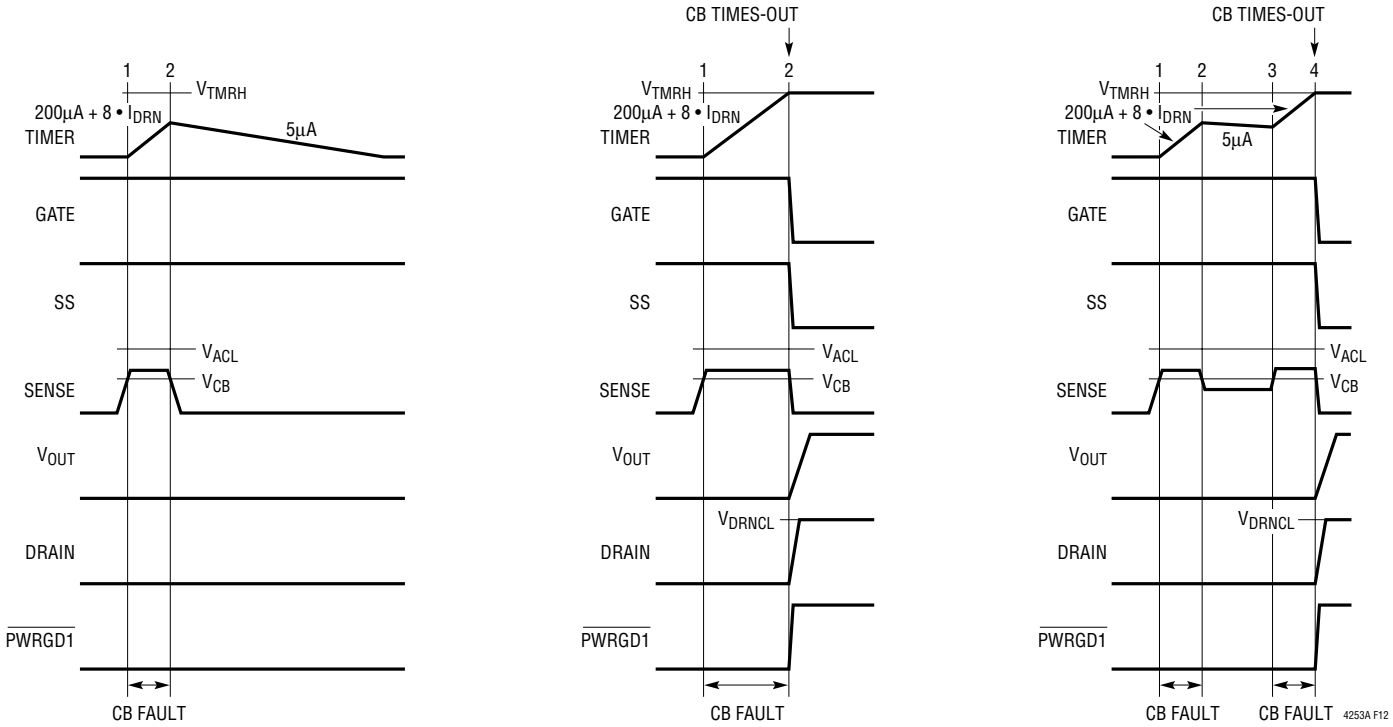
A latched circuit breaker fault of the LTC4253A-ADJ has the benefit of a long cooling time. The latched fault can be reset by pulsing the RESET pin high for >20µs to overcome the internal glitch filter as shown in Figure 13b. After the RESET pulse, SS and GATE ramp up without an initial timing cycle provided the interlock conditions are satisfied.

Alternative methods of reset include using an external switch to pulse the UVL/UV pin below V_{UVLO} or the V_{IN} pin below ($V_{LKO} – V_{LKH}$). Pulling the TIMER pin below V_{TMRL} and the SS pin to 0V then simultaneously releasing them also achieves a reset. An initial timing cycle is generated for reset by pulsing the UVL/UV pin or V_{IN} pin, while no initial timing cycle is generated for reset by pulsing of the TIMER and SS pins.

Using Reset as an ON/OFF Switch

The asynchronous RESET pin can be used as an on/off function to cut off supply to the external power modules or loads controlled by the chip. Pulling RESET high will pull GATE, SS, TIMER and SQTIMER low and the $\overline{PWRGD}$ signal high. The supply is fully cut off if the RESET pulse is maintained wide enough to overcome the internal 20µs glitch filter. As long as RESET is high, GATE, SS, TIMER and SQTIMER are strapped to V_{EE} and the supply is cut off. When RESET is released, the chip waits for the interlock conditions before recovering as described in the Operation, Interlock Conditions section and Figure 13c.

APPLICATIONS INFORMATION



(12a) Momentary Circuit Breaker Fault **(12b) Circuit Breaker Time-Out** **(12c) Multiple Circuit Breaker Fault**

Figure 12. Circuit Breaker Timing Behavior (All Waveforms are Referenced to V_{EE})

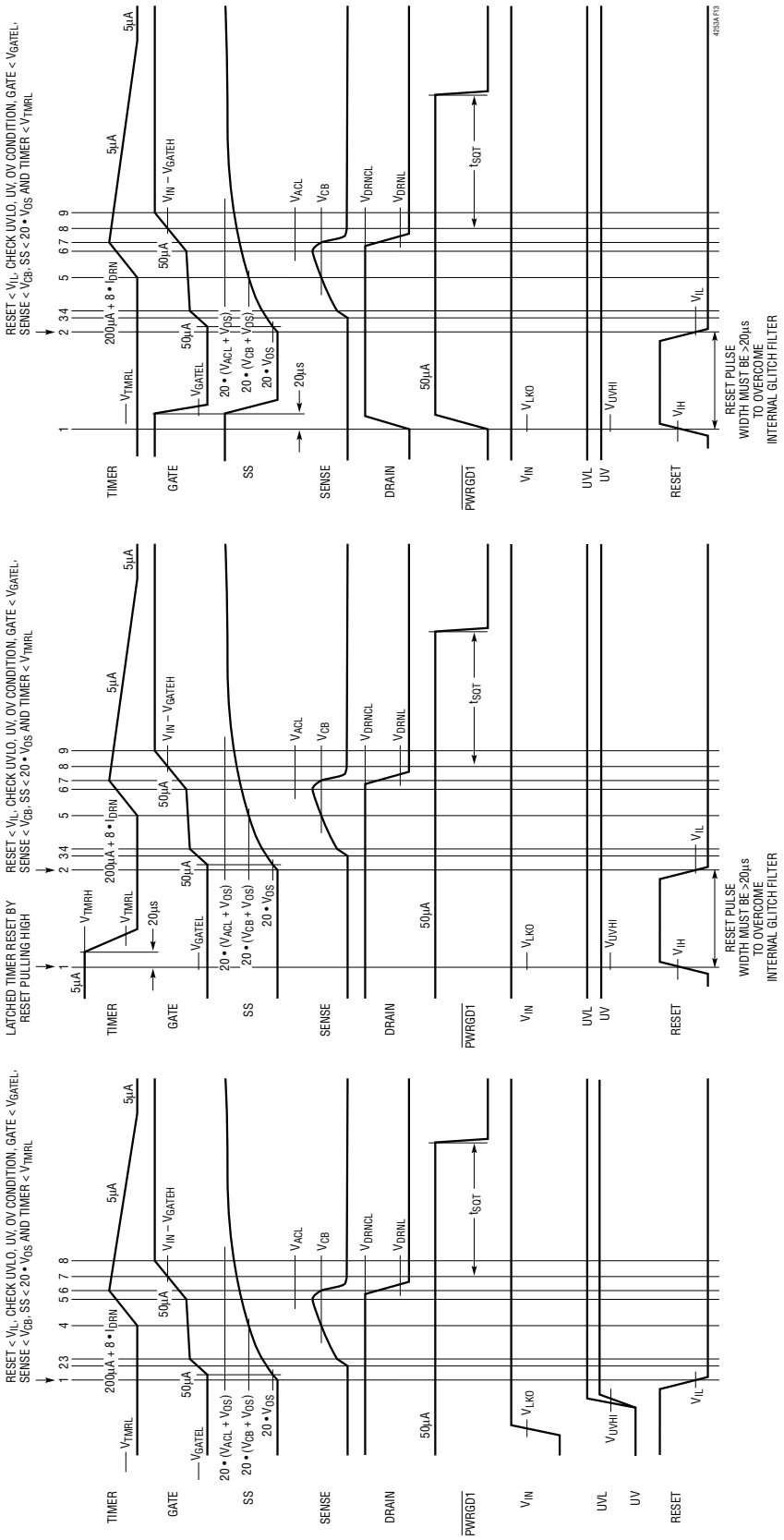
Analog Current Limit and Fast Current Limit

In Figure 14a, when SENSE exceeds V_{ACL}, GATE is regulated by the analog current limit amplifier loop. When SENSE drops below V_{ACL}, GATE is allowed to pull up. In Figure 14b, when a severe fault occurs, SENSE exceeds V_{FCL} and GATE immediately pulls down until the analog current amplifier establishes control. If the severe fault causes V_{OUT} to exceed V_{DRNCL}, the DRAIN pin is clamped at V_{DRNCL}. I_{DRN} flows into the DRAIN pin and is multiplied by 8. This extra current is added to the TIMER pull-up current of 200µA. This accelerated TIMER current of (200µA + 8 • I_{DRN}) produces a shorter circuit breaker fault delay. Careful selection of C_T, R_D and MOSFET helps prevent SOA damage in a low impedance fault condition.

Soft-Start

If SEL is floated high and the SS pin is not connected, this pin defaults to a linear voltage ramp, from 0V to 1.4V in about 200µs at GATE start-up, as shown in Figure 15a. If a soft-start capacitor, C_{SS}, is connected to this SS pin, the soft-start response is modified from a linear ramp to an RC response (Equation 8), as shown in Figure 15b. This feature allows load current to slowly ramp-up at GATE start-up. Soft-start is initiated at time point 3 by a TIMER transition from V_{TMRH} to V_{TMRL} (time points 1 and 2), by the OVL pin falling below the V_{OVLO} threshold after an OV condition, or by the RESET pin falling < 0.8V after a Reset condition. When the SS pin is below 0.2V, the analog current limit amplifier keeps GATE low. Above 0.2V, GATE is released and 50µA ramps up the compensation network and GATE capacitance at time point 4. Meanwhile, the SS pin voltage continues to ramp up. When GATE reaches the MOSFET's threshold, the MOSFET begins to conduct. Due to the MOSFET's high g_m, the MOSFET current quickly reaches the soft-start control value of $V_{ACL}(t)$ (Equation 7). At time point 6, the GATE voltage is controlled by the current limit amplifier. The soft-start control voltage reaches the circuit breaker voltage, V_{CB} at time point 7 and the circuit breaker TIMER activates. As the load capacitor nears full charge, load current begins

APPLICATIONS INFORMATION



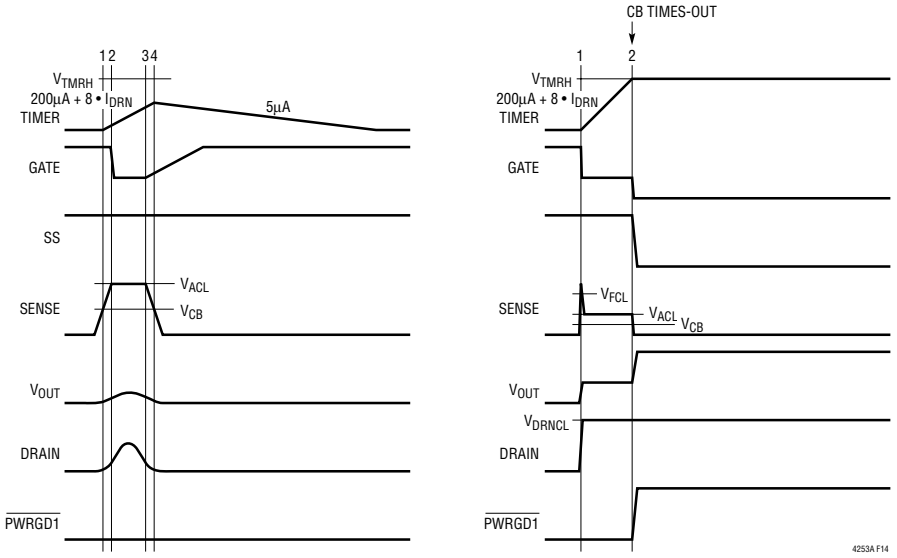
(13a) Reset Forcing Start-Up Without Initial TIMER Cycle

(13b) Reset of LTC4253-ADJ's Latched Fault

(13c) Reset as an ON/OFF Switch

Figure 13. Reset Functions (All Waveforms are Referenced to V_{EE})

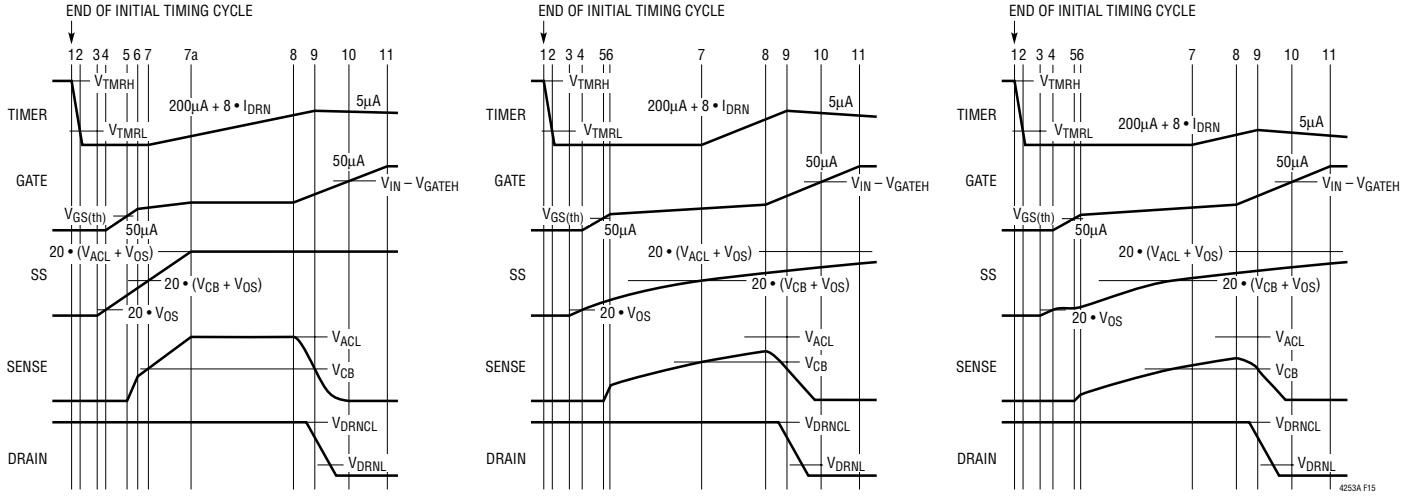
APPLICATIONS INFORMATION



(14a) Analog Current Limit Fault

(14b) Fast Current Limit Fault

Figure 14. Current Limit Behavior (All Waveforms are Referenced to V_{EE})



(15a) Without External C_{SS}

(15b) With External C_{SS}

(15c) With SEL = Low and External C_{SS}

Figure 15. Soft-Start Timing (All Waveforms are Referenced to V_{EE})

to decline below $V_{ACL}(t)$. The current limit loop shuts off and GATE releases at time point 8. At time point 9, SENSE voltage falls below V_{CB} and TIMER deactivates.

A third Soft-Start mode is shown in Figure 15c. The SEL pin is tied low and a soft-start capacitor, C_{SS}, is connected to the SS pin. The behavior is similar to Figure 15b until time point 4 when GATE is released and starts to ramp up. Instead of continuing its ramp-up as in mode two, the SS pin voltage is servoed at a voltage that is just above 0.2V (20 • V_{OS}) to keep the current limit amplifier off and the GATE ramping up freely. At time point 5, GATE ramps past the external MOSFET's threshold and inrush current starts to flow. At time point 6, V_{SENSE} goes above V_{ACL} (t) and the servo on SS is released while the GATE voltage is controlled by the current limit amplifier with V_{ACL} (t) ramping up from near zero. The result is a current profile (as

APPLICATIONS INFORMATION

reflected in V_{SENSE}) that ramps up smoothly from near zero. V_{SENSE} does not show a large kink as in Figure 15b when V_{ACL} (t) already has a substantial offset from zero at time point 6. SEL tied low chooses this SS servo mode during soft-start while SEL set high allows the SS pin to do an open-loop ramp-up as in Figures 15a and 15b. The stability of the SS servo loop requires a C_{SS} > 5nF.

Large values of C_{SS} can cause premature circuit breaker time-out as V_{ACL}(t) may marginally exceed the V_{CB} potential during the circuit breaker delay. The load capacitor is unable to achieve full charge in one GATE start-up cycle. A more serious side effect of a large C_{SS} value is that SOA duration may be exceeded during soft-start into a low impedance load. A soft-start voltage below V_{CB} will not activate the circuit breaker TIMER.

Power Limit Circuit Breaker

Figure 16 shows the LTC4253A-ADJ in a power limit circuit breaking application. The SENSE pin is modulated by board voltage V_{SUPPLY}. The zener voltage, V_Z of D1, is set to be the same as the lowest operating voltage, $V_{SUPPLY(MIN)}$ = 43V. If the goal is to have the high supply operating voltage, $V_{SUPPLY(MAX)}$ = 71V give the same power as available at $V_{SUPPLY(MIN)}$, then resistors R4 and R5 are selected by:

$$\frac{R5}{R4} = \frac{V_{CB}}{V_{SUPPLY(MAX)}} \tag{17}$$

If R5 is 22Ω, then R4 is 31.6k. The peak circuit breaker power limit is:

$$POWER(MAX) = \frac{\left(V_{SUPPLY(MIN)} + V_{SUPPLY(MAX)}\right)^2}{4 \bullet V_{SUPPLY(MIN)} \bullet V_{SUPPLY(MAX)}} \tag{18}$$

$$\bullet POWER\ AT\ V_{SUPPLY(MIN)}$$

$$= 1.064 \bullet POWER\ AT\ V_{SUPPLY(MIN)}$$

when $V_{SUPPLY} = 0.5 \bullet (V_{SUPPLY(MIN)} + V_{SUPPLY(MAX)})$
$= 57V$

The peak power at the fault current limit occurs at the supply overvoltage threshold. The fault current limited power is:

$$POWER(FAULT) = \frac{(V_{SUPPLY})}{R_S} \bullet \left[V_{ACL} - (V_{SUPPLY} - V_Z) \bullet \frac{R5}{R4}\right] \tag{19}$$

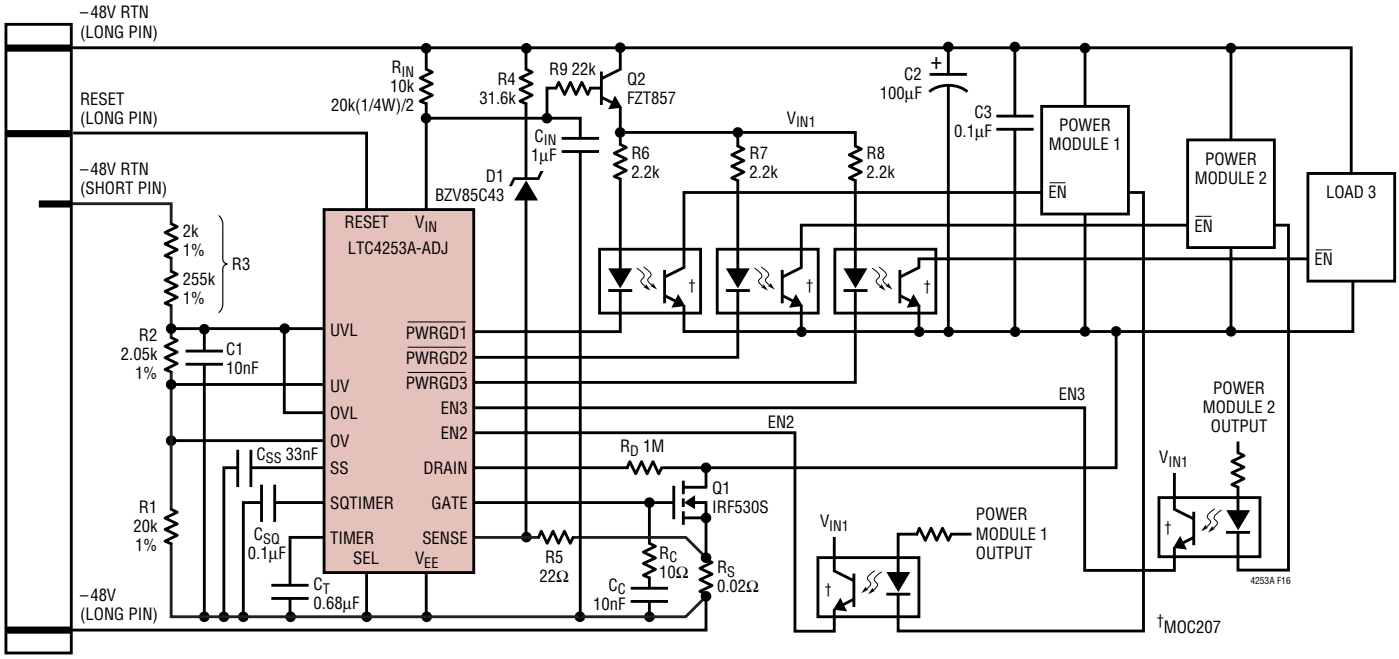
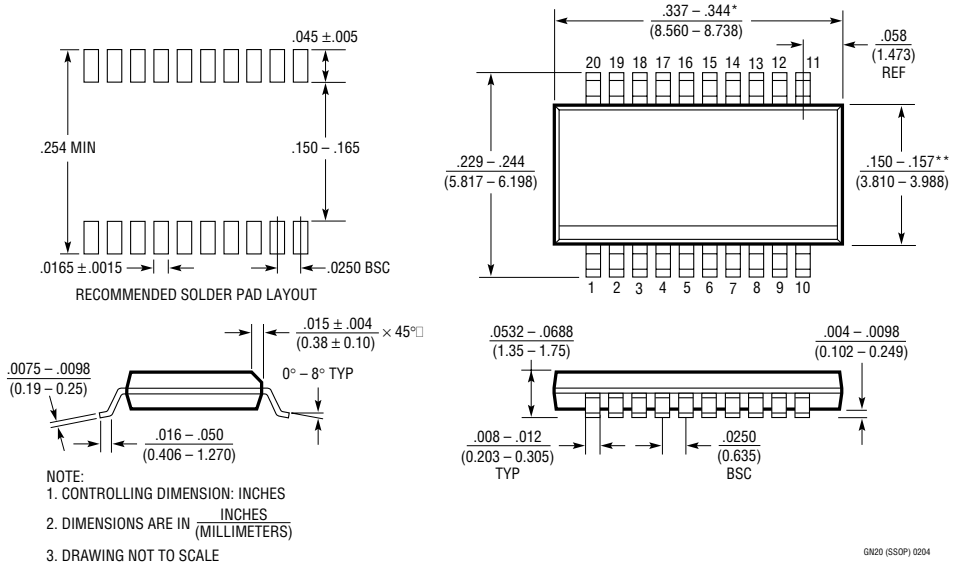


Figure 16. Power Limit Circuit Breaker Application

4253a-adjf

PACKAGE DESCRIPTION

GN Package
20-Lead Plastic SSOP (Narrow .150 Inch)
(Reference LTC DWG # 05-08-1641)

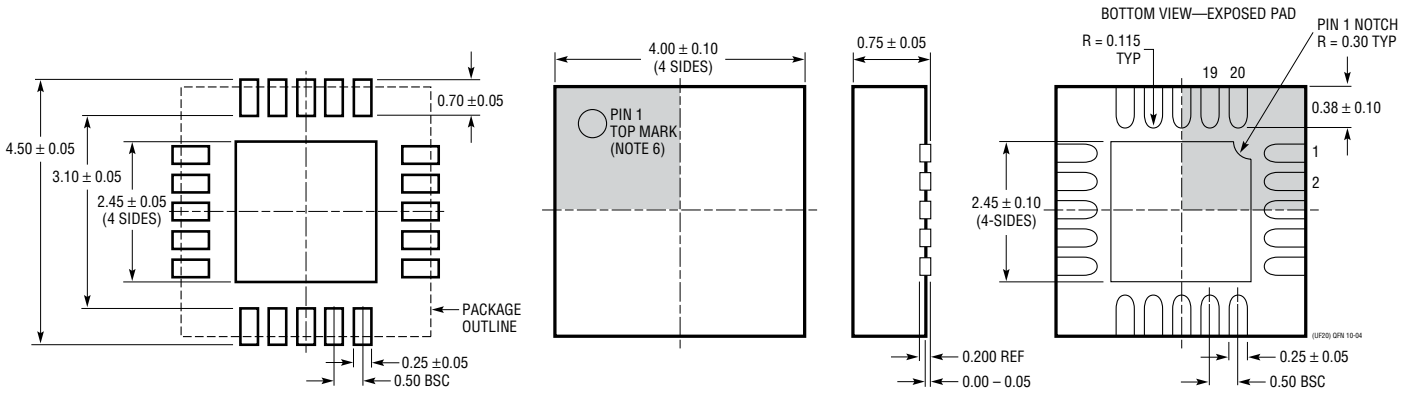


NOTE:
1. CONTROLLING DIMENSION: INCHES
2. DIMENSIONS ARE IN $\frac{\text{INCHES}}{\text{(MILLIMETERS)}}$
3. DRAWING NOT TO SCALE

*DIMENSION DOES NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.006" (0.152mm) PER SIDE

**DIMENSION DOES NOT INCLUDE INTERLEAD FLASH. INTERLEAD FLASH SHALL NOT EXCEED 0.010" (0.254mm) PER SIDE

UF Package
20-Lead Plastic QFN (4mm × 4mm)
(Reference LTC DWG # 05-08-1710)



RECOMMENDED SOLDER PAD PITCH AND DIMENSIONS

NOTE:
1. DRAWING IS PROPOSED TO BE MADE A JEDEC PACKAGE OUTLINE MO-220 VARIATION (WGGD-1)—TO BE APPROVED
2. DRAWING NOT TO SCALE
3. ALL DIMENSIONS ARE IN MILLIMETERS
4. DIMENSIONS OF EXPOSED PAD ON BOTTOM OF PACKAGE DO NOT INCLUDE MOLD FLASH. MOLD FLASH, IF PRESENT, SHALL NOT EXCEED 0.15mm ON ANY SIDE
5. EXPOSED PAD SHALL BE SOLDER PLATED
6. SHADED AREA IS ONLY A REFERENCE FOR PIN 1 LOCATION ON THE TOP AND BOTTOM OF PACKAGE

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

APPLICATIONS INFORMATION

Circuit Breaker with Foldback Current Limit

Figure 17 shows the LTC4253A-ADJ in a foldback current limit application. When V_{OUT} is shorted to the –48V RTN supply, current flows through resistors R4 and R5. This results in a voltage drop across R5 and a corresponding reduction in voltage drop across the sense resistor, R_S, as the ACL amplifier servos the sense voltage between the SENSE and V_{EE} pins to about 60mV. The short-circuit current through R_S reduces as the V_{OUT} voltage increases during an output short-circuit condition. Without foldback current limiting resistor R5, the current is limited to 3A during analog current limit. With R5, the short-circuit current is limited to 0.5A when V_{OUT} is shorted to 71V.

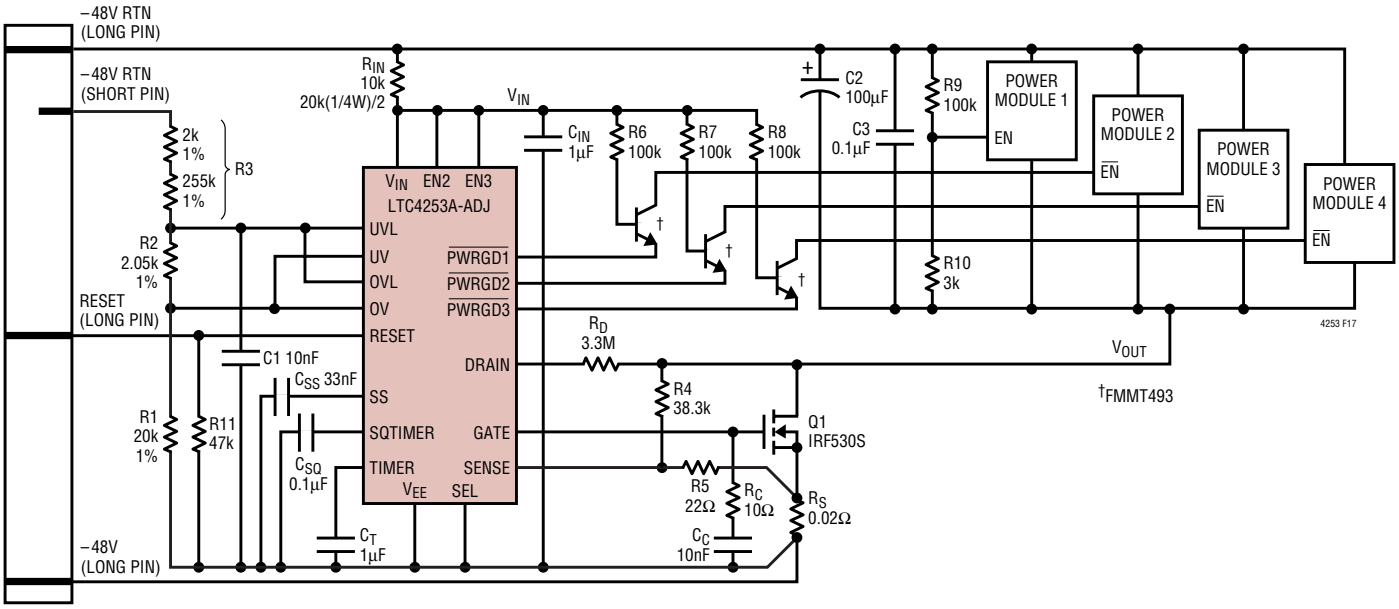


Figure 17. –48V/2.5A Application with Foldback Current Limiting and Transistor Enabled Sequencing Without Feedback

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT1640AH/LT1640AL	Negative High Voltage Hot Swap Controllers in SO-8	Negative High Voltage Supplies from -10V to -80V
LT1641-1/LT1641-2	Positive High Voltage Hot Swap Controllers in SO-8	Supplies from 9V to 80V, Autoretry/Latched Off
LTC1642	Fault Protected Hot Swap Controller	3V to 16.5V, Overvoltage Protection up to 33V
LT4250	–48V Hot Swap Controller	Active Current Limiting, Supplies from –20V to –80V
LTC4251/LTC4251-1 LTC4251-2	–48V Hot Swap Controllers in SOT-23	Fast Active Current Limiting, Supplies from –15V
LTC4252-1/LTC4252-2 LTC4252A-1/LTC4252A-2	–48V Hot Swap Controllers in MS8/MS10	Fast Active Current Limiting, Supplies from –15V, Drain Accelerated Response, 1% Accurate UV/OV Thresholds
LTC4260	Positive Voltage Hot Swap Controller with I^2C Compatible Monitoring	Onboard ADC for Current and Voltage Monitoring, 8.5V to 80V Operation

Linear Technology Corporation
1630 McCarthy Blvd., Milpitas, CA 95035-7417
(408) 432-1900 • FAX: (408) 434-0507 • www.linear.com
LT/TP 0805 500 • PRINTED IN USA
© LINEAR TECHNOLOGY CORPORATION 2005