PCF8532

Universal LCD driver for low multiplex rates

Rev. 2 — 10 February 2011 **Product data sheet**

1. General description

The PCF8532 is a peripheral device which interfaces to almost any Liquid Crystal Display (LCD)[1] with low multiplex rates. It generates the drive signals for any static or multiplexed LCD containing up to four backplanes and up to 160 segments and can easily be cascaded for larger LCD applications. The PCF8532 is compatible with most microprocessors or microcontrollers and communicates via a two-line bidirectional I^2C-bus. Communication overheads are minimized by a display RAM with auto-incremental addressing, by hardware subaddressing and by display memory switching (static and duplex drive modes).

2. Features and benefits

- Single-chip LCD controller and driver for up to 640 elements
- Selectable backplane drive configuration: static or 2, 3 or 4 backplane multiplexing
- 160 segment drives:
  - ◆ Up to 80 7-segment numeric characters
  - ◆ Up to 42 14-segment alphanumeric characters
  - ◆ Any graphics of up to 640 elements
- May be cascaded for large LCD applications (up to 2560 elements possible)
- 160×4-bit RAM for display data storage
- Software programmable frame frequency in steps of 5 Hz in the range of 60 Hz to 90 Hz
- Wide LCD supply range: from 1.8 V for low threshold LCDs and up to 8.0 V for guest-host LCDs and high threshold (automobile) twisted nematic LCDs
- Internal LCD bias generation with voltage-follower buffers
- Selectable display bias configuration: static, $\frac{1}{2}$ or $\frac{1}{3}$
- Wide power supply range: from 1.8 V to 5.5 V
- LCD and logic supplies may be separated
- Low power consumption, typically: $I_{DD} = 4 \mu A$, $I_{DD(LCD)} = 40 \mu A$
- 400 kHz I^2C-bus interface
- Auto-incremental display data loading across device subaddress boundaries
- Versatile blinking modes
- Compatible with Chip-On-Glass (COG) technology
- Two sets of backplane outputs for optimal COG configurations of the application
- Display memory bank switching in static and duplex drive modes
- No external components required

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1. The definition of the abbreviations and acronyms used in this data sheet can be found in Section 15.

■ Manufactured in silicon gate CMOS process

3. Ordering information

Table 1.   Ordering information

Type number	Package		
	Name	**Description**	**Version**
PCF8532U/2DA/1	**PCF8532U**	bare die; 197 bumps; 6.5 × 1.16 × 0.38 mm[1]	PCF8532U

[1]   Chip with bumps in tray.

4. Marking

Table 2.   Marking codes

Type number	Marking code
PCF8532U/2DA/1	PC8532-1

5. Block diagram

Fig 1.   Block diagram of PCF8532

6. Pinning information

6.1 Pinning

Top view. For mechanical details, see Figure 26.

Fig 2. Pin location of PCF8532
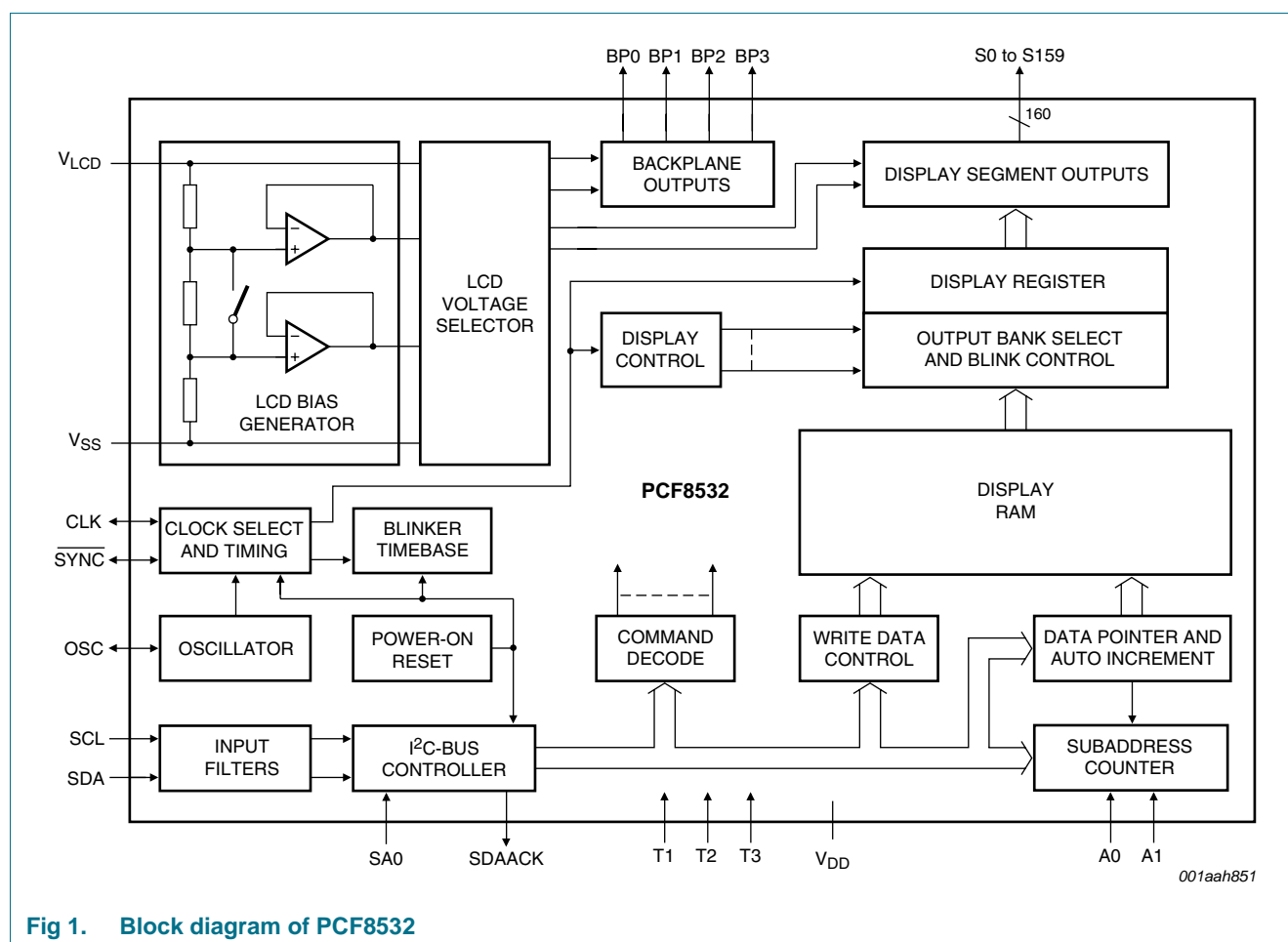
6.2 Pin description

Table 3.   Pin description

Symbol	Pin	Description
SDAACK	1 to 3[1]	I²C-bus acknowledge output
SDA	4 to 6[1]	I²C-bus serial data input
SCL	7 to 9	I²C-bus serial clock input
CLK	10	clock input/output
V_{DD}	11 to 13	supply voltage
$\overline{SYNC}$	14	cascade synchronization input/output
OSC	15	selection of internal or external clock
T1, T2 and T3	16, 17 and 18 to 20	dedicated testing pins; to be tied to V_{SS} in application mode
A0 and A1	21, 22	subaddress inputs
SA0	23	I²C-bus slave address input
V_{SS}	24 to 26[2]	logic ground
V_{LCD}	27 to 29	LCD supply voltage
BP2 and BP0	30, 31	LCD backplane outputs
S0 to S79	32 to 111	LCD segment outputs
BP0, BP2, BP1 and BP3	112 to 115	LCD backplane outputs
S80 to S159	116 to 195	LCD segment outputs
BP3 and BP1	196, 197	LCD backplane outputs

[1]   In most applications SDA and SDAACK can be tied together.

[2]   The substrate (rear side of the die) is wired to V_{SS} but should not be electrically contacted.

7. Functional description

The PCF8532 is a versatile peripheral device designed to interface between any microprocessor or microcontroller to a wide variety of LCD segment or dot matrix displays (see Figure 3). It can directly drive any static or multiplexed LCD containing up to four backplanes and up to 160 segments.

The display configurations possible with the PCF8532 depend on the required number of active backplane outputs. A selection of display configurations is given in Table 4.

All of the display configurations given in Table 4 can be implemented in a typical system as shown in Figure 4.

dot matrix
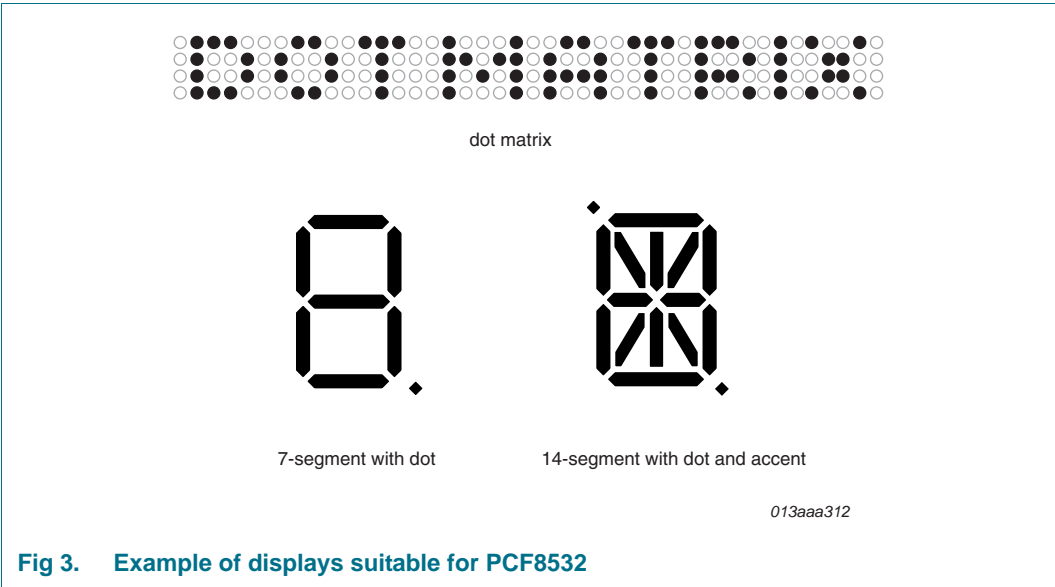
7-segment with dot   14-segment with dot and accent

013aaa312

Fig 3.   Example of displays suitable for PCF8532

Table 4.   Selection of possible display configurations

Number of				
Backplanes	**Icons**	**Digits/Characters**		**Dot matrix/Elements**
		7-segment	**14-segment**	
4	640	80	40	640 dots (4 × 160)
3	480	60	30	480 dots (3 × 160)
2	320	40	20	320 dots (2 × 160)
1	160	20	10	160 dots (1 × 160)
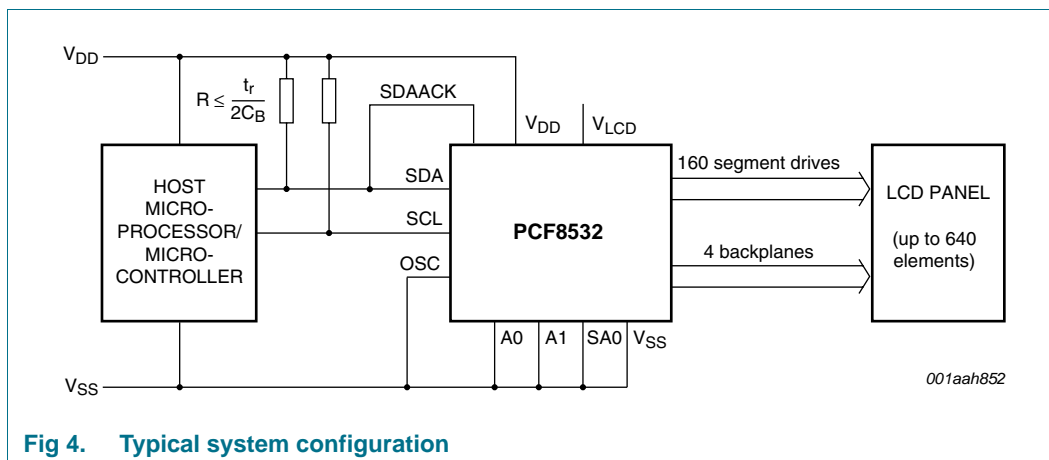
The host microprocessor or microcontroller maintains the 2-line I^2C-bus communication channel with the PCF8532.

Biasing voltages for the multiplexed LCD waveforms are generated internally, removing the need for an external bias generator. The internal oscillator is selected by connecting pin OSC to V_{SS}. The only other connections required to complete the system are the power supplies (V_{DD}, V_{SS} and V_{LCD}) and the LCD panel selected for the application.

7.1 Power-on reset

At power-on the PCF8532 resets to a default starting condition:

- All backplane and segment outputs are set to V_{LCD}
- The selected drive mode is 1:4 multiplex with $\frac{1}{3}$ bias
- Blinking is switched off
- Input and output bank selectors are reset
- The I^2C-bus interface is initialized
- The data pointer and the subaddress counter are cleared (set to logic 0)
- The display is disabled
- If internal oscillator is selected (OSC pin connected to V_{SS}), then there is no clock signal on pin CLK

Remark: Do not transfer data on the I^2C-bus for at least 1 ms after a power-on to allow the reset action to complete.

7.2 LCD bias generator

Fractional LCD biasing voltages are obtained from an internal voltage divider of three series resistors connected between V_{LCD} and V_{SS}. The center resistor can be switched out of the circuit to provide a $\frac{1}{2}$ bias voltage level for the 1:2 multiplex configuration.

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7.3 LCD voltage selector

The LCD voltage selector coordinates the multiplexing of the LCD in accordance with the selected LCD drive configuration. The operation of the voltage selector is controlled by the mode-set command (see Table 9) from the command decoder. The biasing configurations that apply to the preferred modes of operation, together with the biasing characteristics as functions of V_{LCD} and the resulting discrimination ratios (D), are given in Table 5.

Table 5.　Biasing characteristics

LCD drive mode	Number of:		LCD bias configuration	$\dfrac{V_{off(RMS)}}{V_{LCD}}$	$\dfrac{V_{on(RMS)}}{V_{LCD}}$	$D = \dfrac{V_{on(RMS)}}{V_{off(RMS)}}$
	Backplanes	**Levels**				
static	1	2	static	0	1	∞
1:2 multiplex	2	3	$\frac{1}{2}$	0.354	0.791	2.236
1:2 multiplex	2	4	$\frac{1}{3}$	0.333	0.745	2.236
1:3 multiplex	3	4	$\frac{1}{3}$	0.333	0.638	1.915
1:4 multiplex	4	4	$\frac{1}{3}$	0.333	0.577	1.732

A practical value for V_{LCD} is determined by equating $V_{off(RMS)}$ with a defined LCD threshold voltage (V_{th}), typically when the LCD exhibits approximately 10 % contrast. In the static drive mode a suitable choice is $V_{LCD} > 3V_{th}$.

Multiplex drive modes of 1:3 and 1:4 with $\frac{1}{2}$ bias are possible but the discrimination and hence the contrast ratios are smaller.

Bias is calculated by $\dfrac{1}{1+a}$, where the values for a are

a = 1 for $\frac{1}{2}$ bias

a = 2 for $\frac{1}{3}$ bias

The RMS on-state voltage ($V_{on(RMS)}$) for the LCD is calculated with Equation 1

$$V_{on(RMS)} = V_{LCD}\sqrt{\frac{a^2 + 2a + n}{n \times (1+a)^2}} \tag{1}$$

where the values for n are

n = 1 for static mode

n = 2 for 1:2 multiplex

n = 3 for 1:3 multiplex

n = 4 for 1:4 multiplex

The RMS off-state voltage ($V_{off(RMS)}$) for the LCD is calculated with Equation 2:

$$V_{off(RMS)} = V_{LCD}\sqrt{\frac{a^2 - 2a + n}{n \times (1+a)^2}} \tag{2}$$

Discrimination is the ratio of $V_{on(RMS)}$ to $V_{off(RMS)}$ and is determined from Equation 3:

$$D = \frac{V_{on(RMS)}}{V_{off(RMS)}} = \sqrt{\frac{(a+1)^2 + (n-1)}{(a-1)^2 + (n-1)}} \qquad (3)$$

Using Equation 3, the discrimination for an LCD drive mode of 1:3 multiplex with $\frac{1}{2}$ bias is $\sqrt{3} = 1.732$ and the discrimination for an LCD drive mode of 1:4 multiplex with $\frac{1}{2}$ bias is $\frac{\sqrt{21}}{3} = 1.528$.

The advantage of these LCD drive modes is a reduction of the LCD full scale voltage V_{LCD} as follows:

- 1:3 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \sqrt{6} \times V_{off(RMS)} = 2.449 V_{off(RMS)}$

- 1:4 multiplex ($\frac{1}{2}$ bias): $V_{LCD} = \left[\frac{(4 \times \sqrt{3})}{3}\right] = 2.309 V_{off(RMS)}$

These compare with $V_{LCD} = 3 V_{off(RMS)}$ when $\frac{1}{3}$ bias is used.

It should be noted that V_{LCD} is sometimes referred as the LCD operating voltage.

7.3.1 Electro-optical performance

Suitable values for $V_{on(RMS)}$ and $V_{off(RMS)}$ are dependant on the LCD liquid used. The RMS voltage, at which a pixel will be switched on or off, determine the transmissibility of the pixel.

For any given liquid, there are two threshold values defined. One point is at 10 % relative transmission (at V_{low}) and the other at 90% relative transmission (at V_{high}), see Figure 5. For a good contrast performance, the following rules should be followed:

$$V_{on(RMS)} \geq V_{high} \qquad (4)$$

$$V_{off(RMS)} \leq V_{low} \qquad (5)$$

$V_{on(RMS)}$ and $V_{off(RMS)}$ are properties of the display driver and are affected by the selection of a, n (see Equation 1 to Equation 3) and the V_{LCD} voltage.

V_{low} and V_{high} are properties of the LCD liquid and can be provided by the module manufacturer.

It is important to match the module properties to those of the driver in order to achieve optimum performance.
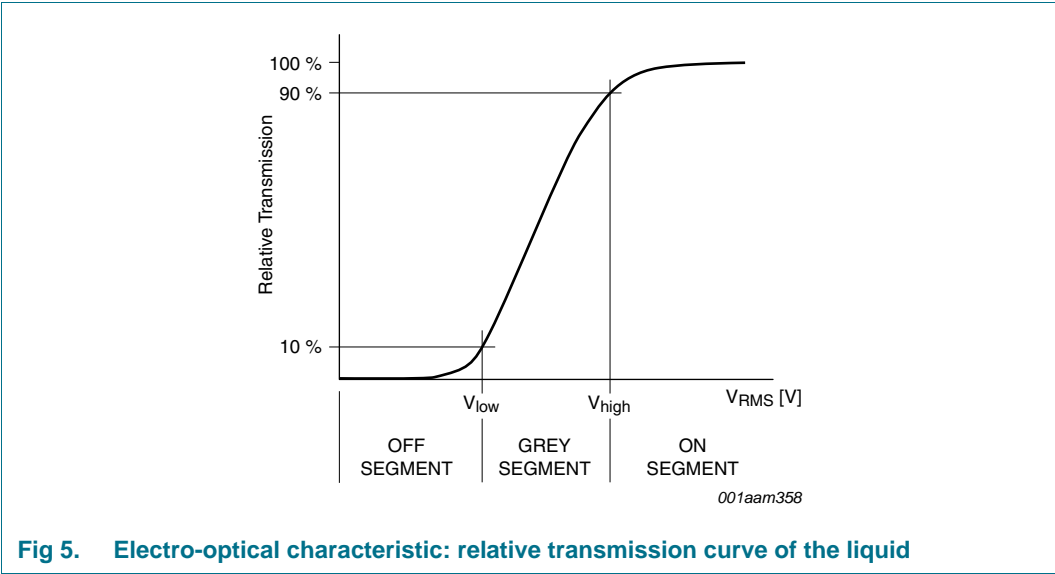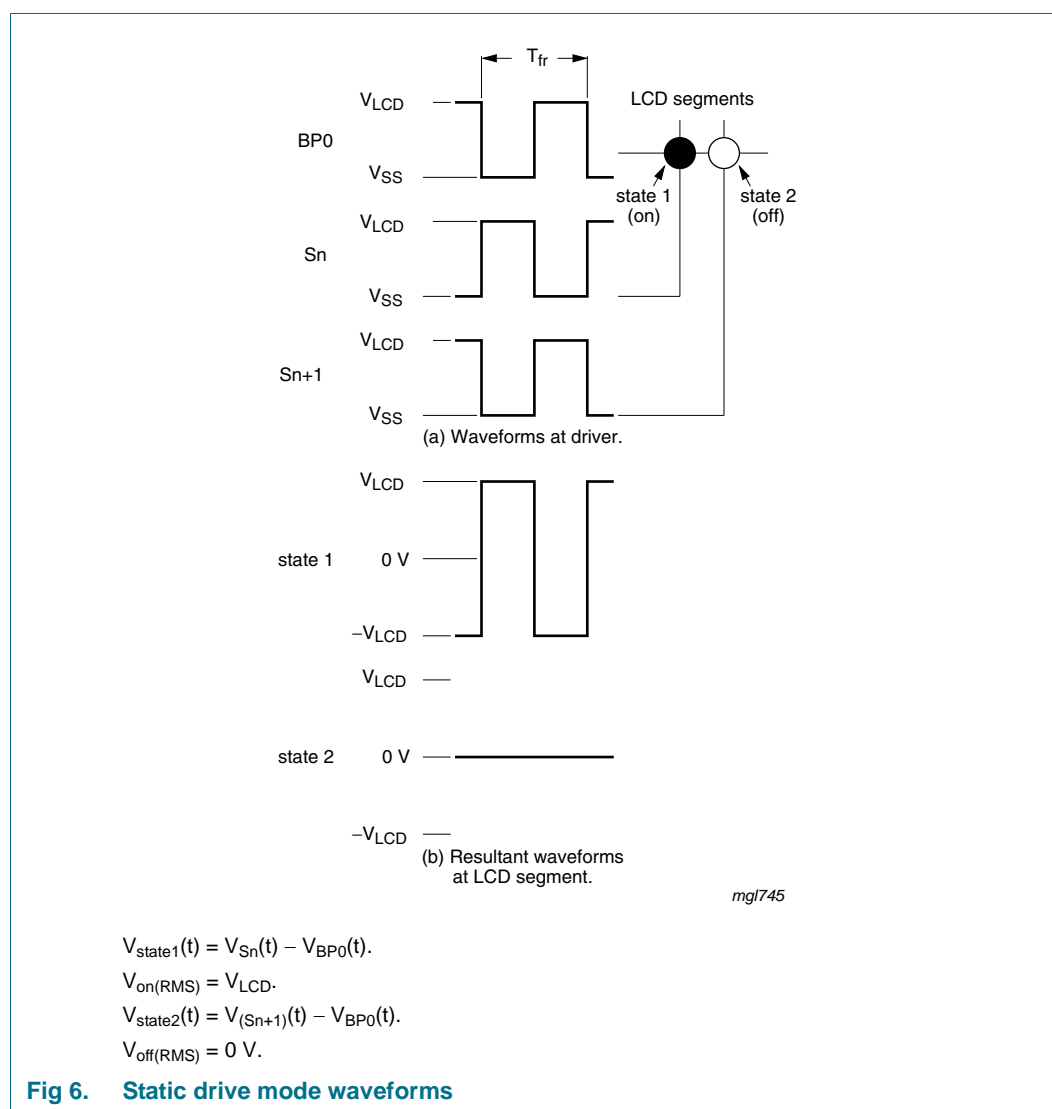
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001aam358

Fig 5. **Electro-optical characteristic: relative transmission curve of the liquid**

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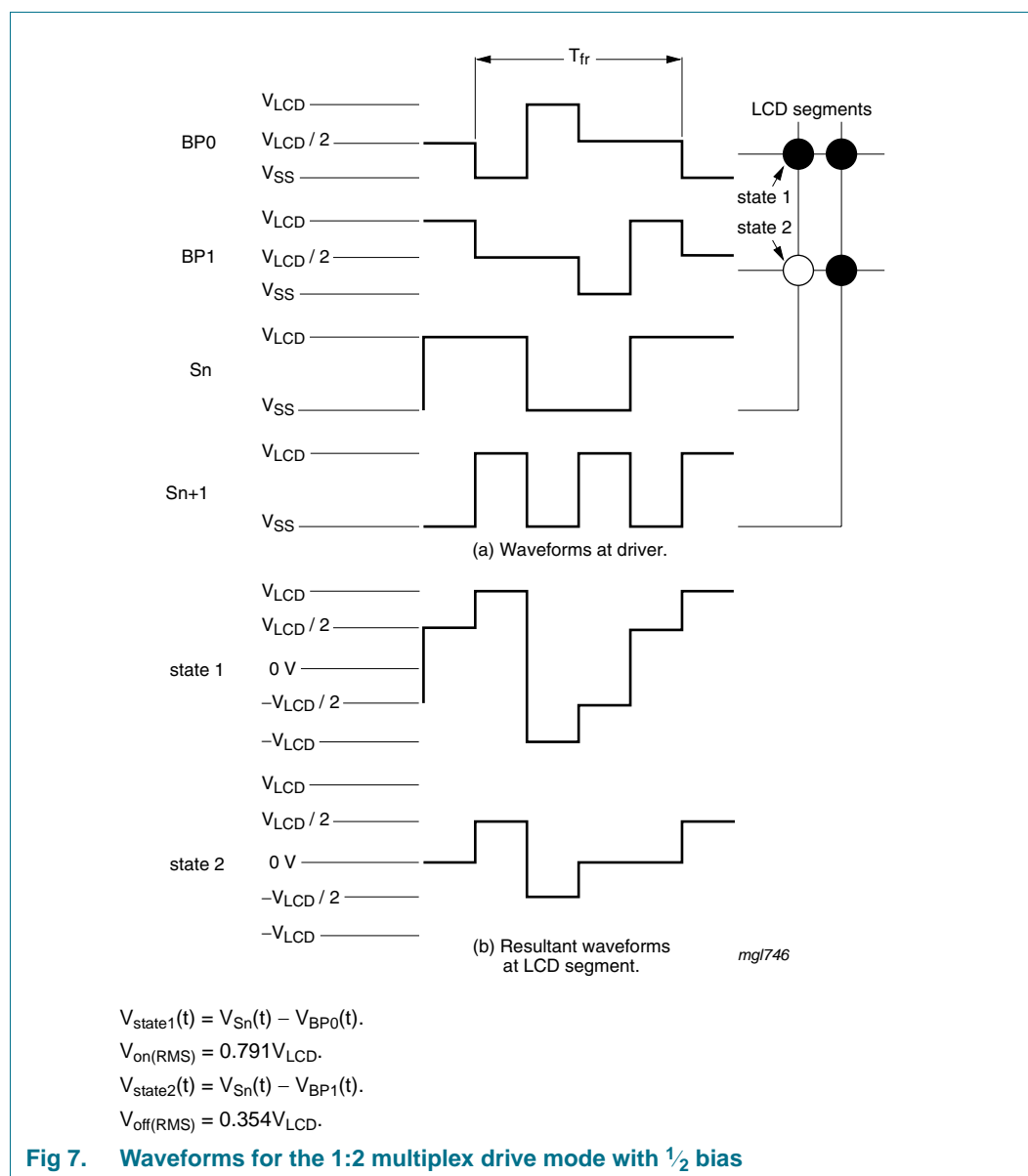**Product data sheet** **Rev. 2 — 10 February 2011** **9 of 49**

7.4 LCD drive mode waveforms

7.4.1 Static drive mode

The static LCD drive mode is used when a single backplane is provided in the LCD. Backplane and segment drive waveforms for this mode are shown in Figure 6.

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$

$V_{on(RMS)} = V_{LCD}.$

$V_{state2}(t) = V_{(Sn+1)}(t) - V_{BP0}(t).$

$V_{off(RMS)} = 0$ V.

Fig 6. Static drive mode waveforms

7.4.2 1:2 multiplex drive mode

When two backplanes are provided in the LCD, the 1:2 multiplex mode applies. The PCF8532 allows the use of $\frac{1}{2}$ bias or $\frac{1}{3}$ bias in this mode as shown in [Figure 7](#) and [Figure 8](#).
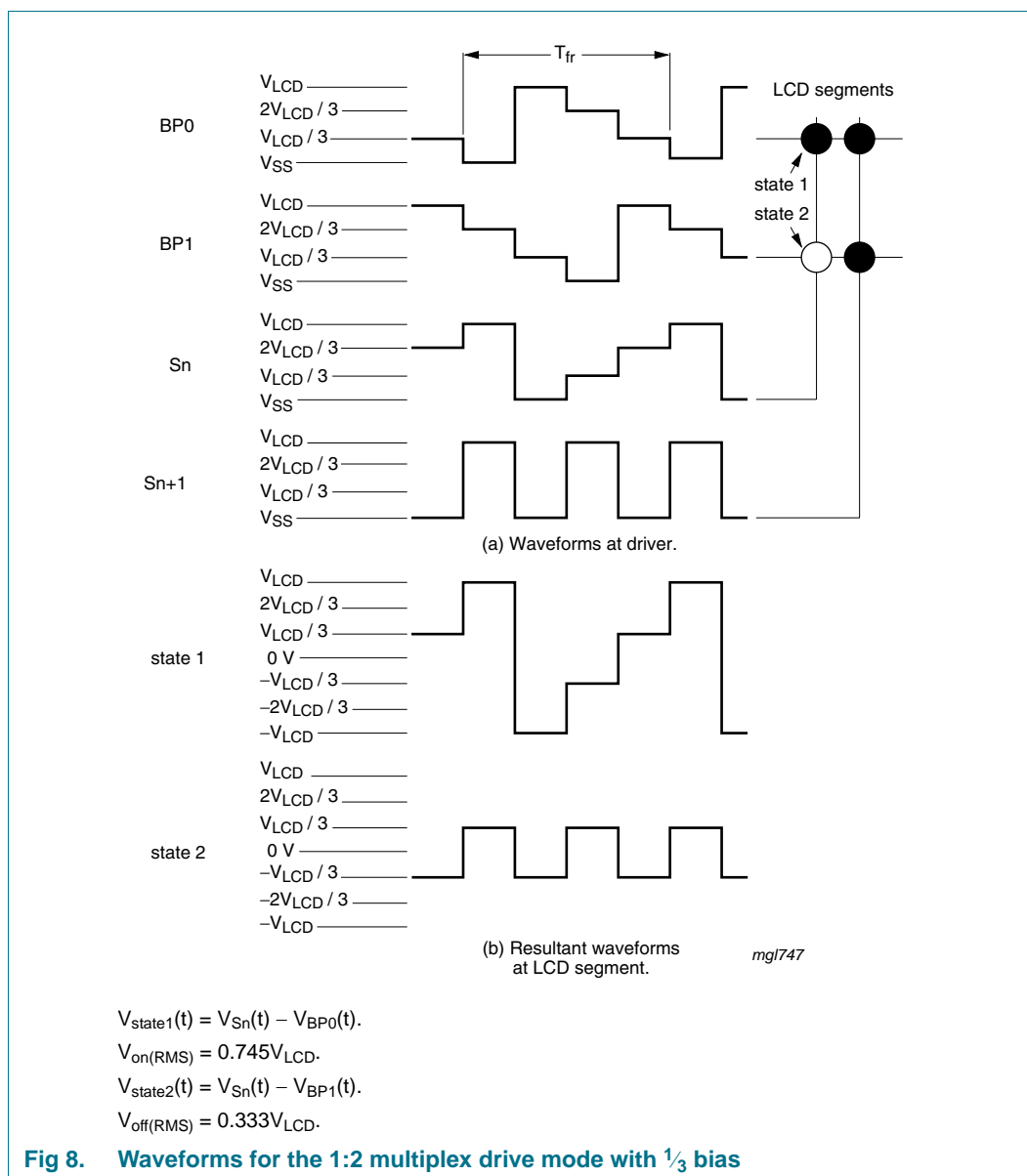

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.791 V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.354 V_{LCD}$.

Fig 7. Waveforms for the 1:2 multiplex drive mode with $\frac{1}{2}$ bias

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t).$

$V_{on(RMS)} = 0.745V_{LCD}.$

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t).$

$V_{off(RMS)} = 0.333V_{LCD}.$

Fig 8.   **Waveforms for the 1:2 multiplex drive mode with $\frac{1}{3}$ bias**

7.4.3 1:3 multiplex drive mode

When three backplanes are provided in the LCD, the 1:3 multiplex drive mode applies as shown in Figure 9.
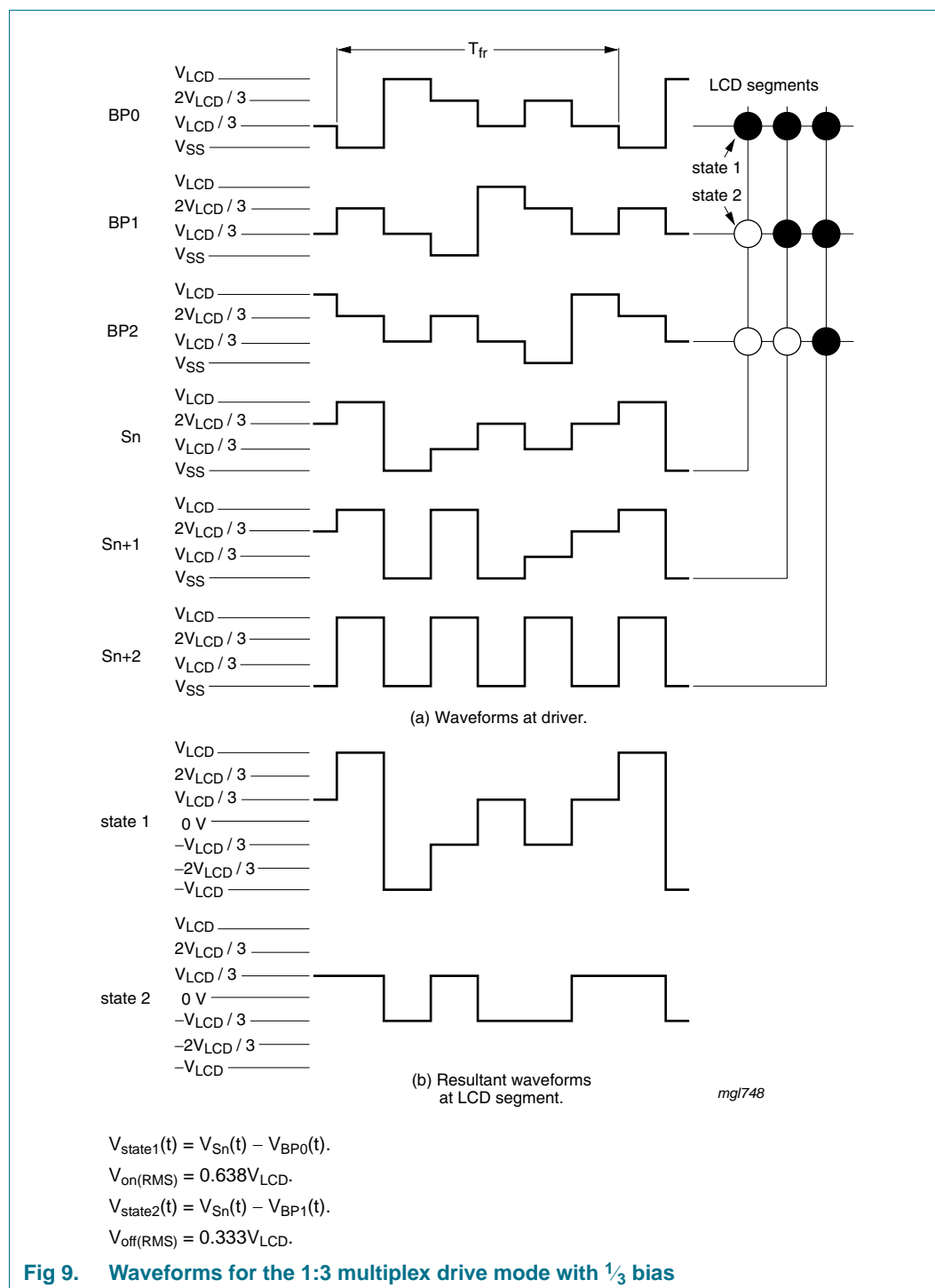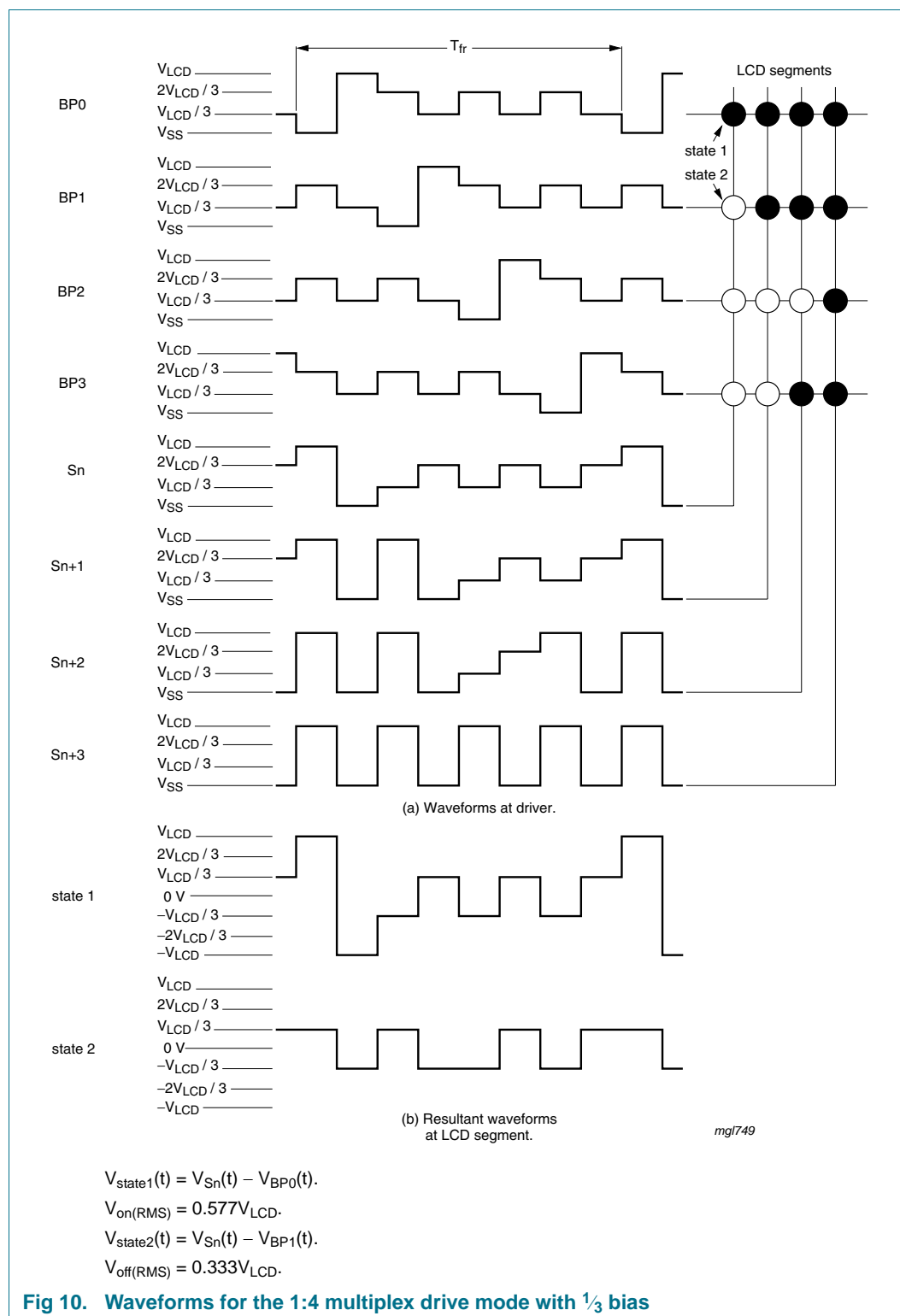

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.638V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 9. Waveforms for the 1:3 multiplex drive mode with $\frac{1}{3}$ bias

7.4.4 1:4 multiplex drive mode

When four backplanes are provided in the LCD, the 1:4 multiplex drive mode applies as shown in Figure 10.

$V_{state1}(t) = V_{Sn}(t) - V_{BP0}(t)$.

$V_{on(RMS)} = 0.577V_{LCD}$.

$V_{state2}(t) = V_{Sn}(t) - V_{BP1}(t)$.

$V_{off(RMS)} = 0.333V_{LCD}$.

Fig 10. Waveforms for the 1:4 multiplex drive mode with $\frac{1}{3}$ bias

7.5 Oscillator

The internal logic and the LCD drive signals of the PCF8532 are timed by a frequency f_{clk} which either is derived from the built-in oscillator frequency f_{osc}:

$$f_{clk} = \frac{f_{osc}}{64}$$

(6)

or equals an external clock frequency $f_{clk(ext)}$:

$$f_{clk} = f_{clk(ext)}$$

(7)

The clock frequency f_{clk} determines the LCD frame frequency f_{fr} (see Table 15).

7.5.1 Internal clock

The internal logic and the LCD drive signals of the PCF8532 are timed either by the built-in oscillator or by an external clock.

The internal oscillator is enabled by connecting pin OSC to pin V_{SS}. In this case the output from pin CLK provides the clock signal for cascaded PCF8532 in the system. However, the clock signal is only available at the pin CLK, if the display is enabled. The display is enabled using the display enable bit (see Table 9).

The nominal output clock frequency is like specified in Table 18 with parameter f_{clk}.

7.5.2 External clock

Connecting pin OSC to V_{DD} enables an external clock source. Pin CLK then becomes the external clock input.

Remark: A clock signal must always be supplied to the device; removing the clock may freeze the LCD in a DC state, which is not suitable for the liquid crystal.

7.6 Timing and frame frequency

The timing of the PCF8532 organizes the internal data flow of the device. This includes the transfer of display data from the display RAM to the display segment outputs. In cascaded applications, the synchronization signal ($\overline{SYNC}$) maintains the correct timing relationship between all the PCF8532 in the system.

The clock frequency can be programmed by software such that the nominal frame frequency can be chosen in steps of 5 Hz in the range of 60 Hz to 90 Hz (see Table 15).

7.7 Display register

The display register holds the display data while the corresponding multiplex signals are generated. There is a one-to-one relationship between the data in the display register, the LCD segment outputs and one column of the display RAM.

7.8 Segment outputs

The LCD drive section includes 160 segment outputs (S0 to S159) which must be connected directly to the LCD. The segment output signals are generated in accordance with the multiplexed backplane signals and with data residing in the display register. When less than 160 segment outputs are required the unused segment outputs must be left open-circuit.

7.9 Backplane outputs

The LCD drive section includes four backplane outputs: BP0 to BP3. The backplane output signals are generated in accordance with the selected LCD drive mode.

- In the 1:4 multiplex drive mode BP0 to BP3 must be connected directly to the LCD.

If less than four backplane outputs are required the unused outputs can be left open-circuit.

- In 1:3 multiplex drive mode BP3 carries the same signal as BP1, therefore these two adjacent outputs can be tied together to give enhanced drive capabilities.
- In 1:2 multiplex drive mode BP0 and BP2, BP1 and BP3 respectively carry the same signals and may also be paired to increase the drive capabilities.
- In static drive mode the same signal is carried by all four backplane outputs and they can be connected in parallel for very high drive requirements.

The pins for the four backplanes BP0 to BP3 are available on both pin bars of the chip. In applications it is possible to use either the pins for the backplanes

- on the top pin bar
- on the bottom pin bar
- or both of them to increase the driving strength of the device.

When using all backplanes available they may be connected to the respective sibling (BP0 on the top pin bar with BP0 on the bottom pin bar and so on).
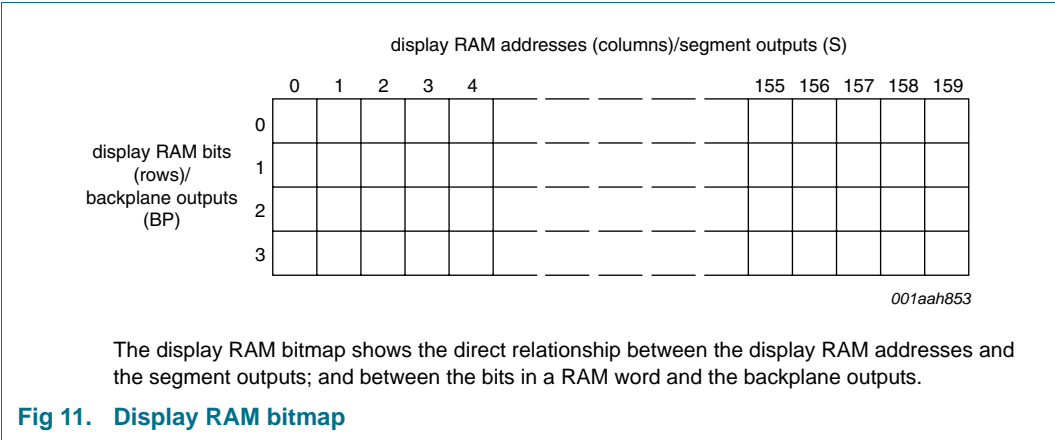
7.10 Display RAM

The display RAM is a static 160×4 bit RAM which stores LCD data. There is a one-to-one correspondence between

- the bits in the RAM bitmap and the LCD elements
- the RAM columns and the segment outputs
- the RAM rows and the backplane outputs.

A logic 1 in the RAM bitmap indicates the on-state of the corresponding LCD element; similarly, a logic 0 indicates the off-state.

The display RAM bit map, Figure 11, shows the rows 0 to 3 which correspond with the backplane outputs BP0 to BP3, and the columns 0 to 159 which correspond with the segment outputs S0 to S159. In multiplexed LCD applications the segment data of the first, second, third, and fourth row of the display RAM are time-multiplexed with BP0, BP1, BP2, and BP3 respectively.

The display RAM bitmap shows the direct relationship between the display RAM addresses and the segment outputs; and between the bits in a RAM word and the backplane outputs.

Fig 11. Display RAM bitmap

When display data is transmitted to the PCF8532 the received display bytes are stored in the display RAM in accordance with the selected LCD drive mode. The data is stored as it arrives and does not wait for the acknowledge cycle as with the commands. Depending on the current multiplex drive mode, data is stored singularly, in pairs, triples, or quadruples. To illustrate the filling order, an example of a 7-segment numeric display showing all drive modes is given in Figure 12; the RAM filling organization depicted applies equally to other LCD types.

The following applies to Figure 12:

- In static drive mode the eight transmitted data bits are placed in row 0 as one byte.

- In 1:2 multiplex drive mode the eight transmitted data bits are placed in pairs into row 0 and 1 as two successive 4-bit RAM words.

- In 1:3 multiplex drive mode the eight bits are placed in triples into row 0, 1, and 2 as three successive 3-bit RAM words, with bit 3 of the third address left unchanged. It is not recommended to use this bit in a display because of the difficult addressing. This last bit may, if necessary, be controlled by an additional transfer to this address but care should be taken to avoid overwriting adjacent data because always full bytes are transmitted.

- In 1:4 multiplex drive mode, the eight transmitted data bits are placed in quadruples into row 0, 1, 2, and 3 as two successive 4-bit RAM words.

drive mode	LCD segments	LCD backplanes	display RAM filling order		transmitted display byte

static

LCD segments: Sn+2 (a), Sn+3 (f), Sn+4 (g), Sn+5 (e), Sn+6 (d), Sn+1 (b), Sn (c), Sn+7 (c), DP

LCD backplanes: BP0

columns — display RAM address/segment outputs (s) — byte1

	n	n + 1	n + 2	n + 3	n + 4	n + 5	n + 6	n + 7
0	c	b	a	f	g	e	d	DP
1	x	x	x	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	x	x	x	x	x	x	x	x

transmitted display byte: MSB ... LSB — c b a f g e d DP

1:2 multiplex

LCD segments: Sn (a), Sn+1 (f), Sn+2 (e), Sn+3 (d), b, g, c, DP

LCD backplanes: BP0, BP1

columns — display RAM address/segment outputs (s) — byte1 / byte2

	n	n + 1	n + 2	n + 3
0	a	f	e	d
1	b	g	c	DP
2	x	x	x	x
3	x	x	x	x

transmitted display byte: MSB ... LSB — a b f g e c d DP

1:3 multiplex

LCD segments: Sn+1 (a), Sn+2 (f), Sn (b), e, g, c, d, DP

LCD backplanes: BP0, BP1, BP2

columns — display RAM address/segment outputs (s) — byte1 / byte2 / byte3

	n	n + 1	n + 2
0	b	a	f
1	DP	d	e
2	c	g	x
3	x	x	x

transmitted display byte: MSB ... LSB — b DP c a d g f e

1:4 multiplex

LCD segments: Sn (a), f, b, g, e, c, Sn+1 (d), DP

LCD backplanes: BP0, BP2, BP1, BP3

columns — display RAM address/segment outputs (s) — byte1 / byte2 / byte3 / byte4 / byte5

	n	n + 1
0	a	f
1	c	e
2	b	g
3	DP	d

transmitted display byte: MSB ... LSB — a c b DP f e g d

001aaj646

x = data bit unchanged

Fig 12. Relationships between LCD layout, drive mode, display RAM filling order and display data transmitted over the I²C-bus

7.11 Data pointer

The addressing mechanism for the display RAM is realized using a data pointer.

This allows the loading of an individual display data byte, or a series of display data bytes, into any location of the display RAM. The sequence commences with the initialization of the data pointer by the load-data-pointer-MSB and load-data-pointer-LSB commands.

Following this two commands, an arriving data byte is stored at the display RAM address indicated by the data pointer. The filling order is shown in Figure 12.

After each byte is stored, the content of the data pointer is automatically incremented by a value dependent on the selected LCD drive mode:

- In static drive mode by eight
- In 1:2 multiplex drive mode by four
- In 1:3 multiplex drive mode by three
- In 1:4 multiplex drive mode by two

If the data pointer reaches 159 it is automatically wrapped around to address 0, consequently the subaddress counter is incremented.

If an I²C-bus data access is terminated early, then the state of the data pointer is unknown. The data pointer must be re-written prior to further RAM accesses.

7.12 Subaddress counter

The storage of display data is conditioned by the contents of the subaddress counter. Storage is allowed only when the content of the subaddress counter match with the hardware subaddress applied to A0 and A1. The subaddress counter value is defined by the device-select command (see Table 12). If the content of the subaddress counter and the hardware subaddress do not match then data storage is inhibited but the data pointer is incremented as if data storage had taken place. The subaddress counter is also incremented when the data pointer overflows.

The storage arrangements described lead to extremely efficient data loading in cascaded applications. When a series of display bytes are sent to the display RAM, automatic wrap-over to the next PCF8532 occurs when the last RAM address is exceeded. Subaddressing across device boundaries is successful even if the change to the next device in the cascade occurs within a transmitted character (such as during the 54th display data byte transmitted in 1:3 multiplex mode).

The hardware subaddress must not be changed whilst the device is being accessed on the I²C-bus interface.

7.13 Output bank selector

The output bank selector selects one of the four rows per display RAM address for transfer to the display register. The actual row selected depends on the particular LCD drive mode in operation and on the instant in the multiplex sequence.

- In 1:4 multiplex mode, all RAM addresses of row 0 are selected, these are followed by the contents of row 1, row 2 and then row 3

- In 1:3 multiplex mode, rows 0, 1 and 2 are selected sequentially
- In 1:2 multiplex mode, rows 0 and 1 are selected
- In the static mode, row 0 is selected.

The PCF8532 includes a RAM bank switching feature in the static and 1:2 multiplex drive modes. In the static drive mode, the bank-select command may request the contents of row 2 to be selected for display instead of the contents of bit 0. In the 1:2 multiplex drive mode, the contents of rows 2 and 3 may be selected instead of rows 0 and 1. This gives the provision for preparing display information in an alternative bank and to be able to switch to it once it is assembled.

7.14 Input bank selector

The input bank selector loads display data into the display RAM in accordance with the selected LCD drive configuration. Display data can be loaded in row 2 in static drive mode or in rows 2 and 3 in 1:2 multiplex drive mode by using the bank-select command. The input bank selector functions independently to the output bank selector.

7.15 Blinker

The display blinking capabilities of the PCF8532 are very versatile. The whole display can blink at frequencies selected by the blink-select command (see Table 14). The blink frequencies are fractions of the clock frequency. The ratios between the clock and blink frequencies depend on the blink mode in which the device is operating (see Table 6).

Table 6.   Blink frequencies
Assuming that f_{clk} = 1.800 kHz.

Blink mode	Operating mode ratio	Blink frequency
off	-	blinking off
1	$f_{blink} = \dfrac{f_{clk}}{768}$	~2.34 Hz
2	$f_{blink} = \dfrac{f_{clk}}{1536}$	~1.17 Hz
3	$f_{blink} = \dfrac{f_{clk}}{3072}$	~0.59 Hz

An additional feature is for an arbitrary selection of LCD segments to blink. This applies to the static and 1:2 multiplex drive modes and can be implemented without any communication overheads. By means of the output bank selector, the displayed RAM banks are exchanged with alternate RAM banks at the blink frequency. This mode can also be specified by the blink-select command.

In the 1:3 and 1:4 multiplex modes, where no alternate RAM bank is available, groups of LCD segments can blink selectively by changing the display RAM data at fixed time intervals.

If the entire display can blink at a frequency other than the nominal blink frequency. This can be effectively performed by resetting and setting the display enable bit E at the required rate using the mode-set command (see Table 6).

7.16 Characteristics of the I²C-bus

The I²C-bus is for bidirectional, two-line communication between different ICs or modules. The two lines are a Serial DAta line (SDA) and a Serial CLock line (SCL). Both lines must be connected to a positive supply via a pull-up resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

In Chip-On-Glass (COG) applications, where the track resistance between the SDA output pin to the system SDA input line can be significant, the bus pull-up resistor and the Indium Tin Oxide (ITO) track resistance may generate a voltage divider. As a consequence it may be possible that the acknowledge cycle, generated by the LCD driver, cannot be interpreted as logic 0 by the master. Therefore it is an advantage for COG applications to have the acknowledge output separated from the data line. For that reason, the SDA line of the PCF8532 is split into SDA and SDAACK.

In COG applications where the acknowledge cycle is required, it is necessary to minimize the track resistance from the SDAACK pin to the system SDA line to guarantee a valid LOW level.

By splitting the SDA line into SDA and SDAACK (having the SDAACK open circuit), the device could be used in a mode that ignores the acknowledge cycle. Separating the acknowledge output from the serial data line can avoid design efforts to generate a valid acknowledge level. However, in that case the I²C-bus master has to be set up in such a way that it ignores the acknowledge cycle.[2]

By connecting pin SDAACK to pin SDA the SDA line becomes fully I²C-bus compatible. The following definition assumes SDA and SDAACK are connected and refers to the pair as SDA.

7.16.1 Bit transfer

One data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the HIGH period of the clock pulse as changes in the data line at this time will be interpreted as a control signal. Bit transfer is shown in Figure 13.

SDA

SCL

data line stable; data valid

change of data allowed

mba607
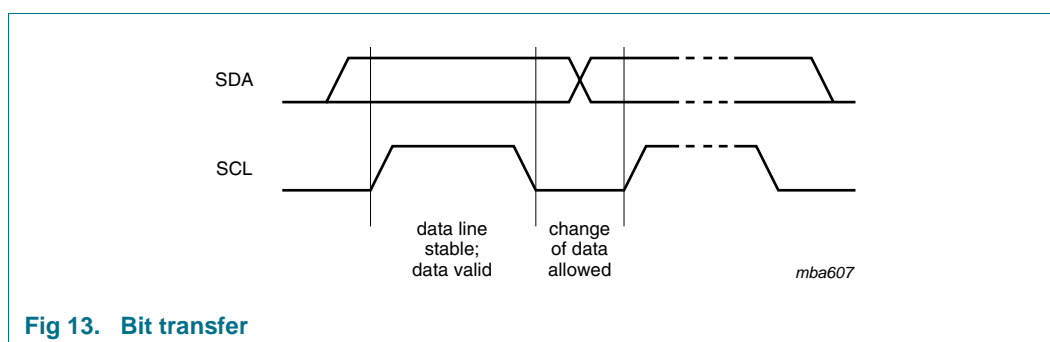
Fig 13. Bit transfer

7.16.2 START and STOP conditions

Both data and clock lines remain HIGH when the bus is not busy.

A HIGH-to-LOW change of the data line, while the clock is HIGH is defined as the START condition (S).

2. For further information, please consider the NXP application note: Ref. 1 "AN10170".

A LOW-to-HIGH change of the data line while the clock is HIGH is defined as the STOP condition (P).

The START and STOP conditions are shown in Figure 14.

Fig 14. Definition of START and STOP conditions
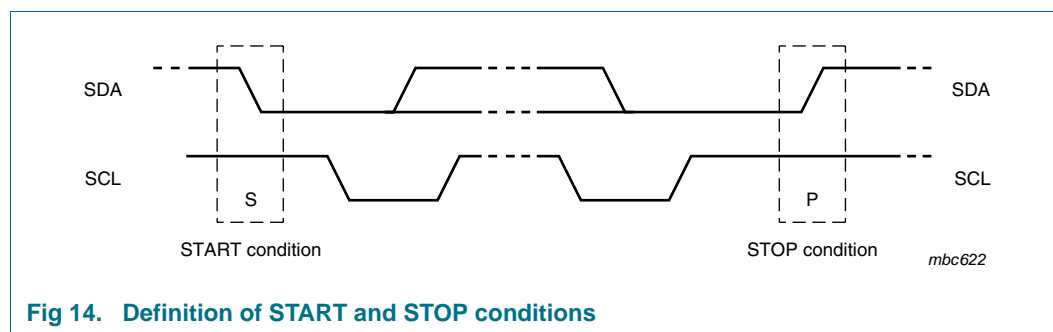
7.16.3 System configuration

A device generating a message is a transmitter, a device receiving a message is the receiver. The device that controls the message is the master and the devices which are controlled by the master are the slaves. The system configuration is shown in Figure 15.

Fig 15. System configuration
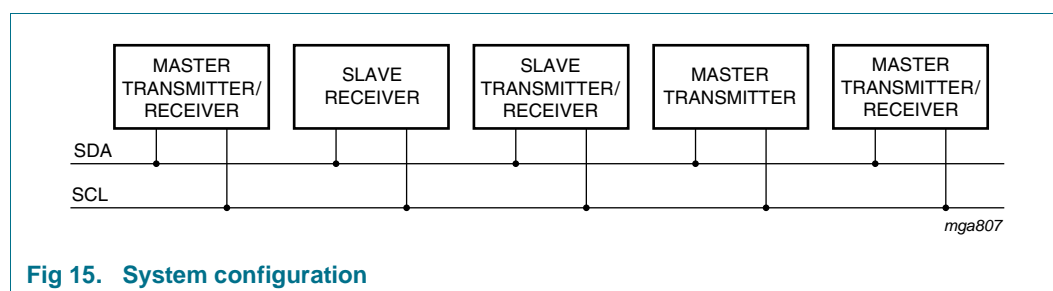
7.16.4 Acknowledge

The number of data bytes transferred between the START and STOP conditions from transmitter to receiver is unlimited. Each byte of eight bits is followed by an acknowledge cycle.

- A slave receiver which is addressed must generate an acknowledge after the reception of each byte.

- Also a master receiver must generate an acknowledge after the reception of each byte that has been clocked out of the slave transmitter.

- The device that acknowledges must pull-down the SDA line during the acknowledge clock pulse, so that the SDA line is stable LOW during the HIGH period of the acknowledge related clock pulse (set-up and hold times must be taken into consideration).

- A master receiver must signal an end of data to the transmitter by not generating an acknowledge on the last byte that has been clocked out of the slave. In this event the transmitter must leave the data line HIGH to enable the master to generate a STOP condition.

Acknowledgement on the I^{2}C-bus is shown in Figure 16.

Fig 16. Acknowledgement on the I²C-bus
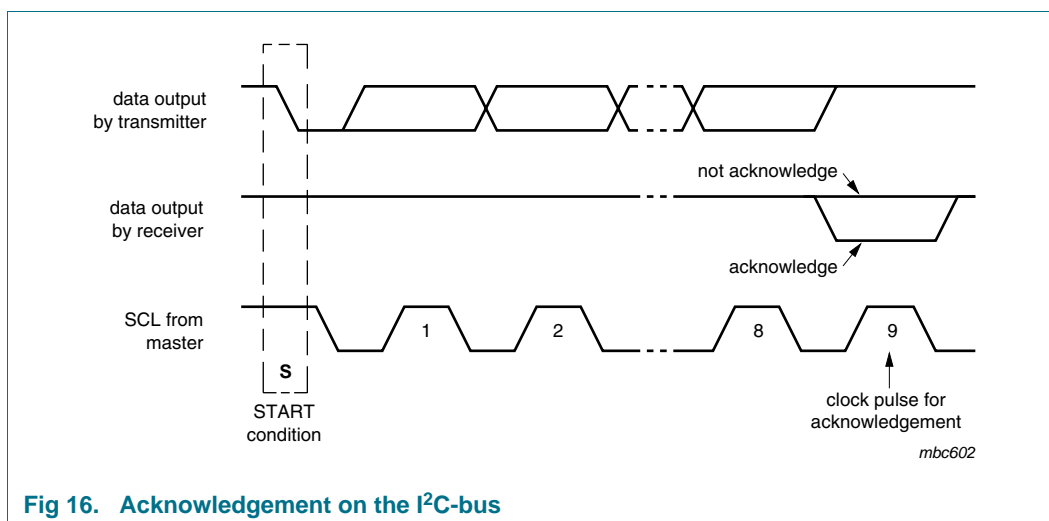
7.16.5 I²C-bus controller

The PCF8532 acts as an I²C-bus slave receiver. It does not initiate I²C-bus transfers or transmit data to an I²C-bus master receiver. The only data output from the PCF8532 are the acknowledge signals of the selected devices. Device selection depends on the I²C-bus slave address, on the transferred command data and on the hardware subaddress.

In single device application, the hardware subaddress inputs A0 and A1 are normally tied to V_{SS} which defines the hardware subaddress 0. In multiple device applications A0 and A1 are tied to V_{SS} or V_{DD} in accordance with a binary coding scheme such that no two devices with a common I²C-bus slave address have the same hardware subaddress.

7.16.6 Input filters

To enhance noise immunity in electrically adverse environments, RC low-pass filters are provided on the SDA and SCL lines.

7.16.7 I²C-bus protocol

Two I²C-bus slave addresses (0111 000 and 0111 001) are reserved for the PCF8532. The least significant bit of the slave address that a PCF8532 responds to is defined by the level tied at its input SA0. The PCF8532 is a write only device and does not respond to a read access. Two types of PCF8532 can be distinguished on the same I²C-bus which allows:

- Up to 8 PCF8532 on the same I²C-bus for very large LCD applications
- The use of two types of LCD multiplex on the same I²C-bus.

The I²C-bus protocol is shown in Figure 17. The sequence is initiated with a START condition (S) from the I²C-bus master which is followed by one of the two PCF8532 slave addresses available. All PCF8532 with the corresponding SA0 level acknowledge in parallel to the slave address, but all PCF8532 with the alternative SA0 level ignore the whole I²C-bus transfer.

After acknowledgement, a control byte follows which defines if the next byte is RAM or command information. The control byte also defines if the next following byte is a control byte or further RAM/command data.

In this way it is possible to configure the device then fill the display RAM with little overhead.

The command bytes and control bytes are also acknowledged by all addressed PCF8532 connected to the bus.

The display bytes are stored in the display RAM at the address specified by the data pointer and the subaddress counter. Both data pointer and subaddress counter are automatically updated and the data is directed to the intended PCF8532 device.

The acknowledgement after each byte is made only by the (A0 and A1) addressed PCF8532. After the last (display) byte, the I²C-bus master issues a STOP condition (P). Alternatively a START may be issued to RESTART an I²C-bus access.
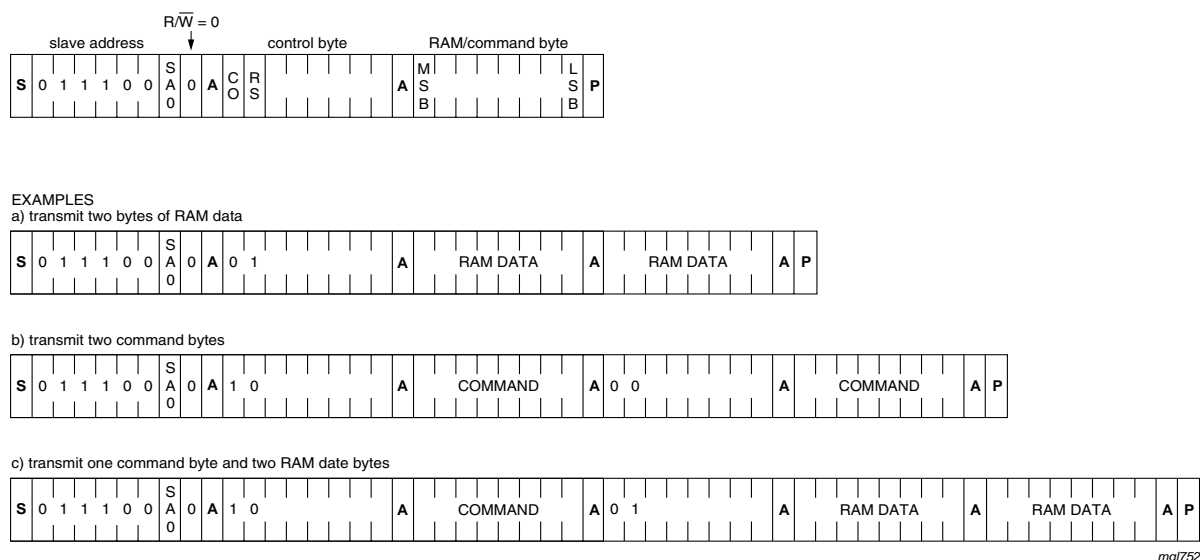
Fig 17. I²C-bus protocol
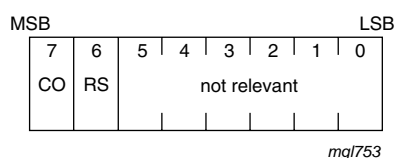
Fig 18. Control byte format

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Table 7.   Control byte description

Bit	Symbol	Value	Description
7	CO		**continue bit**
		0	last control byte
		1	control bytes continue
6	RS		**register selection**
		0	command register
		1	data register
5 to 0	-		not relevant

7.17 Command decoder

The command decoder identifies command bytes that arrive on the I^{2}C-bus. The commands available to the PCF8532 are defined in Table 8.

Table 8.   Definition of PCF8532 commands

Command	Operation code								Reference
Bit	7	6	5	4	3	2	1	0	
mode-set	1	1	0	0	E	B	M1	M0	Table 9
load-data-pointer-MSB	0	0	0	0	P7	P6	P5	P4	Table 10
load-data-pointer-LSB	0	1	0	0	P3	P2	P1	P0	Table 11
device-select	1	1	1	0	0	0	A1	A0	Table 12
bank-select	1	1	1	1	1	0	I	O	Table 13
blink-select	1	1	1	1	0	A	BF1	BF0	Table 14
frequency-prescaler	1	1	1	0	1	F2	F1	F0	Table 15

Table 9.   Mode-set command bits description

Bit	Symbol	Value	Description
7 to 4	-	1100	fixed value
3	E		**display status**
		0[1]	disabled (blank)[2]
		1	enabled
2	B		**LCD bias configuration**[3]
		0[1]	$^1/_3$ bias
		1	$^1/_2$ bias
1 to 0	M[1:0]		**LCD drive mode selection**
		01	static; BP0
		10	1:2 multiplex; BP0, BP1
		11	1:3 multiplex; BP0, BP1, BP2
		00[1]	1:4 multiplex; BP0, BP1, BP2, BP3

[1] Power-on and reset value.

[2] The possibility to disable the display allows implementation of blinking under external control; the enable bit determines also whether the internal clock signal is available at the CLK pin (see Section 7.5.1).

[3] Not applicable for static drive mode.

Table 10.   Load-data-pointer-MSB command bits description

Bit	Symbol	Value	Description
7 to 4	-	0000	fixed value
3 to 0	P[7:4]	0000[1] to 1001	P7 to P4 defines the first 4 (most significant) bits of the data pointer that indicates one of the 160 display RAM addresses

[1]   Power-on and reset value.

Table 11.   Load-data-pointer-LSB command bits description

Bit	Symbol	Value	Description
7 to 4	-	0100	fixed value
3 to 0	P[3:0]	0000[1] to 1111	P3 to P0 defines the last 4 (least significant) bits of the data pointer that indicates one of the 160 display RAM addresses

[1]   Power-on and reset value.

Table 12.   Device-select command bits description

Bit	Symbol	Value	Description
7 to 2	-	111000	fixed value
1 to 0	A[1:0]	00[1] to 11	two bits of immediate data, bits A0 to A1, are transferred to the subaddress counter to define one of four hardware subaddresses

[1]   Power-on and reset value.

Table 13.   Bank-select command bits description

Bit	Symbol	Value	Description	
			Static	**1:2 multiplex[1]**
7 to 2	-	111110	fixed value	
1	I		**input bank selection**; storage of arriving display data	
		0[2]	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3
0	O		**output bank selection**; retrieval of LCD display data	
		0[2]	RAM bit 0	RAM bits 0 and 1
		1	RAM bit 2	RAM bits 2 and 3

[1]   The bank-select command has no effect in 1:3 and 1:4 multiplex drive modes.

[2]   Power-on and reset value.

Table 14. Blink-select command bits description

Bit	Symbol	Value	Description
7 to 3	-	11110	fixed value
2	A		**blink mode selection**
		0[1]	normal blinking[2]
		1	alternate RAM bank blinking[3]
1 to 0	BF[1:0]		**blink frequency selection**
		00[1]	off
		01	1
		10	2
		11	3

[1] Power-on and reset value.

[2] Normal blinking is assumed when the LCD multiplex drive modes 1:3 or 1:4 are selected.

[3] Alternate RAM bank blinking does not apply in 1:3 and 1:4 multiplex drive modes.

Table 15. Frame-frequency prescaler

Bit	Symbol	Value	Description	
			Nominal frame frequency[1]	**Equation**
7 to 4	-	11101	fixed value	
3 to 0	F[2:0]		**division factor definition for the frame frequency**	
		000	60 Hz	$f_{fr} = \frac{64}{80} \times \frac{f_{clk}}{24}$
		001	65 Hz	$f_{fr} = \frac{64}{74} \times \frac{f_{clk}}{24}$
		010	70 Hz	$f_{fr} = \frac{64}{68} \times \frac{f_{clk}}{24}$
		011[2]	75 Hz	$f_{fr} = \frac{f_{clk}}{24}$
		100	80 Hz	$f_{fr} = \frac{64}{60} \times \frac{f_{clk}}{24}$
		101	85 Hz	$f_{fr} = \frac{64}{56} \times \frac{f_{clk}}{24}$
		110	90 Hz	$f_{fr} = \frac{64}{53} \times \frac{f_{clk}}{24}$
		111	75 Hz	$f_{fr} = \frac{f_{clk}}{24}$

[1] Nominal frame frequency calculated for an internal operating frequency of 1.800 kHz.

[2] Power-on and reset value.

7.18 Display controller

The display controller executes the commands identified by the command decoder. It contains the status registers of the PCF8532 and co-ordinates their effects. The display controller is also responsible for loading display data into the display RAM as required by the filling order.
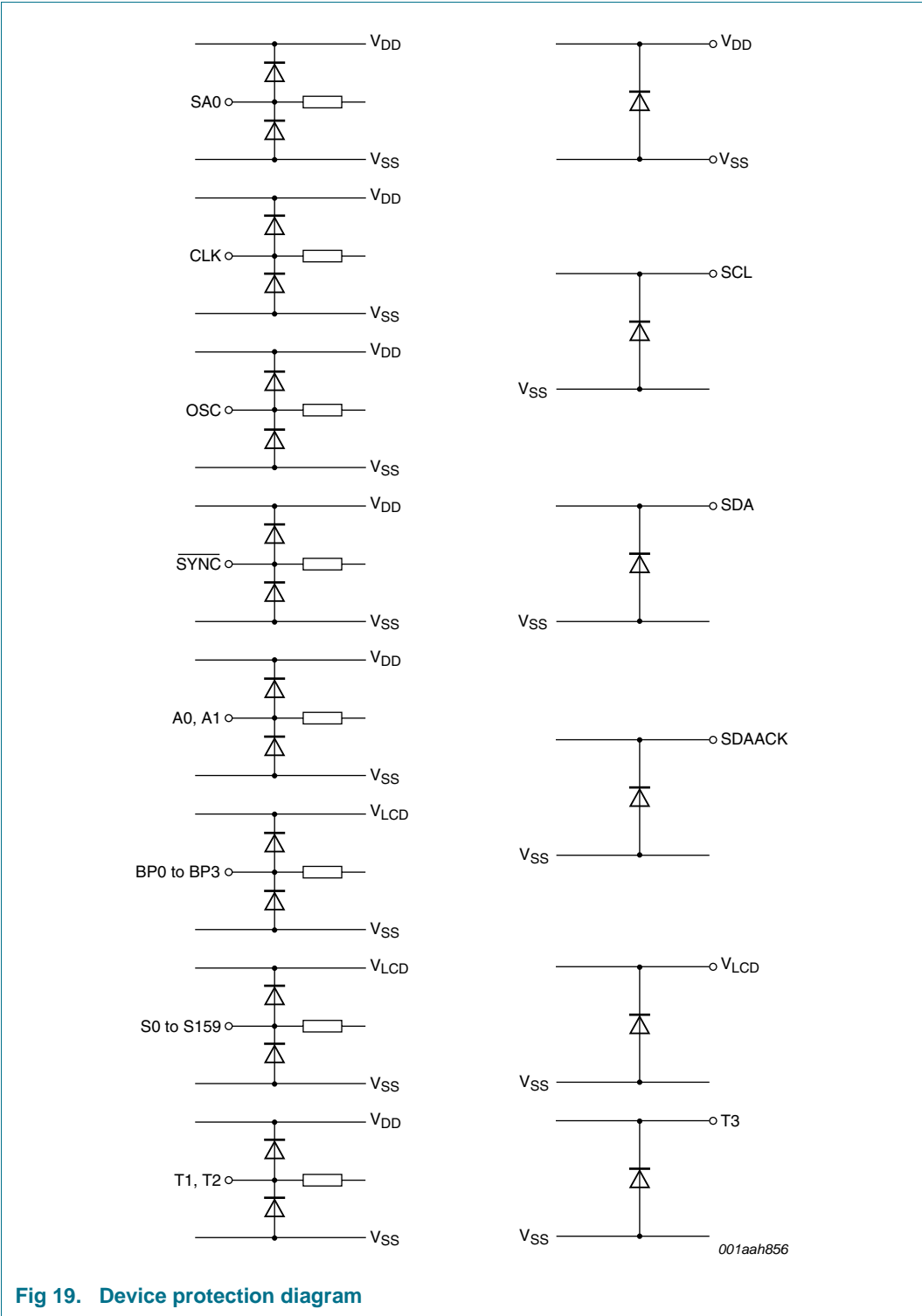
8. Internal circuitry

Fig 19. Device protection diagram

9. Limiting values

CAUTION

⚠

Static voltages across the liquid crystal display can build up when the LCD supply voltage (V_{LCD}) is on while the IC supply voltage (V_{DD}) is off, or vice versa. This may cause unwanted display artifacts. To avoid such artifacts, V_{LCD} and V_{DD} must be applied or removed together.

Table 16.   Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+6.5	V
I_{DD}	supply current			−50	+50	mA
V_{LCD}	LCD supply voltage			−0.5	+9.0	V
$I_{DD(LCD)}$	LCD supply current			−50	+50	mA
V_I	input voltage	on pins CLK, $\overline{SYNC}$, SA0, OSC, SDA, SCL and A0, A1, T1, T2, T3		−0.5	+6.5	V
I_I	input current			−10	+10	mA
V_O	output voltage	on pins S0 to S159 and BP0 to BP3		−0.5	+7.5	V
		on pins SDAACK, CLK, $\overline{SYNC}$		−0.5	+6.5	V
I_O	output current			−10	+10	mA
I_{SS}	ground supply current			−50	+50	mA
P_{tot}	total power dissipation			-	400	mW
P/out	power dissipation per output			-	100	mW
V_{ESD}	electrostatic discharge voltage	HBM	[2]	-	±4500	V
		MM	[3]	-	±250	V
I_{lu}	latch-up current		[4]	-	200	mA
T_{stg}	storage temperature		[5]	−65	+150	°C

[1] Stresses above these values listed may cause permanent damage to the device.

[2] Pass level; Human Body Model (HBM) according to Ref. 6 "JESD22-A114".

[3] Pass level; Machine Model (MM), according to Ref. 7 "JESD22-A115".

[4] Pass level; latch-up testing according to Ref. 8 "JESD78" at maximum ambient temperature ($T_{amb(max)}$).

[5] According to the NXP store and transport requirements (see Ref. 10 "NX3-00092") the devices have to be stored at a temperature of +8 °C to +45 °C and a humidity of 25 % to 75 %. For long-term storage products, divergent conditions are described in that document.

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10. Static characteristics

Table 17.   Static characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 1.8 V to 8.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Supplies							
V_{DD}	supply voltage			1.8	-	5.5	V
V_{LCD}	LCD supply voltage			1.8	-	8.0	V
I_{DD}	supply current	$f_{clk(ext)}$ = 1.800 kHz	[1][2]	-	4	20	μA
		with internal oscillator running	[1]	-	18	60	μA
$I_{DD(LCD)}$	LCD supply current	$f_{clk(ext)}$ = 1.800 kHz	[1][2]	-	30	70	μA
		with internal oscillator running	[1]	-	30	70	μA
Logic							
V_I	input voltage	on pins SDA, SDAACK and SCL		−0.5	-	5.5	V
		all other input pins		−0.5	-	V_{DD} + 0.5	V
V_{IH}	HIGH-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0, A1, SA0, SCL and SDA		0.7V_{DD}	-	-	V
V_{IL}	LOW-level input voltage	on pins CLK, $\overline{SYNC}$, OSC, A0, A1, SA0, SCL and SDA		-	-	0.3V_{DD}	V
V_O	output voltage	on pins SCL and $\overline{SYNC}$		−0.5	-	V_{DD} + 0.5	V
		pin SDAACK		−0.5	-	5.5	V
I_{OH}	HIGH-level output current	V_{OH} = 4.6 V; V_{DD} = 5 V; on pin CLK		-	-	−1.5	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V; V_{DD} = 5 V;					
		on pins CLK and $\overline{SYNC}$		1.5	-	-	mA
		on pin SDAACK					
		$V_{DD} \leq$ 2 V; V_{OL} = 0.2V_{DD}		3	-	-	mA
		2 V < V_{DD} < 3 V; V_{OL} = 0.4 V		3	-	-	mA
		$V_{DD} \geq$ 3 V; V_{OL} = 0.4 V		6	-	-	mA
V_{POR}	power-on reset voltage			1.0	1.3	1.6	V
I_L	leakage current	$V_I = V_{DD}$ or V_{SS}; on pin OSC, CLK, A0, A1, SA0, SDA, SDAACK and SCL		−1	-	+1	μA
LCD outputs							
ΔV_O	output voltage variation	on pins BP0 to BP3 and S0 to S159	[3][4]	−30	-	+30	mV
R_O	output resistance	V_{LCD} = 5 V; on pins BP0 to BP3		-	1.5	5	kΩ
		V_{LCD} = 5 V; on pins S0 to S159		-	2.0	5	kΩ

[1]   LCD outputs are open-circuit; inputs at V_{SS} or V_{DD}; I²C-bus inactive; V_{LCD} = 8.0 V, V_{DD} = 5.0 V and RAM written with all logic 1.

[2]   External clock with 50 % duty factor.

[3]   Variation between any 2 backplanes on a given voltage level; static measured.

[4]   Variation between any 2 segments on a given voltage level; static measured.

T_{amb} = 25 °C; MUX 1:4; all RAM written with logic 1; no display connected; external clock with $f_{clk(ext)}$ = 1.800 kHz.

Fig 20. $I_{DD(LCD)}$ (typical) with respect to V_{LCD}

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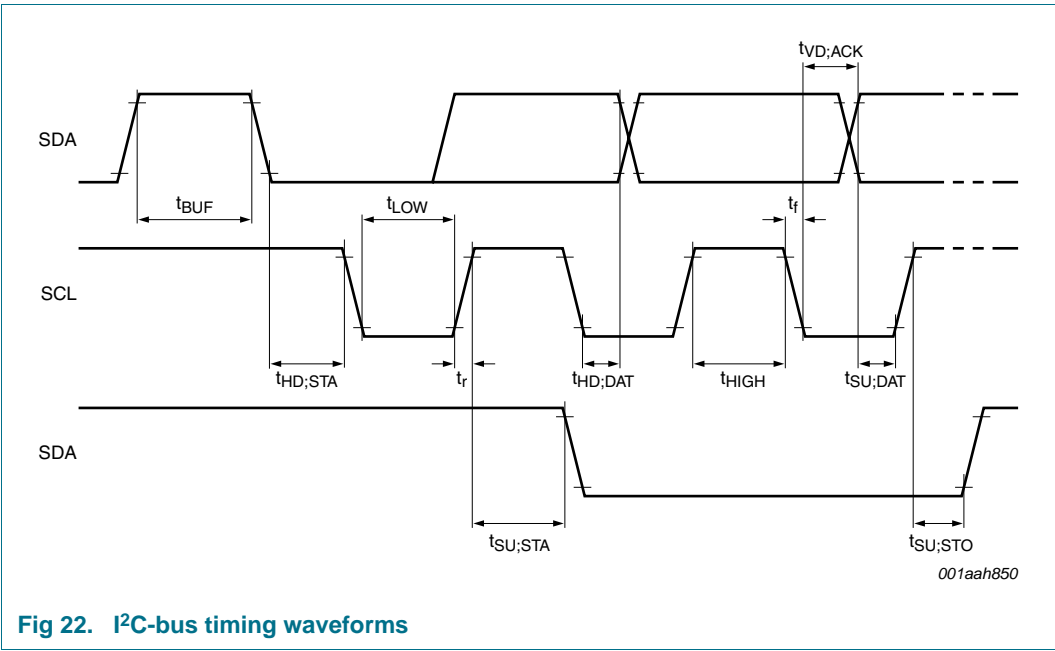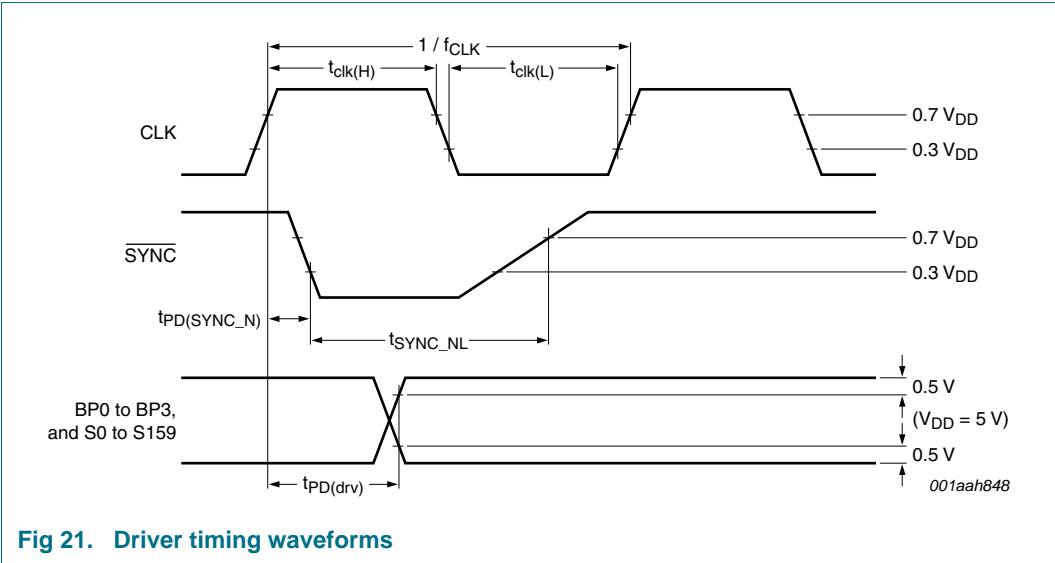
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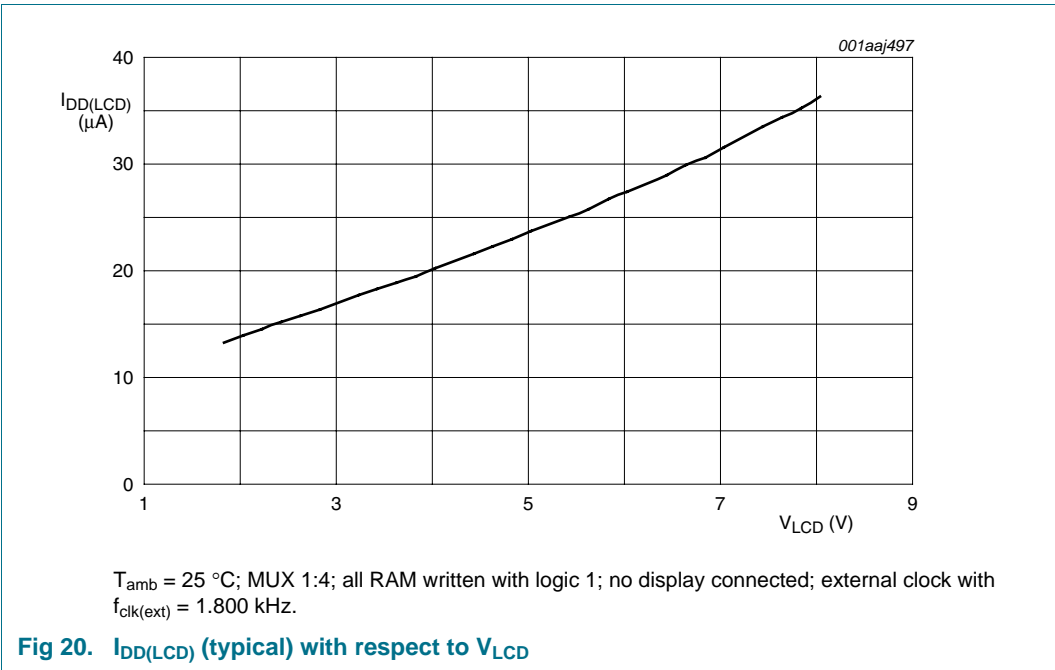
11. Dynamic characteristics

Table 18.   Dynamic characteristics

V_{DD} = 1.8 V to 5.5 V; V_{SS} = 0 V; V_{LCD} = 1.8 V to 8.0 V; T_{amb} = −40 °C to +85 °C; unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
f_{clk}	clock frequency	on pin CLK; see Table 15	[1]	900	1800	3000	Hz
$f_{clk(ext)}$	external clock frequency		[2]	700	-	5000	Hz
$t_{clk(H)}$	HIGH-level clock time	external clock source used		100	-	-	μs
$t_{clk(L)}$	LOW-level clock time	external clock source used		100	-	-	μs
$t_{PD(SYNC\_N)}$	$\overline{SYNC}$ propagation delay			-	30	-	ns
t_{SYNC_NL}	$\overline{SYNC}$ LOW time			100	-	-	μs
$t_{PD(drv)}$	driver propagation delay	V_{LCD} = 5 V		-	10	-	μs
Timing characteristics: I2C-bus			[3]				
f_{SCL}	SCL clock frequency			-	-	400	kHz
t_{BUF}	bus free time between a STOP and START condition			1.3	-	-	μs
$t_{HD;STA}$	hold time (repeated) START condition			0.6	-	-	μs
$t_{SU;STA}$	set-up time for a repeated START condition			0.6	-	-	μs
$t_{VD;ACK}$	data valid acknowledge time			-	-	1.2	μs
t_{HIGH}	HIGH period of the SCL clock			0.6	-	-	μs
t_{LOW}	LOW period of the SCL clock			1.3	-	-	μs
t_f	fall time	of both SDA and SCL signals		-	-	0.3	μs
t_r	rise time	of both SDA and SCL signals		-	-	0.3	μs
C_b	capacitive load for each bus line			-	-	400	pF
$t_{SU;DAT}$	data set-up time			200	-	-	ns
$t_{HD;DAT}$	data hold time			0	-	-	ns
$t_{SU;STO}$	set-up time for STOP condition			0.6	-	-	μs
$t_{w(spike)}$	spike pulse width			-	-	50	ns

[1]   Typical output duty factor: 50 % measured at the CLK output pin.

[2]   For $f_{clk(ext)}$ > 4 kHz it is recommended to use an external pull-up resistor between pin $\overline{SYNC}$ and pin V_{DD}. The value of the resistor should be between 100 kΩ and 1 MΩ. This resistor should be present even when no cascading configuration is used!

[3]   All timing values are valid within the operating supply voltage and ambient temperature range and are referenced to V_{IL} and V_{IH} with an input voltage swing of V_{SS} to V_{DD}.

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Fig 21. Driver timing waveforms

Fig 22. I2C-bus timing waveforms

12. Application information

12.1 Cascaded operation

In large display configurations, up to 8 PCF8532 can be distinguished on the same I^{2}C-bus by using the 2-bit hardware subaddress (A0 and A1) and the programmable I^{2}C-bus slave address (SA0). When cascaded PCF8532 are synchronized, they can share the backplane signals from one of the devices in the cascade. Such an arrangement is cost-effective in large LCD applications since the backplane outputs of only one device need to be through-plated to the backplane electrodes of the display. The other PCF8532 of the cascade contribute additional segment outputs but their backplane outputs are left open-circuit (see Figure 23).

For display sizes that are not multiple of 640 elements, a mixed cascaded system can be considered containing only devices like PCF8532 and PCF8533. Depending on the application, one must take care of the software commands compatibility and pin connection compatibility.

The $\overline{\text{SYNC}}$ line is provided to maintain the correct synchronization between all cascaded PCF8532. This synchronization is guaranteed after the power-on reset. The only time that $\overline{\text{SYNC}}$ is likely to be needed is if synchronization is accidentally lost (e.g. by noise in adverse electrical environments, or by the definition of a multiplex mode when PCF8532 with different SA0 levels are cascaded). $\overline{\text{SYNC}}$ is organized as an input/output pin; the output selection being realized as an open-drain driver with an internal pull-up resistor. A PCF8532 asserts the $\overline{\text{SYNC}}$ line at the onset of its last active backplane signal and monitors the $\overline{\text{SYNC}}$ line at all other times. Should synchronization in the cascade be lost, it will be restored by the first PCF8532 to assert $\overline{\text{SYNC}}$. The timing relationship between the backplane waveforms and the $\overline{\text{SYNC}}$ signal for the various drive modes of the PCF8532 are shown in Figure 25.

When using an external clock signal with high frequencies ($f_{\text{clk(ext)}} > 4$ kHz) it is recommended to have an external pull-up resistor between pin $\overline{\text{SYNC}}$ and pin V_{DD} (see Table 18). This resistor should be present even when no cascading configuration is used! When using it in a cascaded configuration, care must be taken not to route the $\overline{\text{SYNC}}$ signal to close to noisy signals.

The contact resistance between the $\overline{\text{SYNC}}$ pads of cascaded devices must be controlled. If the resistance is too high, the device will not be able to synchronize properly. This is particularly applicable to COG applications. Table 19 shows the limiting values for contact resistance.

In the cascaded applications, the OSC pin of the PCF8532 with subaddress 0 is connected to V_{SS} so that this device uses its internal clock to generate a clock signal at the CLK pin. The other PCF8532 devices are having the OSC pin connected to V_{DD}, meaning that this devices are ready to receive external clock, the signal being provided by the device with subaddress 0.

In the case that the master is providing the clock signal to the slave devices, care must be taken that the sending of display enable or disable will be received by both, the master and the slaves at the same time. When the display is disabled the output from pin CLK is disabled too. The disconnection of the clock may result in a DC component for the display.

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Alternatively the schematic can be also constructed such that all the devices have OSC pin connected to V_{DD} and thus an external CLK being provided for the system (all devices connected to the same external CLK).

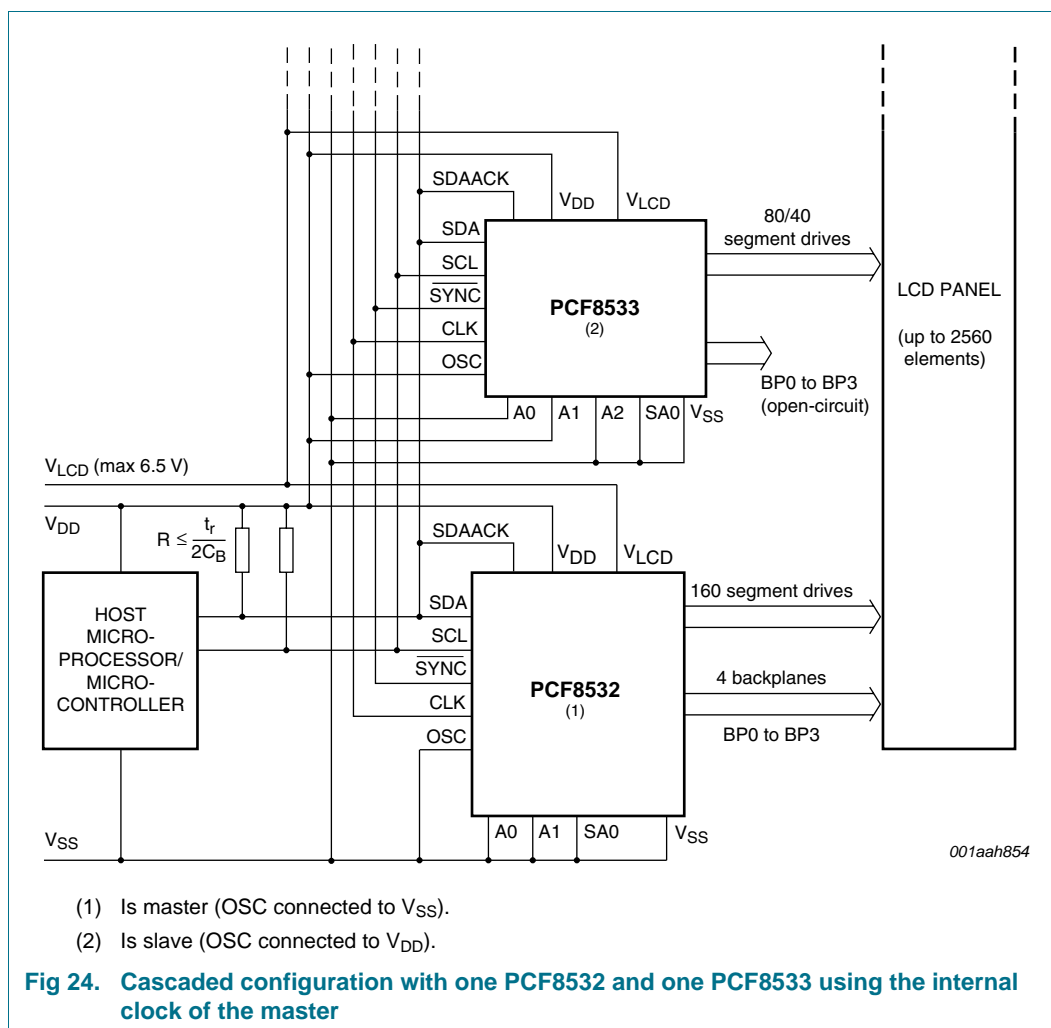A configuration where $\overline{SYNC}$ is connected but all PCF8532 are using the internal clock (OSC pin tied to V_{SS}) is not recommended and may lead to display artefacts!

Table 19. $\overline{SYNC}$ contact resistance

Number of devices	Maximum contact resistance
2	6000 Ω
3 to 5	2200 Ω
6 to 8	1200 Ω

(1) Is master (OSC connected to V_{SS}).

(2) Is slave (OSC connected to V_{DD}).

Fig 23.   Cascaded configuration with two PCF8532 using the internal clock of the master

(1) Is master (OSC connected to V_{SS}).

(2) Is slave (OSC connected to V_{DD}).

Fig 24. Cascaded configuration with one PCF8532 and one PCF8533 using the internal clock of the master
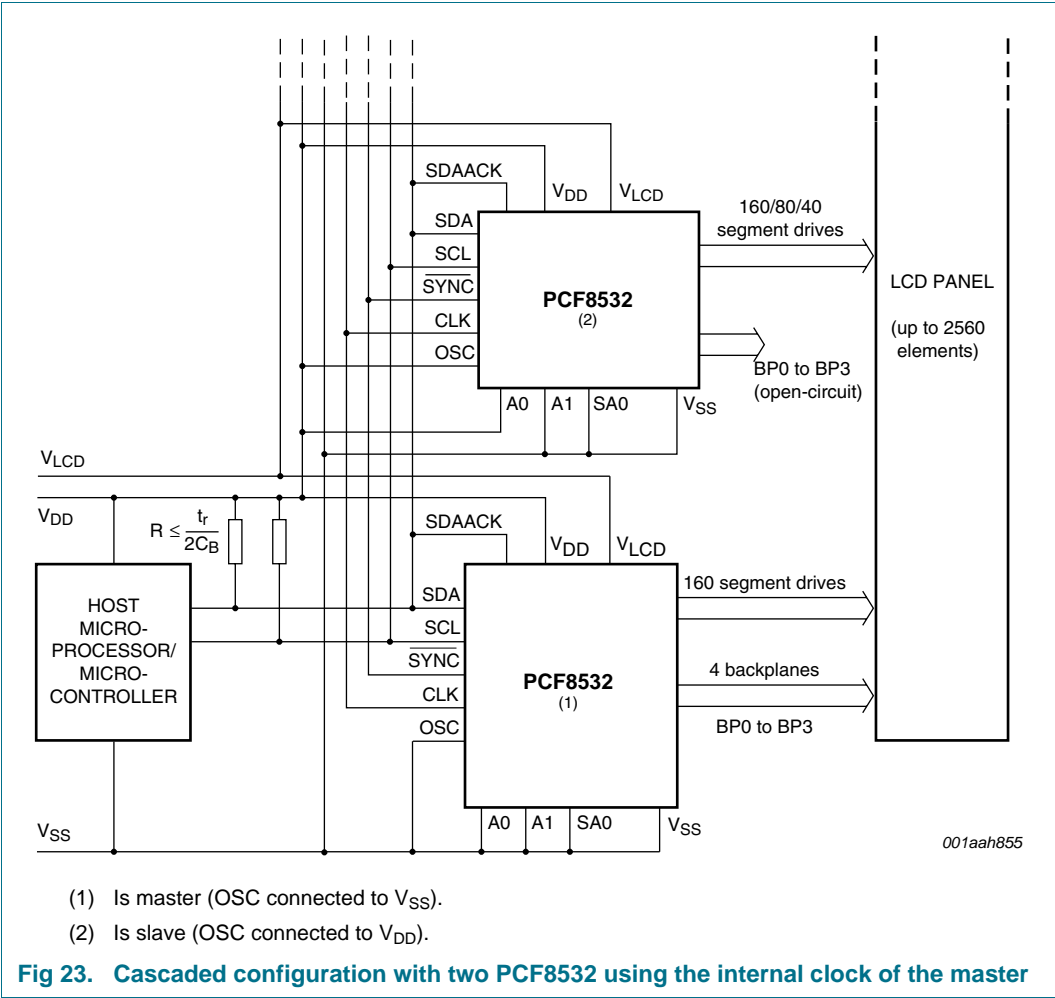
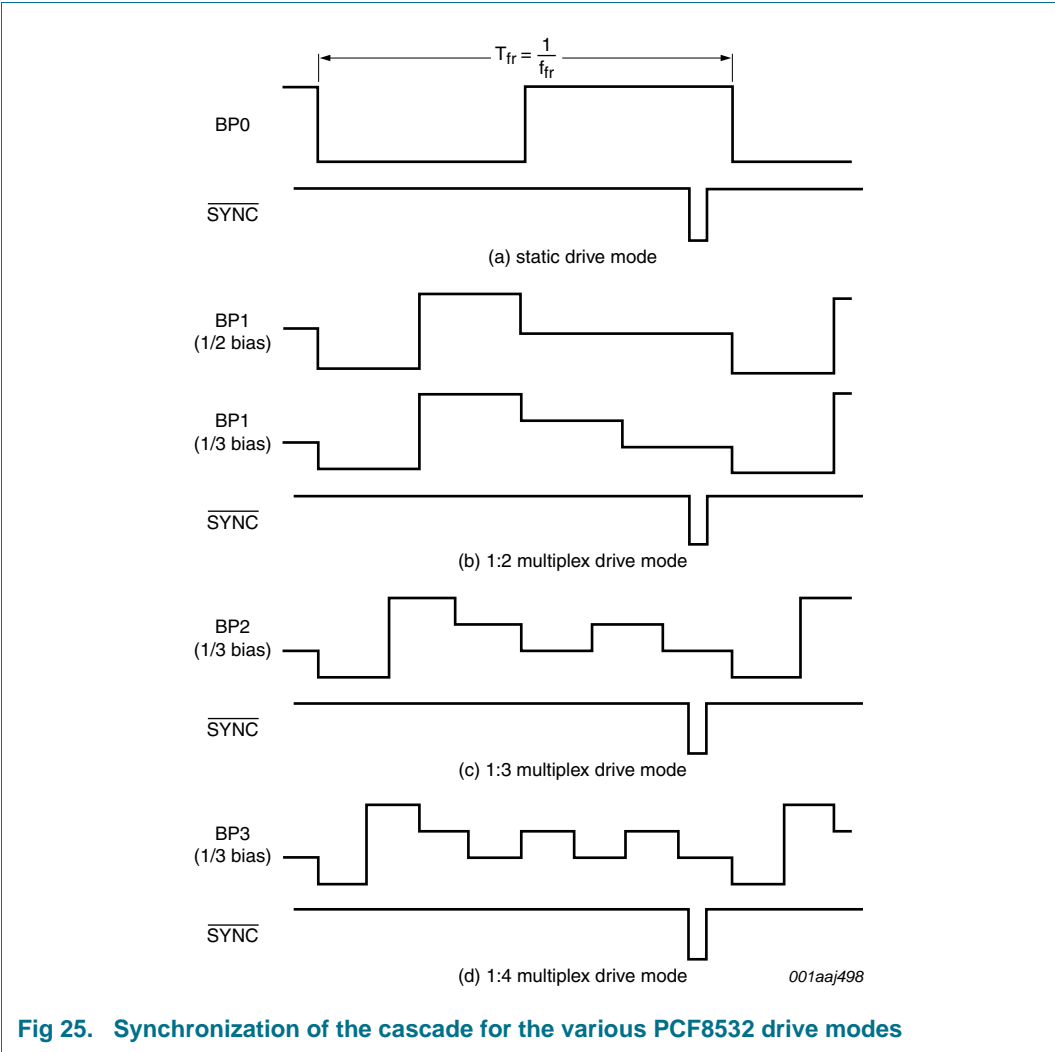**Fig 25. Synchronization of the cascade for the various PCF8532 drive modes**

13. Bare die outline

Bare die; 197 bumps; 6.5 x 1.16 x 0.38 mm   **PCF8532U**

DIMENSIONS (mm are the original dimensions)

UNIT		A	A_1	b	D	E	e^{(1)}	e_1^{(1)}	L
mm	max nom min	0.380	0.018 0.015 0.012	0.0338	6.5	1.16	0.054	0.203	0.090

Note

1. Dimension not drawn to scale.
2. All bumps are the same size.

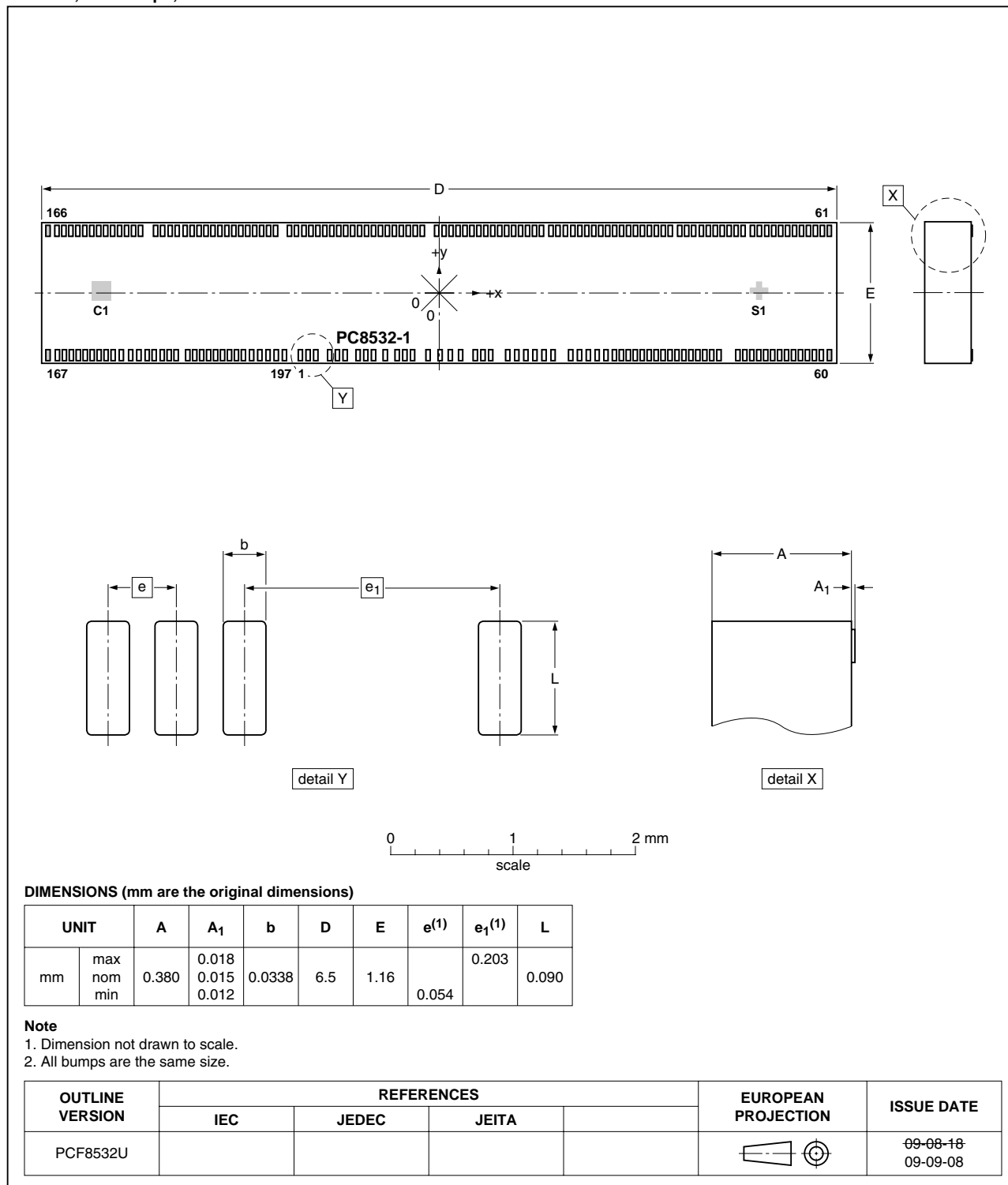| OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
PCF8532U						09-08-18 09-09-08

Fig 26. Bare die outline of PCF8532U

Table 20. Bump locations

All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 26.

Symbol	Bump	X (μm)	Y (μm)	Symbol	Bump	X (μm)	Y (μm)
SDAACK	1	−1165.3	−481.5	S68	100	750.2	481.5
SDAACK	2	−1111.3	−481.5	S69	101	696.2	481.5
SDAACK	3	−1057.3	−481.5	S70	102	642.2	481.5
SDA	4	−854.8	−481.5	S71	103	588.2	481.5
SDA	5	−800.8	−481.5	S72	104	534.2	481.5
SDA	6	−746.8	−481.5	S73	105	480.2	481.5
SCL	7	−575.8	−481.5	S74	106	426.2	481.5
SCL	8	−521.8	−481.5	S75	107	372.2	481.5
SCL	9	−467.8	−481.5	S76	108	318.2	481.5
CLK	10	−316.2	−481.5	S77	109	264.2	481.5
V_{DD}	11	−204.1	−481.5	S78	110	210.2	481.5
V_{DD}	12	−150.1	−481.5	S79	111	156.2	481.5
V_{DD}	13	−96.1	−481.5	BP0	112	86.8	481.5
$\overline{SYNC}$	14	6.9	−481.5	BP2	113	32.8	481.5
OSC	15	119.4	−481.5	BP1	114	−21.2	481.5
T1	16	203.1	−481.5	BP3	115	−75.2	481.5
T2	17	286.8	−481.5	S80	116	−190.7	481.5
T3	18	389.9	−481.5	S81	117	−244.7	481.5
T3	19	443.9	−481.5	S82	118	−298.7	481.5
T3	20	497.9	−481.5	S83	119	−352.7	481.5
A0	21	640.5	−481.5	S84	120	−406.7	481.5
A1	22	724.2	−481.5	S85	121	−460.7	481.5
SA0	23	807.9	−481.5	S86	122	−514.7	481.5
V_{SS}	24	893.0	−481.5	S87	123	−568.7	481.5
V_{SS}	25	947.0	−481.5	S88	124	−622.7	481.5
V_{SS}	26	1001.0	−481.5	S89	125	−676.7	481.5
V_{LCD}	27	1107.2	−481.5	S90	126	−730.7	481.5
V_{LCD}	28	1161.2	−481.5	S91	127	−784.7	481.5
V_{LCD}	29	1215.2	−481.5	S92	128	−838.7	481.5
BP2	30	1303.4	−481.5	S93	129	−892.7	481.5
BP0	31	1357.4	−481.5	S94	130	−946.7	481.5
S0	32	1411.4	−481.5	S95	131	−1000.7	481.5
S1	33	1465.4	−481.5	S96	132	−1054.7	481.5
S2	34	1519.4	−481.5	S97	133	−1108.7	481.5
S3	35	1573.4	−481.5	S98	134	−1224.2	481.5
S4	36	1627.4	−481.5	S99	135	−1278.2	481.5
S5	37	1681.4	−481.5	S100	136	−1332.2	481.5
S6	38	1735.4	−481.5	S101	137	−1386.2	481.5
S7	39	1789.4	−481.5	S102	138	−1440.2	481.5

PCF8532

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Table 20.   Bump locations *…continued*
All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 26.

Symbol	Bump	X (μm)	Y (μm)	Symbol	Bump	X (μm)	Y (μm)
S8	40	1843.4	−481.5	S103	139	−1494.2	481.5
S9	41	1897.4	−481.5	S104	140	−1548.2	481.5
S10	42	1951.4	−481.5	S105	141	−1602.2	481.5
S11	43	2005.4	−481.5	S106	142	−1656.2	481.5
S12	44	2059.4	−481.5	S107	143	−1710.2	481.5
S13	45	2113.4	−481.5	S108	144	−1764.2	481.5
S14	46	2167.4	−481.5	S109	145	−1818.2	481.5
S15	47	2221.4	−481.5	S110	146	−1872.2	481.5
S16	48	2363.9	−481.5	S111	147	−1926.2	481.5
S17	49	2417.9	−481.5	S112	148	−1980.2	481.5
S18	50	2471.9	−481.5	S113	149	−2034.2	481.5
S19	51	2525.9	−481.5	S114	150	−2088.2	481.5
S20	52	2579.9	−481.5	S115	151	−2142.2	481.5
S21	53	2633.9	−481.5	S116	152	−2284.7	481.5
S22	54	2687.9	−481.5	S117	153	−2338.7	481.5
S23	55	2741.9	−481.5	S118	154	−2392.7	481.5
S24	56	2795.9	−481.5	S119	155	−2446.7	481.5
S25	57	2849.9	−481.5	S120	156	−2500.7	481.5
S26	58	2903.9	−481.5	S121	157	−2554.7	481.5
S27	59	2957.9	−481.5	S122	158	−2608.7	481.5
S28	60	3011.9	−481.5	S123	159	−2662.7	481.5
S29	61	3067.7	481.5	S124	160	−2716.7	481.5
S30	62	3013.7	481.5	S125	161	−2770.7	481.5
S31	63	2959.7	481.5	S126	162	−2824.7	481.5
S32	64	2905.7	481.5	S127	163	−2878.7	481.5
S33	65	2851.7	481.5	S128	164	−2932.7	481.5
S34	66	2797.7	481.5	S129	165	−2986.7	481.5
S35	67	2743.7	481.5	S130	166	−3040.7	481.5
S36	68	2689.7	481.5	S131	167	−3025.2	−481.5
S37	69	2635.7	481.5	S132	168	−2971.2	−481.5
S38	70	2520.2	481.5	S133	169	−2917.2	−481.5
S39	71	2466.2	481.5	S134	170	−2863.2	−481.5
S40	72	2412.2	481.5	S135	171	−2809.2	−481.5
S41	73	2358.2	481.5	S136	172	−2755.2	−481.5
S42	74	2304.2	481.5	S137	173	−2701.2	−481.5
S43	75	2250.2	481.5	S138	174	−2647.2	−481.5
S44	76	2196.2	481.5	S139	175	−2593.2	−481.5
S45	77	2142.2	481.5	S140	176	−2539.2	−481.5
S46	78	2088.2	481.5	S141	177	−2485.2	−481.5

Table 20.   Bump locations *…continued*
All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 26.

Symbol	Bump	X (μm)	Y (μm)	Symbol	Bump	X (μm)	Y (μm)
S47	79	2034.2	481.5	S142	178	−2431.2	−481.5
S48	80	1891.7	481.5	S143	179	−2377.2	−481.5
S49	81	1837.7	481.5	S144	180	−2234.7	−481.5
S50	82	1783.7	481.5	S145	181	−2180.7	−481.5
S51	83	1729.7	481.5	S146	182	−2126.7	−481.5
S52	84	1675.7	481.5	S147	183	−2072.7	−481.5
S53	85	1621.7	481.5	S148	184	−2018.7	−481.5
S54	86	1567.7	481.5	S149	185	−1964.7	−481.5
S55	87	1513.7	481.5	S150	186	−1910.7	−481.5
S56	88	1459.7	481.5	S151	187	−1856.7	−481.5
S57	89	1405.7	481.5	S152	188	−1802.7	−481.5
S58	90	1351.7	481.5	S153	189	−1748.7	−481.5
S59	91	1297.7	481.5	S154	190	−1694.7	−481.5
S60	92	1243.7	481.5	S155	191	−1640.7	−481.5
S61	93	1189.7	481.5	S156	192	−1586.7	−481.5
S62	94	1135.7	481.5	S157	193	−1532.7	−481.5
S63	95	1081.7	481.5	S158	194	−1478.7	−481.5
S64	96	1027.7	481.5	S159	195	−1424.7	−481.5
S65	97	973.7	481.5	BP3	196	−1370.7	−481.5
S66	98	858.2	481.5	BP1	197	−1316.7	−481.5
S67	99	804.2	481.5	-	-	-	-

The dummy bumps are connected to the pins shown in Table 21, but are not tested.

Table 21.   Dummy bumps
All x/y coordinates represent the position of the center of each bump with respect to the center (x/y = 0) of the chip; see Figure 26.

Symbol	Connected to pin	X (μm)	Y (μm)
D1	S131	−3079.2	−481.5
D2	S28	3065.9	−481.5
D3	S29	3121.7	481.5
D4	S130	−3094.7	481.5

The alignment marks are shown in Table 22.

Table 22.   Alignment marks
All x/y coordinates represent the position of the REF point (see Figure 27) with respect to the center (x/y = 0) of the chip; see Figure 26.

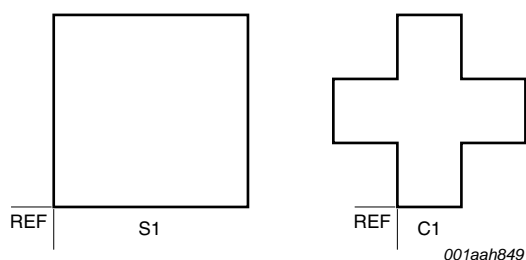| Symbol	Size (μm)	X (μm)	Y (μm)
S1	121.5 × 121.5	−2733.75	−47.25
C1	121.5 × 121.5	2603.7	−47.25

Fig 27. Alignment marks

14. Packing information

Table 23.   Tray dimensions
Tray details are shown in Figure 28.

Symbol	Description	Value
A	pocket pitch in x direction	8.8 mm
B	pocket pitch in y direction	3.6 mm
C	pocket width in x direction	6.65 mm
D	pocket width in y direction	1.31 mm
E	tray width in x direction	50.8 mm
F	tray width in y direction	50.8 mm
x	number of pockets, x direction	5
y	number of pockets, y direction	12
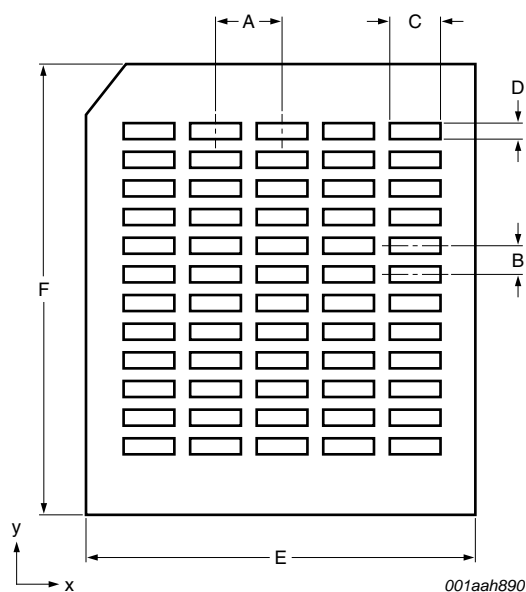
Fig 28. Tray details
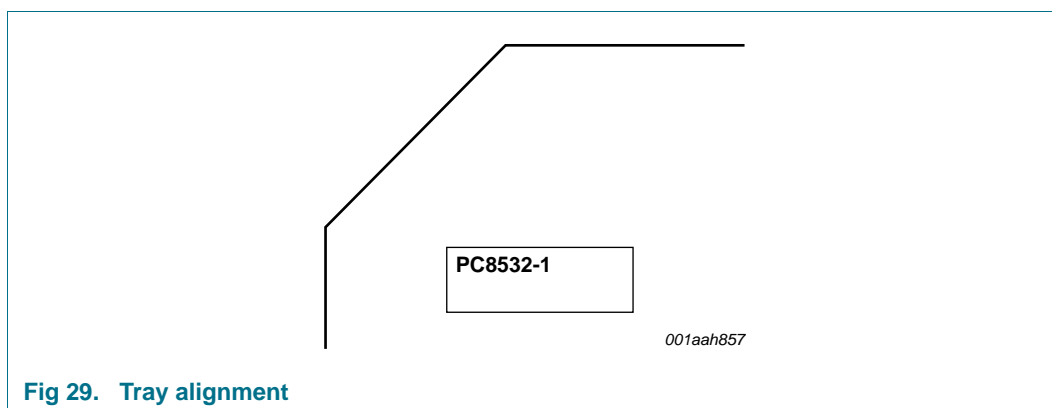
Fig 29. Tray alignment

15. Abbreviations

Table 24. Abbreviations

Acronym	Description
CMOS	Complementary Metal Oxide Semiconductor
COG	Chip-On-Glass
HBM	Human Body Model
I^{2}C	Inter-Integrated Circuit
ITO	Indium Tin Oxide
LCD	Liquid Crystal Display
LSB	Least Significant Bit
MM	Machine Model
MSB	Most Significant Bit
RAM	Random Access Memory
RMS	Root Mean Square

16. References

[1]   **AN10170 —** Design guidelines for COG modules with NXP monochrome LCD drivers

[2]   **AN10706 —** Handling bare die

[3]   **AN10853 —** ESD and EMC sensitivity of IC

[4]   **IEC 60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[5]   **IEC 61340-5 —** Protection of electronic devices from electrostatic phenomena

[6]   **JESD22-A114 —** Electrostatic Discharge (ESD) Sensitivity Testing Human Body Model (HBM)

[7]   **JESD22-A115 —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[8]   **JESD78 —** IC Latch-Up Test

[9]   **JESD625-A —** Requirements for Handling Electrostatic-Discharge-Sensitive (ESDS) Devices

[10] **NX3-00092 —** NXP store and transport requirements

[11] **UM10204 —** I^2C-bus specification and user manual

17. Revision history

Table 25. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCF8532 v.2	20110210	Product data sheet	-	PCF8532_1

Modifications:		• Corrected drawings of Figure 2 and Figure 26
		 • Added table note to Table 9
		 • Corrected LCD voltage equations
		 • Reworked sections
		   – Display RAM
		   – Data pointer
		   – Subaddress counter
		   – Output bank selector
		   – Input bank selector		

PCF8532_1	20090210	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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20. Contents