

1. Overview

The M32C/80 Group microcomputer is a single-chip control unit that utilizes high-performance silicon gate CMOS technology with the M32C/80 series CPU core. The M32C/80 Group is available in 100-pin plastic molded LQFP/QFP package.

With a 16-Mbyte address space, this microcomputer combines advanced instruction manipulation capabilities to process complex instructions by less bytes and execute instructions at higher speed.

It incorporates a multiplier and DMAC adequate for office automation, communication devices and industrial equipments and other high-speed processing applications.

The M32C/80 Group is ROMless device.
Use the M32C/80 Group in microprocessor mode after reset.

1.1 Applications

Audio, cameras, office equipment, communications equipment, portable equipment, etc.

1.2 Performance Overview

Table 1.1 lists performance overview of the M32C/80 Group.

Table 1.1 M32C/80 Group Performance

Item		Performance
CPU	Basic Instructions	108 instructions
	Minimum Instruction Execution Time	31.3 ns (f(BCLK)=32 MHz, Vcc1=4.2 to 5.5 V) 41.7 ns (f(BCLK)=24 MHz, Vcc1=3.0 to 5.5 V)
	Operating Mode	Single-chip mode, Memory expansion mode, Microprocessor mode
	Memory Space	16 Mbytes
	Memory Capacity	See Table 1.2
Peripheral function	I/O Port	47 I/O pins (when using 16-bit bus) and 1 input pin
	Multifunction Timer	Timer A: 16 bits x 5 channels, Timer B: 16 bits x 6 channels Three-phase motor control circuit
	Intelligent I/O Communication Function	2 channels
	Serial I/O	5 channels Clock synchronous serial I/O, Clock asynchronous serial I/O, IEBus ⁽¹⁾ , I ² C Bus ⁽²⁾
	A/D Converter	10-bit A/D converter: 1 circuit, 10 channels
	D/A Converter	8 bits x 2 channels
	DMAC	4 channels
	DMAC II	Can be activated by all peripheral function interrupt sources Immediate transfer, operation and chain transfer function
	CRC Calculation Circuit	CRC-CCITT
	X/Y Converter	16 bits x 16 bits
	Watchdog Timer	15 bits x 1 channel (with prescaler)
	Interrupt	34 internal sources and 8 external sources, 5 software sources Interrupt priority level: 7
	Clock Generation Circuit	4 circuits Main Clock oscillation circuit (*), Sub clock oscillation circuit (*), On-chip oscillator, PLL frequency synthesizer (*)Equipped with a built-in feedback resistor
Electrical Characteristics	Supply Voltage	Vcc1=4.2 to 5.5 V, Vcc2=3.0 to Vcc1 (f(BCLK)=32 MHz) Vcc1=3.0 to 5.5 V, Vcc2=3.0 to Vcc1 (f(BCLK)=24 MHz)
	Power Consumption	22 mA (Vcc1=Vcc2=5 V, f(BCLK)=32 MHz) 17 mA (Vcc1=Vcc2=3.3 V, f(BCLK)=24 MHz) 10 μA (Vcc1=Vcc2=3.3 V, f(BCLK)=32 kHz, in wait mode)
Operating Ambient Temperature		–20 to 85°C, –40 to 85°C(optional)
Package		100-pin plastic molded LQFP/QFP

NOTES:

1. IEBus is a trademark of NEC Electronics Corporation.
2. I²C bus is a trademark of Koninklijke Philips Electronics N. V.

All options are on a request basis.

1.3 Block Diagram

Figure 1.1 shows a block diagram of the M32C/80 Group microcomputer.

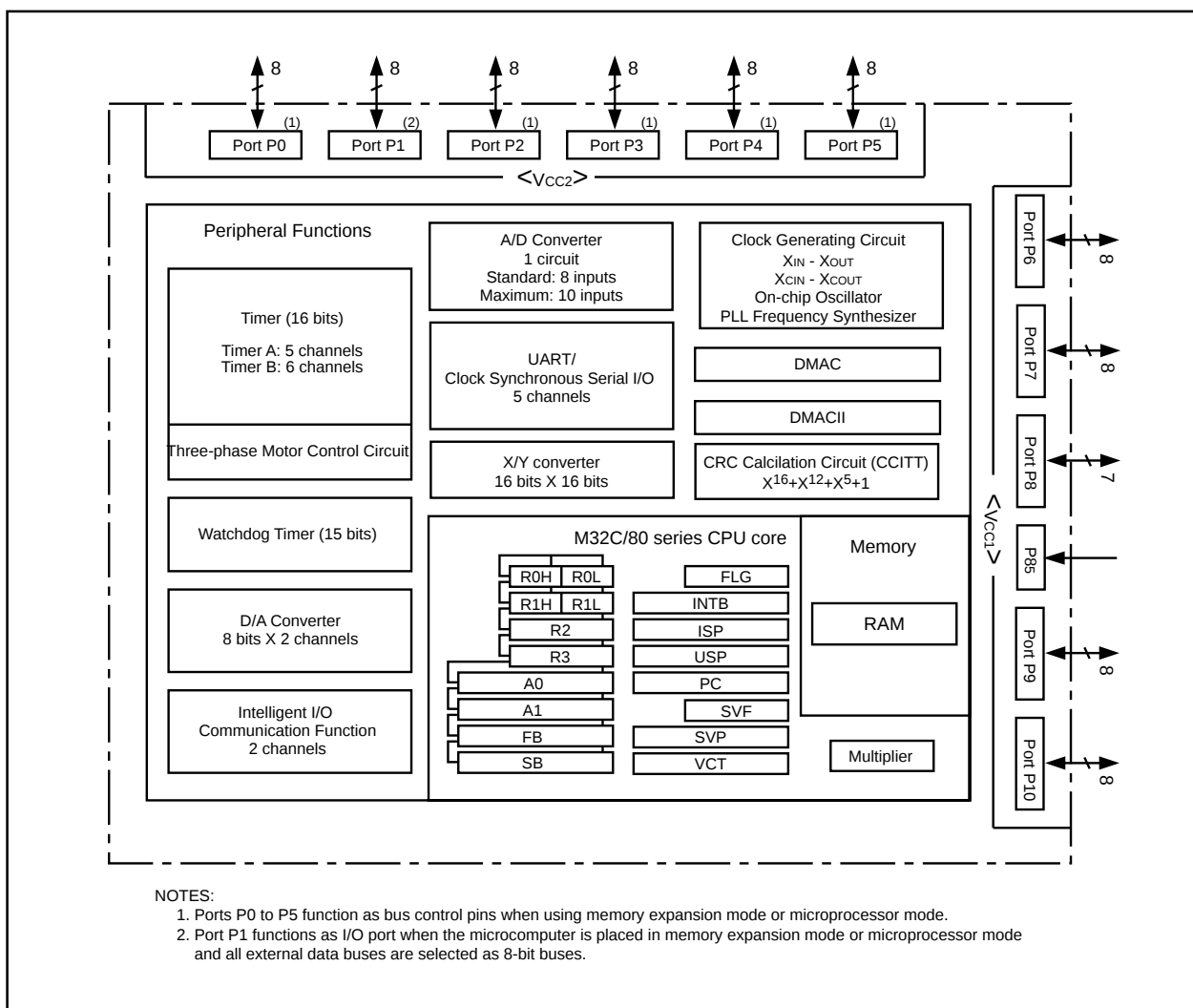


Figure 1.1 M32C/80 Group Block Diagram

1.4 Product Information

Table 1.2 lists the product information. Figure 1.2 shows the product numbering system.

Table 1.2 M32C/80 Group

As of November, 2005

Type Number	Package Type	ROM Capacity	RAM Capacity	Remarks
M30800SAGP	PLQP0100KB-A (100P6Q-A)	—	8K	ROMless
M30800SAFP	PRQP0100JB-A (100P6S-A)			
M30800SAGP-BL	PLQP0100KB-A (100P6Q-A)			ROMless with on-chip boot loader
M30800SAFP-BL	PRQP0100JB-A (100P6S-A)			

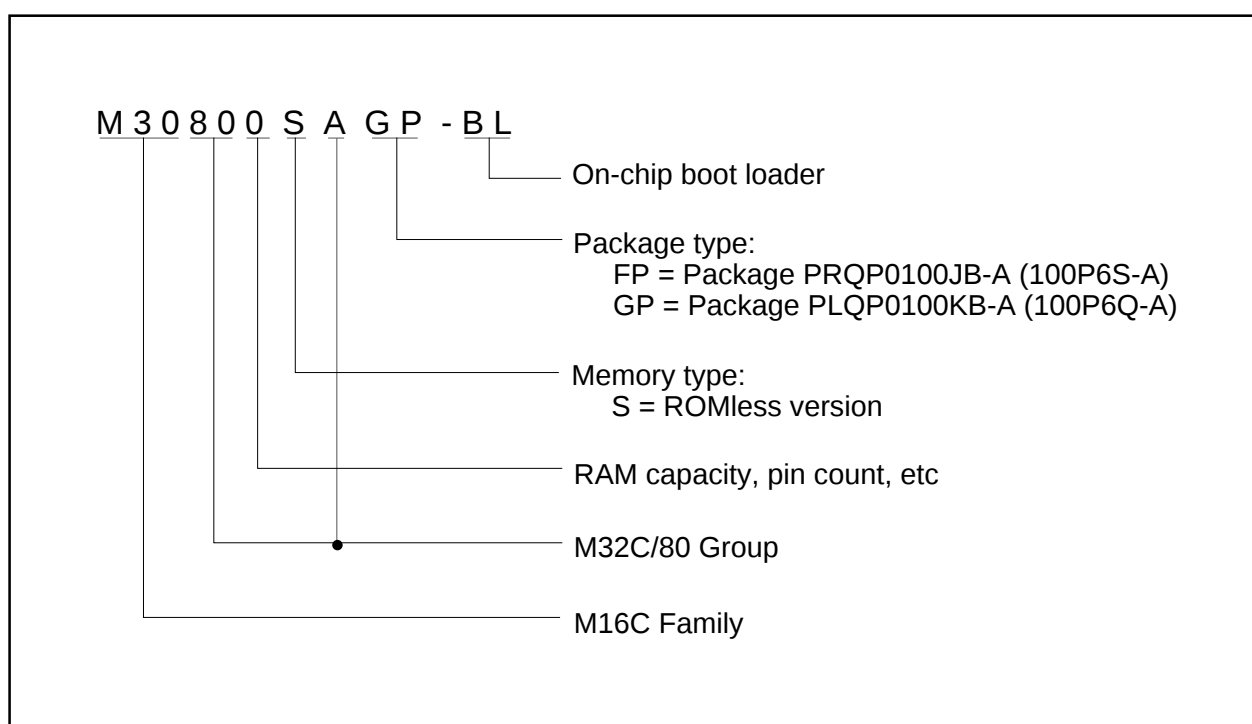


Figure 1.2 Product Numbering System

1.5 Pin Assignment

Figures 1.3 and 1.4 show pin assignments (top view).

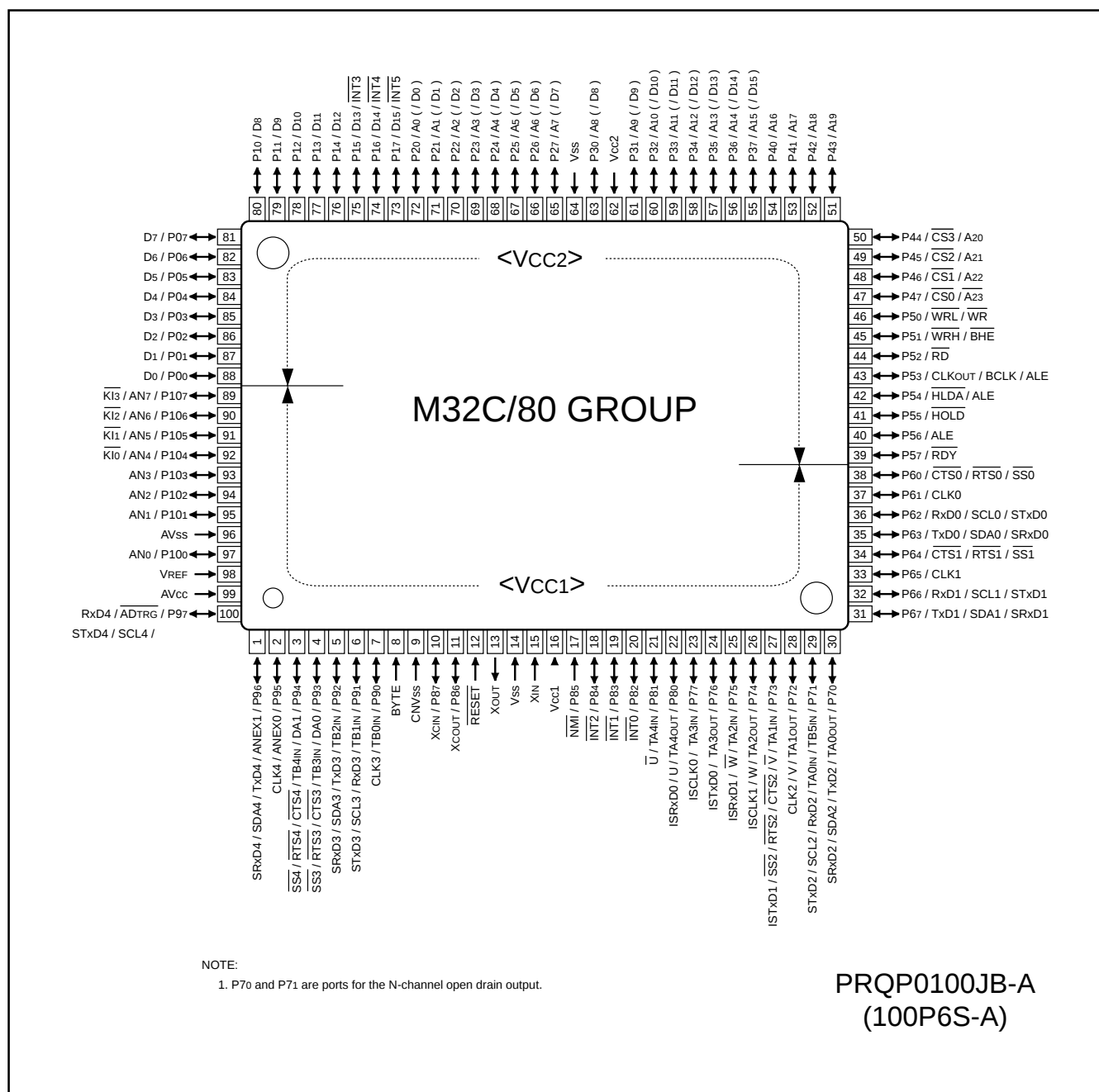


Figure 1.3 Pin Assignment

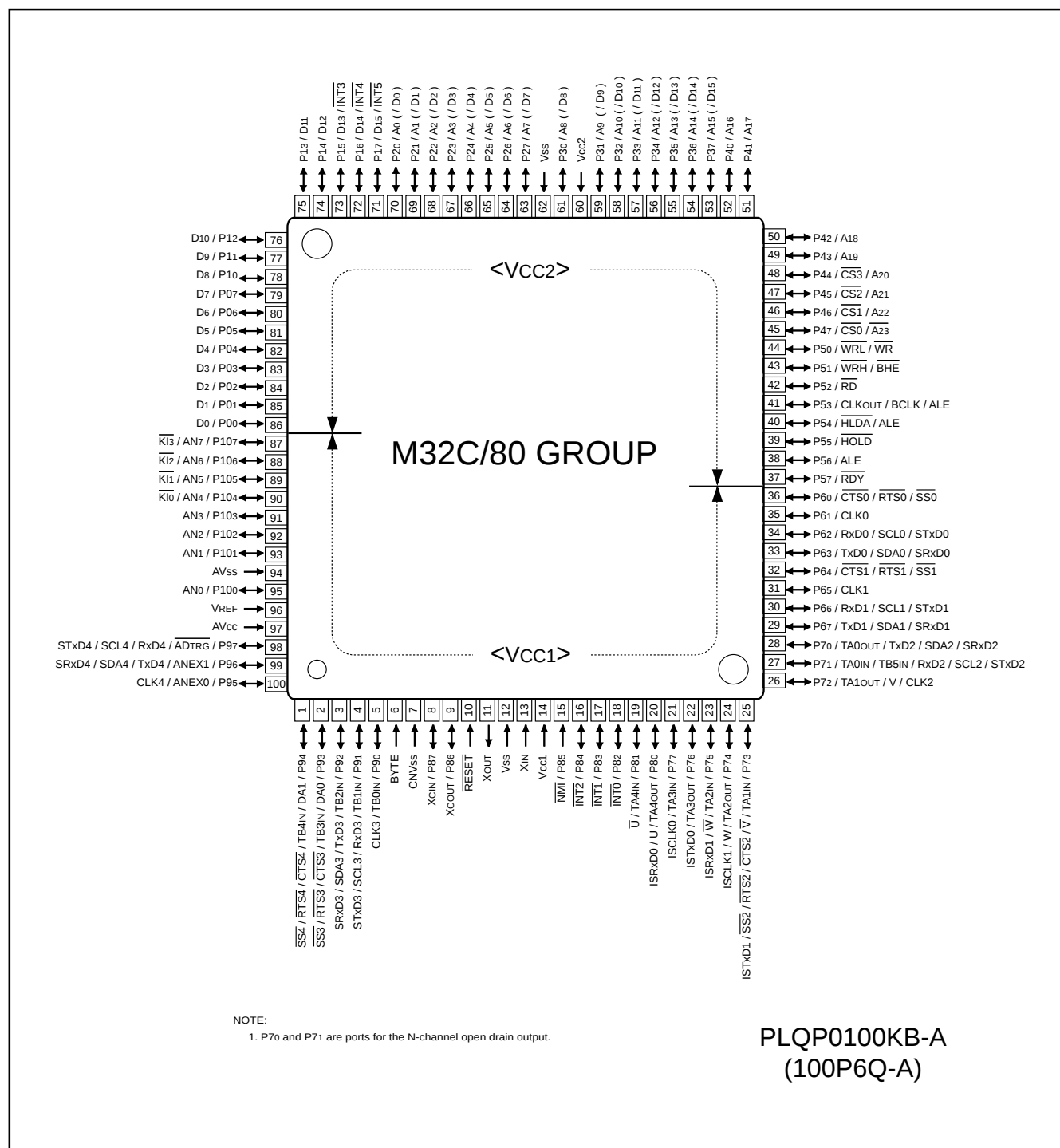


Figure 1.4 Pin Assignment

Table 1.3 Pin Characteristics

Package Pin No		Control pins	Port	Interrupt pins	Timer pins	UART pins	Analog pins	Bus control pins	Intelligent I/O pins
FP	GP								
1	99		P96			TxD4/SDA4/SRxD4	ANEX1		
2	100		P95			CLK4	ANEX0		
3	1		P94		TB4IN	CTS4/RTS4/SS4	DA1		
4	2		P93		TB3IN	CTS3/RTS3/SS3	DA0		
5	3		P92		TB2IN	TxD3/SDA3/SRxD3			
6	4		P91		TB1IN	RxD3/SCL3/STxD3			
7	5		P90		TB0IN	CLK3			
8	6	BYTE							
9	7	CNV _{SS}							
10	8	X _{CIN}	P87						
11	9	X _{COUT}	P86						
12	10	RESET							
13	11	X _{OUT}							
14	12	V _{SS}							
15	13	X _{IN}							
16	14	V _{CC1}							
17	15		P85	NMI					
18	16		P84	INT2					
19	17		P83	INT1					
20	18		P82	INT0					
21	19		P81		TA4IN/ $\bar{U}$				
22	20		P80		TA4OUT/U				ISRxD0
23	21		P77		TA3IN				ISCLK0
24	22		P76		TA3OUT				ISTxD0
25	23		P75		TA2IN/ $\bar{W}$				ISRxD1
26	24		P74		TA2OUT/W				ISCLK1
27	25		P73		TA1IN/ $\bar{V}$	CTS2/RTS2/SS2			ISTxD1
28	26		P72		TA1OUT/V	CLK2			
29	27		P71		TB5IN/TA0IN	RxD2/SCL2/STxD2			
30	28		P70		TA0OUT	TxD2/SDA2/SRxD2			
31	29		P67			TxD1/SDA1/SRxD1			
32	30		P66			RxD1/SCL1/STxD1			
33	31		P65			CLK1			
34	32		P64			CTS1/RTS1/SS1			
35	33		P63			TxD0/SDA0/SRxD0			
36	34		P62			RxD0/SCL0/STxD0			
37	35		P61			CLK0			
38	36		P60			CTS0/RTS0/SS0			
39	37		P57					RDY	
40	38		P56					ALE	
41	39		P55					HOLD	
42	40		P54					HLDA/ALE	
43	41		P53					CLKout/BCLK/ALE	
44	42		P52					RD	
45	43		P51					WRH/BHE	
46	44		P50					WRL/WR	
47	45		P47					CS0/A23	
48	46		P46					CS1/A22	
49	47		P45					CS2/A21	
50	48		P44					CS3/A20	

Table 1.3 Pin Characteristics (Continued)

Package pin No		Control pins	Port	Interrupt pins	Timer pins	UART pins	Analog pins	Bus control pins	Intelligent I/O pins
FP	GP								
51	49		P43					A19	
52	50		P42					A18	
53	51		P41					A17	
54	52		P40					A16	
55	53		P37					A15(/D15)	
56	54		P36					A14(/D14)	
57	55		P35					A13(/D13)	
58	56		P34					A12(/D12)	
59	57		P33					A11(/D11)	
60	58		P32					A10(/D10)	
61	59		P31					A9(/D9)	
62	60	VCC2							
63	61		P30					A8(/D8)	
64	62	VSS							
65	63		P27					A7(/D7)	
66	64		P26					A6(/D6)	
67	65		P25					A5(/D5)	
68	66		P24					A4(/D4)	
69	67		P23					A3(/D3)	
70	68		P22					A2(/D2)	
71	69		P21					A1(/D1)	
72	70		P20					A0(/D0)	
73	71		P17	INT5				D15	
74	72		P16	INT4				D14	
75	73		P15	INT3				D13	
76	74		P14					D12	
77	75		P13					D11	
78	76		P12					D10	
79	77		P11					D9	
80	78		P10					D8	
81	79		P07					D7	
82	80		P06					D6	
83	81		P05					D5	
84	82		P04					D4	
85	83		P03					D3	
86	84		P02					D2	
87	85		P01					D1	
88	86		P00					D0	
89	87		P107	KI3			AN7		
90	88		P106	KI2			AN6		
91	89		P105	KI1			AN5		
92	90		P104	KI0			AN4		
93	91		P103				AN3		
94	92		P102				AN2		
95	93		P101				AN1		
96	94	AVSS							
97	95		P100				AN0		
98	96						VREF		
99	97	AVCC							
100	98		P97			RxD4/SCL4/STxD4	ADTRG		

1.6 Pin Description

Table 1.4 Pin Description

Signal name	Pin name	I/O type	Supply voltage	Description
Power supply	VCC1, VCC2 VSS	I	-	Apply 3.0 to 5.5 V to both VCC1 and VCC2 pins. Apply 0 V to the VSS pin. $V_{CC1} \geq V_{CC2}^{(1)}$
Analog power supply input	AVCC AVSS	I	VCC1	Supplies power for the A/D converter. Connect the AVCC pin to VCC1 and the AVSS pin to VSS
Reset input	RESET	I	VCC1	The microcomputer is in a reset state when "L" is applied to the RESET pin
CNVss	CNVss	I	VCC1	Connect this pin to VCC1
External data bus width select input	BYTE	I	VCC1	Switches the data bus in external memory space 3. The data bus is 16 bits long when the this pin is held "L" and 8 bits long when the this pin is held "H". Set it to either one.
Bus control pins	D0 to D7	I/O	VCC2	Inputs and outputs data (D0 to D7) while accessing an external memory space with separate bus
	D8 to D15	I/O	VCC2	Inputs and outputs data (D8 to D15) while accessing an external memory space with 16-bit separate bus
	A0 to A22	O	VCC2	Outputs address bits (A0 to A22)
	A23	O	VCC2	Outputs inversed address bit A23
	A0/D0 to A7/D7	I/O	VCC2	Inputs and outputs data (D0 to D7) and outputs 8 low-order address bits (A0 to A7) by time-sharing while accessing an external memory space with multiplexed bus
	A8/D8 to A15/D15	I/O	VCC2	Inputs and outputs data (D8 to D15) and outputs 8 middle-order address bits (A8 to A15) by time-sharing while accessing an external memory space with multiplexed bus
	CS0 to CS3	O	VCC2	Output CS0 to CS3 that are chip-select signals specifying an external space
	WRL/WR WRH/BHE RD	O	VCC2	Outputs WRL, WRH, (WR, BHE) and RD signals. WRL and WRH can be switched with WR and BHE by program ■ WRL, WRH and RD are selected: If external data bus is 16 bits wide, data is writtenn to an even address when WRL is held "L". Data is written to an odd address when WRH is held "L". Data is read when RD is held "L". ■ WR, BHE and RD are selected Data is written to external memory space when WR is held "L". Data is read when RD is held "L". An odd address is accessed when BHE is held "L". Select WR, BHE and RD for an external 8-bit data bus
	ALE	O	VCC2	ALE is a signal latching address
	HOLD	I	VCC2	The microcomputer is placed in a hold state while the HOLD pin is held "L"
	HLDA	O	VCC2	Outputs an "L" signal while the microcomputer is placed in a hold state
	RDY	I	VCC2	Bus is placed in a wait state while the RDY pin is held "L"

I: Input O: Output I/O: Input and output

NOTE:

1. In this manual, hereafter, Vcc refers to VCC1 unless otherwise noted.

Table 1.4 Pin Description (Continued)

Signal name	Pin name	I/O type	Supply voltage	Description
Main clock input	XIN	I	VCC1	I/O pins for the main clock generation circuit. Connect a ceramic resonator or crystal oscillator between XIN and XOUT. To apply external clock, input the clock from XIN and leave XOUT open
Main clock output	XOUT	O	VCC1	
Sub clock input	XCIN	I	VCC1	I/O pins for a sub clock oscillation circuit. Connect a crystal oscillator between XCIN and XCOUT. To apply external clock, input the clock from XCIN and leave XCOUT open
Sub clock output	XCOUT	O	VCC1	
BCLK output	BCLK	O	VCC2	Outputs BCLK signal
Clock output	CLKOUT	O	VCC2	Outputs clock having the same frequency as fc, f8, or f32
INT interrupt input	INT0 to INT2	I	VCC1	Input pins for the INT interrupt
	INT3 to INT5		VCC2	
NMI interrupt input	NMI	I	VCC1	Input pin for the NMI interrupt
Key input interrupt	KI0 to KI3	I	VCC1	Input pins for the key input interrupt
Timer A	TA0OUT to TA4OUT	I/O	VCC1	I/O pins for the timer A0 to A4 (TA0OUT is a pin for the N-channel open drain output.)
	TA0IN to TA4IN	I	VCC1	Input pins for the timer A0 to A4
Timer B	TB0IN to TB5IN	I	VCC1	Input pins for the timer B0 to B5
Three-phase motor control output	U, $\bar{U}$, V, $\bar{V}$, W, $\bar{W}$	O	VCC1	output pins for the three-phase motor control timer
Serial I/O	CTS0 to CTS4	I	VCC1	Input pins for data transmission control
	RTS0 to RTS4	O	VCC1	Output pins for data reception control
	CLK0 to CLK4	I/O	VCC1	Inputs and outputs the transfer clock
	RxD0 to RxD4	I	VCC1	Inputs serial data
	TxD0 to TxD4	O	VCC1	Outputs serial data (TxD2 is a pin for the N-channel open drain output.)
I ² C mode	SDA0 to SDA4	I/O	VCC1	Inputs and outputs serial data (SDA2 is a pin for the N-channel open drain output.)
	SCL0 to SCL4	I/O	VCC1	Inputs and outputs the transfer clock (SCL2 is a pin for the N-channel open drain output.)
Serial I/O special function	STxD0 to STxD4	I	VCC1	Outputs serial data when slave mode is selected (SDA2 is a pin for the N-channel open drain output.)
	SRxD0 to SRxD4	I	VCC1	Inputs serial data when slave mode is selected
	SS0 to SS4	I	VCC1	Input pins to control serial I/O special function

I: Input O: Output I/O: Input and output

Table 1.5 Pin Description (Continued)

Signal name	Pin name	I/O type	Supply voltage	Description
Reference voltage input	VREF	I	-	Applies reference voltage for the A/D converter and D/A converter
A/D converter	AN0 to AN7	I	VCC1	Analog input pins for the A/D converter
	ADTRG	I	VCC1	Input pin for an external A/D trigger
	ANEX0	I/O	VCC1	Extended analog input pin for the A/D converter and output pin in external op-amp connection mode
	ANEX1	I	VCC1	Extended analog input pin for the A/D converter
D/A converter	DA0, DA1	O	VCC1	Output pin for the D/A converter
Intelligent I/O communication function	ISCLK0	I/O	VCC1	Inputs and outputs clock for the intelligent I/O communication function
	ISCLK1			
	ISTxD0	O	VCC1	Outputs data for the intelligent I/O communication function
	ISTxD1			
	ISRxD0	I	VCC1	Inputs data for the intelligent I/O communication function
	ISRxD1			
I/O port	P00 to P07 ⁽¹⁾ P10 to P17 ⁽²⁾ P20 to P27 ⁽¹⁾ P30 to P37 ⁽¹⁾ P40 to P47 ⁽¹⁾ P50 to P57 ⁽¹⁾	I/O	VCC2	I/O ports for CMOS. Each port can be programmed for input or output under the control of the direction register. An input port can be set, by program, for a pull-up resistor available or for no pull-up resistor available in 4-bit units
	P60 to P67 P70 to P77 P90 to P97 P100 to P107	I/O	VCC1	I/O ports having equivalent functions to P0 (P70 and P71 are ports for the N-channel open drain output.)
	P80 to P84, P86, P87	I/O	VCC1	I/O ports having equivalent functions to P0
	P85	I	VCC1	Shares a pin with $\overline{\text{NMI}}$. $\overline{\text{NMI}}$ input state can be got by reading P85

I: Input O: Output I/O: Input and output

NOTES:

1. Ports P0 to P5 function as bus control pins when using memory expansion mode or microprocessor mode. They cannot be used as I/O ports.
2. Port P1 functions as I/O port when the microcomputer is placed in memory expansion mode or microprocessor mode and all external data buses are selected as 8-bit buses.

2. Central Processing Unit (CPU)

Figure 2.1 shows the CPU registers.

The register bank is comprised of 8 registers (R0, R1, R2, R3, A0, A1, SB and FB) out of 28 CPU registers. Two sets of register banks are provided.

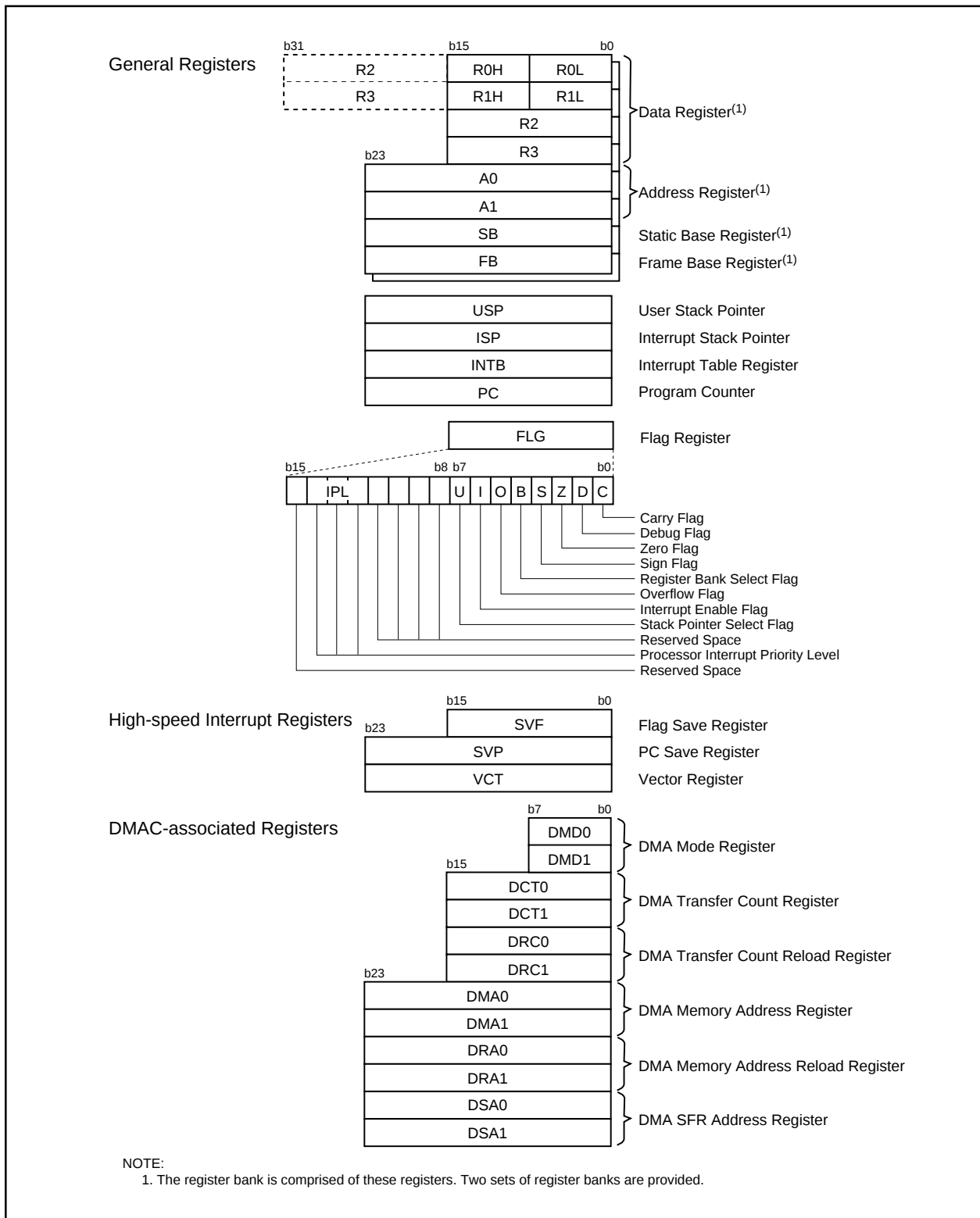


Figure 2.1 CPU Register

2.1 General Registers

2.1.1 Data Registers (R0, R1, R2 and R3)

R0, R1, R2 and R3 are 16-bit registers for transfer, arithmetic and logic operations. R0 and R1 can be split into high-order bits (R0H) and low-order bits (R0L) to be used separately as 8-bit data registers. R0 can be combined with R2 to be used as a 32-bit data register (R2R0). The same applies to R1 and R3.

2.1.2 Address Registers (A0 and A1)

A0 and A1 are 24-bit registers for A0-/A1-indirect addressing, A0-/A1-relative addressing, transfer, arithmetic and logic operations.

2.1.3 Static Base Register (SB)

SB is a 24-bit register for SB-relative addressing.

2.1.4 Frame Base Register (FB)

FB is a 24-bit register for FB-relative addressing.

2.1.5 Program Counter (PC)

PC, 24 bits wide, indicates the address of an instruction to be executed.

2.1.6 Interrupt Table Register (INTB)

INTB is a 24-bit register indicating the starting address of an relocatable interrupt vector table.

2.1.7 User Stack Pointer (USP), Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are 24 bits wide each. The U flag is used to switch between USP and ISP. Refer to **2.1.8 Flag Register (FLG)** for details on the U flag. Set USP and ISP to even addresses to execute an interrupt sequence efficiently.

2.1.8 Flag Register (FLG)

FLG is a 16-bit register indicating a CPU state.

2.1.8.1 Carry Flag (C)

The C flag indicates whether carry or borrow has occurred after executing an instruction.

2.1.8.2 Debug Flag (D)

The D flag is for debug only. Set to "0".

2.1.8.3 Zero Flag (Z)

The Z flag is set to "1" when the value of zero is obtained from an arithmetic operation; otherwise "0".

2.1.8.4 Sign Flag (S)

The S flag is set to "1" when a negative value is obtained from an arithmetic operation; otherwise "0".

2.1.8.5 Register Bank Select Flag (B)

The register bank 0 is selected when the B flag is set to "0". The register bank 1 is selected when this flag is set to "1".

2.1.8.6 Overflow Flag (O)

The O flag is set to "1" when the result of an arithmetic operation overflows; otherwise "0".

2.1.8.7 Interrupt Enable Flag (I)

The I flag enables a maskable interrupt.

Interrupt is disabled when the I flag is set to "0" and enabled when the I flag is set to "1". The I flag is set to "0" when an interrupt is acknowledged.

2.1.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is set to "0". USP is selected when this flag is set to "1".

The U flag is set to "0" when a hardware interrupt is acknowledged or the INT instruction of software interrupt numbers 0 to 31 is executed.

2.1.8.9 Processor Interrupt Priority Level (IPL)

IPL, 3 bits wide, assigns processor interrupt priority levels from level 0 to level 7.

If a requested interrupt has greater priority than IPL, the interrupt is enabled.

2.1.8.10 Reserved Space

When writing to a reserved space, set to "0". When reading, its content is indeterminate.

2.2 High-Speed Interrupt Registers

Registers associated with the high-speed interrupt are as follows:

- Flag save register (SVF)
- PC save register (SVP)
- Vector register (VCT)

2.3 DMAC-Associated Registers

Registers associated with DMAC are as follows:

- DMA mode register (DMD0, DMD1)
- DMA transfer count register (DCT0, DCT1)
- DMA transfer count reload register (DRC0, DRC1)
- DMA memory address register (DMA0, DMA1)
- DMA SFR address register (DSA0, DSA1)
- DMA memory address reload register (DRA0, DRA1)

3. Memory

Figure 3.1 shows a memory map of the M32C/80 Group.

The M32C/80 Group provides 16-Mbyte address space addressed from 000000₁₆ to FFFFFFF₁₆.

The fixed interrupt vectors are allocated from address FFFFD₁₆ to FFFFFFF₁₆. It stores the starting address of each interrupt routine.

The internal RAM is allocated from address 000400₁₆ to higher. For example, a 8-Kbyte internal RAM is allocated from address 000400₁₆ to 0023FF₁₆. Besides storing data, it becomes stacks when the subroutine is called or an interrupt is acknowledged.

SFRs, consisting of control registers for peripheral functions such as I/O port, A/D converter, serial I/O, timers, is allocated from address 000000₁₆ to 0003FF₁₆. All blank spaces within SFRs are reserved and cannot be accessed by users.

The special page vector table is addressed from FFFE00₁₆ to FFFFD₁₆. It is used for the JMPS instruction and JSRS instruction. Refer to the Renesas publication **M32C/80 Series Software Manual** for details. In microprocessor mode, some spaces are reserved and cannot be accessed by users.

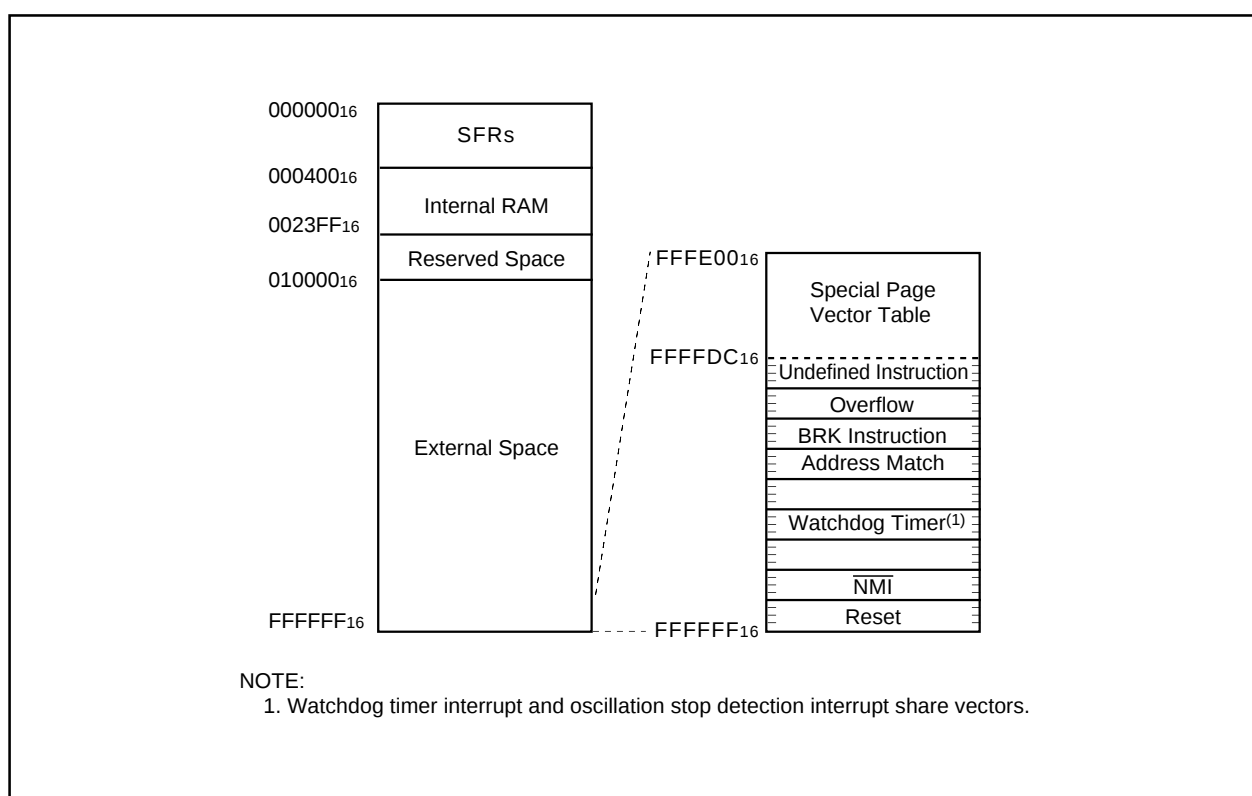


Figure 3.1 Memory Map

4. Special Function Registers (SFRs)

Address	Register	Symbol	Value after RESET
0000 ₁₆			
0001 ₁₆			
0002 ₁₆			
0003 ₁₆			
0004 ₁₆	Processor Mode Register ⁽¹⁾	PM0	0000 0011 ₂ (CNVss pin ="H")
0005 ₁₆	Processor Mode Register 1	PM1	00 ₁₆
0006 ₁₆	System Clock Control Register 0	CM0	0000 1000 ₂
0007 ₁₆	System Clock Control Register 1	CM1	0010 0000 ₂
0008 ₁₆			
0009 ₁₆	Address Match Interrupt Enable Register	AIER	00 ₁₆
000A ₁₆	Protect Register	PRCR	XXXX 0000 ₂
000B ₁₆	External Data Bus Width Control Register	DS	XXXX 1000 ₂ (BYTE pin ="L") XXXX 0000 ₂ (BYTE pin ="H")
000C ₁₆	Main Clock Division Register	MCD	XXX0 1000 ₂
000D ₁₆	Oscillation Stop Detection Register	CM2	00 ₁₆
000E ₁₆	Watchdog Timer Start Register	WDTS	XX ₁₆
000F ₁₆	Watchdog Timer Control Register	WDC	000X XXXX ₂
0010 ₁₆			
0011 ₁₆	Address Match Interrupt Register 0	RMAD0	000000 ₁₆
0012 ₁₆			
0013 ₁₆	Processor Mode Register 2	PM2	00 ₁₆
0014 ₁₆			
0015 ₁₆	Address Match Interrupt Register 1	RMAD1	000000 ₁₆
0016 ₁₆			
0017 ₁₆			
0018 ₁₆			
0019 ₁₆	Address Match Interrupt Register 2	RMAD2	000000 ₁₆
001A ₁₆			
001B ₁₆			
001C ₁₆			
001D ₁₆	Address Match Interrupt Register 3	RMAD3	000000 ₁₆
001E ₁₆			
001F ₁₆			
0020 ₁₆			
0021 ₁₆			
0022 ₁₆			
0023 ₁₆			
0024 ₁₆			
0025 ₁₆			
0026 ₁₆	PLL Control Register 0	PLC0	0001 X010 ₂
0027 ₁₆	PLL Control Register 1	PLC1	000X 0000 ₂
0028 ₁₆			
0029 ₁₆	Address Match Interrupt Register 4	RMAD4	000000 ₁₆
002A ₁₆			
002B ₁₆			
002C ₁₆			
002D ₁₆	Address Match Interrupt Register 5	RMAD5	000000 ₁₆
002E ₁₆			
002F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. The PM01 and PM00 bits in the PM0 register maintain values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0030 ₁₆			
0031 ₁₆			
0032 ₁₆			
0033 ₁₆			
0034 ₁₆			
0035 ₁₆			
0036 ₁₆			
0037 ₁₆			
0038 ₁₆ 0039 ₁₆ 003A ₁₆	Address Match Interrupt Register 6	RMAD6	000000 ₁₆
003B ₁₆			
003C ₁₆ 003D ₁₆ 003E ₁₆	Address Match Interrupt Register 7	RMAD7	000000 ₁₆
003F ₁₆			
0040 ₁₆			
0041 ₁₆			
0042 ₁₆			
0043 ₁₆			
0044 ₁₆			
0045 ₁₆			
0046 ₁₆			
0047 ₁₆			
0048 ₁₆	External Space Wait Control Register 0	EWCR0	X0X0 0011 ₂
0049 ₁₆	External Space Wait Control Register 1	EWCR1	X0X0 0011 ₂
004A ₁₆	External Space Wait Control Register 2	EWCR2	X0X0 0011 ₂
004B ₁₆	External Space Wait Control Register 3	EWCR3	X0X0 0011 ₂
004C ₁₆			
004D ₁₆			
004E ₁₆			
004F ₁₆			
0050 ₁₆			
0051 ₁₆			
0052 ₁₆			
0053 ₁₆			
0054 ₁₆			
0055 ₁₆			
0056 ₁₆			
0057 ₁₆			
0058 ₁₆			
0059 ₁₆			
005A ₁₆			
005B ₁₆			
005C ₁₆			
005D ₁₆			
005E ₁₆			
005F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
0060 ₁₆			
0061 ₁₆			
0062 ₁₆			
0063 ₁₆			
0064 ₁₆			
0065 ₁₆			
0066 ₁₆			
0067 ₁₆			
0068 ₁₆	DMA0 Interrupt Control Register	DM0IC	XXXX X000 ₂
0069 ₁₆	Timer B5 Interrupt Control Register	TB5IC	XXXX X000 ₂
006A ₁₆	DMA2 Interrupt Control Register	DM2IC	XXXX X000 ₂
006B ₁₆	UART2 Receive /ACK Interrupt Control Register	S2RIC	XXXX X000 ₂
006C ₁₆	Timer A0 Interrupt Control Register	TA0IC	XXXX X000 ₂
006D ₁₆	UART3 Receive /ACK Interrupt Control Register	S3RIC	XXXX X000 ₂
006E ₁₆	Timer A2 Interrupt Control Register	TA2IC	XXXX X000 ₂
006F ₁₆	UART4 Receive /ACK Interrupt Control Register	S4RIC	XXXX X000 ₂
0070 ₁₆	Timer A4 Interrupt Control Register	TA4IC	XXXX X000 ₂
0071 ₁₆	UART0/UART3 Bus Conflict Detect Interrupt Control Register	BCN0IC/BCN3IC	XXXX X000 ₂
0072 ₁₆	UART0 Receive/ACK Interrupt Control Register	S0RIC	XXXX X000 ₂
0073 ₁₆	A/D0 Conversion Interrupt Control Register	AD0IC	XXXX X000 ₂
0074 ₁₆	UART1 Receive/ACK Interrupt Control Register	S1RIC	XXXX X000 ₂
0075 ₁₆	Intelligent I/O Interrupt Control Register 0	IIO0IC	XXXX X000 ₂
0076 ₁₆	Timer B1 Interrupt Control Register	TB1IC	XXXX X000 ₂
0077 ₁₆	Intelligent I/O Interrupt Control Register 2	IIO2IC	XXXX X000 ₂
0078 ₁₆	Timer B3 Interrupt Control Register	TB3IC	XXXX X000 ₂
0079 ₁₆	Intelligent I/O Interrupt Control Register 4	IIO4IC	XXXX X000 ₂
007A ₁₆	INT5 Interrupt Control Register	INT5IC	XX00 X000 ₂
007B ₁₆			
007C ₁₆	INT3 Interrupt Control Register	INT3IC	XX00 X000 ₂
007D ₁₆			
007E ₁₆	INT1 Interrupt Control Register	INT1IC	XX00 X000 ₂
007F ₁₆			
0080 ₁₆			
0081 ₁₆			
0082 ₁₆			
0083 ₁₆			
0084 ₁₆			
0085 ₁₆			
0086 ₁₆			
0087 ₁₆			
0088 ₁₆	DMA1 Interrupt Control Register	DM1IC	XXXX X000 ₂
0089 ₁₆	UART2 Transmit /NACK Interrupt Control Register	S2TIC	XXXX X000 ₂
008A ₁₆	DMA3 Interrupt Control Register	DM3IC	XXXX X000 ₂
008B ₁₆	UART3 Transmit /NACK Interrupt Control Register	S3TIC	XXXX X000 ₂
008C ₁₆	Timer A1 Interrupt Control Register	TA1IC	XXXX X000 ₂
008D ₁₆	UART4 Transmit /NACK Interrupt Control Register	S4TIC	XXXX X000 ₂
008E ₁₆	Timer A3 Interrupt Control Register	TA3IC	XXXX X000 ₂
008F ₁₆	UART2 Bus Conflict Detect Interrupt Control Register	BCN2IC	XXXX X000 ₂

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0090 ₁₆	UART0 Transmit /NACK Interrupt Control Register	S0TIC	XXXX X000 ₂
0091 ₁₆	UART1/UART4 Bus Conflict Detect Interrupt Control Register	BCN1IC/BCN4IC	XXXX X000 ₂
0092 ₁₆	UART1 Transmit/NACK Interrupt Control Register	S1TIC	XXXX X000 ₂
0093 ₁₆	Key Input Interrupt Control Register	KUPIC	XXXX X000 ₂
0094 ₁₆	Timer B0 Interrupt Control Register	TB0IC	XXXX X000 ₂
0095 ₁₆	Intelligent I/O Interrupt Control Register 1	IIO1IC	XXXX X000 ₂
0096 ₁₆	Timer B2 Interrupt Control Register	TB2IC	XXXX X000 ₂
0097 ₁₆	Intelligent I/O Interrupt Control Register 3	IIO3IC	XXXX X000 ₂
0098 ₁₆	Timer B4 Interrupt Control Register	TB4IC	XXXX X000 ₂
0099 ₁₆			
009A ₁₆	INT4 Interrupt Control Register	INT4IC	XX00 X000 ₂
009B ₁₆			
009C ₁₆	INT2 Interrupt Control Register	INT2IC	XX00 X000 ₂
009D ₁₆			
009E ₁₆	INT0 Interrupt Control Register	INT0IC	XX00 X000 ₂
009F ₁₆	Exit Priority Control Register	RLVL	XXXX 0000 ₂
00A0 ₁₆	Interrupt Request Register 0	IIO0IR	0000 000X ₂
00A1 ₁₆	Interrupt Request Register 1	IIO1IR	0000 000X ₂
00A2 ₁₆	Interrupt Request Register 2	IIO2IR	0000 000X ₂
00A3 ₁₆	Interrupt Request Register 3	IIO3IR	0000 000X ₂
00A4 ₁₆	Interrupt Request Register 4	IIO4IR	0000 000X ₂
00A5 ₁₆			
00A6 ₁₆			
00A7 ₁₆			
00A8 ₁₆			
00A9 ₁₆			
00AA ₁₆			
00AB ₁₆			
00AC ₁₆			
00AD ₁₆			
00AE ₁₆			
00AF ₁₆			
00B0 ₁₆	Interrupt Enable Register 0	IIO0IE	00 ₁₆
00B1 ₁₆	Interrupt Enable Register 1	IIO1IE	00 ₁₆
00B2 ₁₆	Interrupt Enable Register 2	IIO2IE	00 ₁₆
00B3 ₁₆	Interrupt Enable Register 3	IIO3IE	00 ₁₆
00B4 ₁₆	Interrupt Enable Register 4	IIO4IE	00 ₁₆
00B5 ₁₆			
00B6 ₁₆			
00B7 ₁₆			
00B8 ₁₆			
00B9 ₁₆			
00BA ₁₆			
00BB ₁₆			
00BC ₁₆			
00BD ₁₆			
00BE ₁₆			
00BF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
00C0 ₁₆			
00C1 ₁₆			
00C2 ₁₆			
00C3 ₁₆			
00C4 ₁₆			
00C5 ₁₆			
00C6 ₁₆			
00C7 ₁₆			
00C8 ₁₆			
00C9 ₁₆			
00CA ₁₆			
00CB ₁₆			
00CC ₁₆			
00CD ₁₆			
00CE ₁₆			
00CF ₁₆			
00D0 ₁₆			
00D1 ₁₆			
00D2 ₁₆			
00D3 ₁₆			
00D4 ₁₆			
00D5 ₁₆			
00D6 ₁₆			
00D7 ₁₆			
00D8 ₁₆			
00D9 ₁₆			
00DA ₁₆			
00DB ₁₆			
00DC ₁₆			
00DD ₁₆			
00DE ₁₆			
00DF ₁₆			
00E0 ₁₆			
00E1 ₁₆			
00E2 ₁₆			
00E3 ₁₆			
00E4 ₁₆			
00E5 ₁₆			
00E6 ₁₆			
00E7 ₁₆			
00E8 ₁₆ 00E9 ₁₆	SI/O Receive Buffer Register 0	G0RB	XXXX XXXX ₂ XXX0 XXXX ₂
00EA ₁₆ 00EB ₁₆	Transmit Buffer/Receive Data Register 0	G0TB/G0DR	XX ₁₆
00EC ₁₆	Receive Input Register 0	G0RI	XX ₁₆
00ED ₁₆	SI/O Communication Mode Register 0	G0MR	00 ₁₆
00EE ₁₆	Transmit Output Register 0	G0TO	XX ₁₆
00EF ₁₆	SI/O Communication Control Register 0	G0CR	0000 X011 ₂

X: Indeterminate

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Address	Register	Symbol	Value after RESET
00F0 ₁₆	Data Compare Register 00	G0CMP0	XX ₁₆
00F1 ₁₆	Data Compare Register 01	G0CMP1	XX ₁₆
00F2 ₁₆	Data Compare Register 02	G0CMP2	XX ₁₆
00F3 ₁₆	Data Compare Register 03	G0CMP3	XX ₁₆
00F4 ₁₆	Data Mask Register 00	G0MSK0	XX ₁₆
00F5 ₁₆	Data Mask Register 01	G0MSK1	XX ₁₆
00F6 ₁₆	Communication Clock Select Register	CCS	XXXX 0000 ₂
00F7 ₁₆			
00F8 ₁₆	Receive CRC Code Register 0	G0RCRC	XX ₁₆
00F9 ₁₆			XX ₁₆
00FA ₁₆	Transmit CRC Code Register 0	G0TCRC	00 ₁₆
00FB ₁₆			00 ₁₆
00FC ₁₆	SI/O Expansion Mode Register 0	G0EMR	00 ₁₆
00FD ₁₆	SI/O Expansion Receive Control Register 0	G0ERC	00 ₁₆
00FE ₁₆	SI/O Special Communication Interrupt Detect Register 0	G0IRF	00 ₁₆
00FF ₁₆	SI/O Expansion Transmit Control Register 0	G0ETC	0000 0XXX ₂
0100 ₁₆			
0101 ₁₆			
0102 ₁₆			
0103 ₁₆			
0104 ₁₆			
0105 ₁₆			
0106 ₁₆			
0107 ₁₆			
0108 ₁₆			
0109 ₁₆			
010A ₁₆			
010B ₁₆			
010C ₁₆			
010D ₁₆			
010E ₁₆			
010F ₁₆			
0110 ₁₆			
0111 ₁₆			
0112 ₁₆			
0113 ₁₆			
0114 ₁₆			
0115 ₁₆			
0116 ₁₆			
0117 ₁₆			
0118 ₁₆			
0119 ₁₆			
011A ₁₆			
011B ₁₆			
011C ₁₆			
011D ₁₆			
011E ₁₆			
011F ₁₆			

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0120 ₁₆			
0121 ₁₆			
0122 ₁₆			
0123 ₁₆			
0124 ₁₆			
0125 ₁₆			
0126 ₁₆			
0127 ₁₆			
0128 ₁₆ 0129 ₁₆	SI/O Receive Buffer Register 1	G1RB	XXXX XXXX ₂ XXX0 XXXX ₂
012A ₁₆ 012B ₁₆	Transmit Buffer/Receive Data Register 1	G1TB/G1DR	XX ₁₆
012C ₁₆	Receive Input Register 1	G1RI	XX ₁₆
012D ₁₆	SI/O Communication Mode Register 1	G1MR	00 ₁₆
012E ₁₆	Transmit Output Register 1	G1TO	XX ₁₆
012F ₁₆	SI/O Communication Control Register 1	G1CR	0000 X011 ₂
0130 ₁₆	Data Compare Register 10	G1CMP0	XX ₁₆
0131 ₁₆	Data Compare Register 11	G1CMP1	XX ₁₆
0132 ₁₆	Data Compare Register 12	G1CMP2	XX ₁₆
0133 ₁₆	Data Compare Register 13	G1CMP3	XX ₁₆
0134 ₁₆	Data Mask Register 10	G1MSK0	XX ₁₆
0135 ₁₆	Data Mask Register 11	G1MSK1	XX ₁₆
0136 ₁₆			
0137 ₁₆			
0138 ₁₆ 0139 ₁₆	Receive CRC Code Register 1	G1RCRC	XX ₁₆ XX ₁₆
013A ₁₆ 013B ₁₆	Transmit CRC Code Register 1	G1TCRC	00 ₁₆ 00 ₁₆
013C ₁₆	SI/O Expansion Mode Register 1	G1EMR	00 ₁₆
013D ₁₆	SI/O Expansion Receive Control Register 1	G1ERC	00 ₁₆
013E ₁₆	SI/O Special Communication Interrupt Detection Register 1	G1IRF	00 ₁₆
013F ₁₆	SI/O Expansion Transmit Control Register 1	G1ETC	0000 0XXX ₂
0140 ₁₆			
0141 ₁₆			
0142 ₁₆			
0143 ₁₆			
0144 ₁₆			
0145 ₁₆			
0146 ₁₆			
0147 ₁₆			
0148 ₁₆			
0149 ₁₆			
014A ₁₆			
014B ₁₆			
014C ₁₆			
014D ₁₆ to 02AF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
02B1 ₁₆			
02B2 ₁₆			
02B3 ₁₆			
02B4 ₁₆			
02B5 ₁₆			
02B6 ₁₆			
02B7 ₁₆			
02B8 ₁₆			
02B9 ₁₆			
02BA ₁₆			
02BB ₁₆			
02BC ₁₆			
02BD ₁₆			
02BE ₁₆			
02BF ₁₆			
02C0 ₁₆ 02C1 ₁₆	X0 Register Y0 Register	X0R,Y0R	XX ₁₆ XX ₁₆
02C2 ₁₆ 02C3 ₁₆	X1 Register Y1 Register	X1R,Y1R	XX ₁₆ XX ₁₆
02C4 ₁₆ 02C5 ₁₆	X2 Register Y2 Register	X2R,Y2R	XX ₁₆ XX ₁₆
02C6 ₁₆ 02C7 ₁₆	X3 Register Y3 Register	X3R,Y3R	XX ₁₆ XX ₁₆
02C8 ₁₆ 02C9 ₁₆	X4 Register Y4 Register	X4R,Y4R	XX ₁₆ XX ₁₆
02CA ₁₆ 02CB ₁₆	X5 Register Y5 Register	X5R,Y5R	XX ₁₆ XX ₁₆
02CC ₁₆ 02CD ₁₆	X6 Register Y6 Register	X6R,Y6R	XX ₁₆ XX ₁₆
02CE ₁₆ 02CF ₁₆	X7 Register Y7 Register	X7R,Y7R	XX ₁₆ XX ₁₆
02D0 ₁₆ 02D1 ₁₆	X8 Register Y8 Register	X8R,Y8R	XX ₁₆ XX ₁₆
02D2 ₁₆ 02D3 ₁₆	X9 Register Y9 Register	X9R,Y9R	XX ₁₆ XX ₁₆
02D4 ₁₆ 02D5 ₁₆	X10 Register Y10 Register	X10R,Y10R	XX ₁₆ XX ₁₆
02D6 ₁₆ 02D7 ₁₆	X11 Register Y11 Register	X11R,Y11R	XX ₁₆ XX ₁₆
02D8 ₁₆ 02D9 ₁₆	X12 Register Y12 Register	X12R,Y12R	XX ₁₆ XX ₁₆
02DA ₁₆ 02DB ₁₆	X13 Register Y13 Register	X13R,Y13R	XX ₁₆ XX ₁₆
02DC ₁₆ 02DD ₁₆	X14 Register Y14 Register	X14R,Y14R	XX ₁₆ XX ₁₆
02DE ₁₆ 02DF ₁₆	X15 Register Y15 Register	X15R,Y15R	XX ₁₆ XX ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
02E0 ₁₆	X/Y Control Register	XYC	XXXX XX00 ₂
02E1 ₁₆			
02E2 ₁₆			
02E3 ₁₆			
02E4 ₁₆	UART1 Special Mode Register 4	U1SMR4	00 ₁₆
02E5 ₁₆	UART1 Special Mode Register 3	U1SMR3	00 ₁₆
02E6 ₁₆	UART1 Special Mode Register 2	U1SMR2	00 ₁₆
02E7 ₁₆	UART1 Special Mode Register	U1SMR	00 ₁₆
02E8 ₁₆	UART1 Transmit/Receive Mode Register	U1MR	00 ₁₆
02E9 ₁₆	UART1 Bit Rate Register	U1BRG	XX ₁₆
02EA ₁₆	UART1 Transmit Buffer Register	U1TB	XX ₁₆
02EB ₁₆			XX ₁₆
02EC ₁₆	UART1 Transmit/Receive Control Register 0	U1C0	0000 1000 ₂
02ED ₁₆	UART1 Transmit/Receive Control Register 1	U1C1	0000 0010 ₂
02EE ₁₆	UART1 Receive Buffer Register	U1RB	XX ₁₆
02EF ₁₆			XX ₁₆
02F0 ₁₆			
02F1 ₁₆			
02F2 ₁₆			
02F3 ₁₆			
02F4 ₁₆	UART4 Special Mode Register 4	U4SMR4	00 ₁₆
02F5 ₁₆	UART4 Special Mode Register 3	U4SMR3	00 ₁₆
02F6 ₁₆	UART4 Special Mode Register 2	U4SMR2	00 ₁₆
02F7 ₁₆	UART4 Special Mode Register	U4SMR	00 ₁₆
02F8 ₁₆	UART4 Transmit/Receive Mode Register	U4MR	00 ₁₆
02F9 ₁₆	UART4 Bit Rate Register	U4BRG	XX ₁₆
02FA ₁₆	UART4 Transmit Buffer Register	U4TB	XX ₁₆
02FB ₁₆			XX ₁₆
02FC ₁₆	UART4 Transmit/Receive Control Register 0	U4C0	0000 1000 ₂
02FD ₁₆	UART4 Transmit/Receive Control Register 1	U4C1	0000 0010 ₂
02FE ₁₆	UART4 Receive Buffer Register	U4RB	XX ₁₆
02FF ₁₆			XX ₁₆
0300 ₁₆	Timer B3, B4, B5 Count Start Flag	TBSR	000X XXXX ₂
0301 ₁₆			
0302 ₁₆	Timer A1-1 Register	TA11	XX ₁₆
0303 ₁₆			XX ₁₆
0304 ₁₆	Timer A2-1 Register	TA21	XX ₁₆
0305 ₁₆			XX ₁₆
0306 ₁₆	Timer A4-1 Register	TA41	XX ₁₆
0307 ₁₆			XX ₁₆
0308 ₁₆	Three-Phase PWM Control Register 0	INVC0	00 ₁₆
0309 ₁₆	Three-Phase PWM Control Register 1	INVC1	00 ₁₆
030A ₁₆	Three-Phase Output Buffer Register 0	IDB0	XX11 1111 ₂
030B ₁₆	Three-Phase Output Buffer Register 1	IDB1	XX11 1111 ₂
030C ₁₆	Dead Time Timer	DTT	XX ₁₆
030D ₁₆	Timer B2 Interrupt Generation Frequency Set Counter	ICTB2	XX ₁₆
030E ₁₆			
030F ₁₆			

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Address	Register	Symbol	Value after RESET
0310 ₁₆ 0311 ₁₆	Timer B3 Register	TB3	XX ₁₆ XX ₁₆
0312 ₁₆ 0313 ₁₆	Timer B4 Register	TB4	XX ₁₆ XX ₁₆
0314 ₁₆ 0315 ₁₆	Timer B5 Register	TB5	XX ₁₆ XX ₁₆
0316 ₁₆			
0317 ₁₆			
0318 ₁₆			
0319 ₁₆			
031A ₁₆			
031B ₁₆	Timer B3 Mode Register	TB3MR	00XX 0000 ₂
031C ₁₆	Timer B4 Mode Register	TB4MR	00XX 0000 ₂
031D ₁₆	Timer B5 Mode Register	TB5MR	00XX 0000 ₂
031E ₁₆			
031F ₁₆	External Interrupt Request Source Select Register	IFSR	00 ₁₆
0320 ₁₆			
0321 ₁₆			
0322 ₁₆			
0323 ₁₆			
0324 ₁₆	UART3 Special Mode Register 4	U3SMR4	00 ₁₆
0325 ₁₆	UART3 Special Mode Register 3	U3SMR3	00 ₁₆
0326 ₁₆	UART3 Special Mode Register 2	U3SMR2	00 ₁₆
0327 ₁₆	UART3 Special Mode Register	U3SMR	00 ₁₆
0328 ₁₆	UART3 Transmit/Receive Mode Register	U3MR	00 ₁₆
0329 ₁₆	UART3 Bit Rate Register	U3BRG	XX ₁₆
032A ₁₆ 032B ₁₆	UART3 Transmit Buffer Register	U3TB	XX ₁₆ XX ₁₆
032C ₁₆	UART3 Transmit/Receive Control Register 0	U3C0	0000 1000 ₂
032D ₁₆	UART3 Transmit/Receive Control Register 1	U3C1	0000 0010 ₂
032E ₁₆ 032F ₁₆	UART3 Receive Buffer Register	U3RB	XX ₁₆ XX ₁₆
0330 ₁₆			
0331 ₁₆			
0332 ₁₆			
0333 ₁₆			
0334 ₁₆	UART2 Special Mode Register 4	U2SMR4	00 ₁₆
0335 ₁₆	UART2 Special Mode Register 3	U2SMR3	00 ₁₆
0336 ₁₆	UART2 Special Mode Register 2	U2SMR2	00 ₁₆
0337 ₁₆	UART2 Special Mode Register	U2SMR	00 ₁₆
0338 ₁₆	UART2 Transmit/Receive Mode Register	U2MR	00 ₁₆
0339 ₁₆	UART2 Bit Rate Register	U2BRG	XX ₁₆
033A ₁₆ 033B ₁₆	UART2 Transmit Buffer Register	U2TB	XX ₁₆ XX ₁₆
033C ₁₆	UART2 Transmit/Receive Control Register 0	U2C0	0000 1000 ₂
033D ₁₆	UART2 Transmit/Receive Control Register 1	U2C1	0000 0010 ₂
033E ₁₆ 033F ₁₆	UART2 Receive Buffer Register	U2RB	XX ₁₆ XX ₁₆

X: Indeterminate

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Address	Register	Symbol	Value after RESET
0340 ₁₆	Count Start Flag	TABSR	00 ₁₆
0341 ₁₆	Clock Prescaler Reset Flag	CPSRF	0XXX XXXX ₂
0342 ₁₆	One-Shot Start Flag	ONSF	00 ₁₆
0343 ₁₆	Trigger Select Register	TRGSR	00 ₁₆
0344 ₁₆	Up/Down Flag	UDF	00 ₁₆
0345 ₁₆			
0346 ₁₆ 0347 ₁₆	Timer A0 Register	TA0	XX ₁₆ XX ₁₆
0348 ₁₆ 0349 ₁₆	Timer A1 Register	TA1	XX ₁₆ XX ₁₆
034A ₁₆ 034B ₁₆	Timer A2 Register	TA2	XX ₁₆ XX ₁₆
034C ₁₆ 034D ₁₆	Timer A3 Register	TA3	XX ₁₆ XX ₁₆
034E ₁₆ 034F ₁₆	Timer A4 Register	TA4	XX ₁₆ XX ₁₆
0350 ₁₆ 0351 ₁₆	Timer B0 Register	TB0	XX ₁₆ XX ₁₆
0352 ₁₆ 0353 ₁₆	Timer B1 Register	TB1	XX ₁₆ XX ₁₆
0354 ₁₆ 0355 ₁₆	Timer B2 Register	TB2	XX ₁₆ XX ₁₆
0356 ₁₆	Timer A0 Mode Register	TA0MR	00 ₁₆
0357 ₁₆	Timer A1 Mode Register	TA1MR	00 ₁₆
0358 ₁₆	Timer A2 Mode Register	TA2MR	00 ₁₆
0359 ₁₆	Timer A3 Mode Register	TA3MR	00 ₁₆
035A ₁₆	Timer A4 Mode Register	TA4MR	00 ₁₆
035B ₁₆	Timer B0 Mode Register	TB0MR	00XX 0000 ₂
035C ₁₆	Timer B1 Mode Register	TB1MR	00XX 0000 ₂
035D ₁₆	Timer B2 Mode Register	TB2MR	00XX 0000 ₂
035E ₁₆	Timer B2 Special Mode Register	TB2SC	XXXX XXX0 ₂
035F ₁₆	Count Source Prescaler Register ⁽¹⁾	TCSPPR	0XXX 0000 ₂
0360 ₁₆			
0361 ₁₆			
0362 ₁₆			
0363 ₁₆			
0364 ₁₆	UART0 Special Mode Register 4	U0SMR4	00 ₁₆
0365 ₁₆	UART0 Special Mode Register 3	U0SMR3	00 ₁₆
0366 ₁₆	UART0 Special Mode Register 2	U0SMR2	00 ₁₆
0367 ₁₆	UART0 Special Mode Register	U0SMR	00 ₁₆
0368 ₁₆	UART0 Transmit/Receive Mode Register	U0MR	00 ₁₆
0369 ₁₆	UART0 Bit Rate Register	U0BRG	XX ₁₆
036A ₁₆ 036B ₁₆	UART0 Transmit Buffer Register	U0TB	XX ₁₆ XX ₁₆
036C ₁₆	UART0 Transmit/Receive Control Register 0	U0C0	0000 1000 ₂
036D ₁₆	UART0 Transmit/Receive Control Register 1	U0C1	0000 0010 ₂
036E ₁₆ 036F ₁₆	UART0 Receive Buffer Register	U0RB	XX ₁₆ XX ₁₆

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. The TCSPPR register maintains values set before reset, even after software reset or watchdog timer reset has been performed.

Address	Register	Symbol	Value after RESET
0370 ₁₆			
0371 ₁₆			
0372 ₁₆			
0373 ₁₆			
0374 ₁₆			
0375 ₁₆			
0376 ₁₆			
0377 ₁₆			
0378 ₁₆	DMA0 Request Source Select Register	DM0SL	0X00 0000 ₂
0379 ₁₆	DMA1 Request Source Select Register	DM1SL	0X00 0000 ₂
037A ₁₆	DMA2 Request Source Select Register	DM2SL	0X00 0000 ₂
037B ₁₆	DMA3 Request Source Select Register	DM3SL	0X00 0000 ₂
037C ₁₆	CRC Data Register	CRCD	XX ₁₆
037D ₁₆			XX ₁₆
037E ₁₆	CRC Input Register	CRCIN	XX ₁₆
037F ₁₆			
0380 ₁₆	A/D0 Register 0	AD00	XXXX XXXX ₂
0381 ₁₆			0000 0000 ₂
0382 ₁₆	A/D0 Register 1	AD01	XX ₁₆
0383 ₁₆			XX ₁₆
0384 ₁₆	A/D0 Register 2	AD02	XX ₁₆
0385 ₁₆			XX ₁₆
0386 ₁₆	A/D0 Register 3	AD03	XX ₁₆
0387 ₁₆			XX ₁₆
0388 ₁₆	A/D0 Register 4	AD04	XX ₁₆
0389 ₁₆			XX ₁₆
038A ₁₆	A/D0 Register 5	AD05	XX ₁₆
038B ₁₆			XX ₁₆
038C ₁₆	A/D0 Register 6	AD06	XX ₁₆
038D ₁₆			XX ₁₆
038E ₁₆	A/D0 Register 7	AD07	XX ₁₆
038F ₁₆			XX ₁₆
0390 ₁₆			
0391 ₁₆			
0392 ₁₆			
0393 ₁₆			
0394 ₁₆	A/D0 Control Register 2	AD0CON2	XX0X XXX0 ₂
0395 ₁₆	A/D0 Control Register 3	AD0CON3	XXXX X000 ₂
0396 ₁₆	A/D0 Control Register 0	AD0CON0	00 ₁₆
0397 ₁₆	A/D0 Control Register 1	AD0CON1	00 ₁₆
0398 ₁₆	D/A Register 0	DA0	XX ₁₆
0399 ₁₆			
039A ₁₆	D/A Register 1	DA1	XX ₁₆
039B ₁₆			
039C ₁₆	D/A Control Register	DACON	XXXX XX00 ₂
039D ₁₆			
039E ₁₆			
039F ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
03A0 ₁₆			
03A1 ₁₆			
03A2 ₁₆			
03A3 ₁₆			
03A4 ₁₆			
03A5 ₁₆			
03A6 ₁₆			
03A7 ₁₆	Function Select Register D1	PSD1	X0XX XX00 ₂
03A8 ₁₆			
03A9 ₁₆			
03AA ₁₆			
03AB ₁₆			
03AC ₁₆			
03AD ₁₆	Function Select Register C3	PSC3	X0XX XXXX ₂
03AE ₁₆			
03AF ₁₆	Function Select Register C	PSC	00X0 0000 ₂
03B0 ₁₆	Function Select Register A0	PS0	00 ₁₆
03B1 ₁₆	Function Select Register A1	PS1	00 ₁₆
03B2 ₁₆	Function Select Register B0	PSL0	00 ₁₆
03B3 ₁₆	Function Select Register B1	PSL1	00 ₁₆
03B4 ₁₆	Function Select Register A2	PS2	00X0 0000 ₂
03B5 ₁₆	Function Select Register A3	PS3	00 ₁₆
03B6 ₁₆	Function Select Register B2	PSL2	00X0 0000 ₂
03B7 ₁₆	Function Select Register B3	PSL3	00 ₁₆
03B8 ₁₆			
03B9 ₁₆			
03BA ₁₆			
03BB ₁₆			
03BC ₁₆			
03BD ₁₆			
03BE ₁₆			
03BF ₁₆			
03C0 ₁₆	Port P6 Register	P6	XX ₁₆
03C1 ₁₆	Port P7 Register	P7	XX ₁₆
03C2 ₁₆	Port P6 Direction Register	PD6	00 ₁₆
03C3 ₁₆	Port P7 Direction Register	PD7	00 ₁₆
03C4 ₁₆	Port P8 Register	P8	XX ₁₆
03C5 ₁₆	Port P9 Register	P9	XX ₁₆
03C6 ₁₆	Port P8 Direction Register	PD8	00X0 0000 ₂
03C7 ₁₆	Port P9 Direction Register	PD9	00 ₁₆
03C8 ₁₆	Port P10 Register	P10	XX ₁₆
03C9 ₁₆			
03CA ₁₆	Port P10 Direction Register	PD10	00 ₁₆
03CB ₁₆			
03CC ₁₆			
03CD ₁₆			
03CE ₁₆			
03CF ₁₆			

X: Indeterminate

Blank spaces are reserved. No access is allowed.

Address	Register	Symbol	Value after RESET
03D0 ₁₆			
03D1 ₁₆			
03D2 ₁₆			
03D3 ₁₆			
03D4 ₁₆			
03D5 ₁₆			
03D6 ₁₆			
03D7 ₁₆			
03D8 ₁₆			
03D9 ₁₆			
03DA ₁₆	Pull-Up Control Register 2	PUR2	00 ₁₆
03DB ₁₆	Pull-Up Control Register 3	PUR3	00 ₁₆
03DC ₁₆			
03DD ₁₆			
03DE ₁₆			
03DF ₁₆			
03E0 ₁₆	Port P0 Register ⁽¹⁾	P0	XX ₁₆
03E1 ₁₆	Port P1 Register ⁽¹⁾	P1	XX ₁₆
03E2 ₁₆	Port P0 Direction Register ⁽¹⁾	PD0	00 ₁₆
03E3 ₁₆	Port P1 Direction Register ⁽¹⁾	PD1	00 ₁₆
03E4 ₁₆	Port P2 Register ⁽¹⁾	P2	XX ₁₆
03E5 ₁₆	Port P3 Register ⁽¹⁾	P3	XX ₁₆
03E6 ₁₆	Port P2 Direction Register ⁽¹⁾	PD2	00 ₁₆
03E7 ₁₆	Port P3 Direction Register ⁽¹⁾	PD3	00 ₁₆
03E8 ₁₆	Port P4 Register ⁽¹⁾	P4	XX ₁₆
03E9 ₁₆	Port P5 Register ⁽¹⁾	P5	XX ₁₆
03EA ₁₆	Port P4 Direction Register ⁽¹⁾	PD4	00 ₁₆
03EB ₁₆	Port P5 Direction Register ⁽¹⁾	PD5	00 ₁₆
03EC ₁₆			
03ED ₁₆			
03EE ₁₆			
03EF ₁₆			
03F0 ₁₆	Pull-up Control Register 0	PUR0	00 ₁₆
03F1 ₁₆	Pull-up Control Register 1	PUR1	XXXX 0000 ₂
03F2 ₁₆			
03F3 ₁₆			
03F4 ₁₆			
03F5 ₁₆			
03F6 ₁₆			
03F7 ₁₆			
03F8 ₁₆			
03F9 ₁₆			
03FA ₁₆			
03FB ₁₆			
03FC ₁₆			
03FD ₁₆			
03FE ₁₆			
03FF ₁₆	Port Control Register	PCR	XXXX XXX0 ₂

X: Indeterminate

Blank spaces are reserved. No access is allowed.

NOTE:

1. Pins, functioning as bus control pins, cannot be selected as I/O ports.

5. Electrical Characteristics

Table 5.1 Absolute Maximum Ratings

Symbol	Parameter		Condition	Value	Unit
V _{CC1} , V _{CC2}	Supply Voltage		V _{CC1} =AV _{CC}	-0.3 to 6.0	V
V _{CC2}	Supply Voltage		-	-0.3 to V _{CC1}	V
AV _{CC}	Analog Supply Voltage		V _{CC1} =AV _{CC}	-0.3 to 6.0	V
V _I	Input Voltage	RESET, CNV _{SS} , BYTE, P60-P67, P72-P77, P80-P87, P90-P97, P100-P107, V _{REF} , X _{IN}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
V _O	Output Voltage	P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107, X _{OUT}		-0.3 to V _{CC1} +0.3	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57		-0.3 to V _{CC2} +0.3	
		P70, P71		-0.3 to 6.0	
P _d	Power Dissipation		T _{opr} =25° C	500	mW
T _{opr}	Operating Ambient Temperature			-20 to 85/ -40 to 85 ⁽¹⁾	° C
T _{stg}	Storage Temperature			-65 to 150	° C

NOTE:

1. Contact our sales office if temperature range of -40 to 85° C is required.

Table 5.2 Recommended Operating Conditions
(V_{CC1}= V_{CC2}=3.0V to 5.5V at Topr=– 20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
V _{CC1} , V _{CC2}	Supply Voltage (V _{CC1} ≥ V _{CC2})		3.0	5.0	5.5	V
AV _{CC}	Analog Supply Voltage			V _{CC1}		V
V _{SS}	Supply Voltage			0		V
AV _{SS}	Analog Supply Voltage			0		V
V _{IH}	Input High ("H") Voltage	P20-P27, P30-P37, P40-P47, P50-P57	0.8V _{CC2}		V _{CC2}	V
		P60-P67, P72-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, X _{IN} , RESET, CNV _{SS} , BYTE	0.8V _{CC1}		V _{CC1}	
		P70, P71	0.8V _{CC1}		6.0	
		P00-P07, P10-P17 (in single-chip mode)	0.8V _{CC2}		V _{CC2}	
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0.5V _{CC2}		V _{CC2}	
V _{IL}	Input Low ("L") Voltage	P20-P27, P30-P37, P40-P47, P50-P57	0		0.2V _{CC2}	V
		P60-P67, P70-P77, P80-P87 ⁽³⁾ , P90-P97, P100-P107, X _{IN} , RESET, CNV _{SS} , BYTE	0		0.2V _{CC1}	
		P00-P07, P10-P17 (in single-chip mode)	0		0.2V _{CC2}	
		P00-P07, P10-P17 (in memory expansion mode and microprocessor mode)	0		0.16V _{CC2}	
I _{OH(peak)}	Peak Output High ("H") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107			-10.0	mA
I _{OH(avg)}	Average Output High ("H") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107			-5.0	mA
I _{OL(peak)}	Peak Output Low ("L") Current ⁽²⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107			10.0	mA
I _{OL(avg)}	Average Output Low ("L") Current ⁽¹⁾	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107			5.0	mA

NOTES:

1. Typical values when average output current is 100 ms.
2. Total I_{OL(peak)} for P0, P1, P2, P86, P87, P9, and P10 must be 80 mA or less.
 Total I_{OL(peak)} for P3, P4, P5, P6, P7, and P80 to P84 must be 80 mA or less.
 Total I_{OH(peak)} for P0, P1, and P2 must be -40 mA or less.
 Total I_{OH(peak)} for P86, P87, P9, and P10 must be -40 mA or less.
 Total I_{OH(peak)} for P3, P4, and P5 must be -40 mA or less.
 Total I_{OH(peak)} for P6, P7, and P80 to P84 must be -40 mA or less.
3. V_{IH} and V_{IL} reference for P87 applies when P87 is used as a programmable input port.
 It does not apply when P87 is used as X_{CIN}.

Table 5.2 Recommended Operating Conditions (Continued)
(V_{CC1}=V_{CC2}=3.0V to 5.5V at T_{opr}=−20 to 85°C unless otherwise specified)

Symbol	Parameter		Standard			Unit
			Min.	Typ.	Max.	
f _(BCLK)	CPU Operation Frequency	V _{CC1} =4.2 to 5.5 V	0		32	MHz
		V _{CC1} =3.0 to 5.5 V	0		24	MHz
f _(XIN)	Main Clock Input Frequency	V _{CC1} =4.2 to 5.5 V	0		32	MHz
		V _{CC1} =3.0 to 5.5 V	0		24	MHz
f _(XCIN)	Sub Clock Frequency			32.768	50	kHz
f _(Ring)	On-chip Oscillator Frequency (T _{opr} =25° C)		0.5	1	2	MHz
f _(PLL)	PLL Clock Frequency	V _{CC1} =4.2 to 5.5 V	10		32	MHz
		V _{CC1} =3.0 to 5.5 V	10		24	MHz
t _{SU(PLL)}	Wait Time to Stabilize PLL Frequency Synthesizer	V _{CC1} =5.0 V			5	ms
		V _{CC1} =3.3 V			10	ms

$$V_{CC1}=V_{CC2}=5V$$

Table 5.3 Electrical Characteristics

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK)=32MHz$ unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57	I _{OH} =-5mA	V _{CC2} -2.0		V _{CC2}	V
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107	I _{OH} =-5mA	V _{CC1} -2.0		V _{CC1}	
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57	I _{OH} =-200μA	V _{CC2} -0.3		V _{CC2}	V
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107	I _{OH} =-200μA	V _{CC1} -0.3		V _{CC1}	
		X _{OUT}	I _{OH} =-1mA	3.0		V _{CC1}	V
		X _{COUT}	High Power		2.5		V
			Low Power		1.6		
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107	I _{OL} =5mA			2.0	V
		P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107	I _{OL} =200μA			0.45	V
		X _{OUT}	I _{OL} =1mA			2.0	V
		X _{COUT}	High Power		0		V
			Low Power		0		
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0 _{IN} -TA4 _{IN} , TB0 _{IN} -TB5 _{IN} , INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0 _{OUT} -TA4 _{OUT} , NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, X _{IN} , RESET, CNV _{SS} , BYTE	V _I =5V			5.0	μA
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-5.0	μA
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107	V _I =0V	20	40	167	kΩ
R _{fXIN}	Feedback Resistance	X _{IN}			1.5		MΩ
R _{fXCIN}	Feedback Resistance	X _{CIN}			15		MΩ
V _{RAM}	RAM Standby Voltage	In stop mode		2.0			V
I _{CC}	Power Supply Current	In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(BCLK)=32 MHz, Square wave, No division		22	60	mA
			f(BCLK)=32 kHz, In wait mode, T _{opr} =25° C		10		μA
			While clock stops, T _{opr} =25° C		0.8	5	μA
			While clock stops, T _{opr} =85° C			20	μA

$$V_{CC1}=V_{CC2}=5V$$

Table 5.4 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=4.2$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution	$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	$V_{REF}=V_{CC1}=V_{CC2}=5V$			± 3	LSB
						LSB
		External op-amp connection mode			± 7	LSB
DNL	Differential Nonlinearity Error				± 1	LSB
-	Offset Error				± 3	LSB
-	Gain Error				± 3	LSB
RLADDER	Resistor Ladder	$V_{REF}=V_{CC1}$	8		40	k Ω
t _{CONV}	10-bit Conversion Time ^(1, 2)		2.06			μs
t _{CONV}	8-bit Conversion Time ^(1, 2)		1.75			μs
t _{SAMP}	Sampling Time ⁽¹⁾		0.188			μs
V _{REF}	Reference Voltage		2		V_{CC1}	V
V _{IA}	Analog Input Voltage		0		V_{REF}	V

NOTES:

1. Divide $f(X_{IN})$, if exceeding 16 MHz, to keep ϕ_{AD} frequency at 16 MHz or less.
2. With using the sample and hold function.

Table 5.5 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}=4.2$ to $5.5V$, $V_{SS}=AV_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$, $f(BCLK) = 32MHz$ unless otherwise specified)

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
t _{SU}	Setup Time				3	μs
R _O	Output Resistance		4	10	20	k Ω
I _{VREF}	Reference Power Supply Input Current	(Note 1)			1.5	mA

NOTE:

1. Measurement when using one D/A converter. The DA_i register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
I_{VREF} flows even if the VCUT bit in the AD0CON1 register is set to "0" (no V_{REF} connection).

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.6 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	31.25		ns
$t_{W(H)}$	External Clock Input High ("H") Width	13.75		ns
$t_{W(L)}$	External Clock Input Low ("L") Width	13.75		ns
t_r	External Clock Rise Time		5	ns
t_f	External Clock Fall Time		5	ns

Table 5.7 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexrd bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	26		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	26		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	30		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	$\overline{HLDA}$ Output Delay Time		25	ns

NOTE:

- Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1) \times 2\}+1)$$

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1}=V_{CC2}=4.2$ to $5.5V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.8 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.9 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.10 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.11 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.12 Timer A Input (Counter Increment/Decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{W(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{W(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{SU(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{H(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$$V_{CC1}=V_{CC2}=5V$$

Timing Requirements

($V_{CC1} = V_{CC2} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.13 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{c(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 5.14 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.15 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{w(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{w(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.16 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(AD)}$	ADTRG Input Cycle Time (required for trigger)	1000		ns
$t_{w(ADL)}$	ADTRG Input Low ("L") Width	125		ns

Table 5.17 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{c(CK)}$	CLKi Input Cycle Time	200		ns
$t_{w(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{w(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.18 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{w(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{w(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.19 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{W(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{W(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(bx2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

$$V_{CC1}=V_{CC2}=5V$$

Switching Characteristics

($V_{CC} = 4.2$ to $5.5V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.20 Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		-3		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		(Note 1)		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-5		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		-5		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-ALE)}$	ALE Signal Output Delay Time (BCLK standard)			18	ns
$t_{h(BCLK-ALE)}$	ALE Signal Output Hold Time (BCLK standard)		-5		ns
$t_{d(AD-ALE)}$	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
$t_{h(ALE-AD)}$	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
$t_{dZ(RD-AD)}$	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(RD-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(RD-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 25 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m = (bx2)-1)$$

3. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{d(AD-ALE)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n = a)$$

4. Values can be obtained from the following equations, according to BCLK frequency and external bus cycle.

$$t_{h(ALE-AD)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 10 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n = a)$$

$$V_{CC1}=V_{CC2}=5V$$

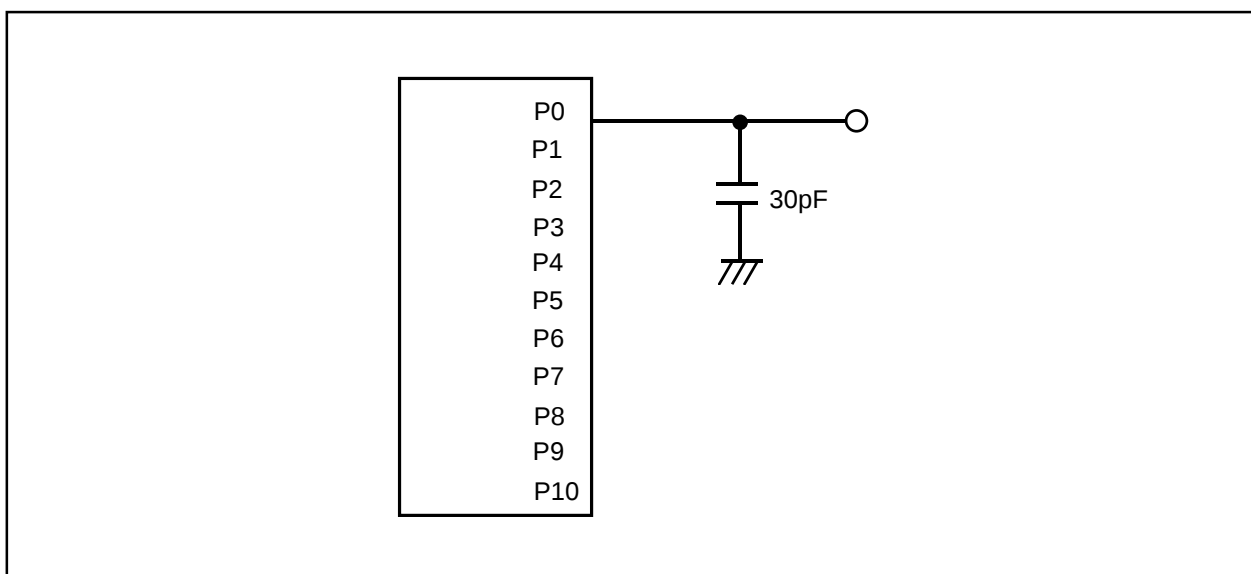
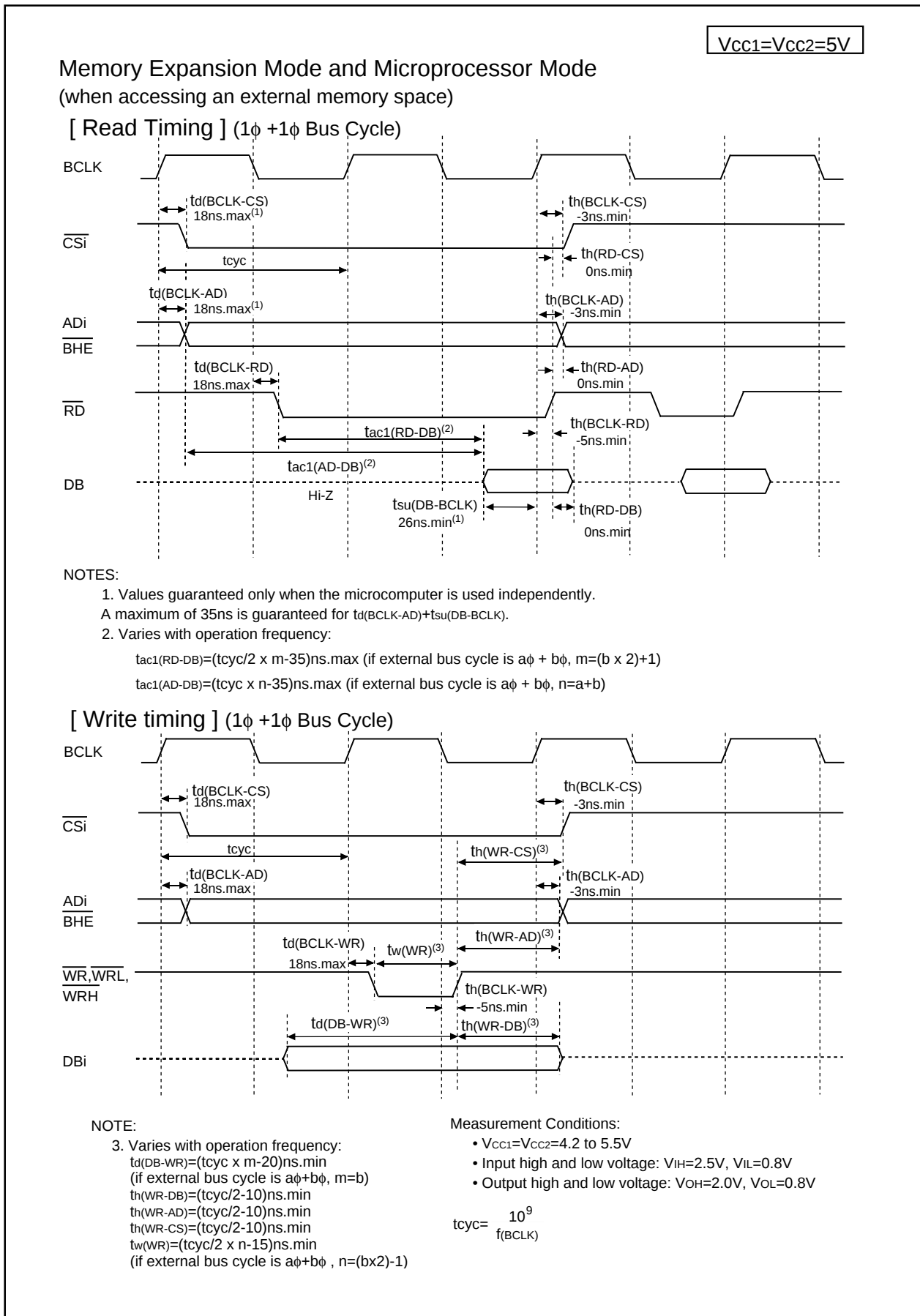


Figure 5.1 P0 to P10 Measurement Circuit

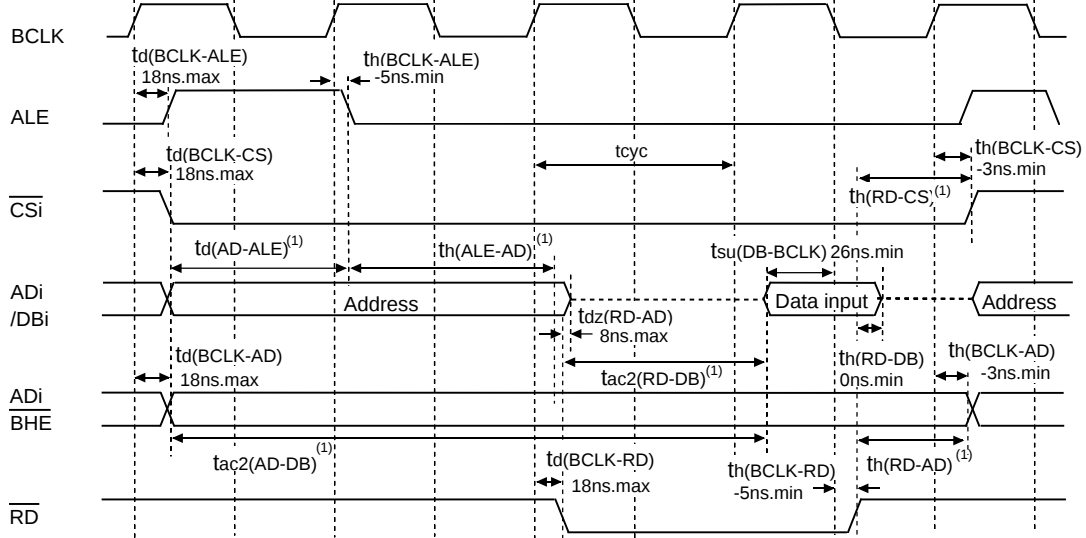
Figure 5.2 V_{CC1}=V_{CC2}=5V Timing Diagram (1)

Memory Expansion Mode and Microprocessor Mode

(when accessing an external memory space with the multiplexed bus)

V_{CC1}=V_{CC2}=5V

[Read Timing] (2φ + 2φ Bus Cycle)



NOTE:

1. Varies with operation frequency:

$t_d(\text{AD-ALE}) = (t_{cyc}/2 \times n - 20)\text{ns.min}$ (if external bus cycle is $a\phi + b\phi$, $n=a$)

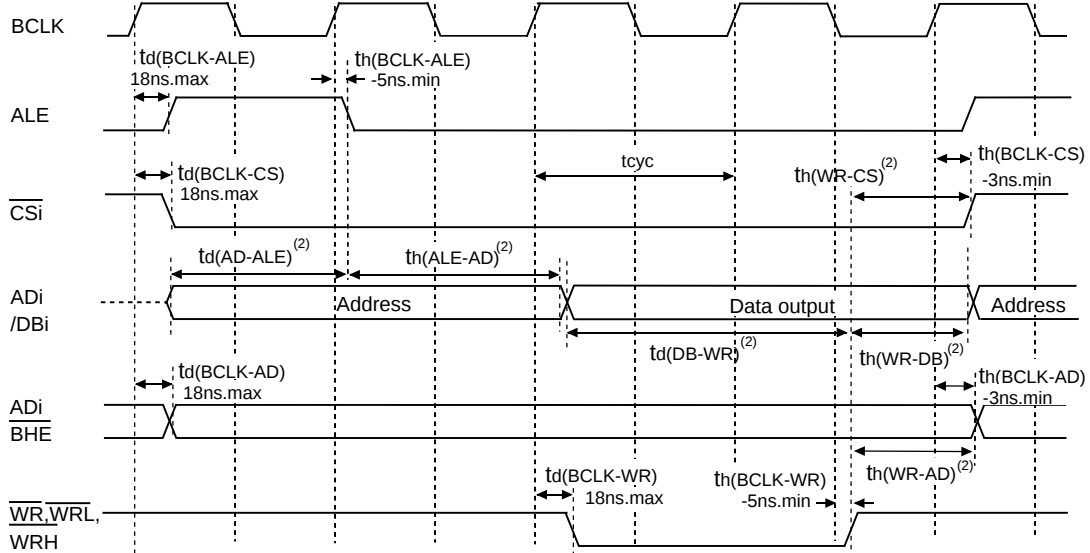
$t_h(\text{ALE-AD}) = (t_{cyc}/2 \times n - 10)\text{ns.min}$ (if external bus cycle is $a\phi + b\phi$, $n=a$)

$t_h(\text{RD-AD}) = (t_{cyc}/2 - 10)\text{ns.min}$, $t_h(\text{RD-CS}) = (t_{cyc}/2 - 10)\text{ns.min}$

$t_{ac2}(\text{RD-DB}) = (t_{cyc}/2 \times m - 35)\text{ns.max}$ (if external bus cycle is $a\phi + b\phi$, $m=(b \times 2) - 1$)

$t_{ac2}(\text{AD-DB}) = (t_{cyc}/2 \times p - 35)\text{ns.max}$ (if external bus cycle is $a\phi + b\phi$, $p=\{(a+b-1) \times 2\} + 1$)

[Write Timing] (2φ + 2φ Bus Cycle)



NOTE:

2. Varies with operation frequency:

$t_d(\text{AD-ALE}) = (t_{cyc}/2 \times n - 20)\text{ns.min}$

(if external bus cycle is $a\phi + b\phi$, $n=a$)

$t_h(\text{ALE-AD}) = (t_{cyc}/2 \times n - 10)\text{ns.min}$

(if external bus cycle is $a\phi + b\phi$, $n=a$)

$t_h(\text{WR-AD}) = (t_{cyc}/2 - 10)\text{ns.min}$,

$t_h(\text{WR-CS}) = (t_{cyc}/2 - 10)\text{ns.min}$, $t_h(\text{WR-DB}) = (t_{cyc}/2 - 10)\text{ns.min}$

$t_d(\text{DB-WR}) = (t_{cyc}/2 \times m - 25)\text{ns.min}$

(if external bus cycle is $a\phi + b\phi$, $m=(b \times 2) - 1$)

Measurement Conditions:

• V_{CC1}=V_{CC2}=4.2 to 5.5V

• Input high and low voltage:

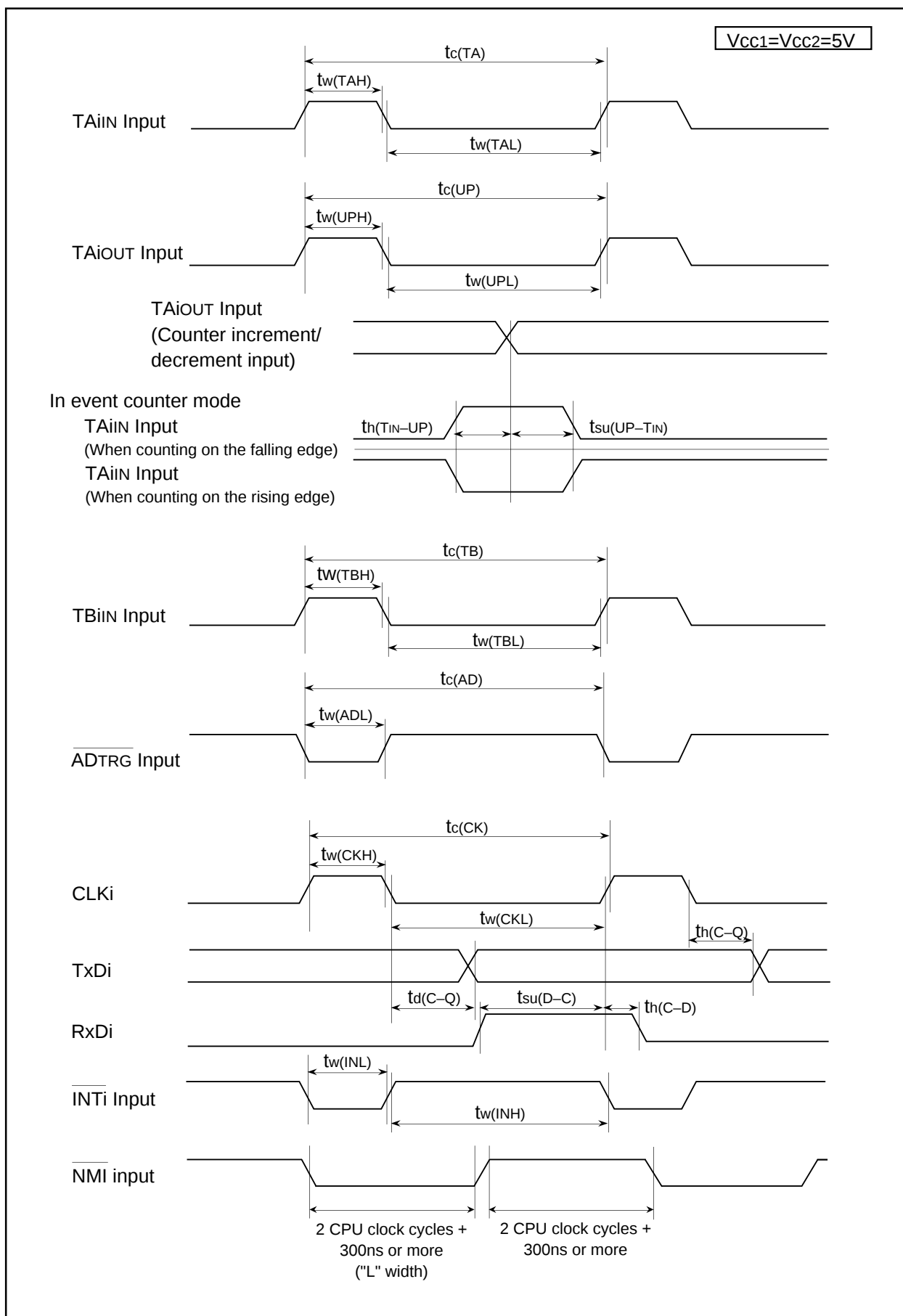
V_{IH}=2.5V, V_{IL}=0.8V

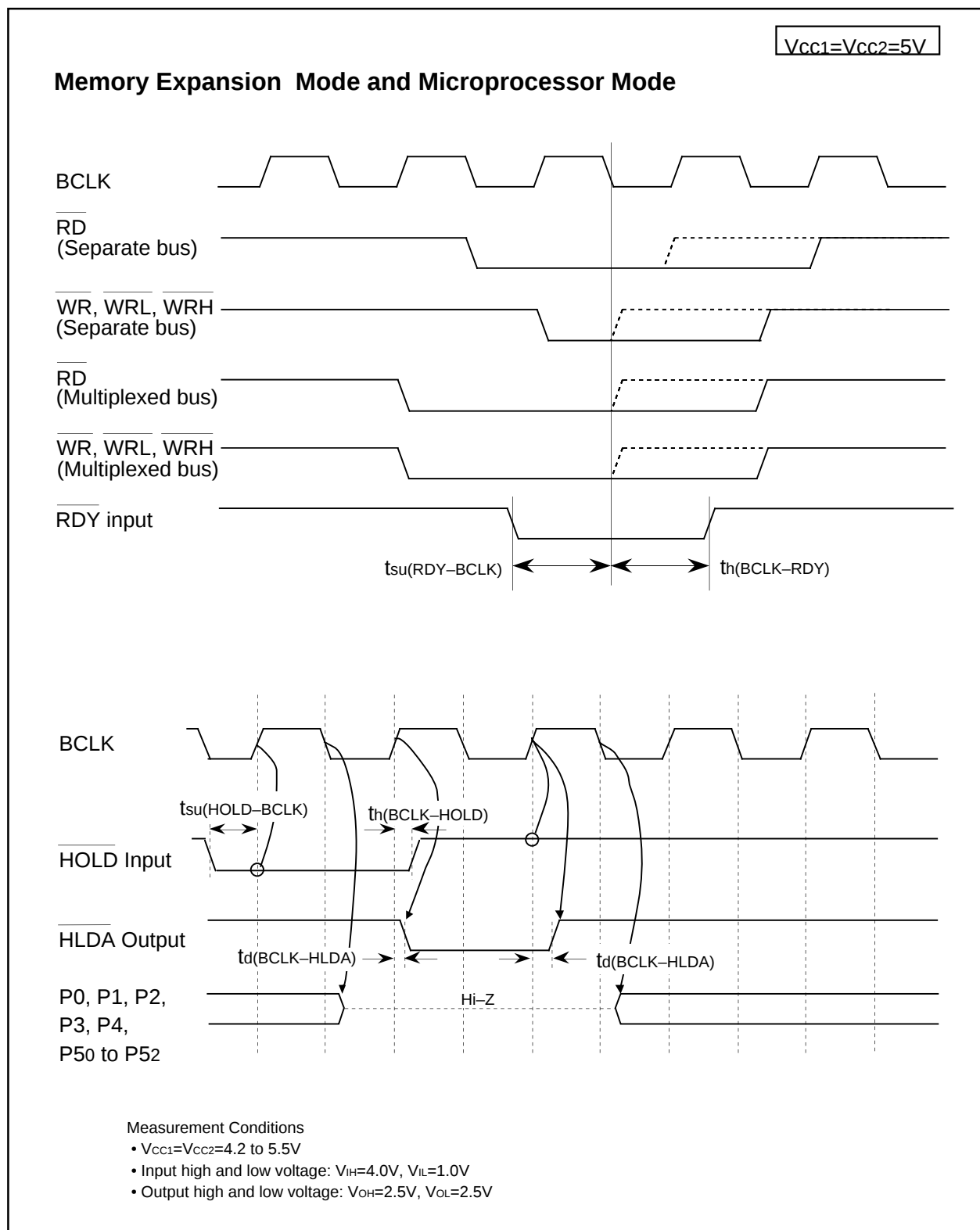
• Output high and low voltage:

V_{OH}=2.0V, V_{OL}=0.8V

$t_{cyc} = \frac{10^9}{f(\text{BCLK})}$

Figure 5.3 V_{CC1}=V_{CC2}=5V Timing Diagram (2)

Figure 5.4 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (3)

Figure 5.5 $V_{CC1}=V_{CC2}=5V$ Timing Diagram (4)

$$V_{CC1}=V_{CC2}=3.3V$$

Table 5.21 Electrical Characteristics ($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS}=0V$ at $T_{opr} = -20$ to $85^{\circ}C$,
 $f(BCLK)=24MHz$ unless otherwise specified)

Symbol	Parameter		Condition	Standard			Unit
				Min.	Typ.	Max.	
V _{OH}	Output High ("H") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57	I _{OH} =-1mA	V _{CC2} -0.6		V _{CC2}	V
		P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107		V _{CC1} -0.6		V _{CC1}	V
		X _{OUT}	I _{OH} =-0.1mA	2.7		V _{CC1}	V
		X _{COUT}	High Power	No load applied	2.5		V
			Low Power	No load applied	1.6		V
V _{OL}	Output Low ("L") Voltage	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P84, P86, P87, P90-P97, P100-P107	I _{OL} =1mA			0.5	V
		X _{OUT}	I _{OL} =0.1mA			0.5	V
		X _{COUT}	High Power	No load applied	0		V
			Low Power	No load applied	0		V
V _{T+} -V _{T-}	Hysteresis	HOLD, RDY, TA0 _{IN} -TA4 _{IN} , TB0 _{IN} -TB5 _{IN} , INT0-INT5, AD _{TRG} , CTS0-CTS4, CLK0-CLK4, TA0 _{OUT} -TA4 _{OUT} , NMI, KI0-KI3, RxD0-RxD4, SCL0-SCL4, SDA0-SDA4		0.2		1.0	V
		RESET		0.2		1.8	V
I _{IH}	Input High ("H") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, X _{IN} , RESET, CNV _{SS} , BYTE	V _I =3V			4.0	μA
I _{IL}	Input Low ("L") Current	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P70-P77, P80-P87, P90-P97, P100-P107, X _{IN} , RESET, CNV _{SS} , BYTE	V _I =0V			-4.0	μA
R _{PULLUP}	Pull-up Resistance	P00-P07, P10-P17, P20-P27, P30-P37, P40-P47, P50-P57, P60-P67, P72-P77, P80-P84, P86, P87, P90-P97, P100-P107	V _I =0V	40	70	500	kΩ
R _{fXIN}	Feedback Resistance	X _{IN}			3.0		MΩ
R _{fXCIN}	Feedback Resistance	X _{CIN}			30.0		MΩ
V _{RAM}	RAM Standby Voltage	in stop mode		2.0			V
I _{CC}	Power Supply Current	Measurement condition: In single-chip mode, output pins are left open and other pins are connected to V _{SS} .	f(BCLK)=24 MHz, Square wave, No division		17	35	mA
			f(BCLK)=32 kHz, In wait mode, T _{opr} =25° C		10		μA
			While clock stops, T _{opr} =25° C		0.8	5	μA
			While clock stops, T _{opr} =85° C			50	μA

$$V_{CC1}=V_{CC2}=3.3V$$

**Table 5.22 A/D Conversion Characteristics ($V_{CC1}=V_{CC2}=AV_{CC}=V_{REF}=3.0$ to $3.6V$, $V_{SS}=AV_{SS}=0V$
at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK) = 24MHz$ unless otherwise specified)**

Symbol	Parameter		Measurement Condition	Standard			Unit
				Min.	Typ.	Max.	
-	Resolution		$V_{REF}=V_{CC1}$			10	Bits
INL	Integral Nonlinearity Error	No S&H (8-bit)	$V_{CC1}=V_{CC2}=V_{REF}=3.3V$			± 2	LSB
DNL	Differential Nonlinearity Error	No S&H (8-bit)				± 1	LSB
-	Offset Error	No S&H (8-bit)				± 2	LSB
-	Gain Error	No S&H (8-bit)				± 2	LSB
RLADDER	Resistor Ladder		$V_{REF}=V_{CC1}$	8.0		40	k Ω
tCONV	8-bit Conversion Time ^(1, 2)			6.1			μs
VREF	Reference Voltage			3.3		V_{CC1}	V
VIA	Analog Input Voltage			0		V_{REF}	V

S&H: Sample and Hold

NOTES:

1. Divide $f(X_{IN})$, if exceeding 10 MHz, to keep ϕAD frequency at 10 MHz or less.
2. S&H not available.

**Table 5.23 D/A Conversion Characteristics ($V_{CC1}=V_{CC2}=V_{REF}=3.0$ to $3.6V$, $V_{SS}=AV_{SS}=0V$
at $T_{opr} = -20$ to $85^{\circ}C$, $f(BCLK) = 24MHz$ unless otherwise specified)**

Symbol	Parameter	Measurement Condition	Standard			Unit
			Min.	Typ.	Max.	
-	Resolution				8	Bits
-	Absolute Accuracy				1.0	%
tsu	Setup Time				3	μs
Ro	Output Resistance		4	10	20	k Ω
IvREF	Reference Power Supply Input Current	(Note 1)			1.0	mA

NOTE:

1. Measurement results when using one D/A converter. The DAi register (i=0, 1) of the D/A converter, not being used, is set to "00₁₆". The resistor ladder in the A/D converter is excluded.
IvREF flows even if the VCUT bit in the AD0CON1 register is set to "0" (no VREF connection).

$$V_{CC1}=V_{CC2}=3.3V$$

Timing Requirements

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.24 External Clock Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
t_c	External Clock Input Cycle Time	41		ns
$t_{w(H)}$	External Clock Input High ("H") Width	18		ns
$t_{w(L)}$	External Clock Input Low ("L") Width	18		ns
t_r	External Clock Rise Time		5	ns
t_f	External Clock Fall Time		5	ns

Table 5.25 Memory Expansion Mode and Microprocessor Mode

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{ac1(RD-DB)}$	Data Input Access Time (RD standard)		(Note 1)	ns
$t_{ac1(AD-DB)}$	Data Input Access Time (AD standard, CS standard)		(Note 1)	ns
$t_{ac2(RD-DB)}$	Data Input Access Time (RD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{ac2(AD-DB)}$	Data Input Access Time (AD standard, when accessing a space with the multiplexed bus)		(Note 1)	ns
$t_{su(DB-BCLK)}$	Data Input Setup Time	30		ns
$t_{su(RDY-BCLK)}$	$\overline{RDY}$ Input Setup Time	40		ns
$t_{su(HOLD-BCLK)}$	$\overline{HOLD}$ Input Setup Time	60		ns
$t_{h(RD-DB)}$	Data Input Hold Time	0		ns
$t_{h(BCLK-RDY)}$	$\overline{RDY}$ Input Hold Time	0		ns
$t_{h(BCLK-HOLD)}$	$\overline{HOLD}$ Input Hold Time	0		ns
$t_{d(BCLK-HLDA)}$	HLDA Output Delay Time		25	ns

NOTE:

1. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles. Insert a wait state or lower the operation frequency, $f_{(BCLK)}$, if the calculated value is negative.

$$t_{ac1(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)+1)$$

$$t_{ac1(AD-DB)} = \frac{10^9 \times n}{f_{(BCLK)}} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, n=a+b)$$

$$t_{ac2(RD-DB)} = \frac{10^9 \times m}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, m=(bx2)-1)$$

$$t_{ac2(AD-DB)} = \frac{10^9 \times p}{f_{(BCLK)} \times 2} - 35 \quad [\text{ns}] \text{ (if external bus cycle is } a\phi + b\phi, p=\{(a+b-1)x2\}+1)$$

$$V_{CC1}=V_{CC2}=3.3V$$

Timing Requirements

($V_{CC1}=V_{CC2}= 3.0$ to $3.6V$, $V_{SS}= 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.26 Timer A Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	100		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	40		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	40		ns

Table 5.27 Timer A Input (Gate Input in Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	400		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	200		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	200		ns

Table 5.28 Timer A Input (External Trigger Input in One-Shot Timer Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TA)}$	TAiIN Input Cycle Time	200		ns
$t_{W(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.29 Timer A Input (External Trigger Input in Pulse Width Modulation Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(TAH)}$	TAiIN Input High ("H") Width	100		ns
$t_{W(TAL)}$	TAiIN Input Low ("L") Width	100		ns

Table 5.30 Timer A Input (Counter Increment/decrement Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(UP)}$	TAiOUT Input Cycle Time	2000		ns
$t_{W(UPH)}$	TAiOUT Input High ("H") Width	1000		ns
$t_{W(UPL)}$	TAiOUT Input Low ("L") Width	1000		ns
$t_{SU(UP-TIN)}$	TAiOUT Input Setup Time	400		ns
$t_{H(TIN-UP)}$	TAiOUT Input Hold Time	400		ns

$$V_{CC1}=V_{CC2}=3.3V$$

Timing Requirements

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS}=0V$ at $T_{opr}=-20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.31 Timer B Input (Count Source Input in Event Counter Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time (counted on one edge)	100		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width (counted on one edge)	40		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width (counted on one edge)	40		ns
$t_{C(TB)}$	TBiIN Input Cycle Time (counted on both edges)	200		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width (counted on both edges)	80		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width (counted on both edges)	80		ns

Table 5.32 Timer B Input (Pulse Period Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.33 Timer B Input (Pulse Width Measurement Mode)

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(TB)}$	TBiIN Input Cycle Time	400		ns
$t_{W(TBH)}$	TBiIN Input High ("H") Width	200		ns
$t_{W(TBL)}$	TBiIN Input Low ("L") Width	200		ns

Table 5.34 A/D Trigger Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(AD)}$	$\overline{AD_{TRG}}$ Input Cycle Time (required for trigger)	1000		ns
$t_{W(ADL)}$	$\overline{AD_{TRG}}$ Input Low ("L") Width	125		ns

Table 5.35 Serial I/O

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{C(CK)}$	CLKi Input Cycle Time	200		ns
$t_{W(CKH)}$	CLKi Input High ("H") Width	100		ns
$t_{W(CKL)}$	CLKi Input Low ("L") Width	100		ns
$t_{d(C-Q)}$	TxDi Output Delay Time		80	ns
$t_{h(C-Q)}$	TxDi Hold Time	0		ns
$t_{su(D-C)}$	RxDi Input Setup Time	30		ns
$t_{h(C-Q)}$	RxDi Input Hold Time	90		ns

Table 5.36 External Interrupt $\overline{INTi}$ Input

Symbol	Parameter	Standard		Unit
		Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ Input High ("H") Width	250		ns
$t_{W(INL)}$	$\overline{INTi}$ Input Low ("L") Width	250		ns

$$V_{CC1}=V_{CC2}=3.3V$$

Switching Characteristics

($V_{CC1}=V_{CC2}=3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.37 Memory Expansion Mode and Microprocessor Mode
(when accessing external memory space)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
$t_{d(BCLK-AD)}$	Address Output Delay Time	See Figure 5.1		18	ns
$t_{h(BCLK-AD)}$	Address Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-AD)}$	Address Output Hold Time (RD standard)		0		ns
$t_{h(WR-AD)}$	Address Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-CS)}$	Chip-Select Signal Output Delay Time			18	ns
$t_{h(BCLK-CS)}$	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
$t_{h(RD-CS)}$	Chip-Select Signal Output Hold Time (RD standard)		0		ns
$t_{h(WR-CS)}$	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
$t_{d(BCLK-RD)}$	RD Signal Output Delay Time			18	ns
$t_{h(BCLK-RD)}$	RD Signal Output Hold Time		-3		ns
$t_{d(BCLK-WR)}$	WR Signal Output Delay Time			18	ns
$t_{h(BCLK-WR)}$	WR Signal Output Hold Time		0		ns
$t_{d(DB-WR)}$	Data Output Delay Time (WR standard)		(Note 2)		ns
$t_{h(WR-DB)}$	Data Output Hold Time (WR standard)		(Note 1)		ns
$t_{w(WR)}$	WR Output Width		(Note 2)		ns

NOTES:

1. Values can be obtained from the following equations, according to BCLK frequency.

$$t_{h(WR-DB)} = \frac{10^9}{f_{(BCLK)} \times 2} - 20 \quad [ns]$$

$$t_{h(WR-AD)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

$$t_{h(WR-CS)} = \frac{10^9}{f_{(BCLK)} \times 2} - 10 \quad [ns]$$

2. Values can be obtained from the following equations, according to BCLK frequency and external bus cycles.

$$t_{w(WR)} = \frac{10^9 \times n}{f_{(BCLK)} \times 2} - 15 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=(b \times 2)-1)$$

$$t_{d(DB-WR)} = \frac{10^9 \times m}{f_{(BCLK)}} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=b)$$

$$V_{CC1}=V_{CC2}=3.3V$$

Switching Characteristics

($V_{CC1} = V_{CC2} = 3.0$ to $3.6V$, $V_{SS} = 0V$ at $T_{opr} = -20$ to $85^{\circ}C$ unless otherwise specified)

Table 5.38 Memory Expansion Mode and Microprocessor Mode
(when accessing an external memory space with the multiplexed bus)

Symbol	Parameter	Measurement Condition	Standard		Unit
			Min.	Max.	
td(BCLK-AD)	Address Output Delay Time	See Figure 5.1		18	ns
th(BCLK-AD)	Address Output Hold Time (BCLK standard)		0		ns
th(RD-AD)	Address Output Hold Time (RD standard)		(Note 1)		ns
th(WR-AD)	Address Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-CS)	Chip-Select Signal Output Delay Time			18	ns
th(BCLK-CS)	Chip-Select Signal Output Hold Time (BCLK standard)		0		ns
th(RD-CS)	Chip-Select Signal Output Hold Time (RD standard)		(Note 1)		ns
th(WR-CS)	Chip-Select Signal Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-RD)	RD Signal Output Delay Time			18	ns
th(BCLK-RD)	RD Signal Output Hold Time		-3		ns
td(BCLK-WR)	WR Signal Output Delay Time			18	ns
th(BCLK-WR)	WR Signal Output Hold Time		0		ns
td(DB-WR)	Data Output delay Time (WR standard)		(Note 2)		ns
th(WR-DB)	Data Output Hold Time (WR standard)		(Note 1)		ns
td(BCLK-ALE)	ALE Signal Output Delay Time (BCLK standard)			18	ns
th(BCLK-ALE)	ALE Signal Output Hold Time (BCLK standard)		-2		ns
td(AD-ALE)	ALE Signal Output Delay Time (address standard)		(Note 3)		ns
th(ALE-AD)	ALE Signal Output Hold Time (address standard)		(Note 4)		ns
tdZ(RD-AD)	Address Output Float Start Time			8	ns

NOTES:

1. Values can be obtained by the following equations, according to BCLK frequency.

$$th(RD - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - AD) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(RD - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - CS) = \frac{10^9}{f(BCLK) \times 2} - 10 \quad [ns]$$

$$th(WR - DB) = \frac{10^9}{f(BCLK) \times 2} - 20 \quad [ns]$$

2. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

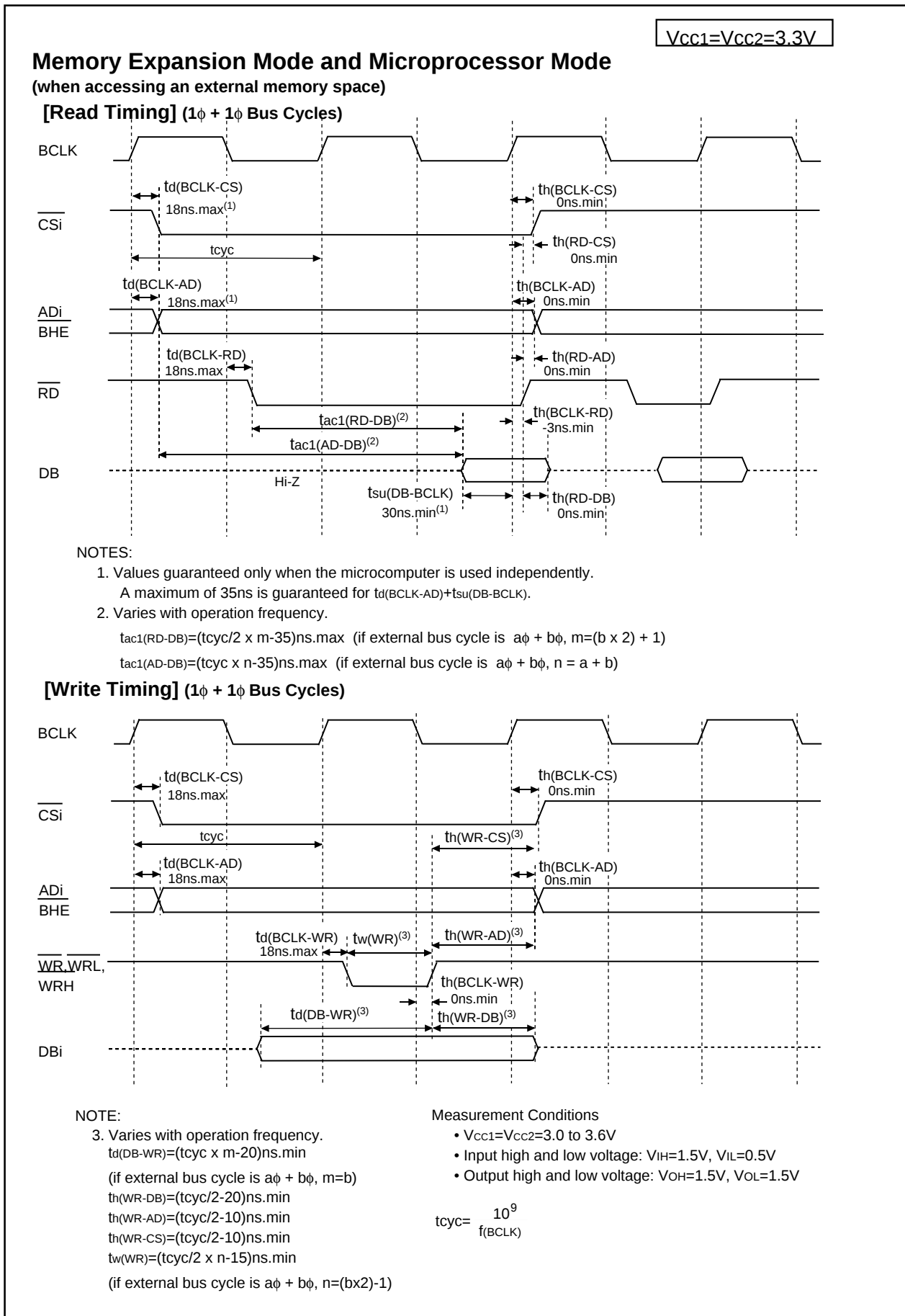
$$td(DB - WR) = \frac{10^9 \times m}{f(BCLK) \times 2} - 25 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, m=(b+2)-1)$$

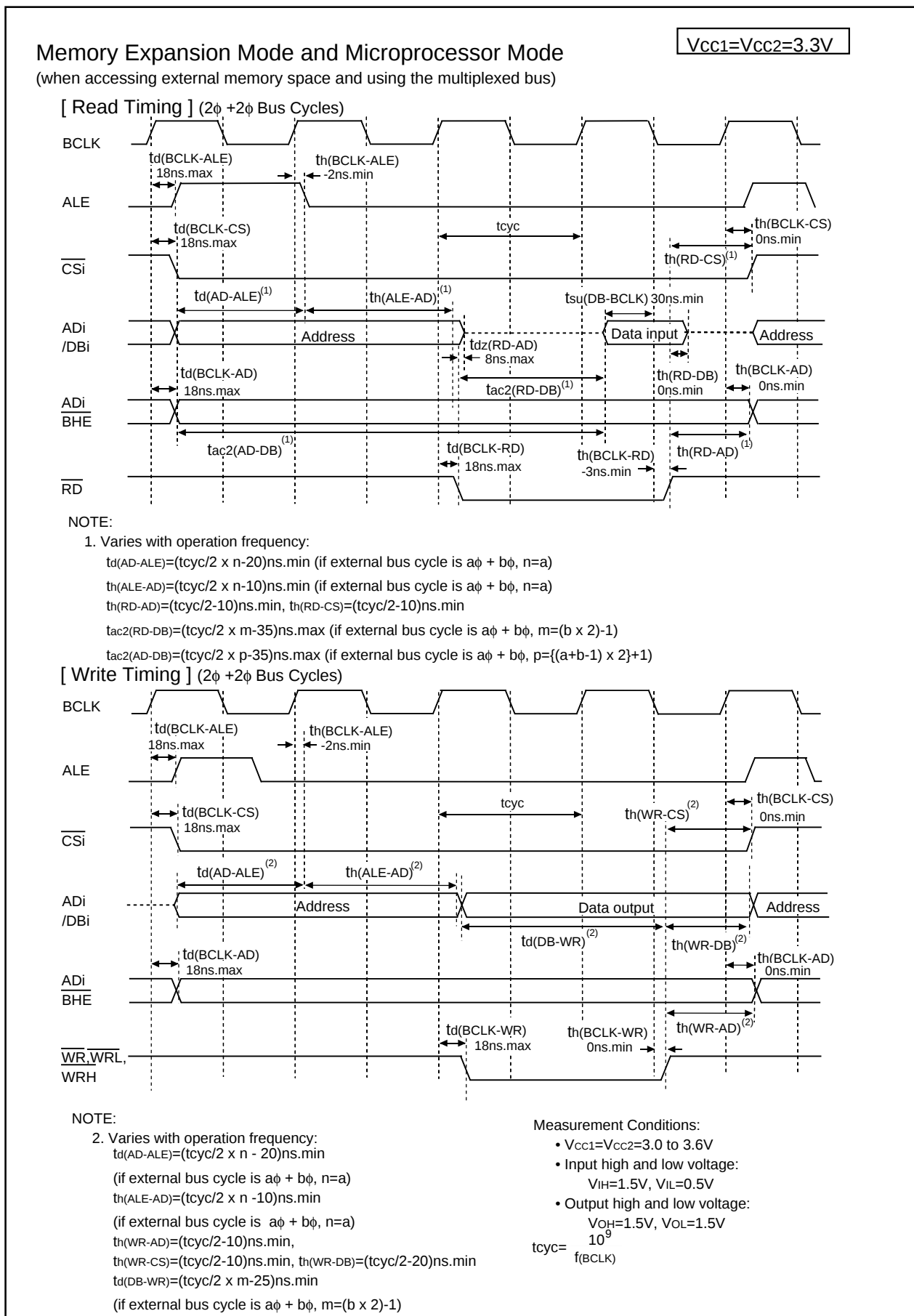
3. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

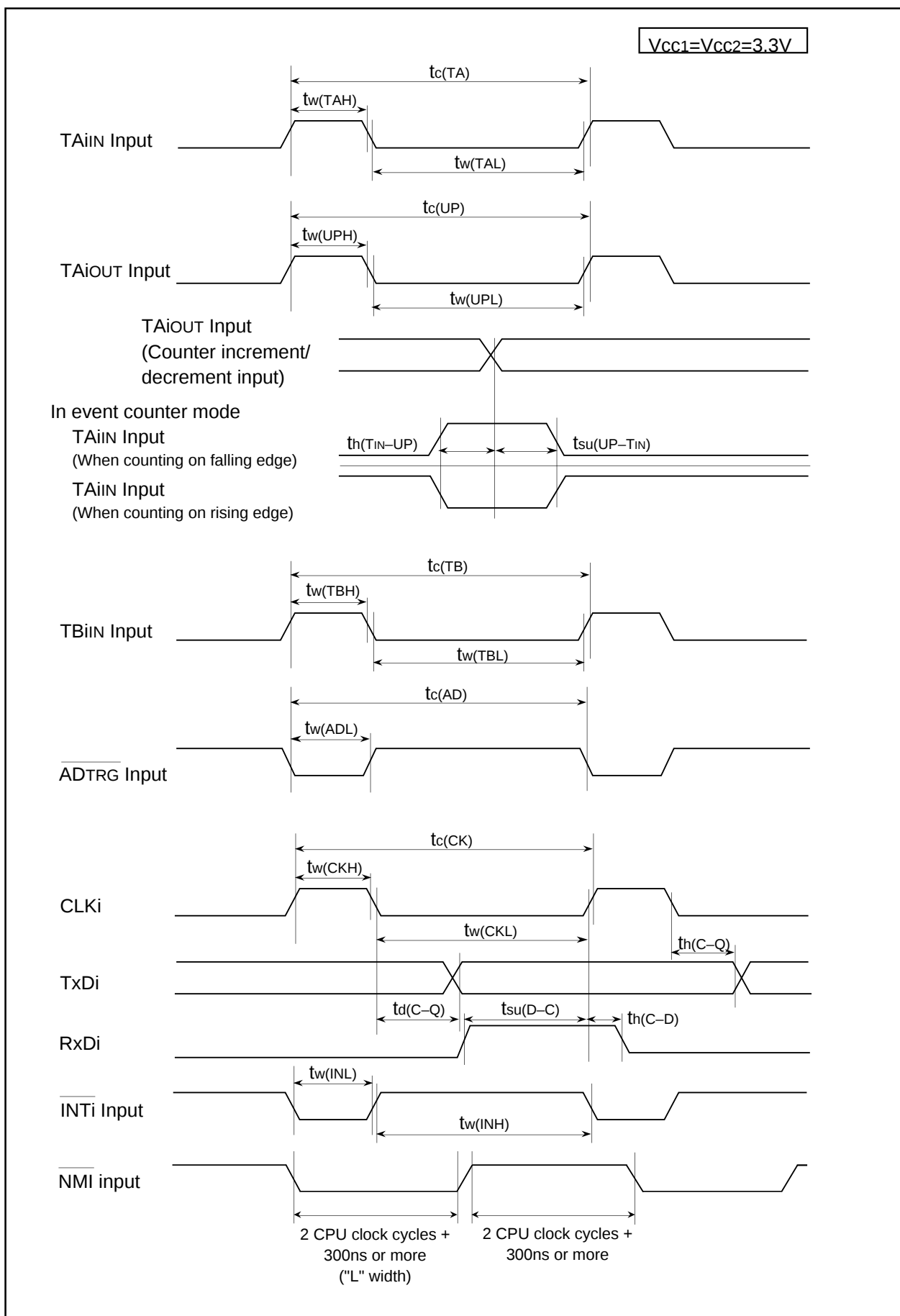
$$td(AD - ALE) = \frac{10^9 \times n}{f(BCLK) \times 2} - 20 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=a)$$

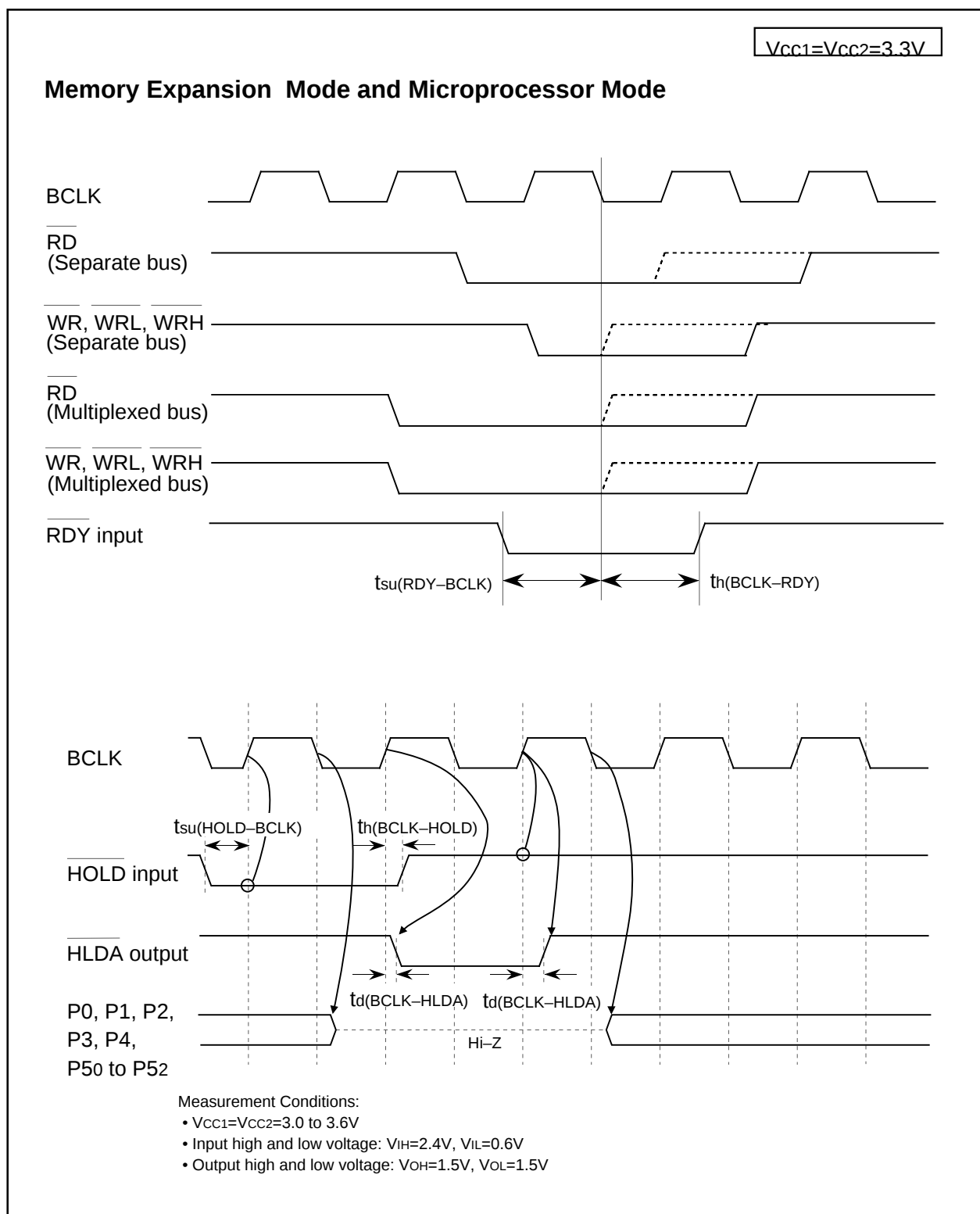
4. Values can be obtained by the following equations, according to BCLK frequency and external bus cycles.

$$th(ALE - AD) = \frac{10^9 \times n}{f(BCLK) \times 2} - 10 \quad [ns] \quad (\text{if external bus cycle is } a\phi + b\phi, n=a)$$

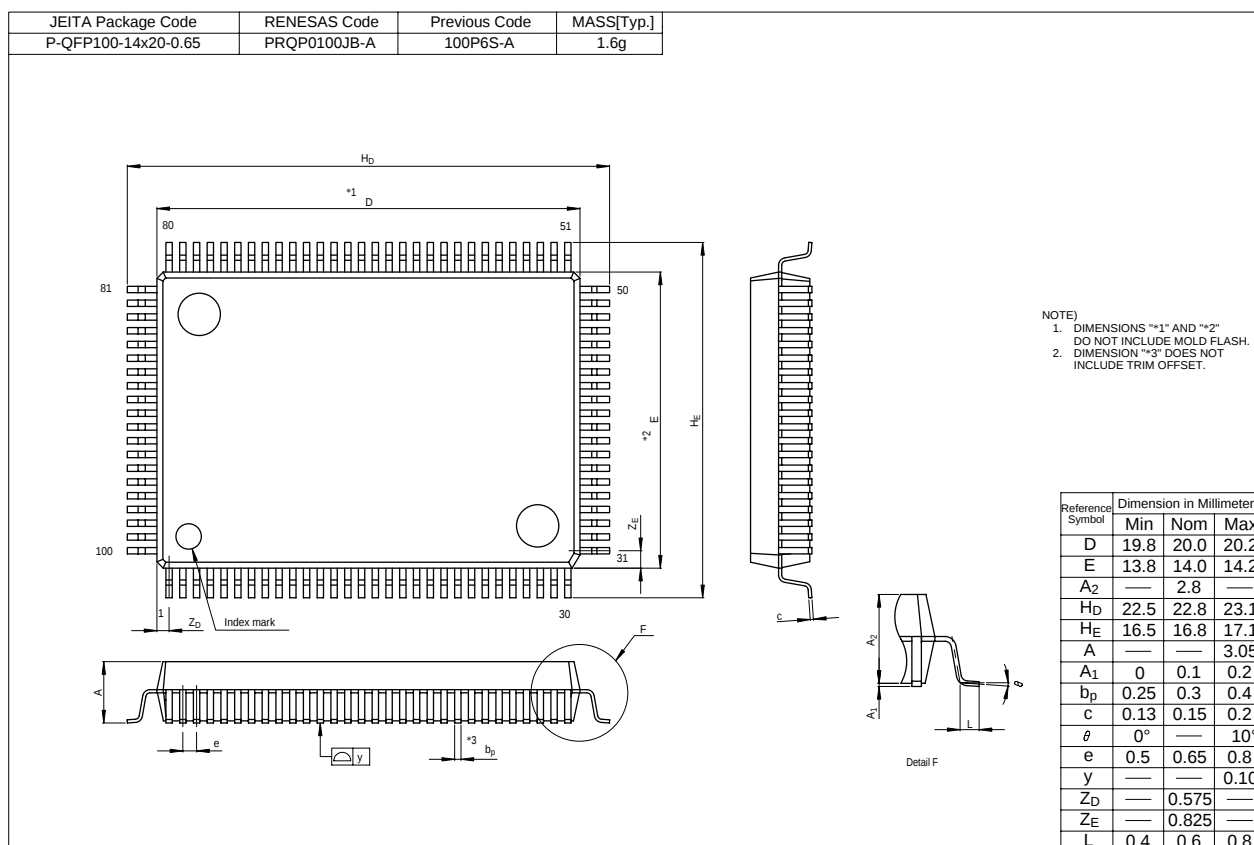
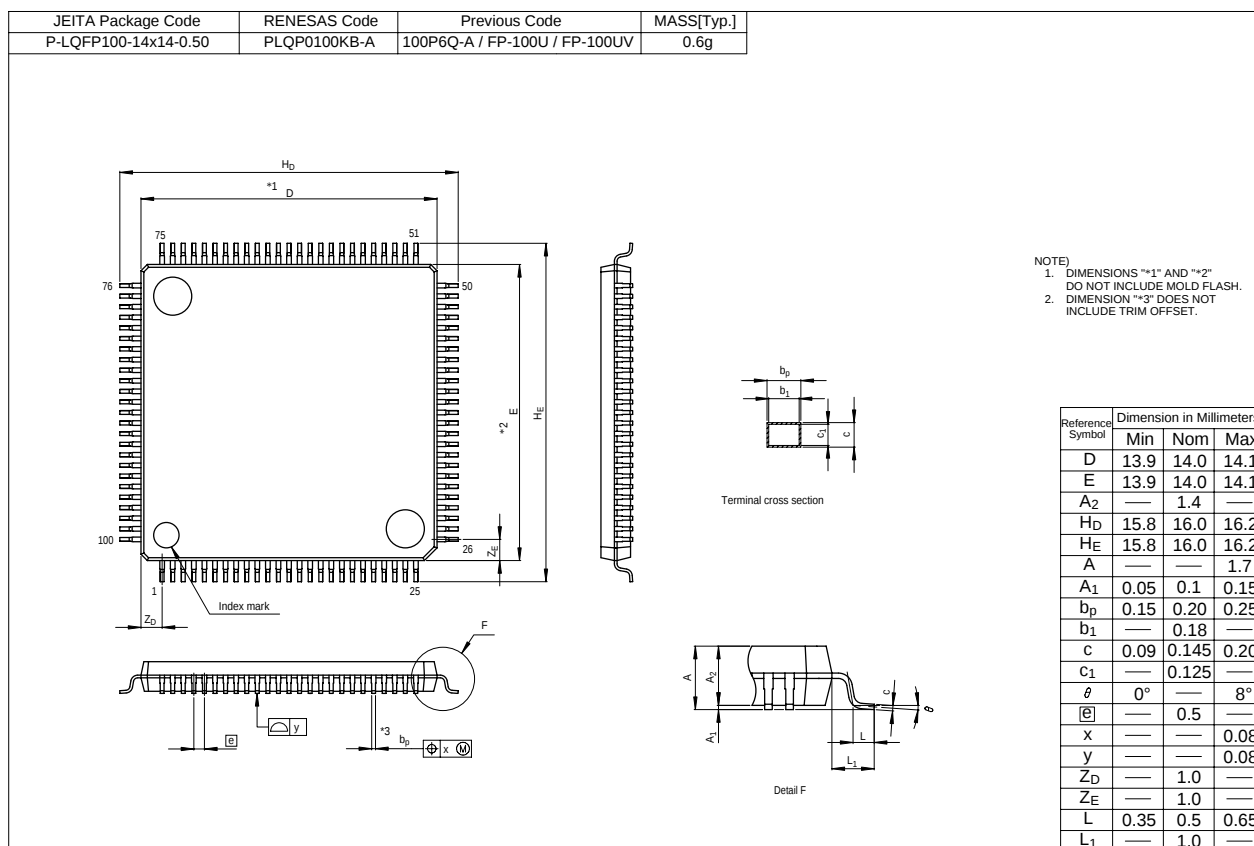
Figure 5.6 V_{CC1}=V_{CC2}=3.3V Timing Diagram (1)

Figure 5.7 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (2)

Figure 5.8 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (3)

Figure 5.9 $V_{CC1}=V_{CC2}=3.3V$ Timing Diagram (4)

Package Dimensions



REVISION HISTORY	M32C/80 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
0.10	Sep., 02	–	New Document
0.11	Sep., 02	3	Table 1.1.1 “CAN” deleted
0.12	Nov., 02	3	Table 1.1.1 “4.2 to 5.5V” --> “3.0 to 5.5V” “3.0 to 3.6V (f(XIN)=20MHz without software wait)” deleted “26mA (f(XIN)=20MHz without software wait,Vcc=3.3V)” deleted
0.30	Aug., 02	–	1. Overview 1.2 Performance Outline 1.3 Block Diagram 1.5 Pin Assignments Table 1.3 Pin Characteristics for 100-Pin Package 1.6 Pin Description 2. Central Processing Unit (CPU) 3. Memory 4. Special Function Registers (SFR) changed changed added changed changed added added added added
0.40	Jun., 04	All pages	Words standardized: On-chip oscillator, A/D converter and D/A converter
1.00	Nov., 04	2, 3 4 5 11 23 16- 16 29	Overview • Table 1.1 and 1.2 M32C/80 Group Performance “When using 16-bit bus” added to I/O ports “Option” deleted from Serial I/O, I²C bus, and IEBus “Voltage Detection Circuit” added Value added to “Power Consumption” “Flash Memory” added • 1.3 Block Diagram Description deleted • Figure 1.2 ROM/RAM Capacity deleted • Table 1.3 M32C/85 Group Note1 deleted • Table 1.5 Pin Description Note 1 added to I/O ports Memory • Chapter Description modified • Figure 3.1 Memory Map modified SFR • “X: Nothing is assigned” modified to “X: Indeterminate” • “?: Indeterminate” modified to “X: Indeterminate” • “Users cannot use any symbols with *” deleted • Register names, symbols, value after RESET of addresses 0017₁₆, 001B₁₆, 001F₁₆, 002B₁₆, 002F₁₆, 004C₁₆, and 004D₁₆ deleted • Value after RESET in the PM0 register revised • Note 3 deleted • Note 1 added to addresses 03E0₁₆ to 03EB₁₆

REVISION HISTORY	M32C/80 Group Datasheet
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Rev.	Date	Description	
		Page	Summary
		30-	Electrical Characteristics • This chapter added
1.10	Nov., 05	All pages	Package code changed: 100P6Q-A to PLQP0100KB-A and 100P6S-A to PRQP0100JB-A
		1	Overview • Note that the M32C/80 Group is ROMless device added
		2	
		3	
		9	
			Table 1.1 M32C/80 Group Performance Item "HDLC Data Processing" changed to "Intelligent I/O Communication Function"; item "Flash Memory" deleted
			Figure 1.1 M32C/80 Group Block Diagram Notes 1 and 2 added
			Table 1.4 Pin Description Supply voltage for analog power supply input modified "-" to "Vcc1"; description for CNVss changed; supply voltage for $\overline{\text{INT}}$ interrupt input modified; note for I/O ports added
		15	Memory • Figure 3.1 Memory Map Diagram changed; note added
		16	Special Function Registers (SFRs) • Note 2 deleted
		17	
		19	
		20	
		21	
		26	
		27, 28	
		28	
		30-	Electrical Characteristics • Ports P11 to P15 deleted
		32	
		33	
		34	
		35	
		41	
		42	
		46	
		47	
		52	
			Table 5.2 Recommended Operating Conditions $f(\text{BCLK})$ standard added
			Table 5.3 Electrical Characteristics Max. standard for ICC modified
			Table 5.4 A/D Conversion Characteristics AN00 to AN07 deleted from "INL" row
			Table 5.7 Memory Expansion Mode and Microprocessor Mode Expressions on note 1 corrected
			Figure 5.2 Vcc1=Vcc2=5V Timing Diagram (1) Expression for tcyc added; note 3 corrected
			Figure 5.3 Vcc1=Vcc2=5V Timing Diagram (2) Expression for tcyc added; notes 1 and 2 corrected
			Table 5.22 A/D Conversion Characteristics Min. standard for VREF modified
			Table 5.25 Memory Expansion Mode and Microprocessor Mode Expressions on note 1 corrected
			Figure 5.6 Vcc1=Vcc2=3.3V Timing Diagram (1) Expression for tcyc added; note 3 corrected

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Renesas Technology America, Inc.

450 Holger Way, San Jose, CA 95134-1368, U.S.A
Tel: <1> (408) 382-7500, Fax: <1> (408) 382-7501

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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
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Tel: <852> 2265-6688, Fax: <852> 2730-6071

Renesas Technology Taiwan Co., Ltd.

10th Floor, No.99, Fushing North Road, Taipei, Taiwan
Tel: <886> (2) 2715-2888, Fax: <886> (2) 2713-2999

Renesas Technology (Shanghai) Co., Ltd.

Unit2607 Ruijing Building, No.205 Maoming Road (S), Shanghai 200020, China
Tel: <86> (21) 6472-1001, Fax: <86> (21) 6415-2952

Renesas Technology Singapore Pte. Ltd.

1 Harbour Front Avenue, #06-10, Keppel Bay Tower, Singapore 098632
Tel: <65> 6213-0200, Fax: <65> 6278-8001

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Kukje Center Bldg. 18th Fl., 191, 2-ka, Hangang-ro, Yongsan-ku, Seoul 140-702, Korea
Tel: <82> 2-796-3115, Fax: <82> 2-796-2145

Renesas Technology Malaysia Sdn. Bhd.

Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No.18, Jalan Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: <603> 7955-9390, Fax: <603> 7955-9510