

To all our customers

Regarding the change of names mentioned in the document, such as Mitsubishi Electric and Mitsubishi XX, to Renesas Technology Corp.

The semiconductor operations of Hitachi and Mitsubishi Electric were transferred to Renesas Technology Corporation on April 1st 2003. These operations include microcomputer, logic, analog and discrete devices, and memory chips other than DRAMs (flash memory, SRAMs etc.)

Accordingly, although Mitsubishi Electric, Mitsubishi Electric Corporation, Mitsubishi Semiconductors, and other Mitsubishi brand names are mentioned in the document, these names have in fact all been changed to Renesas Technology Corp. Thank you for your understanding. Except for our corporate trademark, logo and corporate statement, no changes whatsoever have been made to the contents of the document, and these changes do not constitute any alteration to the contents of the document itself.

Note : Mitsubishi Electric will continue the business operations of high frequency & optical devices and power devices.

Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

MITSUBISHI MICROCOMPUTERS

M35044-XXXSP/FP

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

DESCRIPTION

The M35044-XXXSP/FP is a TV screen display control IC. It uses a silicon gate CMOS process and is housed in a 20-pin shrink DIP package (M35044-XXXSP) or a 20-pin shrink SOP package (M35044-XXXFP).

For M35044-001SP/FP that is a standard ROM version of M35044-XXXSP/FP respectively, the character pattern is also mentioned.

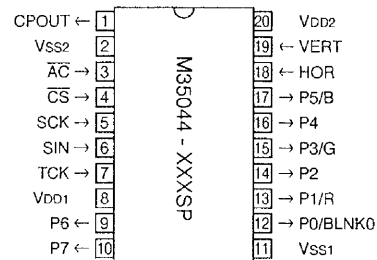
FEATURES

- Screen composition 24 columns × 12 lines
- Number of characters displayed 288 (Max.)
- Character composition 12 × 18 dot matrix
- Characters available 128 characters
- Character sizes available 4 (horizontal) × 4 (vertical)
- Display locations available
 - Horizontal direction 1000 locations
 - Vertical direction 1023 locations
- Blinking Character units
 - Cycle : division of vertical synchronization signal into 64 or 32
 - Duty : 25%, 50%, or 75%
- Data input By the 16-bit serial input function
- Coloring
 - Character color Character unit
 - Background coloring Character unit
 - Matrix-outline (shadow) coloring 8 colors (RGB output)
 - Specified by register
 - Border coloring 8 colors (RGB output)
 - Specified by register
 - Raster coloring 8 colors (RGB output)
 - Specified by register
- Blanking
 - Blanking off
 - Character size blanking
 - Border size blanking
 - Matrix-outline blanking
 - All blanking (all raster area)
- Output ports
 - 4 shared output ports (toggled between RGB output)
 - 4 dedicated output ports
- Display RAM erase function
- Display input frequency range Fosc = 20MHz-80MHz

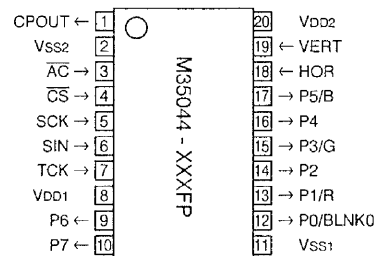
APPLICATION

Monitor

PIN CONFIGURATION (TOP VIEW)

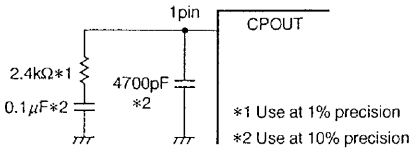


Outline 20P4B

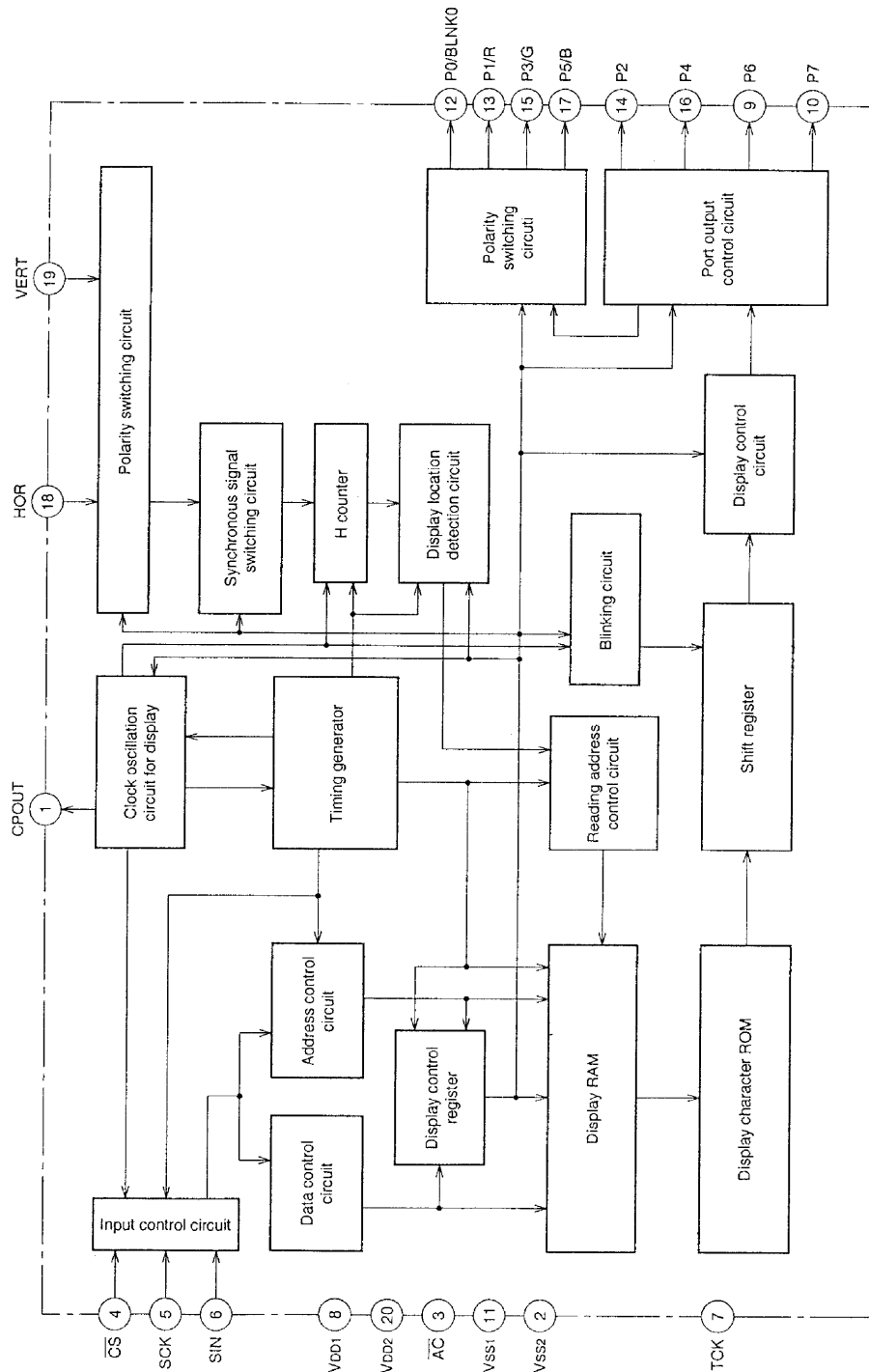


Outline 20P2Q-A

PIN DESCRIPTION

Pin Number	Symbol	Pin name	Input/Output	Function
1	CPOUT	Phase difference	Output	Connect loop filter to this pin.  *1 Use at 1% precision *2 Use at 10% precision
2	VSS2	Earthing pin	—	Please connect to GND using circuit earthing pin.
3	AC	Auto-clear input	Input	When "L", this pin resets the internal IC circuit. Hysteresis input. Includes built-in pull-up resistor.
4	CS	Chip select input	Input	This is the chip select pin, and when serial data transmission is being carried out, it goes to "L". Hysteresis input. Includes built-in pull-up resistor.
5	SCK	Serial clock input	Input	When CS pin is "L", SIN serial data is taken in when SCK rises. Hysteresis input. Built-in pull-up resistor is included.
6	SIN	Serial data input	Input	This is the pin for serial input of data and addresses for the display control register and the display data memory. Hysteresis input. Includes built-in pull-up resistor.
7	TCK	Test clock	Input	Input for test. Please connect to GND using circuit earthing pin.
8	VDD1	Power pin	—	Please connect to +5V with the power pin.
9	P6	Port P6 output	Output	This is the output port. Port data is set by PTD6.
10	P7	Port P7 output	Output	This is the output port. Port data is set by PTD7.
11	VSS1	Earthing pin	—	Please connect to GND using circuit earthing pin.
12	P0/BLNK0	Port P0 output	Output	This pin can be toggled between port pin output and BLNK0 signal output.
13	P1/R	Port P1 output	Output	This pin can be toggled between port pin output and R signal output.
14	P2	Port P2 output	Output	This is the output port. Port data is set by PTD2.
15	P3/G	Port P3 output	Output	This pin can be toggled between port pin output and G signal output.
16	P4	Port P4 output	Output	This is the output port. Port data is set by PTD4.
17	P5/B	Port P5 output	Output	This pin can be toggled between port pin output and B signal output.
18	HOR	Horizontal synchronization signal input	Input	This pin inputs the horizontal synchronization signal. Hysteresis input.
19	VERT	Vertical synchronization signal input	Input	This pin inputs the vertical synchronization signal. Hysteresis input.
20	VDD2	Power pin	—	Please connect to +5V with the power pin.

BLOCK DIAGRAM



SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

MEMORY CONSTITUTION

Address 000₁₆ to 11F₁₆ are assigned to the display RAM, address 120₁₆ to 128₁₆ are assigned to the display control registers. The internal circuit is reset and all display control registers (address 120₁₆ to 128₁₆) are set to "0" and display RAM (address 000₁₆ to 11F₁₆) are set to "FF₁₆" when the AC pin level is "L".

Memory constitution is shown in Figure 1.

SCREEN CONSTITUTION

The screen lines and rows are determined from each address of the display RAM. The screen constitution is shown in Figure 2.

	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0
000 ₁₆	0	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
⋮	⋮	Background coloring			Blinking	Character color			⋮	Character code						
11F ₁₆	0	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0
120 ₁₆	0	0	VJT	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0
121 ₁₆	0	0	PTD7	PTD6	PTD5	PTD4	PTD3	PTD2	PTD1	PTD0	PTC5	PTC4	PTC3	PTC2	PTC1	PTC0
122 ₁₆	0	0	SPACE2	SPACE1	SPACE0	TEST9	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0
123 ₁₆	0	0	TEST3	TEST2	TEST1	TEST0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0
124 ₁₆	0	0	TEST5	TEST4	DSP11	DSP10	DSP9	DSP8	DSP7	DSP6	DSP5	DSP4	DSP3	DSP2	DSP1	DSP0
125 ₁₆	0	0	VSZ1H1	VSZ1H0	VSZ1L1	VSZ1L0	V1SZ1	V1SZ0	LIN9	LIN8	LIN7	LIN6	LIN5	LIN4	LIN3	LIN2
126 ₁₆	0	0	VSZ2H1	VSZ2H0	VSZ2L1	VSZ2L0	V1SZ2	V1SZ0	LIN17	LIN16	LIN15	LIN14	LIN13	LIN12	LIN11	LIN10
127 ₁₆	0	0	HSZ21	HSZ20	HSZ11	HSZ10	BETA14	TEST8	TEST7	TEST6	FB	FG	FR	RB	RG	RR
128 ₁₆	0	0	BLINK2	BLINK1	BLINK0	DSPON	STOP	RAMERS	SYAD	BLK1	BLK0	POLH	POLV	VMASK	B/F	BCOL

Fig. 1 Memory constitution

Row Line	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
1	000 ₁₆	001 ₁₆	002 ₁₆	003 ₁₆	004 ₁₆	005 ₁₆	006 ₁₆	007 ₁₆	008 ₁₆	009 ₁₆	00A ₁₆	00B ₁₆	00C ₁₆	00D ₁₆	00E ₁₆	00F ₁₆	010 ₁₆	011 ₁₆	012 ₁₆	013 ₁₆	014 ₁₆	015 ₁₆	016 ₁₆	017 ₁₆
2	018 ₁₆	019 ₁₆	01A ₁₆	01B ₁₆	01C ₁₆	01D ₁₆	01E ₁₆	01F ₁₆	020 ₁₆	021 ₁₆	022 ₁₆	023 ₁₆	024 ₁₆	025 ₁₆	026 ₁₆	027 ₁₆	028 ₁₆	029 ₁₆	02A ₁₆	02B ₁₆	02C ₁₆	02D ₁₆	02E ₁₆	02F ₁₆
3	030 ₁₆	031 ₁₆	032 ₁₆	033 ₁₆	034 ₁₆	035 ₁₆	036 ₁₆	037 ₁₆	038 ₁₆	039 ₁₆	03A ₁₆	03B ₁₆	03C ₁₆	03D ₁₆	03E ₁₆	03F ₁₆	040 ₁₆	041 ₁₆	042 ₁₆	043 ₁₆	044 ₁₆	045 ₁₆	046 ₁₆	047 ₁₆
4	048 ₁₆	049 ₁₆	04A ₁₆	04B ₁₆	04C ₁₆	04D ₁₆	04E ₁₆	04F ₁₆	050 ₁₆	051 ₁₆	052 ₁₆	053 ₁₆	054 ₁₆	055 ₁₆	056 ₁₆	057 ₁₆	058 ₁₆	059 ₁₆	05A ₁₆	05B ₁₆	05C ₁₆	05D ₁₆	05E ₁₆	05F ₁₆
5	060 ₁₆	061 ₁₆	062 ₁₆	063 ₁₆	064 ₁₆	065 ₁₆	066 ₁₆	067 ₁₆	068 ₁₆	069 ₁₆	06A ₁₆	06B ₁₆	06C ₁₆	06D ₁₆	06E ₁₆	06F ₁₆	070 ₁₆	071 ₁₆	072 ₁₆	073 ₁₆	074 ₁₆	075 ₁₆	076 ₁₆	077 ₁₆
6	078 ₁₆	079 ₁₆	07A ₁₆	07B ₁₆	07C ₁₆	07D ₁₆	07E ₁₆	07F ₁₆	080 ₁₆	081 ₁₆	082 ₁₆	083 ₁₆	084 ₁₆	085 ₁₆	086 ₁₆	087 ₁₆	088 ₁₆	089 ₁₆	08A ₁₆	08B ₁₆	08C ₁₆	08D ₁₆	08E ₁₆	08F ₁₆
7	090 ₁₆	091 ₁₆	092 ₁₆	093 ₁₆	094 ₁₆	095 ₁₆	096 ₁₆	097 ₁₆	098 ₁₆	099 ₁₆	09A ₁₆	09B ₁₆	09C ₁₆	09D ₁₆	09E ₁₆	09F ₁₆	0A0 ₁₆	0A1 ₁₆	0A2 ₁₆	0A3 ₁₆	0A4 ₁₆	0A5 ₁₆	0A6 ₁₆	0A7 ₁₆
8	0A8 ₁₆	0A9 ₁₆	0AA ₁₆	0AB ₁₆	0AC ₁₆	0AD ₁₆	0AE ₁₆	0AF ₁₆	0B0 ₁₆	0B1 ₁₆	0B2 ₁₆	0B3 ₁₆	0B4 ₁₆	0B5 ₁₆	0B6 ₁₆	0B7 ₁₆	0B8 ₁₆	0B9 ₁₆	0BA ₁₆	0BB ₁₆	0BC ₁₆	0BD ₁₆	0BE ₁₆	0BF ₁₆
9	0C0 ₁₆	0C1 ₁₆	0C2 ₁₆	0C3 ₁₆	0C4 ₁₆	0C5 ₁₆	0C6 ₁₆	0C7 ₁₆	0C8 ₁₆	0C9 ₁₆	0CA ₁₆	0CB ₁₆	0CC ₁₆	0CD ₁₆	0CE ₁₆	0CF ₁₆	0D0 ₁₆	0D1 ₁₆	0D2 ₁₆	0D3 ₁₆	0D4 ₁₆	0D5 ₁₆	0D6 ₁₆	0D7 ₁₆
10	0D8 ₁₆	0D9 ₁₆	0DA ₁₆	0DB ₁₆	0DC ₁₆	0DD ₁₆	0DE ₁₆	0DF ₁₆	0E0 ₁₆	0E1 ₁₆	0E2 ₁₆	0E3 ₁₆	0E4 ₁₆	0E5 ₁₆	0E6 ₁₆	0E7 ₁₆	0E8 ₁₆	0E9 ₁₆	0EA ₁₆	0EB ₁₆	0EC ₁₆	0ED ₁₆	0EE ₁₆	0EF ₁₆
11	0F0 ₁₆	0F1 ₁₆	0F2 ₁₆	0F3 ₁₆	0F4 ₁₆	0F5 ₁₆	0F6 ₁₆	0F7 ₁₆	0F8 ₁₆	0F9 ₁₆	0FA ₁₆	0FB ₁₆	0FC ₁₆	0FD ₁₆	0FE ₁₆	0FF ₁₆	100 ₁₆	101 ₁₆	102 ₁₆	103 ₁₆	104 ₁₆	105 ₁₆	106 ₁₆	107 ₁₆
12	108 ₁₆	109 ₁₆	10A ₁₆	10B ₁₆	10C ₁₆	10D ₁₆	10E ₁₆	10F ₁₆	110 ₁₆	111 ₁₆	112 ₁₆	113 ₁₆	114 ₁₆	115 ₁₆	116 ₁₆	117 ₁₆	118 ₁₆	119 ₁₆	11A ₁₆	11B ₁₆	11C ₁₆	11D ₁₆	11E ₁₆	11F ₁₆

※ The hexadecimal numbers in the boxes show the display RAM address.

Fig. 2 Screen constitution

REGISTERS DESCRIPTION

(1) Address 120₁₆

DA	Register	Contents		Remarks																											
		Status	Function																												
0	DIV0	① 1	Set multiply value (frequency value) of horizontal synchronous frequency. $N1 = \sum_{n=0}^{10} (DIVn \times 2^n)$ N1: frequency value	Display frequency is computed as shown below. $FOSC = fH \times N1$ Fosc [MHz] : Display frequency fH [kHz] : Horizontal synchronous signal frequency to HOR pin. N1 : Shown left Set display frequency Fosc to within 20MHz to 80MHz range. When display frequency Fosc, set frequency value N2 in association with DIVS0 and DIVS1.																											
1	DIV1	① 1																													
2	DIV2	① 1																													
3	DIV3	① 1																													
4	DIV4	① 1																													
5	DIV5	① 1																													
6	DIV6	① 1																													
7	DIV7	① 1																													
8	DIV8	① 1																													
9	DIV9	① 1																													
A	DIV10	① 1																													
B	DIVS0	① 1	Set frequency value N2 <table><tr><th colspan="2">DIVS</th><th rowspan="2">Frequency value N2</th></tr><tr><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>Division into 2</td></tr><tr><td>0</td><td>1</td><td>Division into 3</td></tr><tr><td>1</td><td>0</td><td>Division into 4</td></tr><tr><td>1</td><td>1</td><td>Division into 6</td></tr></table>	DIVS		Frequency value N2	1	0	0	0	Division into 2	0	1	Division into 3	1	0	Division into 4	1	1	Division into 6	Set frequency value N2 in association with display frequency range. <table><tr><th>Display frequency</th><th>Frequency value N2</th></tr><tr><td>55 ~ 80MHz</td><td>Division into 2</td></tr><tr><td>40 ~ 55MHz</td><td>Division into 3</td></tr><tr><td>27.5 ~ 40MHz</td><td>Division into 4</td></tr><tr><td>20 ~ 27.5MHz</td><td>Division into 6</td></tr></table>	Display frequency	Frequency value N2	55 ~ 80MHz	Division into 2	40 ~ 55MHz	Division into 3	27.5 ~ 40MHz	Division into 4	20 ~ 27.5MHz	Division into 6
DIVS		Frequency value N2																													
1	0																														
0	0	Division into 2																													
0	1	Division into 3																													
1	0	Division into 4																													
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Display frequency	Frequency value N2																														
55 ~ 80MHz	Division into 2																														
40 ~ 55MHz	Division into 3																														
27.5 ~ 40MHz	Division into 4																														
20 ~ 27.5MHz	Division into 6																														
C	DIVS1	① 1																													
D	VJT	① 1	Normally set to "0". Reduce the continuous jitter of vertical direction.	The continuous jitter occurrence of display character vertical direction which is generated by overlapping of horizontal synchronous signal phase and vertical synchronous signal phase is able to be reduced.																											

Note: The mark ① around the status value means the reset status by the "L" level is input to AC pin.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(2) Address 12116

DA	Register	Contents		Remarks
		Status	Function	
0	PTC0	①	P0 output (port P0). Port data is set by PTD0.	BLNK0 outputs blanking signal. Blanking status is determined by BLK0, BLK1, and DSP0 to DSP11 settings.
		1	BLNK0 output. Polarity is set by PTD0.	
1	PTC1	①	P1 output (port P1). Port data is set by PTD1.	
		1	R signal output. Polarity is set by PTD1.	
2	PTC2	①	P2 output (port P2). Port data is set by PTD2.	
		1	Do not set.	
3	PTC3	①	P3 output (port P3). Port data is set by PTD3.	
		1	G signal output. Polarity is set by PTD3.	
4	PTC4	①	P4 output (port P4). Port data is set by PTD4.	
		1	Do not set.	
5	PTC5	①	P5 output (port P5). Port data is set by PTD5.	
		1	B signal output. Polarity is set by PTD5.	
6	PTD0	①	"L" output (P0 output) or negative polarity output (BLNK0 output).	P0 pin data control.
		1	"H" output (P0 output) or positive polarity output (BLNK0 output).	
7	PTD1	①	"L" output (P1 output) or negative polarity output (R signal output).	P1 pin data control.
		1	"H" output (P1 output) or positive polarity output (R signal output).	
8	PTD2	①	"L" output (P2 output).	P2 pin exclusive port output state control.
		1	"H" output (P2 output).	
9	PTD3	①	"L" output (P3 output) or negative polarity output (G signal output).	P3 pin data control.
		1	"H" output (P3 output) or positive polarity output (G signal output).	
A	PTD4	①	"L" output (P4 output).	P4 pin exclusive port output state control.
		1	"H" output (P4 output).	
B	PTD5	①	"L" output (P5 output) or negative polarity output (B signal output).	P5 pin data control.
		1	"H" output (P5 output) or positive polarity output (B signal output).	
C	PTD6	①	"L" output (P6 output).	P6 pin exclusive port output state control.
		1	"H" output (P6 output).	
D	PTD7	①	"L" output (P7 output).	P7 pin exclusive port output state control.
		1	"H" output (P7 output).	

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(3) Address 122₁₆

DA	Register	Contents		Remarks																																						
		Status	Function																																							
0	HP0 (LSB)	①	If HS is the horizontal display start location, $HS = T \times (\sum_{n=0}^9 2^n HP_n + N).$ T: The cycle of display frequency <table border="1"><tr><th>HSZ11</th><th>HSZ10</th><th rowspan="2">N</th></tr><tr><th>HSZ21</th><th>HSZ20</th></tr><tr><td>0</td><td>0</td><td>6</td></tr><tr><td>0</td><td>1</td><td>7</td></tr><tr><td>1</td><td>0</td><td>8</td></tr><tr><td>1</td><td>1</td><td>9</td></tr></table> 1000 settings are possible.	HSZ11	HSZ10	N	HSZ21	HSZ20	0	0	6	0	1	7	1	0	8	1	1	9																						
		HSZ11		HSZ10	N																																					
HSZ21	HSZ20																																									
0	0	6																																								
0	1	7																																								
1	0	8																																								
1	1	9																																								
1	HP1	①																																								
2	HP2	①																																								
		1																																								
3	HP3	①																																								
		1																																								
4	HP4	①																																								
		1																																								
5	HP5	①																																								
		1																																								
6	HP6	①																																								
		1																																								
7	HP7	①																																								
		1																																								
8	HP8	①																																								
		1																																								
9	HP9 (MSB)	①																																								
		1																																								
A	TEST9	①	Must be cleared to "0".																																							
		1	Do not set.																																							
B	SPACE0	①	<table border="1"><tr><th colspan="3">SPACE</th><th rowspan="2">Number of Lines and Space ([S] represents space)</th></tr><tr><td>2</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>12</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1 [S] 10 [S] 1</td></tr><tr><td>0</td><td>1</td><td>0</td><td>2 [S] 8 [S] 2</td></tr><tr><td>0</td><td>1</td><td>1</td><td>3 [S] 6 [S] 3</td></tr><tr><td>1</td><td>0</td><td>0</td><td>4 [S] 4 [S] 4</td></tr><tr><td>1</td><td>0</td><td>1</td><td>5 [S] 2 [S] 5</td></tr><tr><td>1</td><td>1</td><td>0</td><td>6 [S] 6</td></tr><tr><td>1</td><td>1</td><td>1</td><td>6 [S] [S] 6</td></tr></table>	SPACE			Number of Lines and Space ([S] represents space)	2	1	0	0	0	0	12	0	0	1	1 [S] 10 [S] 1	0	1	0	2 [S] 8 [S] 2	0	1	1	3 [S] 6 [S] 3	1	0	0	4 [S] 4 [S] 4	1	0	1	5 [S] 2 [S] 5	1	1	0	6 [S] 6	1	1	1	6 [S] [S] 6
		SPACE			Number of Lines and Space ([S] represents space)																																					
2	1	0																																								
0	0	0		12																																						
0	0	1		1 [S] 10 [S] 1																																						
0	1	0		2 [S] 8 [S] 2																																						
0	1	1		3 [S] 6 [S] 3																																						
1	0	0		4 [S] 4 [S] 4																																						
1	0	1		5 [S] 2 [S] 5																																						
1	1	0		6 [S] 6																																						
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C	SPACE1	①																																								
		1																																								
D	SPACE2	①																																								
		1																																								

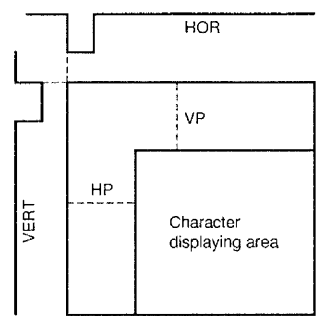
[S] represents one line worth of spaces.

Horizontal display start location is specified using the 10 bits from HP9 to HP0.
Note: HP9 to 0 = (0000000000₂) to (0000010111₂) setting is forbidden

Leave one line worth of space in the vertical direction.
For example, 6 [S] 6 indicates two sets of 6 lines with a line of spaces between lines 6 and 7.
A line is 18 × N horizontal scan lines.
N is determined by the character size in the vertical direction as follows:
×1 N = 1 ×2 N = 2
×3 N = 3 ×4 N = 4

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(4) Address 123:6

DA	Register	Contents		Remarks
		Status	Function	
0	VP0 (LSB)	① 1	If VS is the vertical display start location, $VS = H \times \left(\sum_{n=0}^9 2^n VP_n \right).$ H: Cycle with the horizontal synchronizing pulse 1023 settings are possible. 	The vertical start location is specified using the 10 bits from VP9 to VP0. VP9 to VP0 = (00000000002) setting is forbidden. Note 1: In case of B/F register is "0".
1	VP1	① 1		
2	VP2	① 1		
3	VP3	① 1		
4	VP4	① 1		
5	VP5	① 1		
6	VP6	① 1		
7	VP7	① 1		
8	VP8	① 1		
9	VP9 (MSB)	① 1		
A	TEST0	① 1	Must be cleared to "0". Do not set.	
B	TEST1	① 1	Must be cleared to "0". Do not set.	
C	TEST2	① 1	Must be cleared to "0". Do not set.	
D	TEST3	① 1	Must be cleared to "0". Do not set.	

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(5) Address 124₁₆

DA	Register	Contents		Remarks
		Status	Function	
0	DSP0	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 1.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
1	DSP1	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 2.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
2	DSP2	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 3.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
3	DSP3	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 4.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
4	DSP4	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 5.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
5	DSP5	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 6.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
6	DSP6	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 7.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
7	DSP7	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 8.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
8	DSP8	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 9.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
9	DSP9	①	Blanking is in the display mode specified by BLK0 and BLK1. (Note)	Sets the display mode of line 10.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
A	DSP10	①	Blanking is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 11.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
B	DSP11	①	Blanking is in the display mode specified by BLK0 and BLK1.	Sets the display mode of line 12.
		1	Blanking is in the display mode specified by except BLK0 and BLK1.	
C	TEST4	①	Must be cleared to "0".	
		1	Do not set.	
D	TEST5	①	Must be cleared to "0".	
		1	Do not set.	

Note: Refer to DISPLAY FORM1.

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(6) Address 125₁₆

DA	Register	Contents		Remarks												
		Status	Function													
0	LIN2	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 2nd line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
1	LIN3	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 3rd line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
2	LIN4	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 4th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
3	LIN5	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 5th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
4	LIN6	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 6th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
5	LIN7	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 7th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
6	LIN8	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 8th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
7	LIN9	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 9th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
8	V1SZ0	①	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction for the 1st line. (display monitor 1 ~ 12 line)												
		1	<table><tr><td>V1SZ1</td><td>V1SZ0</td><td>Vertical direction size</td></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>		V1SZ1	V1SZ0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
V1SZ1	V1SZ0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
9	V1SZ1	①	<table><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot				
		0	1	2H/dot												
1	0	3H/dot														
1	1	4H/dot														
1	<table><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	1	1	4H/dot												
1	1	4H/dot														
A	VSZ1L0	①	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 1 line) at "0" state in register LIN2 ~ LIN17.												
		1	<table><tr><td>VSZ1L1</td><td>VSZ1L0</td><td>Vertical direction size</td></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>		VSZ1L1	VSZ1L0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ1L1	VSZ1L0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
B	VSZ1L1	①	<table><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot				
		0	1	2H/dot												
1	0	3H/dot														
1	1	4H/dot														
1	<table><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	1	1	4H/dot												
1	1	4H/dot														
C	VSZ1H0	①	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor 1 line) at "1" state in register LIN2 ~ LIN17.												
		1	<table><tr><td>VSZ1H1</td><td>VSZ1H0</td><td>Vertical direction size</td></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>		VSZ1H1	VSZ1H0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ1H1	VSZ1H0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
D	VSZ1H1	①	<table><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	0	1	2H/dot	1	0	3H/dot	1	1	4H/dot				
		0	1	2H/dot												
1	0	3H/dot														
1	1	4H/dot														
1	<table><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>	1	1	4H/dot												
1	1	4H/dot														

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(7) Address 126₁₆

DA	Register	Contents		Remarks												
		Status	Function													
0	LIN10	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 10th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
1	LIN11	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 11th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
2	LIN12	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 12th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
3	LIN13	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 13th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
4	LIN14	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 14th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
5	LIN15	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 15th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
6	LIN16	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 16th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
7	LIN17	①	The first line is set by VSZ1L0 and VSZ1L1. The second to 12th lines are set by VSZ2L0 and VSZ2L1.	Character size setting in the vertical direction for the 17th line.												
		1	The first line is set by VSZ1H0 and VSZ1H1. The second to 12th lines are set by VSZ2H0 and VSZ2H1.													
8	V18SZ0	①	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction for the 18th line. (display monitor 1 ~ 12 line)												
		1	<table><tr><td>V18SZ1</td><td>V18SZ0</td><td>Vertical direction size</td></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>		V18SZ1	V18SZ0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
V18SZ1	V18SZ0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
9	V18SZ1	①														
		1														
A	VSZ2L0	①	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor for 2 ~ 12 line) at "0" state in register LIN2 ~ LIN17.												
		1	<table><tr><td>VSZ2L1</td><td>VSZ2L0</td><td>Vertical direction size</td></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>		VSZ2L1	VSZ2L0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ2L1	VSZ2L0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
B	VSZ2L1	①														
		1														
C	VSZ2H0	①	H: Cycle with the horizontal synchronizing pulse	Character size setting in the vertical direction (display monitor for 2 ~ 12 line) at "1" state in register LIN2 ~ LIN17.												
		1	<table><tr><td>VSZ2H1</td><td>VSZ2H0</td><td>Vertical direction size</td></tr><tr><td>0</td><td>0</td><td>1H/dot</td></tr><tr><td>0</td><td>1</td><td>2H/dot</td></tr><tr><td>1</td><td>0</td><td>3H/dot</td></tr><tr><td>1</td><td>1</td><td>4H/dot</td></tr></table>		VSZ2H1	VSZ2H0	Vertical direction size	0	0	1H/dot	0	1	2H/dot	1	0	3H/dot
VSZ2H1	VSZ2H0	Vertical direction size														
0	0	1H/dot														
0	1	2H/dot														
1	0	3H/dot														
1	1	4H/dot														
D	VSZ2H1	①														
		1														

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(8) Address 127₁₆

DA	Register	Contents				Remarks																																					
		Status	Function																																								
0	RR	①	<table><tr><th>RB</th><th>RG</th><th>RR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>				RB	RG	RR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the color of all blankings.
		RB	RG	RR	Color																																						
0	0	0	Black																																								
0	0	1	Red																																								
0	1	0	Green																																								
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1	1	0	Cyan																																								
1	1	1	White																																								
1	1	1	1	1	1																																						
1	RG	①	<table><tr><th>RB</th><th>RG</th><th>RR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>				RB	RG	RR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the Border size, or the shadow size.
		RB	RG	RR	Color																																						
0	0	0	Black																																								
0	0	1	Red																																								
0	1	0	Green																																								
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1	0	1	Magenta																																								
1	1	0	Cyan																																								
1	1	1	White																																								
1	1	1	1	1	1																																						
2	RB	①	<table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>				BB	BG	BR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the Border size, or the shadow size.
		BB	BG	BR	Color																																						
0	0	0	Black																																								
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1	1	1	White																																								
1	1	1	1	1	1																																						
3	FR	①	<table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>				BB	BG	BR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the Border size, or the shadow size.
		BB	BG	BR	Color																																						
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0	0	1	Red																																								
0	1	0	Green																																								
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1	0	0	Blue																																								
1	0	1	Magenta																																								
1	1	0	Cyan																																								
1	1	1	White																																								
1	1	1	1	1	1																																						
4	FG	①	<table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>				BB	BG	BR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the Border size, or the shadow size.
		BB	BG	BR	Color																																						
0	0	0	Black																																								
0	0	1	Red																																								
0	1	0	Green																																								
0	1	1	Yellow																																								
1	0	0	Blue																																								
1	0	1	Magenta																																								
1	1	0	Cyan																																								
1	1	1	White																																								
1	1	1	1	1	1																																						
5	FB	①	<table><tr><th>BB</th><th>BG</th><th>BR</th><th>Color</th></tr><tr><td>0</td><td>0</td><td>0</td><td>Black</td></tr><tr><td>0</td><td>0</td><td>1</td><td>Red</td></tr><tr><td>0</td><td>1</td><td>0</td><td>Green</td></tr><tr><td>0</td><td>1</td><td>1</td><td>Yellow</td></tr><tr><td>1</td><td>0</td><td>0</td><td>Blue</td></tr><tr><td>1</td><td>0</td><td>1</td><td>Magenta</td></tr><tr><td>1</td><td>1</td><td>0</td><td>Cyan</td></tr><tr><td>1</td><td>1</td><td>1</td><td>White</td></tr></table>				BB	BG	BR	Color	0	0	0	Black	0	0	1	Red	0	1	0	Green	0	1	1	Yellow	1	0	0	Blue	1	0	1	Magenta	1	1	0	Cyan	1	1	1	White	Sets the blanking color of the Border size, or the shadow size.
		BB	BG	BR	Color																																						
0	0	0	Black																																								
0	0	1	Red																																								
0	1	0	Green																																								
0	1	1	Yellow																																								
1	0	0	Blue																																								
1	0	1	Magenta																																								
1	1	0	Cyan																																								
1	1	1	White																																								
1	1	1	1	1	1																																						
6	TEST6	①	Must be cleared to "0".																																								
		1	Do not set.																																								
7	TEST7	①	Must be cleared to "0".																																								
		1	Do not set.																																								
8	TEST8	①	Must be cleared to "0".																																								
		1	Do not set.																																								
9	BETA14	①	Matrix-outline display (12 × 18 dot)				Set this register to the character font set by display RAM BR, BG and BB.																																				
		1	Matrix-outline display (14 × 18 dot)																																								
A	HSZ10	①	T: Display frequency cycle				Character size setting in the vertical direction for the first line.																																				
		1	<table><tr><th>HSZ11</th><th>HSZ10</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table>					HSZ11	HSZ10	Vertical direction size	0	0	1T/dot	0	1	2T/dot	1	0	3T/dot	1	1	4T/dot																					
HSZ11	HSZ10	Vertical direction size																																									
0	0	1T/dot																																									
0	1	2T/dot																																									
1	0	3T/dot																																									
1	1	4T/dot																																									
B	HSZ11	①																																									
		1																																									
C	HSZ20	①	T: Display frequency cycle				Character size setting in the vertical direction for the 2nd line to 12th line.																																				
		1	<table><tr><th>VSZ21</th><th>HSZ20</th><th>Vertical direction size</th></tr><tr><td>0</td><td>0</td><td>1T/dot</td></tr><tr><td>0</td><td>1</td><td>2T/dot</td></tr><tr><td>1</td><td>0</td><td>3T/dot</td></tr><tr><td>1</td><td>1</td><td>4T/dot</td></tr></table>					VSZ21	HSZ20	Vertical direction size	0	0	1T/dot	0	1	2T/dot	1	0	3T/dot	1	1	4T/dot																					
VSZ21	HSZ20	Vertical direction size																																									
0	0	1T/dot																																									
0	1	2T/dot																																									
1	0	3T/dot																																									
1	1	4T/dot																																									
D	HSZ21	①																																									
		1																																									

SCREEN CHARACTER and PATTERN DISPLAY CONTROLLERS

(9) Address 128₁₆

DA	Register	Contents		Remarks																	
		Status	Function																		
0	BCOL	①	Blanking of BLK0, BLK1	Sets all raster blanking																	
		1	All raster blanking																		
1	B/F	①	Synchronize with the leading edge of horizontal synchronization.	Synchronize with the front porch or back porch of the horizontal synchronazation signal.																	
		1	Synchronize with the trailing edge of horizontal synchronization.																		
2	VMASK	①	Do not mask by VERT input signal	This register has or do not have mask at phase comparison operating.																	
		1	Mask by VERT input signal																		
3	POLV	①	VERT pin polarity is negative electrode	Set VERT pin polarity.																	
		1	VERT pin polarity is positive electrode																		
4	POLH	①	HOR pin polarity is negative electrode	Set HOR pin polarity.																	
		1	HOR pin polarity is positive electrode																		
5	BLK0	①	<table><tr><th colspan="2">BLK</th><th rowspan="2">Blanking mode</th></tr><tr><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table>	BLK		Blanking mode	1	0	0	0	Matrix-outline size	0	1	Character size	1	0	Border size	1	1	Matrix-outline size	Set blanking mode. (Note 1) An example of blanking mode at BCOL = "0", DSPn = "0" (n = 0 ~ 11) shown left.
BLK		Blanking mode																			
1	0																				
0	0	Matrix-outline size																			
0	1	Character size																			
1	0	Border size																			
1	1	Matrix-outline size																			
6	BLK1	①	<table><tr><th colspan="2">BLK</th><th rowspan="2">Blanking mode</th></tr><tr><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>Matrix-outline size</td></tr><tr><td>0</td><td>1</td><td>Character size</td></tr><tr><td>1</td><td>0</td><td>Border size</td></tr><tr><td>1</td><td>1</td><td>Matrix-outline size</td></tr></table>	BLK		Blanking mode	1	0	0	0	Matrix-outline size	0	1	Character size	1	0	Border size	1	1	Matrix-outline size	
BLK		Blanking mode																			
1	0																				
0	0	Matrix-outline size																			
0	1	Character size																			
1	0	Border size																			
1	1	Matrix-outline size																			
7	SYAD	①	Border display of character	(Note 2)																	
		1	Shadow display of character																		
8	RAMERS	①	RAM not erased	There is no need to reset because there is no register for this bit.																	
		1	RAM erased																		
9	STOP	①	Oscillation of clock for display	R, G, B and BLNK0 output can be altered.																	
		1	Stop the oscillation of clock for display																		
A	DSPON	①	Display OFF	Display can be altered.																	
		1	Display ON																		
B	BLINK0	①	<table><tr><th colspan="2">BLINK</th><th rowspan="2">Duty</th></tr><tr><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>Blinking OFF</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table>	BLINK		Duty	1	0	0	0	Blinking OFF	0	1	25%	1	0	50%	1	1	75%	Blinking duty ratio can be altered.
		BLINK		Duty																	
1	0																				
0	0	Blinking OFF																			
0	1	25%																			
1	0	50%																			
1	1	75%																			
C	BLINK1	①	<table><tr><th colspan="2">BLINK</th><th rowspan="2">Duty</th></tr><tr><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>Blinking OFF</td></tr><tr><td>0</td><td>1</td><td>25%</td></tr><tr><td>1</td><td>0</td><td>50%</td></tr><tr><td>1</td><td>1</td><td>75%</td></tr></table>	BLINK		Duty	1	0	0	0	Blinking OFF	0	1	25%	1	0	50%	1	1	75%	
		BLINK		Duty																	
1	0																				
0	0	Blinking OFF																			
0	1	25%																			
1	0	50%																			
1	1	75%																			
D	BLINK2	①	Divided into 64 of vertical synchronous signal	Blinking frequency can be altered.																	
		1	Divided into 32 of vertical synchronous signal																		

Notes 1: Refer to DISPLAY FORM 1

2: Refer to DISPLAY FORM 3

DISPLAY FORM1

Table 1 shows display form of blanking.

Table 1. Display mode

BCOL	Standard blanking		When the all of registers DSPn (Note 2) are set to "0"	When some of registers DSPi are set to "1"		BLNK0 output
	BLK1	BLK0		DSPn = 0	DSPn = 1	
0	0	0	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0" line DSPn = "1" line
	0	1	Character	Character	Border display color set: display RAM (Note 3)	DSPn = "0" line→Character size DSPn = "1" line→Border size
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	DSPn = "0" line→Border size DSPn = "1" line→Matrix-outline size
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	DSPn = "0" line→Matrix-outline size DSPn = "1" line→Character size
1 (Note 1)	0	0	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline and border display. color set: FR, FG, FB or display RAM (Note 4)	Matrix-outline display color set: display RAM (Note 3)	All blanking size
	0	1	Character	Character	Border display color set: display RAM (Note 3)	
	1	0	Border display color set: display RAM (Note 3)	Border display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	
	1	1	Matrix-outline display color set: display RAM (Note 3)	Matrix-outline display color set: display RAM (Note 3)	Character	

Notes 1: Color setting of raster area is set by register RR, RG and RB.

2: DSPn (n = 0 ~ 11)

3: Set by BR, BG and BB of display RAM.

4: Set border by register FR, FG and FB. Set matrix-outline by BR, BG and BB of display RAM.

Display form 2

M35044-XXXSP/FP has the following four display forms.

- (1) Character size
: Blanking same as the character size.
- (2) Border size
: Blanking the background as a size from character.
- (3) Matrix-outline size
: Blanking the background 12 × 18 dot.
When set register BETA14 to "1", setting of blanking the background 14 × 18 dot is possible.
- (4) All blanking size
: When set register BCOL to "1", all raster area is blanking.

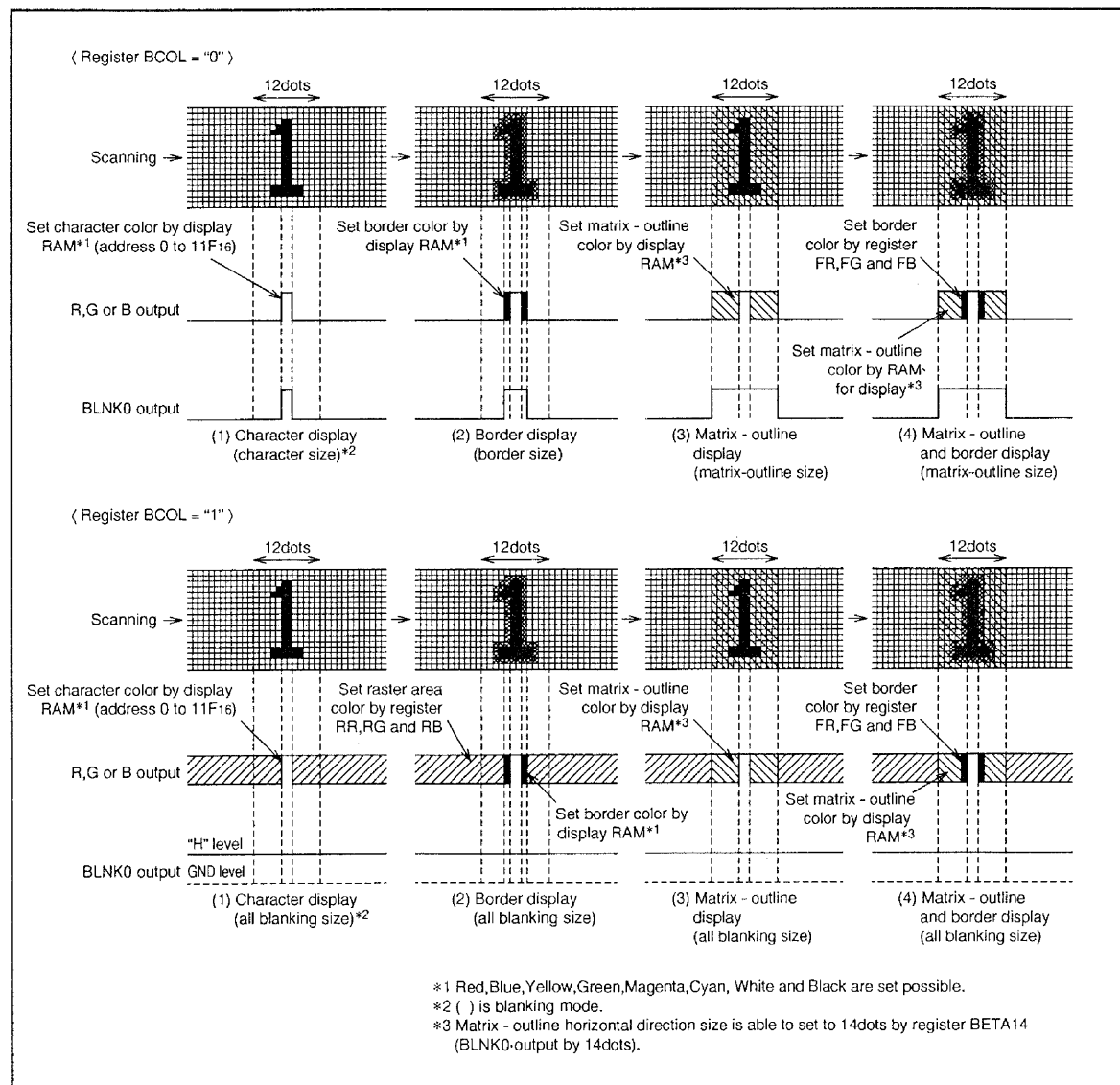


Fig. 3 Display form

Display form 3

When border display mode, if set SYAD = "0" to "1", it change to shadow display mode.

Border and shadow display are shown below.

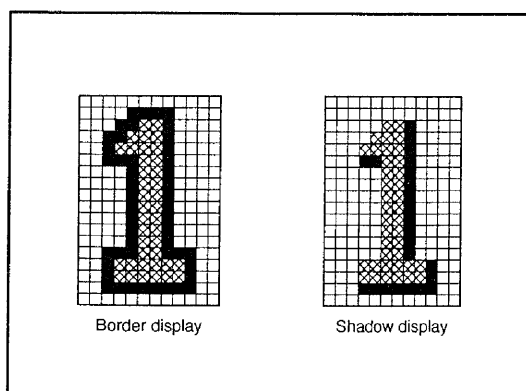


Fig. 4 Border and shadow display

Set shadow display color by display RAM or register FR, FG and FB.

DATA INPUT EXAMPLE

Data of display RAM and display control registers can be set by the serial input function. Example of data setting is shown in Figure 5.

Example of data setting by the serial input function (M35044-XXXSP/FP)																			
No.	Address/Data	DAF	DAE	DAD	DAC	DAB	DAA	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	Addition	
		200 msec hold																System set-up	
1	address 120 ₁₆	0	0	0	0	0	0	0	1	0	0	1	0	0	0	0	0	Address set	
2	data 120 ₁₆	0	0	1	DIVS1	DIVS0	DIV10	DIV9	DIV8	DIV7	DIV6	DIV5	DIV4	DIV3	DIV2	DIV1	DIV0	Setting frequency dividing value (Note 1)	
3	data 121 ₁₆	0	0	PTD7	PTD6	1	PTD4	1	PTD2	1	1	1	0	1	0	1	1	Output setting	
4	data 122 ₁₆	0	0	0	0	0	0	HP9	HP8	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	Horizontal display location setting	
5	data 123 ₁₆	0	0	0	0	0	0	VP9	VP8	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	Vertical display location setting	
6	data 124 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Display form setting	
7	data 125 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting	
8	data 126 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Character size setting	
9	data 127 ₁₆	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Color, character size setting	
10	data 128 ₁₆	0	0	0	0	0	0	0	1	0	1	1	POLH	POLV	0	0	0	Display OFF, display form (Note 2)	
		200 msec hold																	
11	data 000 ₁₆	0	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0	Character setting	
12 ⋮ 297	⋮	⋮	Character background color			Blinking	Character color			⋮	Character code								
298	data 11F ₁₆	0	BB	BG	BR	BLINK	B	G	R	0	C6	C5	C4	C3	C2	C1	C0		
299	address 128 ₁₆	0	0	0	0	0	0	0	1	0	0	1	0	1	0	0	0		Address setting
300	data 128 ₁₆	0	0	0	0	0	1	0	0	0	1	1	POLH	POLV	0	0	0	Display ON, display form (Note 2)	

Notes 1: Input horizontal synchronous signal to HOR pin.
2: Matrix-outline display in this data.

Fig. 5 Example of data setting by the serial input function

SERIAL DATA INPUT TIMING

- (1) Serial data should be input with the LSB first.
- (2) The address consists of 16 bits.
- (3) The data consists of 16 bits.
- (4) The 16 bits in the SCK after the $\overline{CS}$ signal has fallen are the address, and for succeeding input data, the address is incremented every 16 bits.

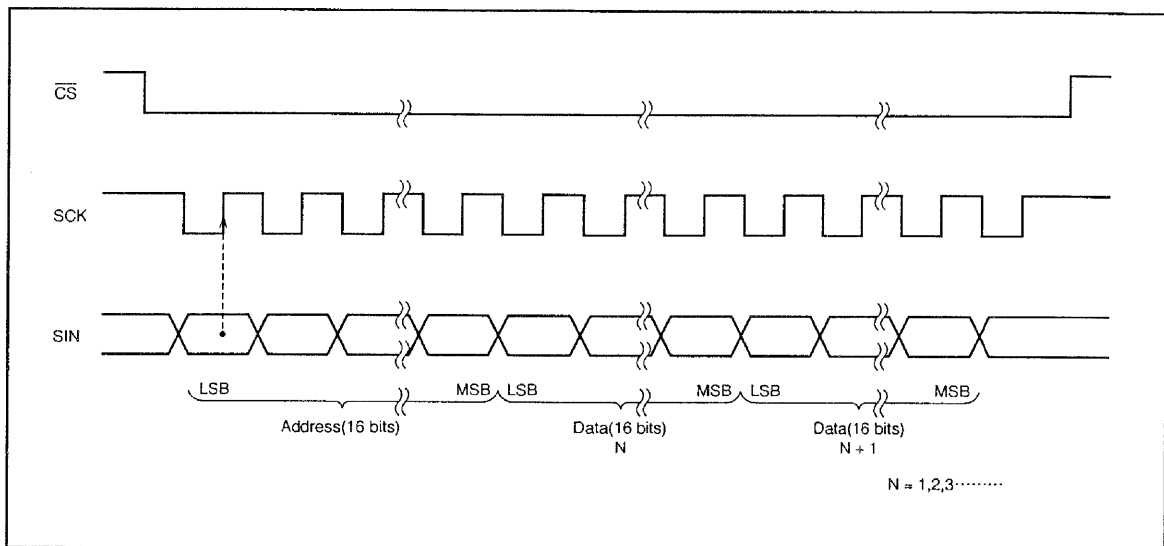


Fig. 6 Serial input timing

CHARACTER FONT

Images are composed on a 12 × 18 dot matrix, and characters can be linked vertically and horizontally with other characters to allow the display the continuous symbols.

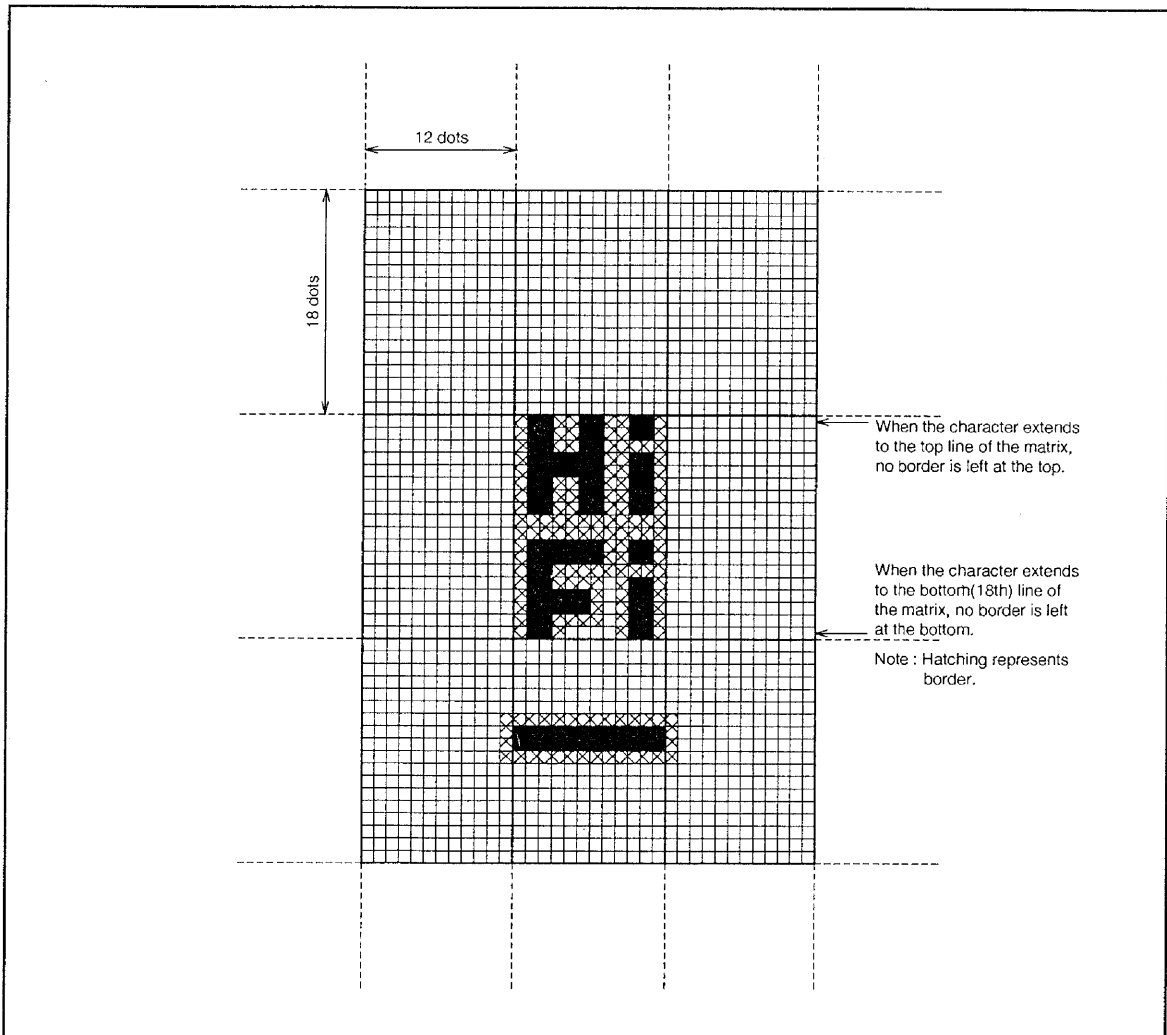


Fig. 7 Example for displaying a continuous pattern after combining characters in the horizontal or vertical direction

Character code FF16 is fixed as a blank without background.
Therefore, you cannot register a character font in this code.

TIMING REQUIREMENTS ($T_a = -20^{\circ}\text{C}$ to $+85^{\circ}\text{C}$, $V_{DD} = 5 \pm 0.25\text{V}$, unless otherwise noted)

Symbol	Parameter	Limits			Unit	Remarks
		Min.	Typ.	Max.		
$t_w(\text{SCK})$	SCK width	200	—	—	ns	See Figure 8
$t_{su}(\overline{\text{CS}})$	$\overline{\text{CS}}$ setup time	200	—	—	ns	
$t_h(\overline{\text{CS}})$	$\overline{\text{CS}}$ hold time	2	—	—	μs	
$t_{su}(\text{SIN})$	SIN setup time	200	—	—	ns	
$t_h(\text{SIN})$	SIN hold time	200	—	—	ns	
t_{word}	1 word writing time	10	—	—	μs	

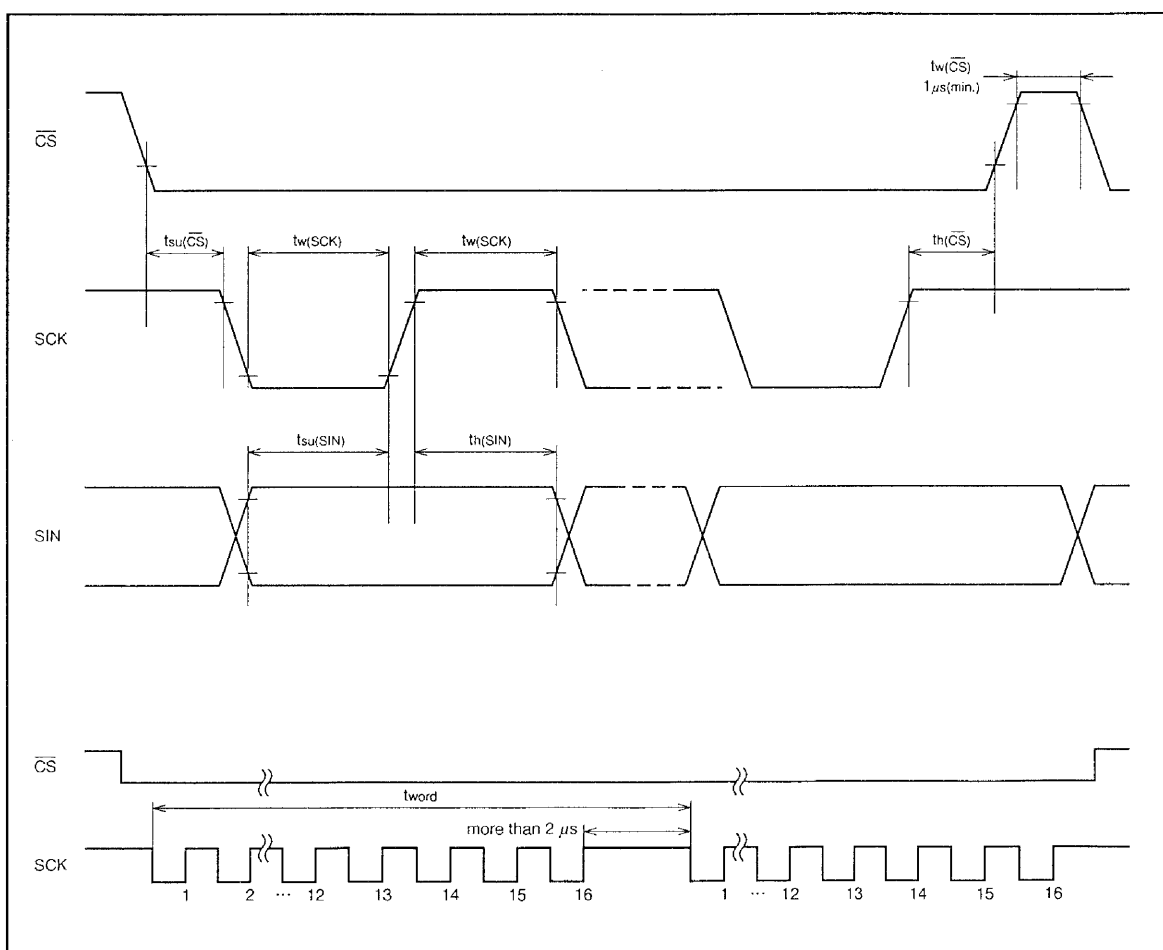


Fig. 8 Serial input timing requirements

EXAMPLE OF THE M35044-XXXSP/FP PERIPHERAL CIRCUIT

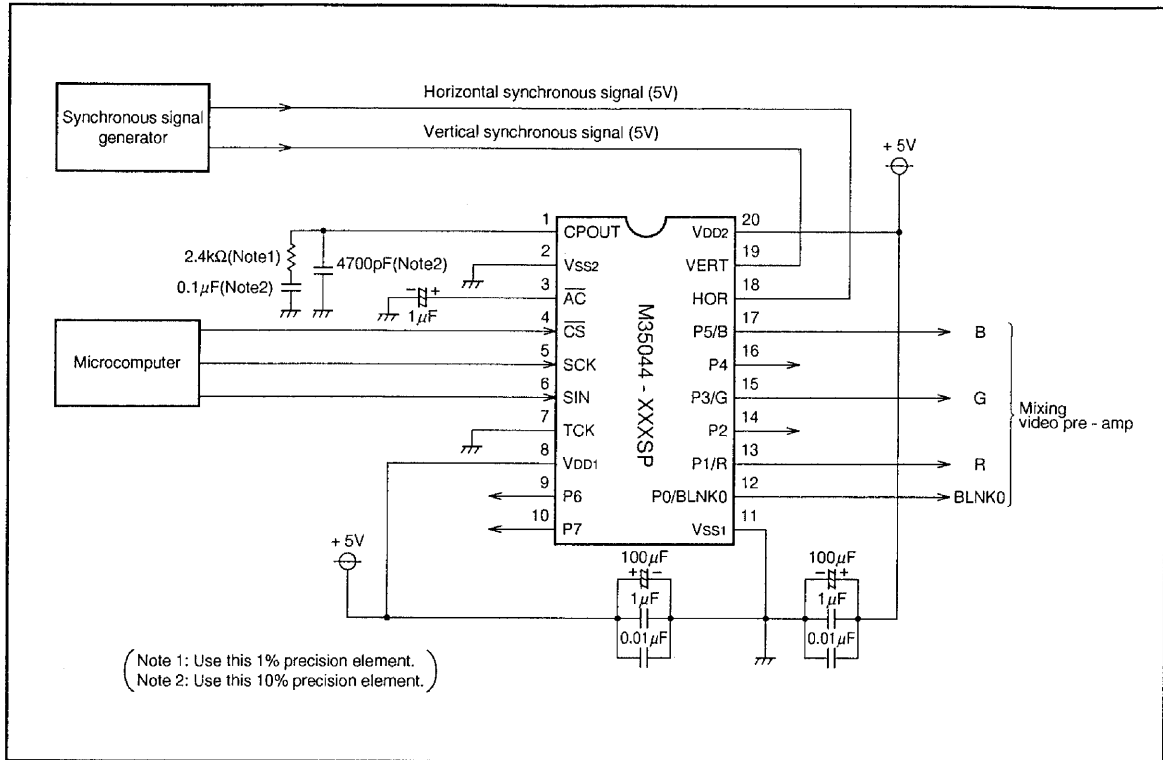


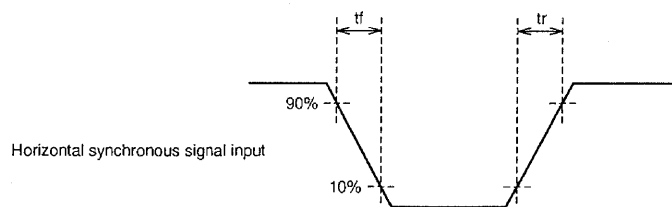
Fig. 9 Example of the M35044-XXXSP peripheral circuit (M35044-XXXFP peripheral circuit is same as that of M35044-XXXSP)

Note for waveform timing of the horizontal signals to the HOR pin.

Set horizontal synchronous signal edge* waveform timing to under 5ns and input to HOR pin.

Set only the side which set by B/F register waveform timing under 5ns and input to HOR pin.

*: Set front porch edge or back porch edge by B/F register.



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
VDD	Supply voltage	With respect to VSS.	-0.3 to +6.0	V
VI	Input voltage		$V_{SS} - 0.3 \leq V_I \leq V_{DD} + 0.3$	V
VO	Output voltage		$V_{SS} \leq V_O \leq V_{DD}$	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		-20 to +85	°C
Tstg	Storage temperature		-40 to +125	°C

RECOMMENDED OPERATING CONDITIONS (VDD = 5V, Ta = -20 to +85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
VDD	Supply voltage	4.75	5.0	5.25	V
VIH	"H" level input voltage SIN, SCK, CS, AC HOR, VERT	0.8VDD	VDD	VDD	V
VIL	"L" level input voltage SIN, SCK, CS, AC HOR, VERT	0	0	0.2VDD	V
FOSC	Oscillating frequency for display	20.0	—	80.0	MHz

ELECTRICAL CHARACTERISTICS (VDD = 5V, Ta = 25°C, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min.	Typ.	Max.	
VDD	Supply voltage		Ta = -20 to +85°C	4.75	5.0	5.25	V
IDD	Supply current		VDD = 5.25V	—	30	50	mA
VOH	"H" level output voltage	P0 ~ P7	VDD = 4.75V, IOH = 0.4mA	3.5	—	—	V
		CPOUT	VDD = 4.75V, IOH = 0.05mA				
VOL	"L" level output voltage	P0 ~ P7	VDD = 4.75V, IOL = 0.4mA	—	—	0.4	V
		CPOUT	VDD = 4.75V, IOL = 0.05mA				
Ri	Pull-up resistance SCK, AC, CS, SIN		VDD = 5.0V	10	30	100	kΩ

Note for Supplying Power

Timing of power supplying to $\overline{AC}$ pin

The internal circuit of M35044-XXXSP/FP is reset when the level of the auto clear input pin $\overline{AC}$ is "L". This pin is hysteresis input with the pull-up resistor. The timing about power supplying of $\overline{AC}$ pin is shown in Figure 10.

Timing of power supplying to V_{DD1} and V_{DD2} .

Supply power to V_{DD1} and V_{DD2} at the same time.

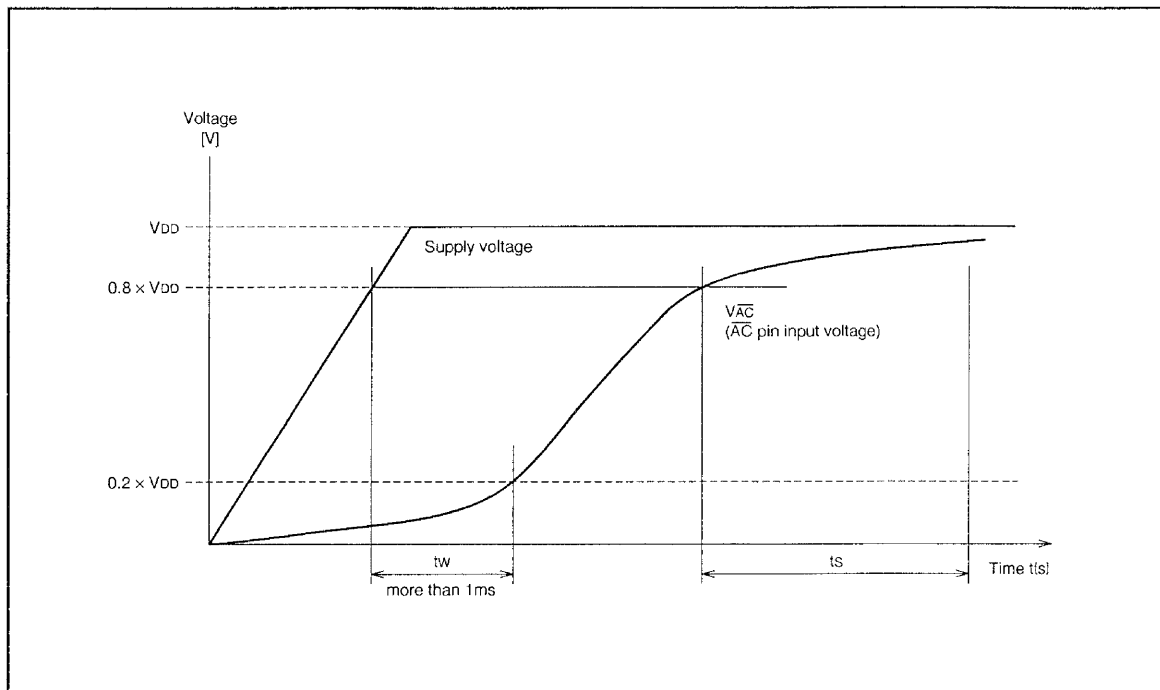


Fig. 10 Timing of power supplying to $\overline{AC}$ pin

After supplying the power (V_{DD} and V_{SS}) to M35044-XXXSP/FP and the supply voltage becomes more than $0.8 \times V_{DD}$, it needs to keep V_{IL} time; t_w of the $\overline{AC}$ pin for more than 1ms.

Start inputting from microcomputer after $\overline{AC}$ pin supply voltage becomes more than $0.8 \times V_{DD}$ and keeping 200ms wait time.

PRECAUTION FOR USE

Notes on noise and latch-up

In order to avoid noise and latch-up, connect a bypass capacitor ($\approx 0.1 \mu F$) directly between the V_{DD1} pin and V_{SS} pin, and the V_{DD2} pin and V_{SS} pin using a heavy wire.

DATA REQUIRED FOR MASK ROM ORDERING

Please send the following data for mask orders.

- (1) M35044-XXXSP/FP mask ROM order confirmation form
- (2) Mask specification form
- (3) ROM data (EPROM 3 sets)
- (4) Floppy disks containing the character font generating program + character data

STANDARD ROM TYPE : M35044-001SP/FP

M35044-001SP/FP is a standard ROM type of M35044-XXXSP/FP.

The character patterns are fixed to the contents of Figure 11 to 13.

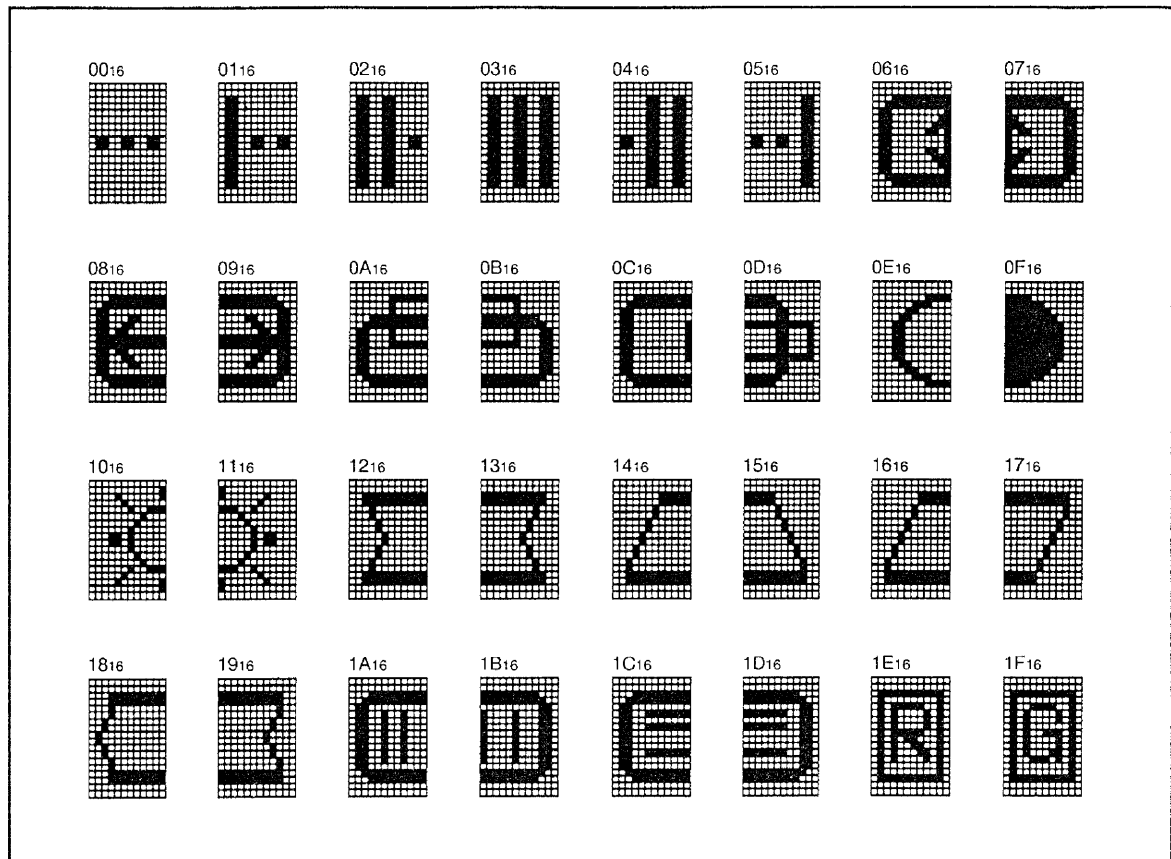


Fig. 11 M35044-001SP/FP character patterns (1)

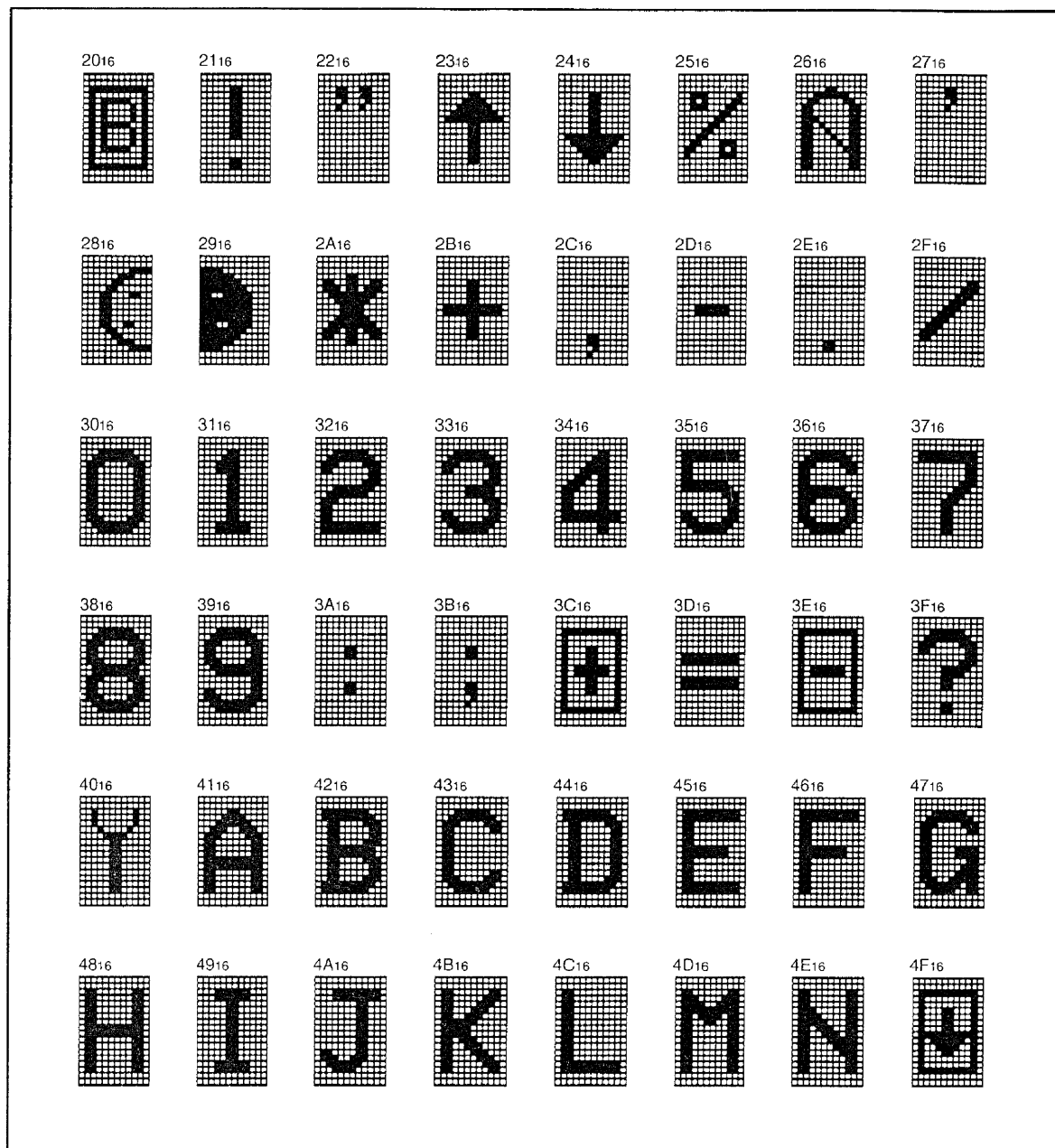


Fig. 12 M35044-001SP/FP character patterns (2)

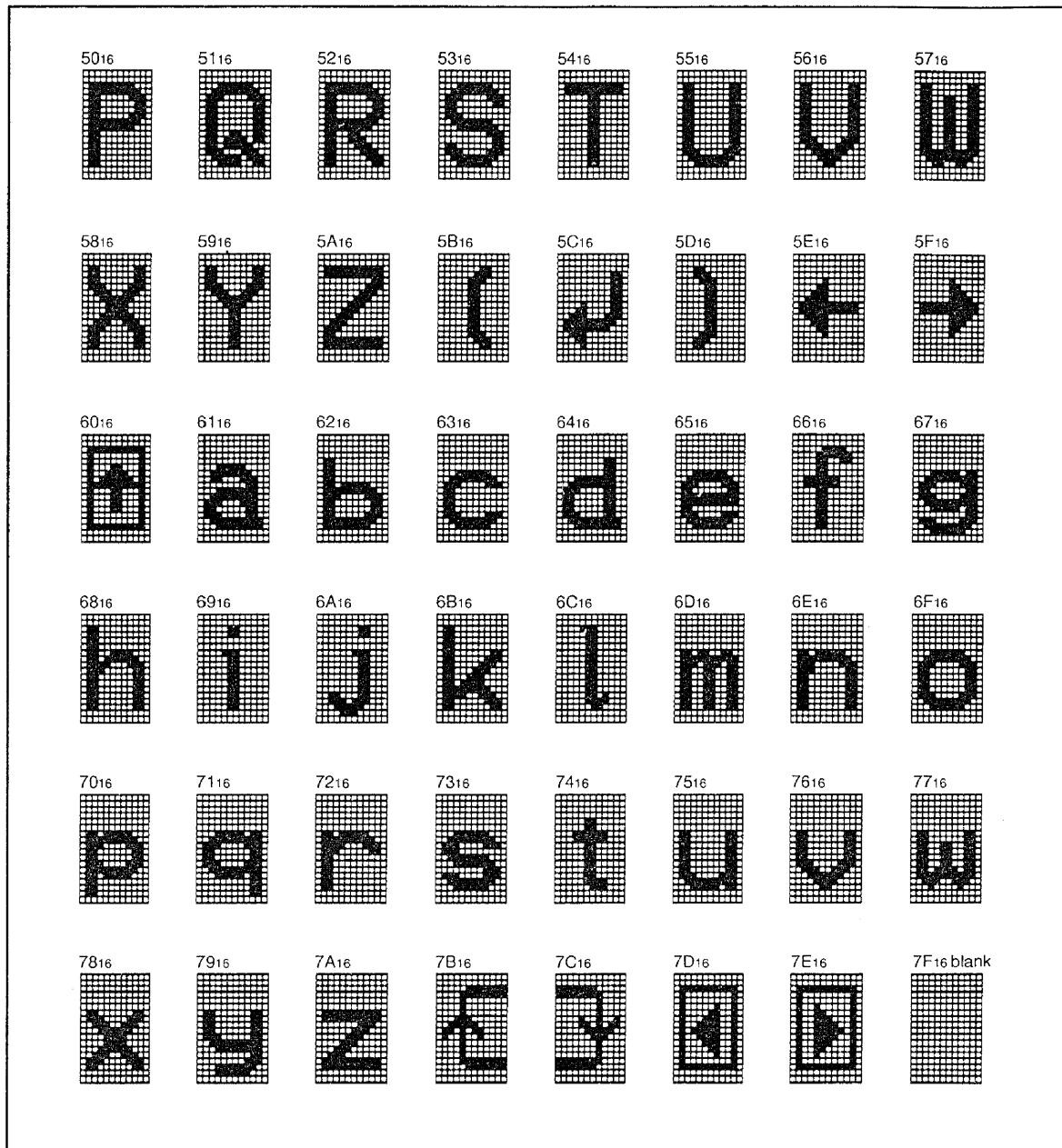


Fig. 13 M35044-001SP/FP character patterns (3)