3826 Group (One Time PROM version)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0181-0100
Rev.1.00
Sep 06, 2006

DESCRIPTION

The 3826 group is the 8-bit microcomputer based on the 740 family core technology.

The 3826 group has the LCD drive control circuit, an 8-channel A/D converter, D/A converter, serial interface and PWM as additional functions.

The various microcomputers in the 3826 group (One Time PROM version) include variations of internal memory size and packaging. This datasheet describes only the One Time PROM version (ROM 60 K version) of 3826 Group.

FEATURES

- Basic machine-language instructions 71
- The minimum instruction execution time .... 0.5 µs (at 8MHz oscillation frequency)
- Memory size
  - ROM .... 60 K bytes
  - RAM .... 2560 bytes
- Programmable input/output ports 55
- Software pull-up resistors .... Built-in
- Output ports 8
- Input ports 1
- Interrupts .... 17 sources, 16 vectors
  - External .... 7 sources (includes key input interrupt)
  - Internal .... 9 sources
  - Software .... 1 source
- Timers .... 8-bit × 3, 16-bit × 2
- Serial interface
  - Serial I/O1 .... 8-bit × 1 (UART or Clock-synchronous)
  - Serial I/O2 .... 8-bit × 1 (Clock-synchronous)
- PWM output .... 8-bit × 1
- A/D converter .... 10-bit × 8 channels or 8-bit × 8 channels
- D/A converter .... 8-bit × 2 channels (used as DTMF and CTCSS function)
- LCD drive control circuit
  - Bias 1/2, 1/3
  - Duty 1/2, 1/3, 1/4
  - Common output 4
  - Segment output 40
- 2 Clock generating circuits (connect to external ceramic resonator or quartz-crystal oscillator)
- Watchdog timer .... 14-bit × 1
- Power source voltage
  - In high-speed mode ($f(X_{IN})$ = 8 MHz) .... 4.0 V to 5.5 V
  - In middle-speed mode ($f(X_{IN})$ = 8 MHz) .... 2.5 V to 5.5 V
  - In low-speed mode .... 2.5 V to 5.5 V
- Power dissipation
  - In high-speed mode .... Typ. 32 mW ($f(X_{IN})$ = 8 MHz, V_{CC} = 5 V, Ta = 25 °C)
  - In low-speed mode .... Typ. 45 µW ($f(X_{IN})$ = stop, $f(X_{CIN})$ = 32 kHz, V_{CC} = 3 V, Ta = 25 °C)
- Operating temperature range .... – 20 to 85°C

APPLICATIONS

Camera, cordless phone, wireless application, household appliances, etc.

PIN CONFIGURATION (TOP VIEW)

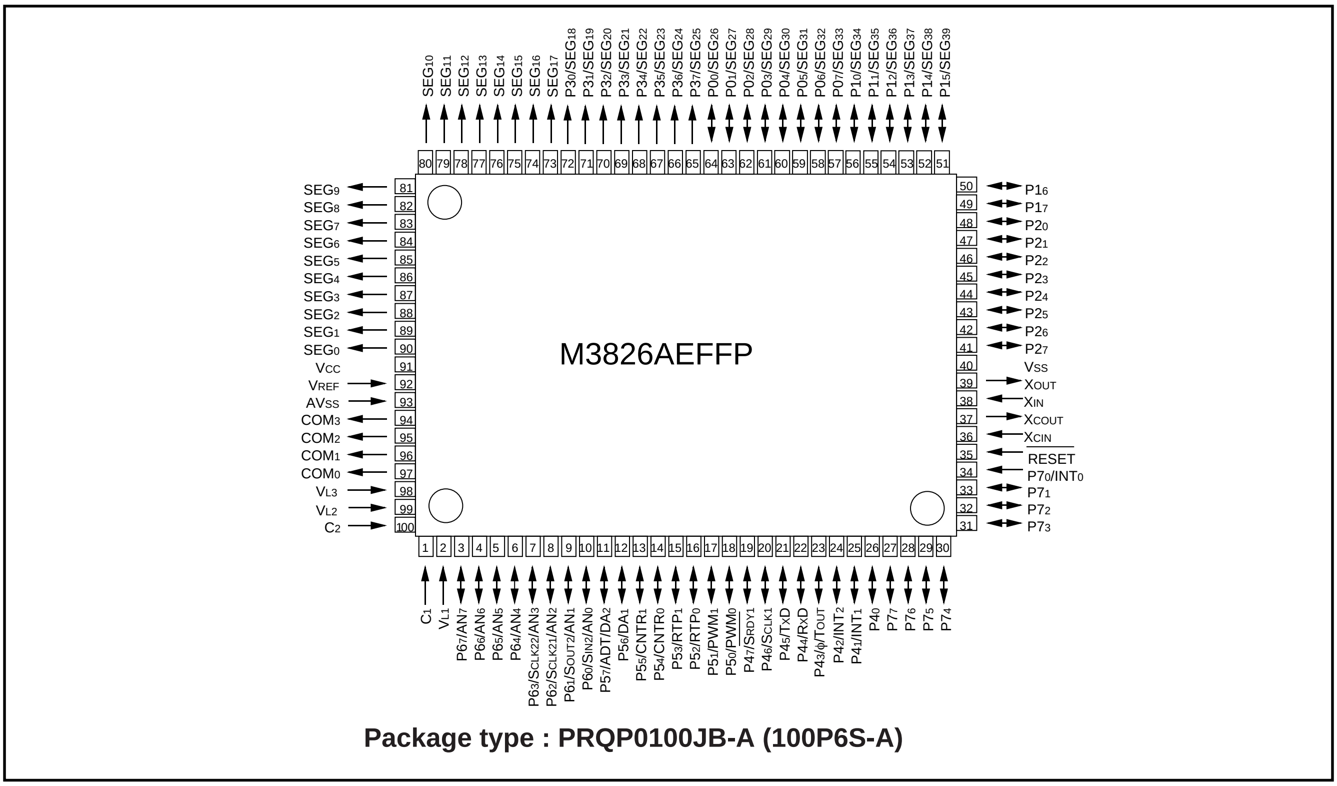


Fig. 1 Pin configuration (Package type: PRQP0100JB-A)

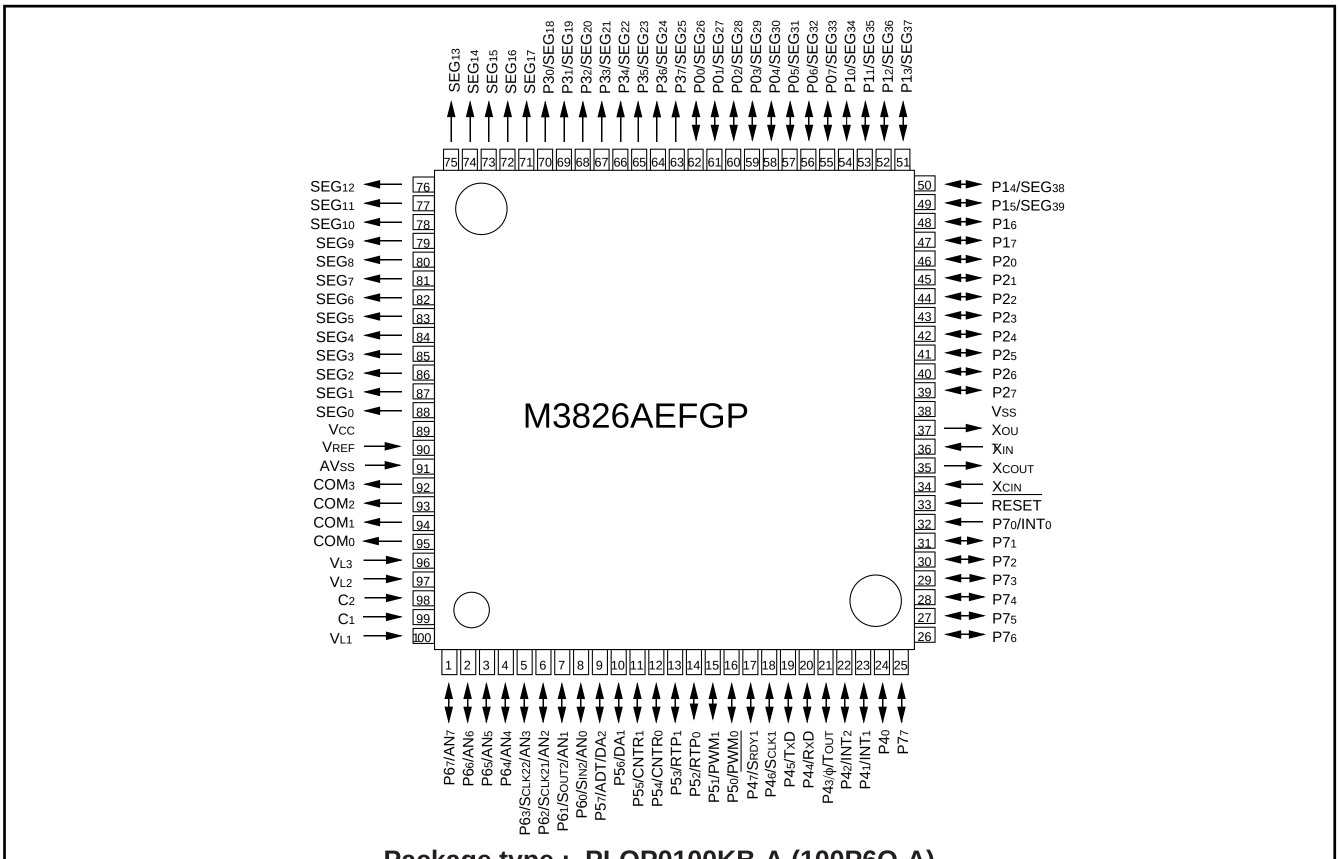


Fig. 2 Pin configuration (Package type: PLQP0100KB-A)

FUNCTIONAL BLOCK DIAGRAM (Package type: PRQP0100JB-A)

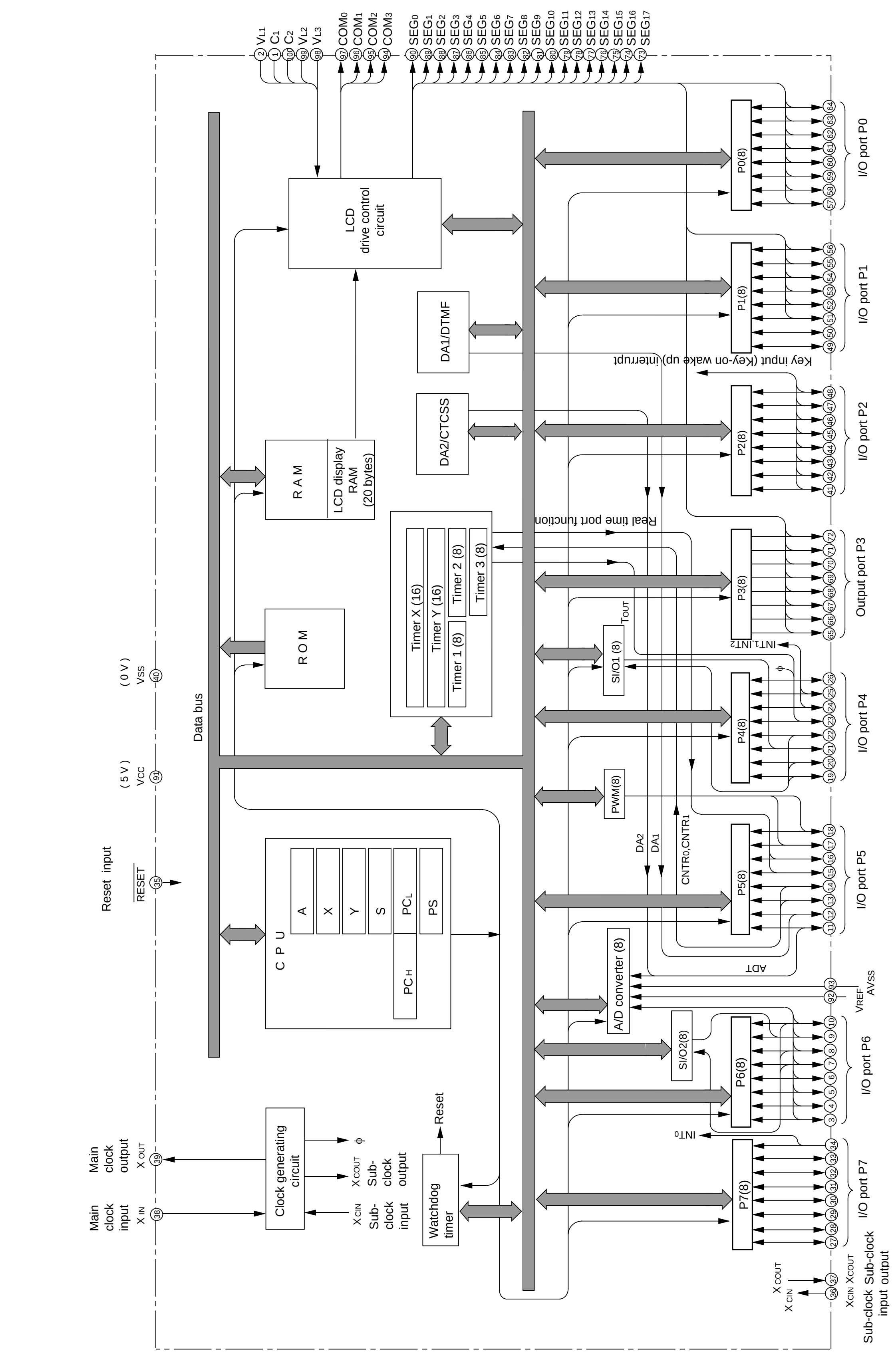


Fig. 3 Functional block diagram

PIN DESCRIPTION

Table 1 Pin description (1)

Pin	Name	Function	Function except a port function
V_{CC} V_{SS}	Power source	•Apply voltage of power source to V_{CC}, and 0 V to V_{SS}. (For the limits of V_{CC}, refer to "Recommended operating conditions".	
V_{REF}	Analog reference voltage	•Reference voltage input pin for A/D converter and D/A converter.	
AV_{SS}	Analog power source	•GND input pin for A/D converter and D/A converter. •Connect to V_{SS}.	
$\overline{RESET}$	Reset input	•Reset input pin for active "L".	
X_{IN}	Clock input	•Input and output pins for the main clock generating circuit. •Connect a ceramic resonator or a quartz-crystal oscillator between the X_{IN} and X_{OUT} pins to set the oscillation frequency. •If an external clock is used, connect the clock source to the X_{IN} pin and leave the X_{OUT} pin open. A feedback resistor is built-in.	
X_{OUT}	Clock output		
V_{L1}–V_{L3}	LCD power source	•Input $0 \leq V_{L1} \leq V_{L2} \leq V_{L3}$ voltage. •Input 0 – V_{L3} voltage to LCD. ($0 \leq V_{L1} \leq V_{L2} \leq V_{L3}$ when a voltage is multiplied.)	
C_1, C_2	Charge-pump capacitor pin	•External capacitor pins for a voltage multiplier (3 times) of LCD control.	
COM_0–COM_3	Common output	•LCD common output pins. •COM_2 and COM_3 are not used at 1/2 duty ratio. •COM_3 is not used at 1/3 duty ratio.	
SEG_0–SEG_{17}	Segment output	•LCD segment output pins.	
$P0_0$/SEG_{26}–$P0_7$/SEG_{33}	I/O port P0	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled. •I/O direction register allows each 8-bit pin to be programmed as either input or output.	•LCD segment output pins
$P1_0$/SEG_{34}–$P1_5$/SEG_{39}	I/O port P1	•6-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •Pull-up control is enabled. •I/O direction register allows each 6-bit pin to be programmed as either input or output.	
$P1_6$, $P1_7$		•2-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	
$P2_0$ – $P2_7$	I/O port P2	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•Key input (key-on wake-up) interrupt input pins
$P3_0$/SEG_{18} – $P3_7$/SEG_{25}	Output port P3	•8-bit output. •CMOS 3-state output structure. •Port output control is enabled.	•LCD segment output pins

Table 2 Pin description (2)

Pin	Name	Function	Function except a port function
$P4_0$	I/O port P4	•1-bit I/O port. •CMOS compatible input level. •N-channel open-drain output structure. •I/O direction register allows this pin to be individually programmed as either input or output.	
$P4_1/INT_1$, $P4_2/INT_2$		•7-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•INT_i interrupt input pins
$P4_3/\phi/T_{OUT}$			•System clock ϕ output pin •Timer 2 output pin
$P4_4/R_XD$, $P4_5/T_XD$, $P4_6/\overline{S_{CLK1}}$, $P4_7/\overline{S_{RDY1}}$			•Serial I/O1 I/O pins
$P5_0/PWM_0$, $P5_1/PWM_1$	I/O port P5	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•PWM output pins
$P5_2/RTP_0$, $P5_3/RTP_1$			•Real time port output pins
$P5_4/CNTR_0$, $P5_5/CNTR_1$			•Timer X, Y I/O pins
$P5_6/DA_1$			•D/A converter output pin
$P5_7/ADT/DA_2$			•D/A converter output pin •A/D external trigger input pin
$P6_0/S_{IN2}/AN_0$, $P6_1/S_{OUT2}/AN_1$, $P6_2/S_{CLK21}/AN_2$, $P6_3/S_{CLK22}/AN_3$	I/O port P6	•8-bit I/O port. •CMOS compatible input level. •CMOS 3-state output structure. •I/O direction register allows each pin to be individually programmed as either input or output. •Pull-up control is enabled.	•A/D converter input pins •Serial I/O2 I/O pins
$P6_4/AN_4$–$P6_7/AN_7$			•A/D converter input pins
$P7_0/INT_0$	Input port P7	•1-bit input port.	•INT_0 interrupt input pin
$P7_1$–$P7_7$	I/O port P7	•7-bit I/O port. •CMOS compatible input level. •N-channel open-drain output structure. •I/O direction register allows each pin to be individually programmed as either input or output.	
X_{COUT}	Sub-clock output	•Sub-clock generating circuit I/O pins. (Connect an oscillator. External clock cannot be used.)	
X_{CIN}	Sub-clock input		

PART NUMBERING

Product M3826 A E F FP

Package type
FP : PRQP0100JB-A
GP : PLQP0100KB-A
FS : 100D0

ROM size
1 : 4096 bytes
2 : 8192 bytes
3 : 12288 bytes
4 : 16384 bytes
5 : 20480 bytes
6 : 24576 bytes
7 : 28672 bytes
8 : 32768 bytes
9 : 36864 bytes
A : 40960 bytes
B : 45056 bytes
C : 49152 bytes
D : 53248 bytes
E : 57344 bytes
F : 61440 bytes

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used.

Memory type
E: EPROM version or One Time PROM version

RAM size
0 : 192 bytes
1 : 256 bytes
2 : 384 bytes
3 : 512 bytes
4 : 640 bytes
5 : 768 bytes
6 : 896 bytes
7 : 1024 bytes
8 : 1536 bytes
9 : 2048 bytes
A : 2560 bytes

Fig. 4 Part numbering

GROUP EXPANSION

Renesas expands the 3826 group as follows.

Memory Type

Support for One Time PROM version or EPROM version.

Memory Size

ROM size .... 60 K bytes
RAM size .... 2560 bytes

Packages

PRQP0100JB-A .... 0.65 mm-pitch plastic molded QFP
PLQP0100KB-A .... 0.5 mm-pitch plastic molded QFP
100D0 .... 0.65 mm-pitch ceramic LCC (EPROM version)

Memory Expansion Plan

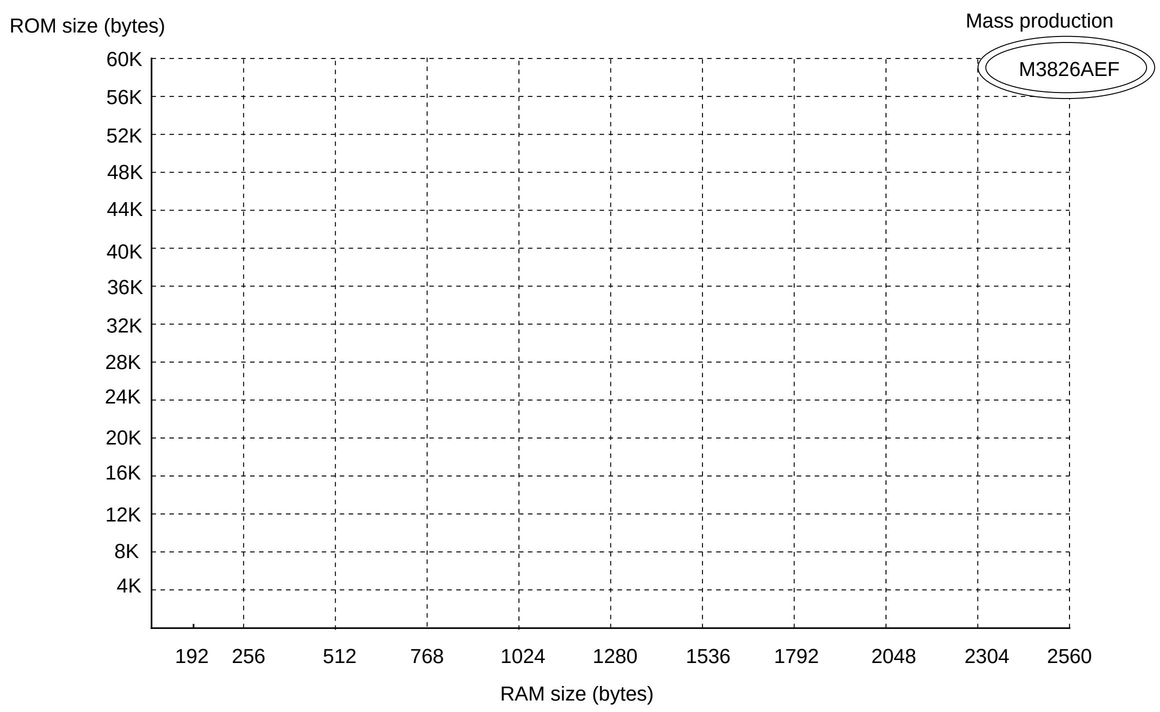


Fig. 5 Memory expansion plan

Currently planning products are listed below.

Table 3 Support products **As of Sep. 2006**

Part number	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M3826AEFFP	61440 (61310)	2560	PRQP0100JB-A	One Time RPOM version
M3826AEFGP			PLQP0100KB-A	One Time PROM version
M3826AEFFS			100D0	EPROM version for development

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3826 group uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.
Machine-resident 740 family instructions are as follows:
The FST and SLW instruction cannot be used.
The STP, WIT, MUL, and DIV instruction can be used.
The central processing unit (CPU) has six registers. Figure 6 shows the 740 Family CPU register structure.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as arithmetic data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts. The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.
Figure 7 shows the operations of pushing register contents onto the stack and popping them from the stack. Table 4 shows the push and pop instructions of accumulator or processor status register.
Store registers other than those described in Figure 7 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

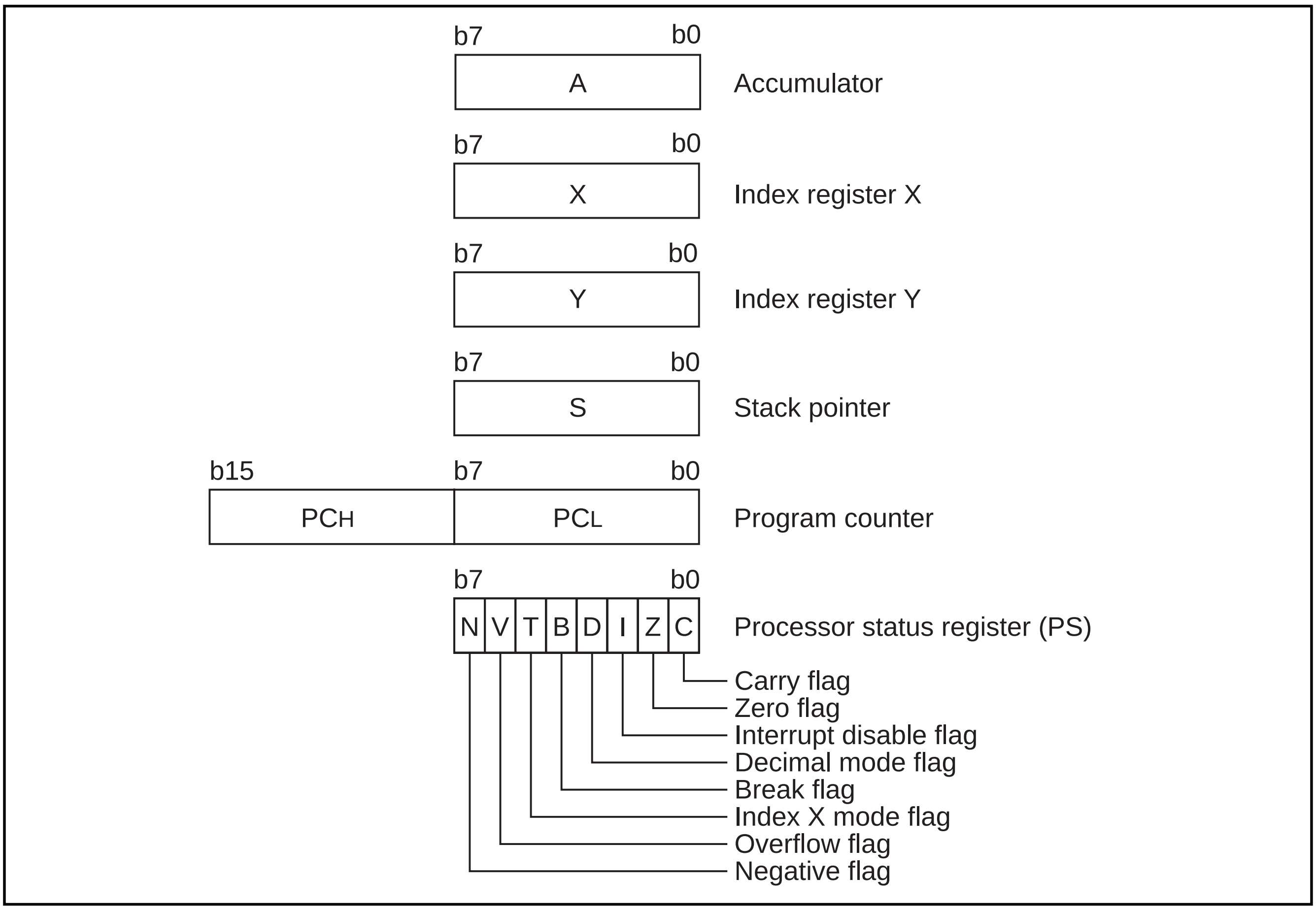
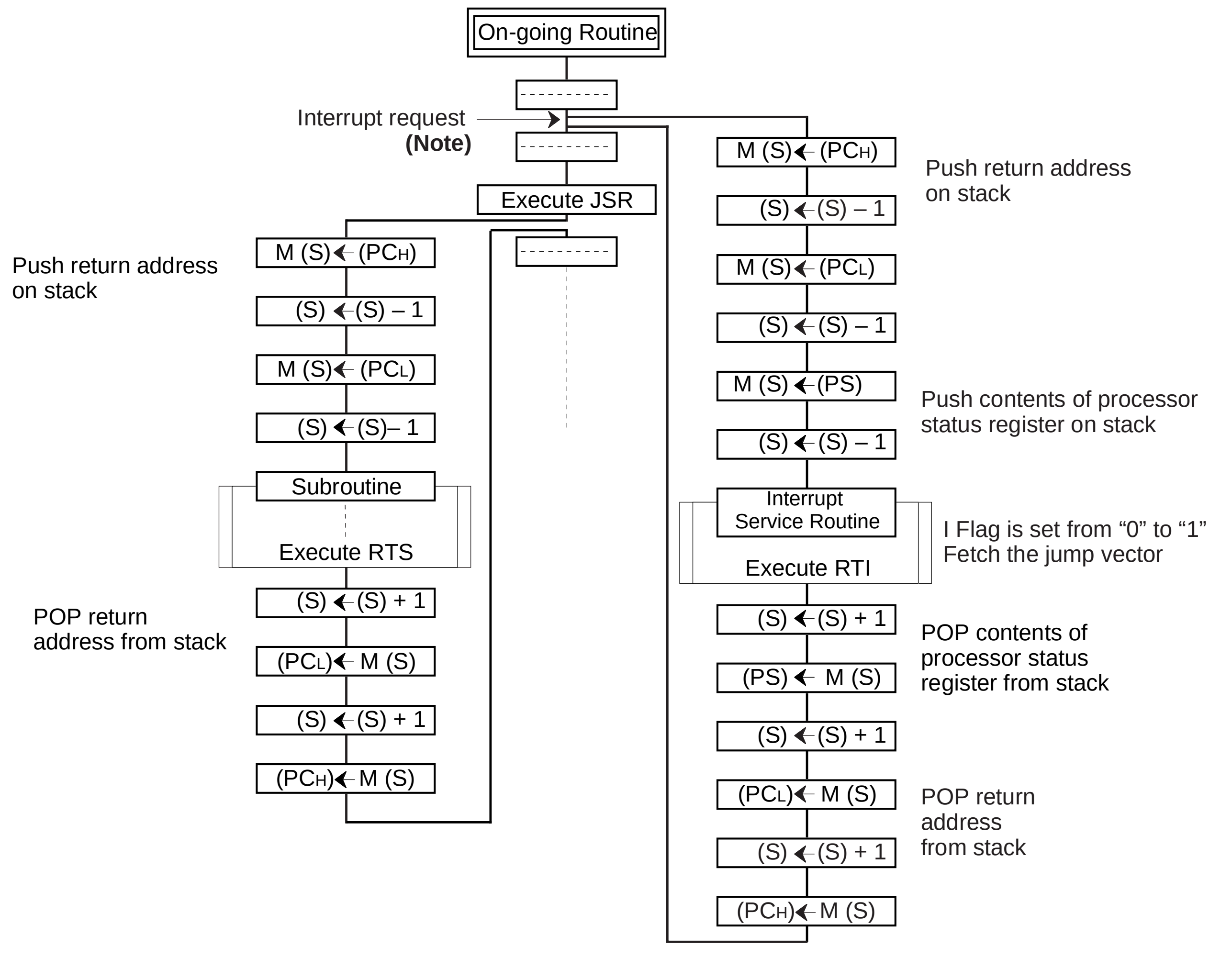


Fig. 6 740 Family CPU register structure



Note: Condition for acceptance of an interrupt request here → Interrupt enable bit corresponding to each interrupt source is “1”
Interrupt disable flag is “0”

Fig. 7 Register push and pop at interrupt generation and subroutine call

Table 4 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

• Bit 0: Carry flag (C)
  The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.
• Bit 1: Zero flag (Z)
  The Z flag is set to “1” if the result of an immediate arithmetic operation or a data transfer is “0”, and set to “0” if the result is anything other than “0”.
• Bit 2: Interrupt disable flag (I)
  The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
  Interrupts are disabled when the I flag is “1”.
• Bit 3: Decimal mode flag (D)
  The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is “0”; decimal arithmetic is executed when it is “1”.
  Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.
• Bit 4: Break flag (B)
  The B flag is used to indicate that the current interrupt was generated by the BRK instruction. When the BRK instruction is generated, the B flag is set to “1” automatically. When the other interrupts are generated, the B flag is set to “0”, and the processor status register is pushed onto the stack.
• Bit 5: Index X mode flag (T)
  When the T flag is “0”, arithmetic operations are performed between accumulator and memory. When the T flag is “1”, direct arithmetic operations and direct data transfers are enabled between memory locations.
• Bit 6: Overflow flag (V)
  The V flag is used during the addition or subtraction of one byte of signed data. It is set to “1” if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the V flag.
• Bit 7: Negative flag (N)
  The N flag is set to “1” if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 5 Instructions to set each bit of processor status register to “0” or “1”

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Instruction setting to “1”	SEC	–	SEI	SED	–	SET	–	–
Instruction setting to “0”	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] $003B_{16}$

The CPU mode register contains the stack page selection bit and the system clock control bits, etc.

The CPU mode register is allocated at address $003B_{16}$.

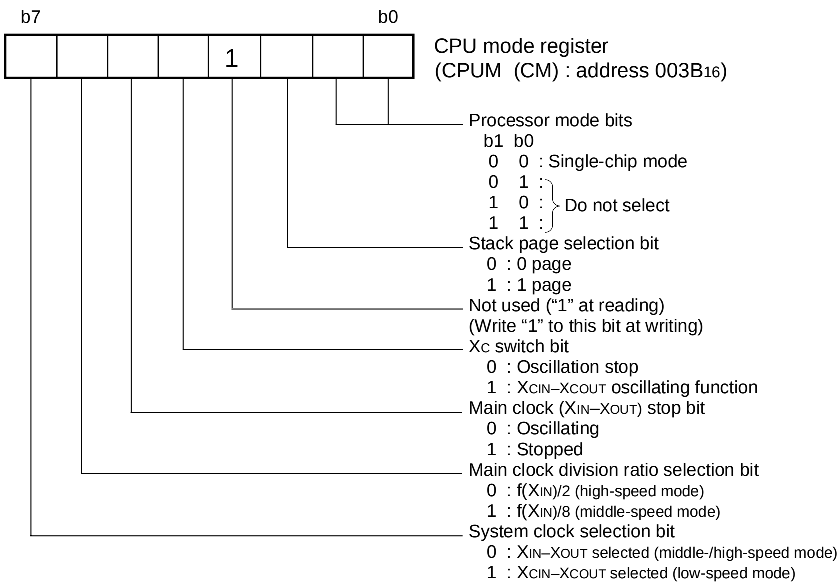


Fig. 8 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000$_{16}$ to 00FF$_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.
The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses FF00$_{16}$ to FFFF$_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address XXXX$_{16}$
192	00FF$_{16}$
256	013F$_{16}$
384	01BF$_{16}$
512	023F$_{16}$
640	02BF$_{16}$
768	033F$_{16}$
896	03BF$_{16}$
1024	043F$_{16}$
1536	063F$_{16}$
2048	083F$_{16}$
2560	0A3F$_{16}$

ROM area

ROM size (bytes)	Address YYYY$_{16}$	Address ZZZZ$_{16}$
4096	F000$_{16}$	F080$_{16}$
8192	E000$_{16}$	E080$_{16}$
12288	D000$_{16}$	D080$_{16}$
16384	C000$_{16}$	C080$_{16}$
20480	B000$_{16}$	B080$_{16}$
24576	A000$_{16}$	A080$_{16}$
28672	9000$_{16}$	9080$_{16}$
32768	8000$_{16}$	8080$_{16}$
36864	7000$_{16}$	7080$_{16}$
40960	6000$_{16}$	6080$_{16}$
45056	5000$_{16}$	5080$_{16}$
49152	4000$_{16}$	4080$_{16}$
53248	3000$_{16}$	3080$_{16}$
57344	2000$_{16}$	2080$_{16}$
61440	1000$_{16}$	1080$_{16}$

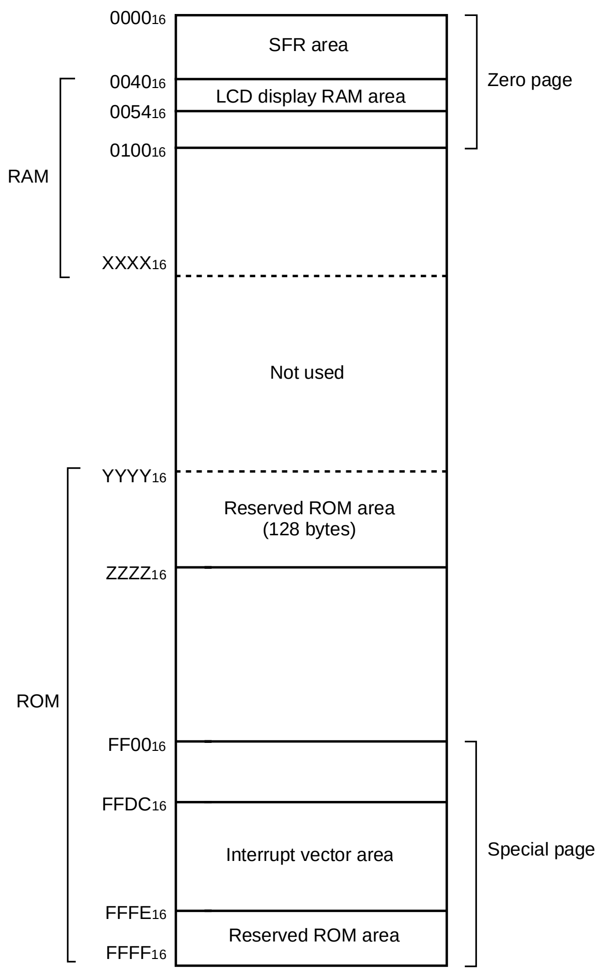


Fig. 9 Memory map diagram

Address	Register	Address	Register
0000_{16}	Port P0 register (P0)	0020_{16}	Timer X low-order register (TXL)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer X high-order register (TXH)
0002_{16}	Port P1 register (P1)	0022_{16}	Timer Y low-order register (TYL)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer Y high-order register (TYH)
0004_{16}	Port P2 register (P2)	0024_{16}	Timer 1 register (T1)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer 2 register (T2)
0006_{16}	Port P3 register (P3)	0026_{16}	Timer 3 register (T3)
0007_{16}	Port P3 output control register (P3C)	0027_{16}	Timer X mode register (TXM)
0008_{16}	Port P4 register (P4)	0028_{16}	Timer Y mode register (TYM)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	Timer 123 mode register (T123M)
$000A_{16}$	Port P5 register (P5)	$002A_{16}$	TOUT/φ output control register (CKOUT)
$000B_{16}$	Port P5 direction register (P5D)	$002B_{16}$	PWM control register (PWMCON)
$000C_{16}$	Port P6 register (P6)	$002C_{16}$	PWM prescaler (PREPWM)
$000D_{16}$	Port P6 direction register (P6D)	$002D_{16}$	PWM register (PWM)
$000E_{16}$	Port P7 register (P7)	$002E_{16}$	CTSCSS timer (low) (CTCSSL)
$000F_{16}$	Port P7 direction register (P7D)	$002F_{16}$	CTSCSS timer (high) (CTCSSH)
0010_{16}		0030_{16}	DTMF high group timer (DTMFH)
0011_{16}		0031_{16}	DTMF low group timer (DTMFL)
0012_{16}		0032_{16}	DA1 conversion register (DA1)
0013_{16}		0033_{16}	DA2 conversion register (DA2)
0014_{16}	AD conversion low-order register (ADL)	0034_{16}	AD control register (ADCON)
0015_{16}	Key input control register (KIC)	0035_{16}	AD conversion high-order register (ADH)
0016_{16}	PULL register A (PULLA)	0036_{16}	DA control register (DACON)
0017_{16}	PULL register B (PULLB)	0037_{16}	Watchdog timer control register (WDTCON)
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	Segment output enable register (SEG)
0019_{16}	Serial I/O1 status register (SIO1STS)	0039_{16}	LCD mode register (LM)
$001A_{16}$	Serial I/O1 control register (SIO1CON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1(IREQ1)
$001D_{16}$	Serial I/O2 control register (SIO2CON)	$003D_{16}$	Interrupt request register 2(IREQ2)
$001E_{16}$	Reserved area **(Note)**	$003E_{16}$	Interrupt control register 1(ICON1)
$001F_{16}$	Serial I/O2 register (SIO2)	$003F_{16}$	Interrupt control register 2(ICON2)

Note: Do not write to the addresses of reserved area.

Fig. 10 Memory map of special function register (SFR)

I/O PORTS

Direction Registers

The I/O ports (ports P0, P1, P2, P4, P5, P6, $P7_1$–$P7_7$) have direction registers. Ports $P1_6$, $P1_7$, P4, P5, P6, and $P7_1$–$P7_7$ can be set to input mode or output mode by each pin individually. $P0_0$–$P0_7$ and $P1_0$-$P1_5$ are respectively set to input mode or output mode in a lump by bit 0 of the direction registers of ports P0 and P1 (see Figure 11).

When “0” is set to the bit corresponding to a pin, that pin becomes an input mode. When “1” is set to that bit, that pin becomes an output mode.

If data is read from a port set to output mode, the value of the port latch is read, not the value of the pin itself. A port set to input mode is floating. If data is read from a port set to input mode, the value of the pin itself is read. If a pin set to input mode is written to, only the port latch is written to and the pin remains floating.

Port P3 Output Control Register

Bit 0 of the port P3 output control register (address 0007_{16}) enables control of the output of ports $P3_0$–$P3_7$.

When the bit is set to “1”, the port output function is valid.

When resetting, bit 0 of the port P3 output control register is set to “0” (the port output function is invalid) and pulled up.

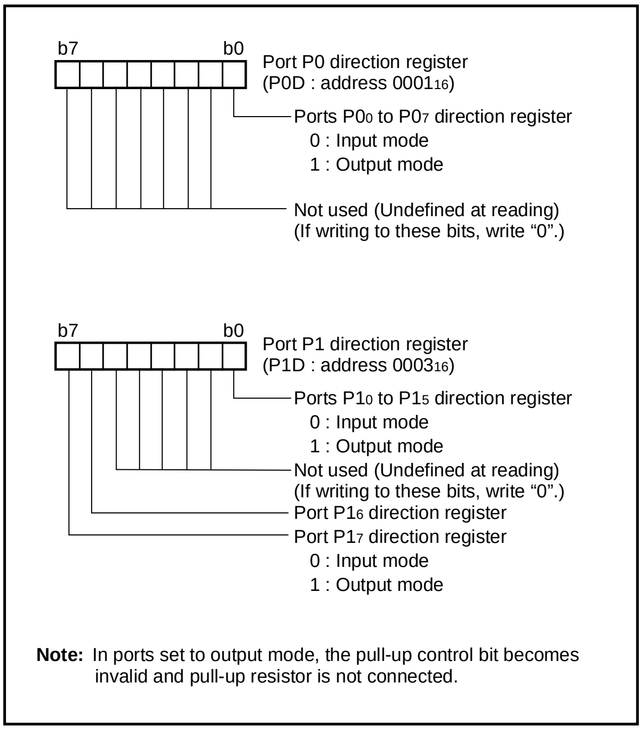


Fig. 11 Structure of port P0 direction register, port P1 direction register

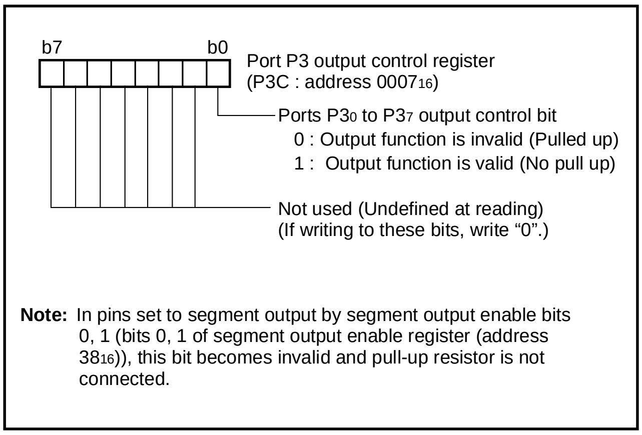


Fig. 12 Structure of port P3 output control register

Pull-up Control

By setting the PULL register A (address 0016_{16}) or the PULL register B (address 0017_{16}), ports P0 to P2, P4 to P6 can control pull-up with a program.

However, the contents of PULL register A and PULL register B do not affect ports set to output mode and the ports are no pulled up. The PULL register A setting is invalid for pins selecting segment output with the segment output enable register and the pins are not pulled up.

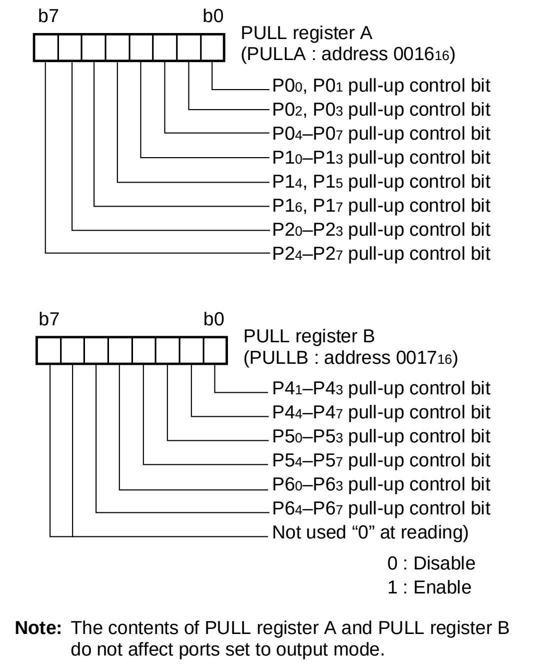


Fig. 13 Structure of PULL register A and PULL register B

Table 6 List of I/O port function (1)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
P0$_0$/SEG$_{26}$–P0$_7$/SEG$_{33}$	Port P0	Input/output, byte unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1) (2)
P1$_0$/SEG$_{34}$–P1$_5$/SEG$_{39}$	Port P1	Input/output, 6-bit unit	CMOS compatible input level CMOS 3-state output	LCD segment output	PULL register A Segment output enable register	(1) (2)
P1$_6$, P1$_7$		Input/output, individual bits	CMOS compatible input level CMOS 3-state output		PULL register A	(4)
P2$_0$–P2$_7$	Port P2	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Key input (key-on wake-up) interrupt input	PULL register A Interrupt control register 2 Key input control register	
P3$_0$/SEG$_{18}$–P3$_7$/SEG$_{25}$	Port P3	Output	CMOS 3-state output	LCD segment output	Segment output enable register Port P3 output control register	(3)
P4$_0$	Port P4	Input/output, individual bits	CMOS compatible input level N-channel open-drain output			(13)
P4$_1$/INT$_1$, P4$_2$/INT$_2$			CMOS compatible input level CMOS 3-state output	INT$_i$ interrupt input	Interrupt edge selection register	(4)
P4$_3$/φ/T$_{OUT}$				Timer 2 output System clock φ output	PULL register B Timer 123 mode register T$_{OUT}$/φ output control register	(12)
P4$_4$/R$_X$D, P4$_5$/T$_X$D, P4$_6$/S$_{CLK1}$, P4$_7$/$\overline{S_{RDY1}}$				Serial I/O1 I/O	PULL register B Serial I/O1 control register Serial I/O1 status register UART control register	(5) (6) (7) (8)
P5$_0$/PWM$_0$, P5$_1$/PWM$_1$	Port P5	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	PWM output	PULL register B PWM control register	(10)
P5$_2$/RTP$_0$, P5$_3$/RTP$_1$				Real time port output	PULL register B Timer X mode register	(9)
P5$_4$/CNTR$_0$				Timer X I/O	PULL register B Timer X mode register	(11)
P5$_5$/CNTR$_1$				Timer Y input	PULL register B Timer Y mode register	(14)
P5$_6$/DA$_1$				DA$_1$ output DTMF input	PULL register B DA control register	(15)
P5$_7$/ADT/DA$_2$				DA$_2$ output CTCSS output A/D external trigger input	PULL register B DA control register AD control register	(15)

Table 7 List of I/O port function (2)

Pin	Name	Input/Output	I/O Format	Non-Port Function	Related SFRs	Diagram No.
$P6_0$/S_{IN2}/AN_0	Port P6	Input/ output, individual bits	CMOS compatible input level CMOS 3-state output	A/D converter input Serial I/O2 I/O	PULL register B AD control register Serial I/O2 control register	(17)
$P6_1$/S_{OUT2}/ AN_1						(18)
$P6_2$/S_{CLK21}/ AN_2						(19)
$P6_3$/S_{CLK22} / AN_3						(20)
$P6_4$/AN_4– $P6_7$/AN_7				A/D converter input	AD control register PULL register B	(16)
$P7_0$/INT_0	Port P7	Input	CMOS compatible input level	INT_0 interrupt input	Interrupt edge selection register	(23)
$P7_1$–$P7_7$		Input/ output, individual bits	CMOS compatible input level N-channel open-drain output			(13)
COM_0–COM_3	Common	Output	LCD common output		LCD mode register	(21)
SEG_0–SEG_{17}	Segment	Output	LCD segment output			(22)

Notes 1: How to use double-function ports as function I/O pins, refer to the applicable sections.

2: Make sure that the input level at each pin is either 0 V or V_{CC} before execution of the STP instruction. When an electric potential is at an intermediate potential, a current will flow from V_{CC} to V_{SS} through the input-stage gate and power source current may increase.

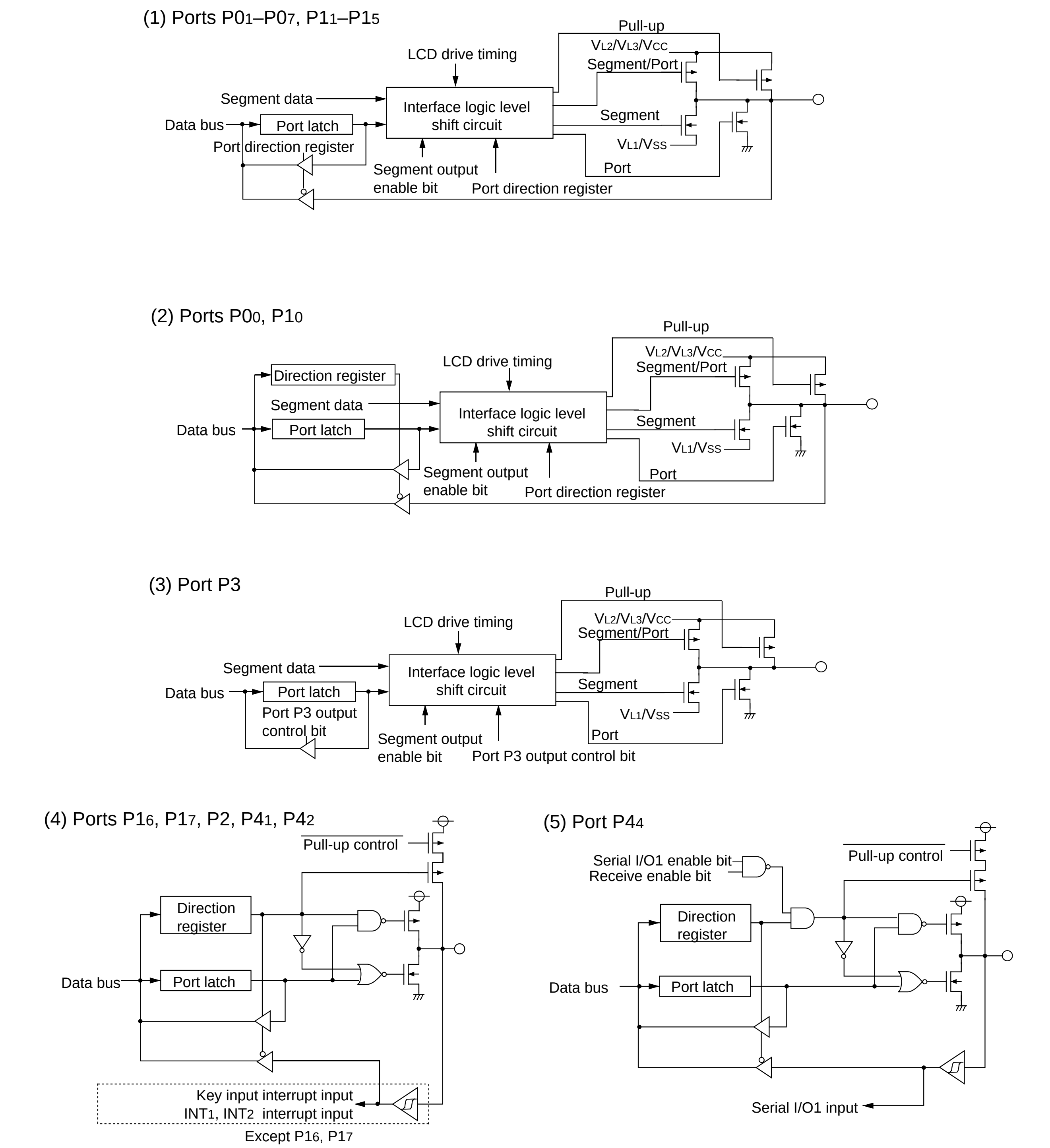


Fig. 14 Port block diagram (1)

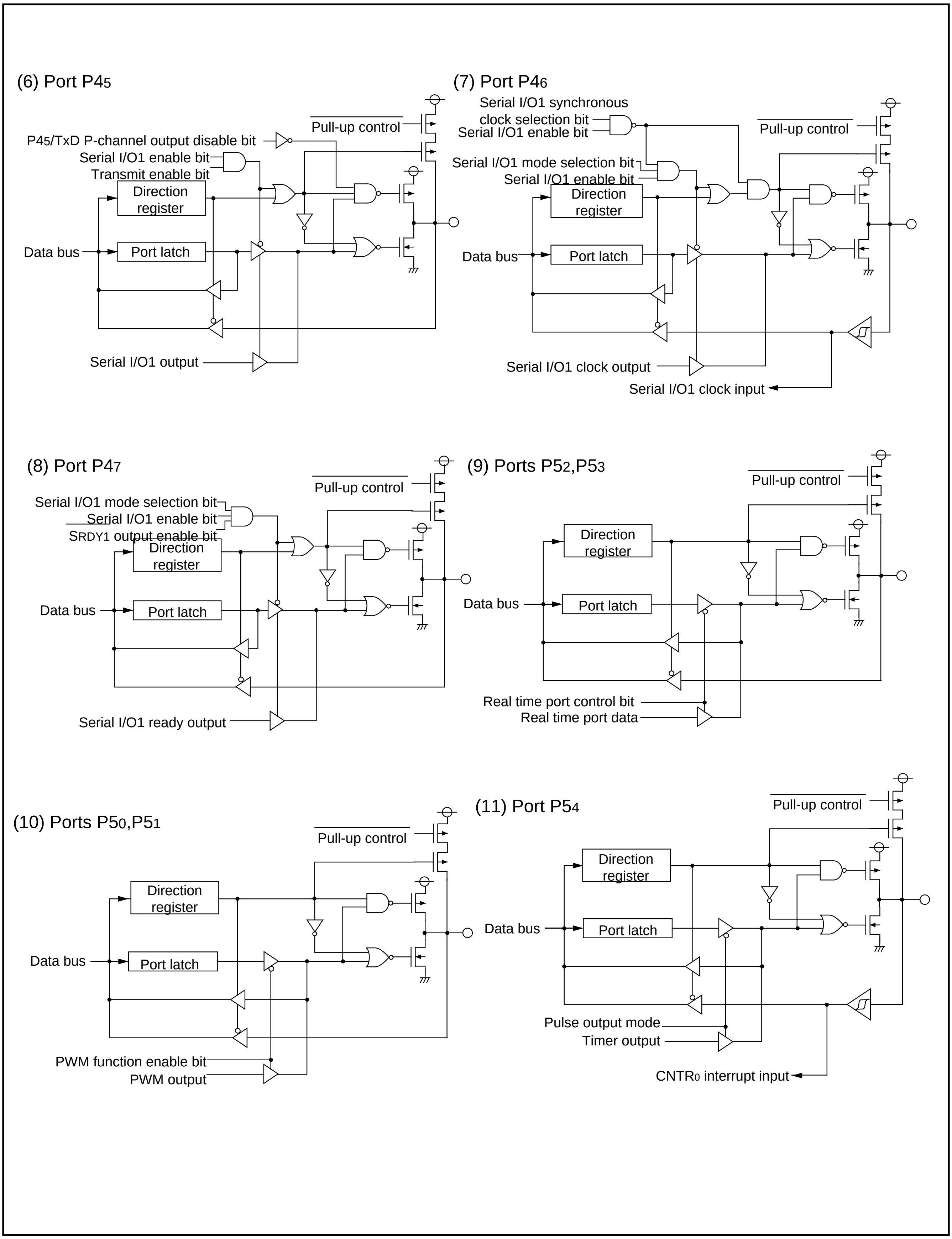


Fig. 15 Port block diagram (2)

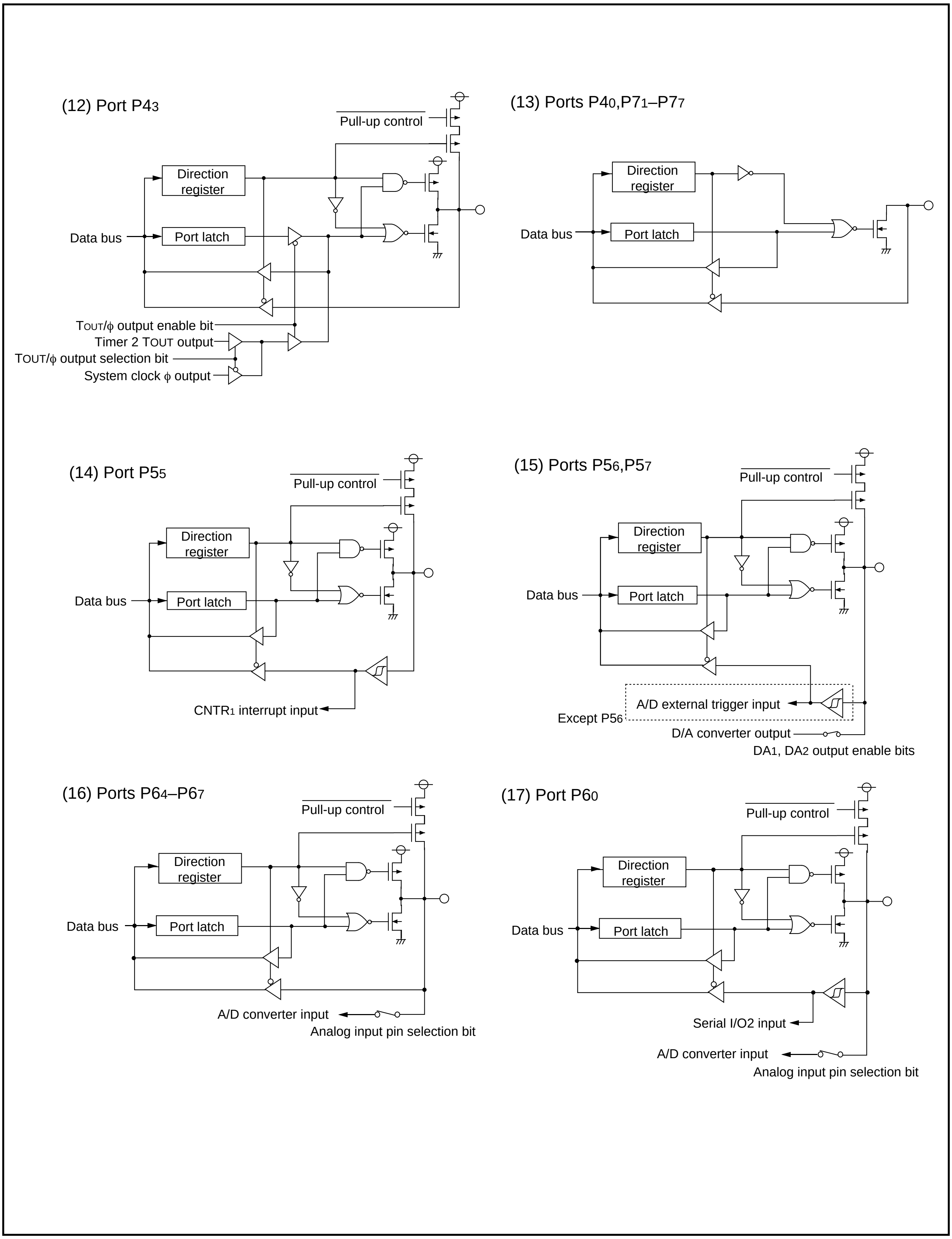


Fig. 16 Port block diagram (3)

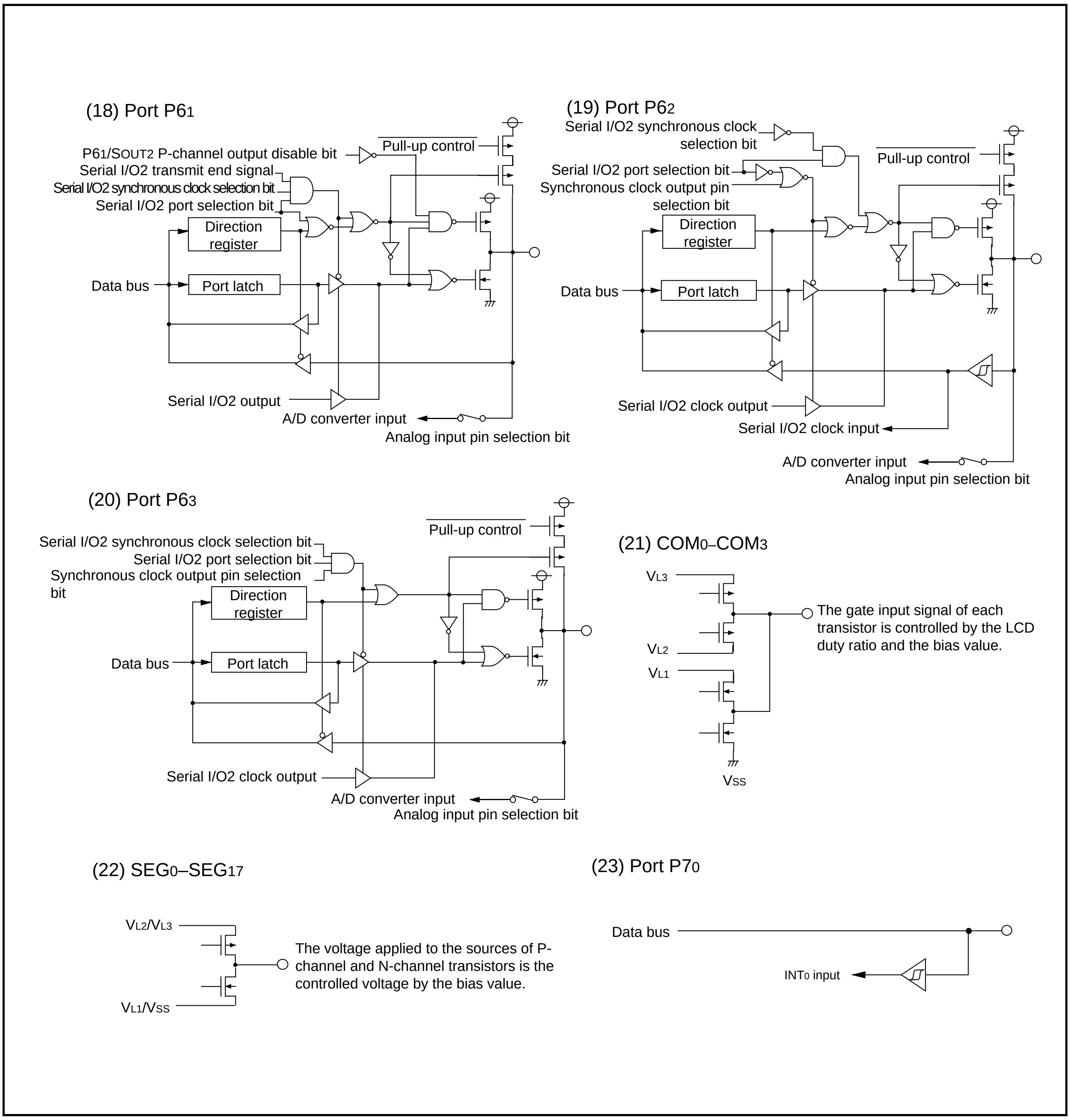


Fig. 17 Port block diagram (4)

INTERRUPTS

Interrupts occur by seventeen sources: seven external, nine internal, and one software. When an interrupt request is accepted, the program branches to the interrupt jump destination address set in the vector address (see Table 8).

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt is accepted if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.
Interrupt enable bits can be set to “0” or “1” by program.
Interrupt request bits can be set to “0” by program, but cannot be set to “1” by program.
The BRK instruction interrupt and reset cannot be disabled with any flag or bit. When the interrupt disable (I) flag is set to “1”, all interrupt requests except the BRK instruction interrupt and reset are not accepted.
When several interrupt requests occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt jump destination address is read from the vector table into the program counter.
3. The interrupt disable flag is set to “1” and the corresponding interrupt request bit is set to “0”.

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset **(Note 2)**	1	FFFD$_{16}$	FFFC$_{16}$	At reset	Non-maskable
INT$_0$	2	FFFB$_{16}$	FFFA$_{16}$	At detection of either rising or falling edge of INT$_0$ input	External interrupt (active edge selectable)
INT$_1$	3	FFF9$_{16}$	FFF8$_{16}$	At detection of either rising or falling edge of INT$_1$ input	External interrupt (active edge selectable)
Serial I/O1 reception	4	FFF7$_{16}$	FFF6$_{16}$	At completion of serial I/O1 data reception	Valid when serial I/O1 is selected
Serial I/O1 transmission	5	FFF5$_{16}$	FFF4$_{16}$	At completion of serial I/O1 transmit shift or when transmission buffer is empty	Valid when serial I/O1 is selected
Timer X	6	FFF3$_{16}$	FFF2$_{16}$	At timer X underflow	
Timer Y	7	FFF1$_{16}$	FFF0$_{16}$	At timer Y underflow	
Timer 2	8	FFEF$_{16}$	FFEE$_{16}$	At timer 2 underflow	
Timer 3	9	FFED$_{16}$	FFEC$_{16}$	At timer 3 underflow	
CNTR$_0$	10	FFEB$_{16}$	FFEA$_{16}$	At detection of either rising or falling edge of CNTR$_0$ input	External interrupt (active edge selectable)
CNTR$_1$	11	FFE9$_{16}$	FFE8$_{16}$	At detection of either rising or falling edge of CNTR$_1$ input	External interrupt (active edge selectable)
Timer 1	12	FFE7$_{16}$	FFE6$_{16}$	At timer 1 underflow	
INT$_2$	13	FFE5$_{16}$	FFE4$_{16}$	At detection of either rising or falling edge of INT$_2$ input	External interrupt (active edge selectable)
Serial I/O2	14	FFE3$_{16}$	FFE2$_{16}$	At completion of serial I/O2 data transmission or reception	Valid when serial I/O2 is selected
Key input (Key-on wake-up)	15	FFE1$_{16}$	FFE0$_{16}$	At falling of conjunction of input level for port P2 (at input mode)	External interrupt (valid at falling)
ADT	16	FFDF$_{16}$	FFDE$_{16}$	At falling edge of ADT input	Valid when ADT interrupt is selected External interrupt (valid at falling)
A/D conversion				At completion of A/D conversion	Valid when A/D interrupt is selected
BRK instruction	17	FFDD$_{16}$	FFDC$_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes1: Vector addresses contain interrupt jump destination addresses.
2: Reset is not an interrupt. Reset has the higher priority than all interrupts.

■Notes on interrupts

When setting the followings, the interrupt request bit may be set to “1”.

•When switching external interrupt active edge

Related register: Interrupt edge selection register (address $3A_{16}$)
Timer X mode register (address 27_{16})
Timer Y mode register (address 28_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

Related register: Interrupt source selection bit of AD control register (bit 6 of address 34_{16})

When not requiring for the interrupt occurrence synchronous with these setting, take the following sequence.

①Set the corresponding interrupt enable bit to “0” (disabled).

②Set the interrupt edge select bit (polarity switch bit) or the interrupt source selection bit.

③Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.

④Set the corresponding interrupt enable bit to “1” (enabled).

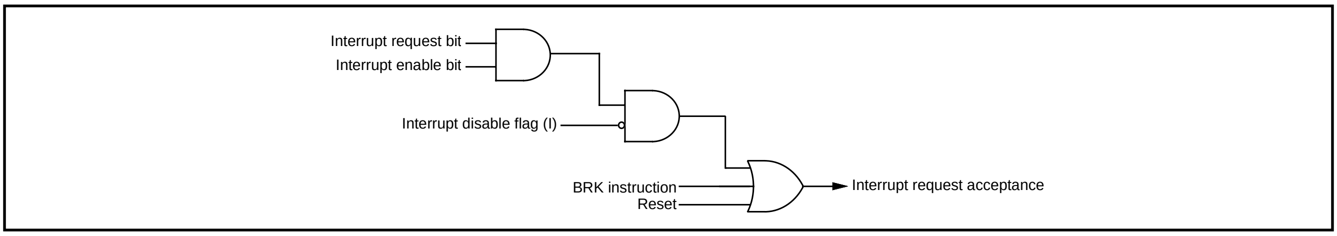


Fig. 18 Interrupt control

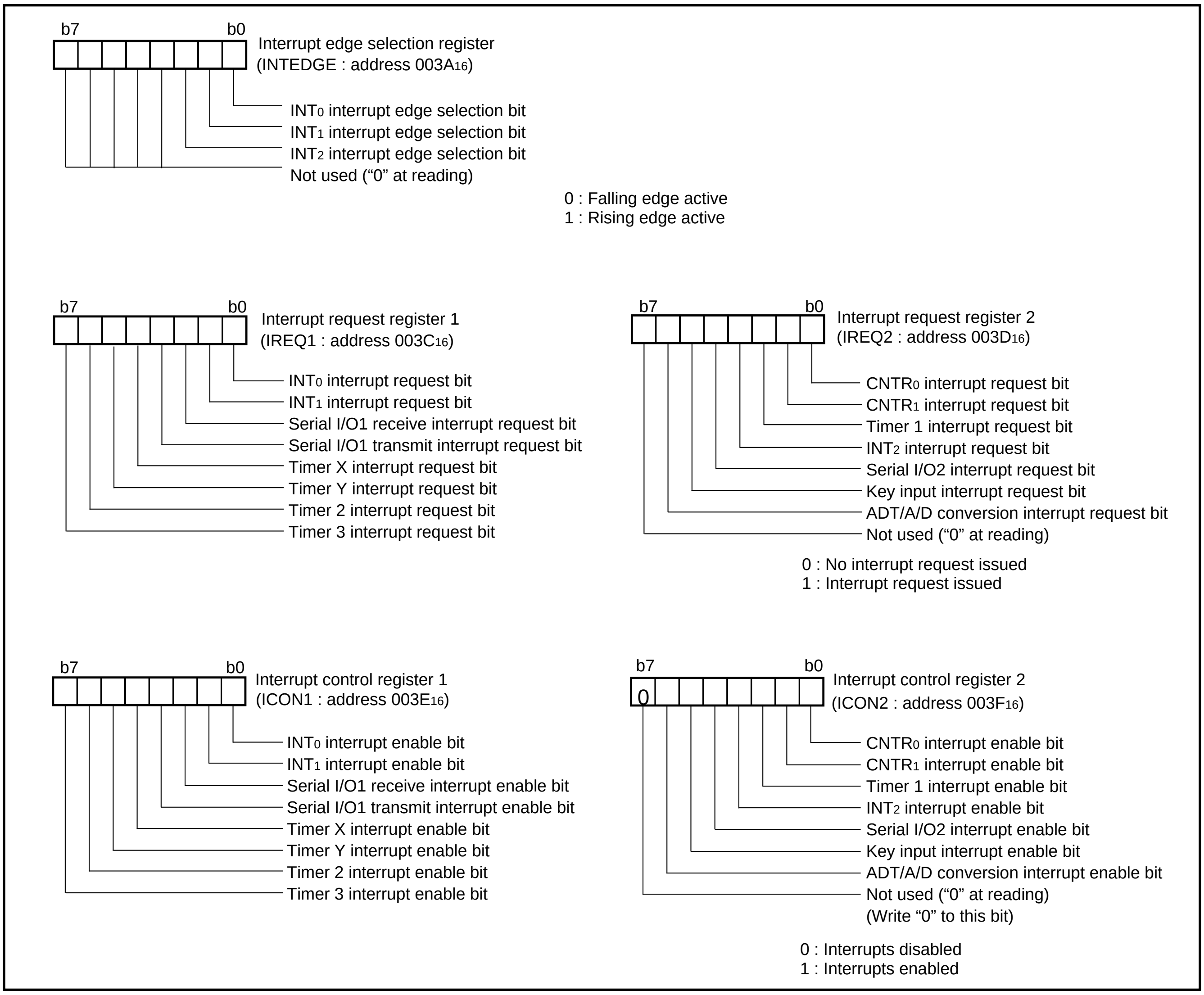


Fig. 19 Structure of interrupt-related registers

Key Input Interrupt (Key-on Wake Up)

The key input interrupt is enabled when any of port P2 is set to input mode and the bit corresponding to key input control register is set to “1”.

A Key input interrupt request is generated by applying “L” level voltage to any pin of port P2 of which key input interrupt is enabled. In other words, it is generated when AND of input level goes from “1” to “0”. A connection example of using a key input interrupt is shown in Figure 20, where an interrupt request is generated by pressing one of the keys consisted as an active-low key matrix which inputs to ports $P2_0$–$P2_3$.

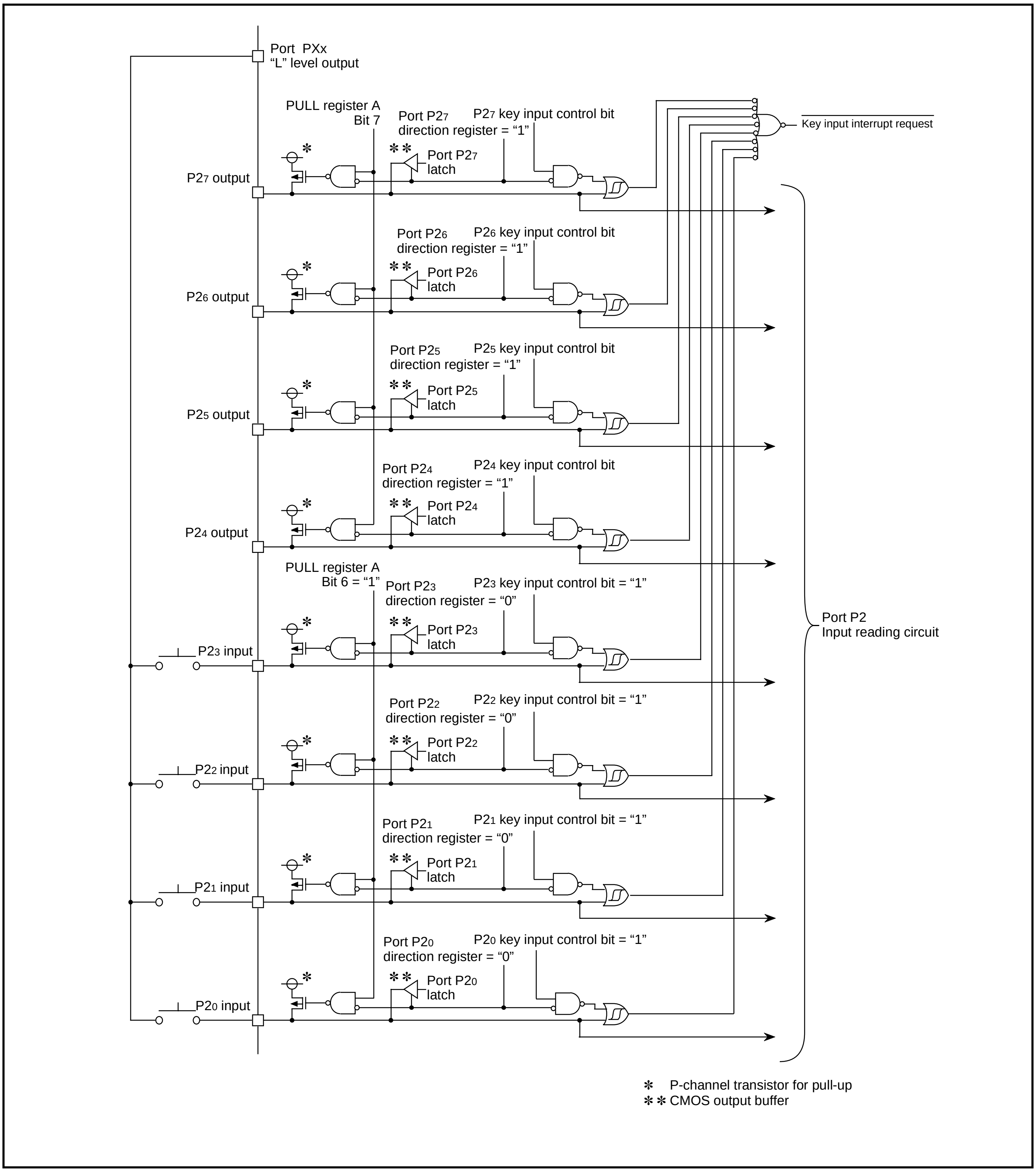


Fig. 20 Connection example when using key input interrupt and port P2 block diagram

The key input interrupt is controlled by the key input control register and the port direction register. When enabling the key input interrupt, set “1” to the key input control bit. A key input can be accepted from pins set as the input mode in ports $P2_0$–$P2_7$.

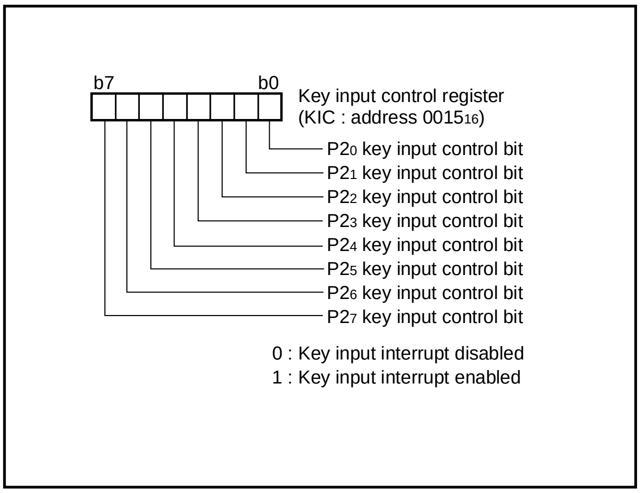


Fig. 21 Structure of key input control register

TIMERS

The 3826 group has five timers: timer X, timer Y, timer 1, timer 2, and timer 3. Timer X and timer Y are 16-bit timers, and timer 1, timer 2, and timer 3 are 8-bit timers.
All timers are down count timers. When the timer reaches “0”, an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to “1”.

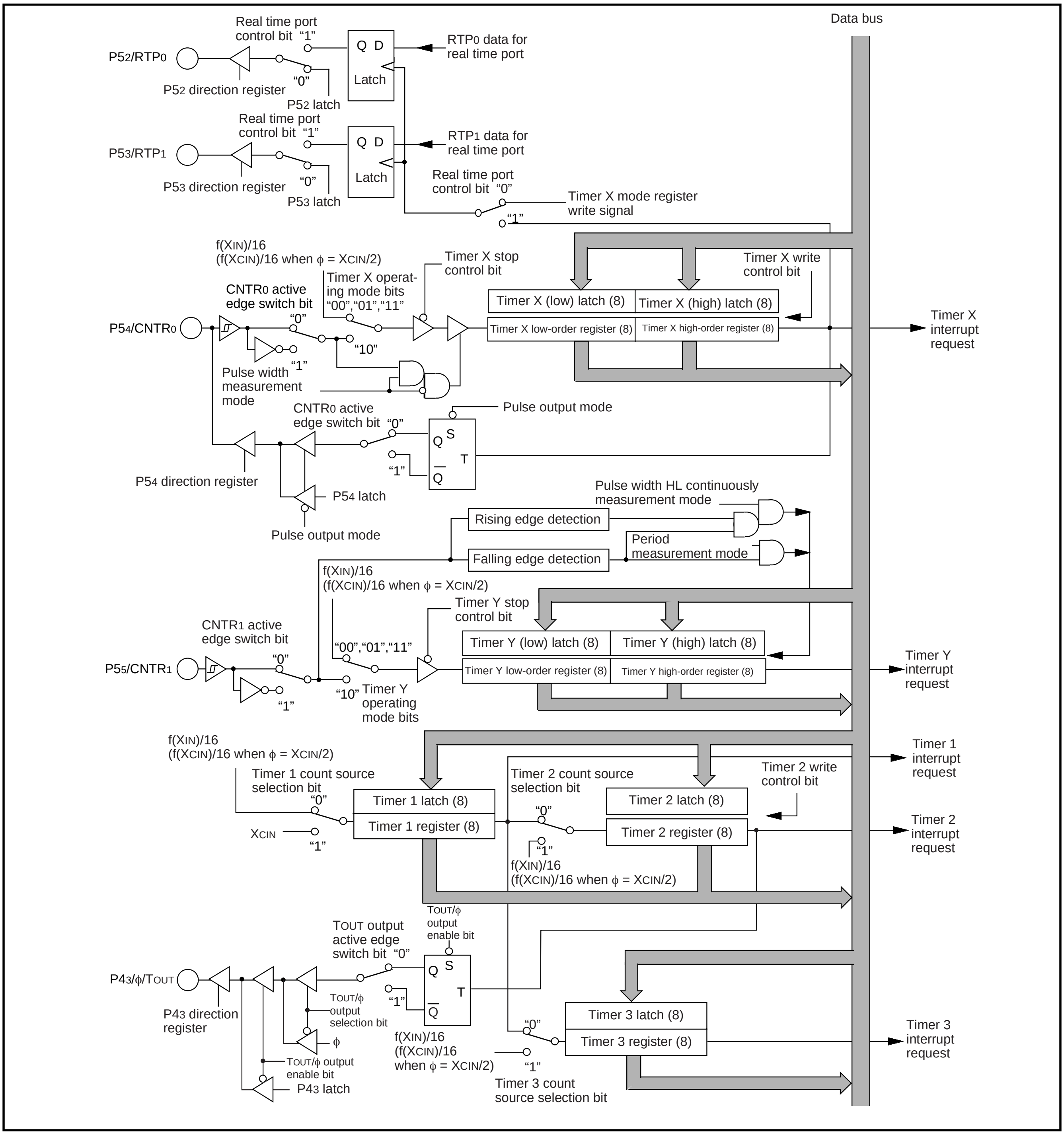


Fig. 22 Timer block diagram

Timer X

Timer X is a 16-bit timer and is equipped with the timer latch. The division ratio of timer X is given by 1/(n+1), where n is the value in the timer latch. Timer X is a down-counter. When the contents of timer X reach “0000_{16}”, an underflow occurs at the next count pulse and the contents of the timer latch are reloaded into the timer and the count is continued. When the timer underflows, the timer X interrupt request bit is set to “1”.
Timer X can be selected in one of four modes by the timer X mode register and can be controlled the timer X write and the real time port.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Pulse output mode

Each time the timer underflows, a signal output from the $CNTR_0$ pin is inverted. Except for this, the operation in pulse output mode is the same as in timer mode. When using a timer in this mode, set the $P5_4/CNTR_0$ pin to output mode (set “1” to bit 4 of port P5 direction register).

(3) Event counter mode

The timer counts signals input through the $CNTR_0$ pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the $P5_4/CNTR_0$ pin to input mode (set “0” to bit 4 of port P5 direction register).

(4) Pulse width measurement mode

The count source is $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode). If $CNTR_0$ active edge switch bit is “0”, the timer counts while the input signal of $CNTR_0$ pin is at “H”. If it is “1”, the timer counts while the input signal of $CNTR_0$ pin is at “L”. When using a timer in this mode, set the $P5_4/CNTR_0$ pin to input mode (set “0” to bit 4 of port P5 direction register).

●Read and write to timer X high-order, low-order registers

When reading and writing to the timer X high-order and low-order registers, be sure to read/write both the timer X high- and low-order registers.
When reading the timer X high-order and low-order registers, read the high-order register first. When writing to the timer X high-order and low-order registers, write the low-order register first. The timer X cannot perform the correct operation if the next operation is performed.
•Write operation to the high- or low-order register before reading the timer X low-order register
•Read operation from the high- or low-order register before writing to the timer X high-order register

●Timer X Write Control

Which write control can be selected by the timer X write control bit (bit 0) of the timer X mode register (address 0027_{16}), writing data to both the latch and the timer at the same time or writing data only to the latch. When the operation “writing data only to the latch” is selected, the value is set to the timer latch by writing data to the timer X register and the timer is updated at next underflow. After reset, the operation “writing data to both the latch and the timer at the same time” is selected, and the value is set to both the latch and the timer at the same time by writing data to the timer X register. The write operation is independent of timer X count operation, operating or stopping.
When the value is written in latch only, a value is simultaneously set to the timer X and the timer X latch if the writing in the high-order register and the underflow of timer X are performed at the same timing. Unexpected value may be set in the high-order timer on this occasion.

●Real Time Port Control

While the real time port function is valid, data for the real time port are output from ports $P5_2$ and $P5_3$ each time the timer X underflows. (However, if the real time port control bit is changed from “0” to “1” after set of the real time port data, data are output independent of the timer X operation.) If the data for the real time port is changed while the real time port function is valid, the changed data are output at the next underflow of timer X.
Before using this function, set the $P5_2/RTP_0$, $P5_3/RTP_1$ pins to output mode (set “1” to bits 2, 3 of port P5 direction register).

■Note on $CNTR_0$ interrupt active edge selection

$CNTR_0$ interrupt active edge depends on the $CNTR_0$ active edge switch bit.

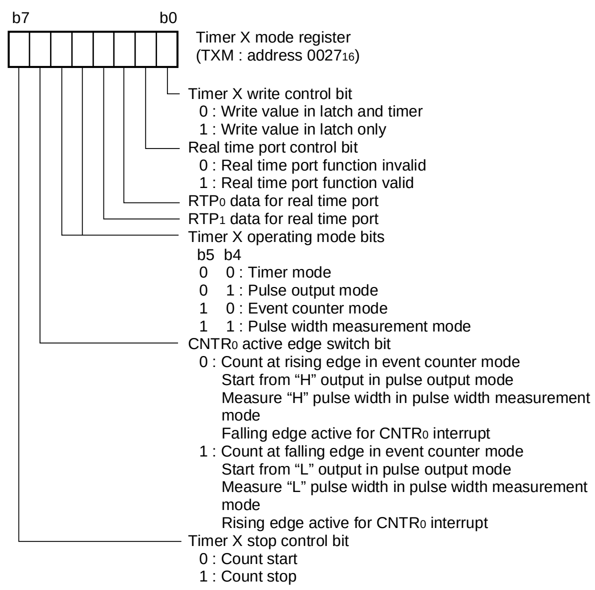


Fig. 23 Structure of timer X mode register

Timer Y

Timer Y is a 16-bit timer and is equipped with the timer latch. The division ratio of timer Y is given by 1/(n+1), where n is the value in the timer latch. Timer Y is a down-counter. When the contents of timer Y reach "0000_{16}", an underflow occurs at the next count pulse and the contents of the timer latch are reloaded into the timer and the count is continued. When the timer underflows, the timer Y interrupt request bit is set to "1".
Timer Y can be selected in one of four modes by the timer Y mode register.

(1) Timer mode

The timer counts $f(X_{IN})/16$ (or $f(X_{CIN})/16$ in low-speed mode).

(2) Period measurement mode

$CNTR_1$ interrupt request is generated at rising or falling edge of $CNTR_1$ pin input signal. Simultaneously, the value in timer Y latch is reloaded in timer Y and timer Y continues counting down. Except for this, the operation in period measurement mode is the same as in timer mode.
The timer value just before the reloading at rising or falling of $CNTR_1$ pin input signal is retained until the next valid edge is input.
The rising or falling timing of $CNTR_1$ pin input signal can be discriminated by $CNTR_1$ interrupt. When using a timer in this mode, set the $P5_5/CNTR_1$ pin to input mode (set "0" to bit 5 of port P5 direction register).

(3) Event counter mode

The timer counts signals input through the $CNTR_1$ pin.
Except for this, the operation in event counter mode is the same as in timer mode. When using a timer in this mode, set the $P5_5/CNTR_1$ pin to input mode (set "0" to bit 5 of port P5 direction register).

(4) Pulse width HL continuously measurement mode

$CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal. Except for this, the operation in pulse width HL continuously measurement mode is the same as in period measurement mode. When using a timer in this mode, set the $P5_5/CNTR_1$ pin to input mode (set "0" to bit 5 of port P5 direction register).

■Note on $CNTR_1$ interrupt active edge selection

$CNTR_1$ interrupt active edge depends on the value of the $CNTR_1$ active edge switch bit. However, in pulse width HL continuously measurement mode, $CNTR_1$ interrupt request is generated at both rising and falling edges of $CNTR_1$ pin input signal regardless of the value of $CNTR_1$ active edge switch bit.

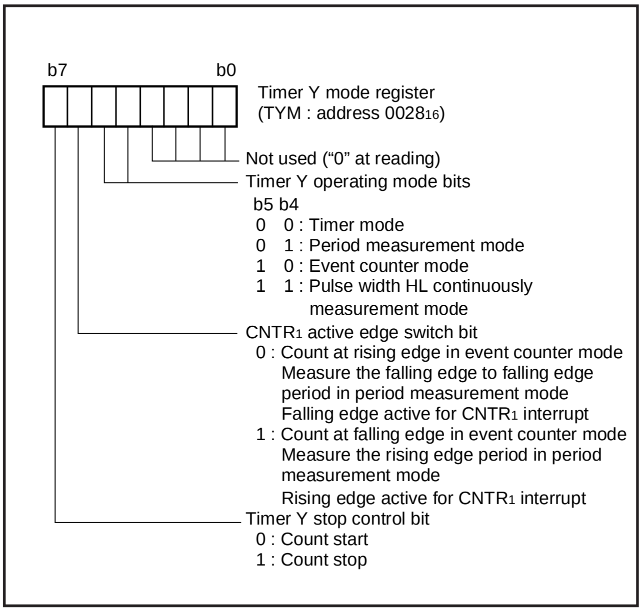


Fig. 24 Structure of timer Y mode register

Timer 1, Timer 2, Timer 3

Timer 1, timer 2, and timer 3 are 8-bit timers and are equipped with the timer latch. The count source for each timer can be selected by the timer 123 mode register.

The division ratio of each timer is given by 1/(n+1), where n is the value in the timer latch. All timers are down-counters. When the contents of the timer reach "00_{16}", an underflow occurs at the next count pulse and the contents of the timer latch are reloaded into the timer and the count is continued. When the timer underflows, the interrupt request bit corresponding to that timer is set to "1".

When a value is written to the timer 1 register and the timer 3 register, a value is simultaneously set as the timer latch and the timer. When the timer 1 register, the timer 2 register, or the timer 3 register is read, the count value of the timer can be read.

●Timer 2 Write Control

Which write can be selected by the timer 2 write control bit (bit 2) of the timer 123 mode register (address 0029_{16}), writing data to both the latch and the timer at the same time or writing data only to the latch. When the operation "writing data only to the latch" is selected, the value is set to the timer 2 latch by writing data to the timer 2 register and the timer 2 is updated at next underflow. After reset, the operation "writing data to both the latch and the timer at the same time" is selected, and the value is set to both the timer 2 latch and the timer 2 at the same time by writing data to the timer 2 register.

If the value is written in latch only, a value is simultaneously set to the timer 2 and the timer 2 latch when the writing in the high-order register and the underflow of timer 2 are performed at the same timing.

●Timer 2 Output Control

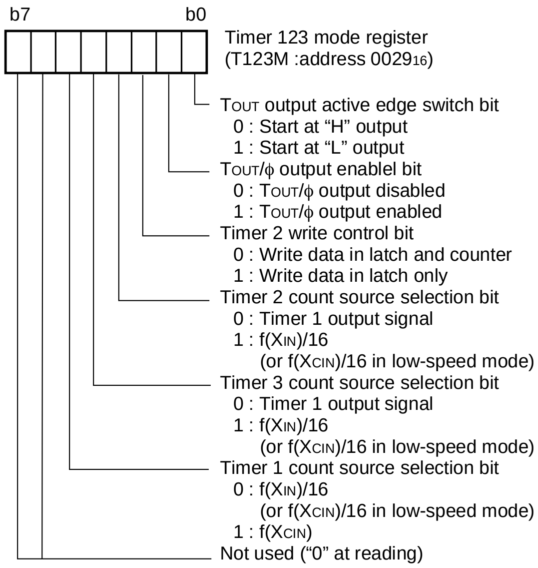
When the timer 2 (T_{OUT}) output is enabled by the T_{OUT}/ϕ output enable bit and the T_{OUT}/ϕ output selection bit, an inversion signal from the T_{OUT} pin is output each time timer 2 underflows.

In this case, set the $P4_3/\phi/T_{OUT}$ pin to output mode (set "1" to bit 3 of port P4 direction register).

■Note on Timer 1 to Timer 3

When the count source of timers 1 to 3 is changed, the timer counting value may become arbitrary value because a thin pulse is generated in count input of timer. If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may become undefined value because a thin pulse is generated in timer 1 output.

Therefore, set the value of timer in the order of timer 1, timer 2 and timer 3 after the count source selection of timer 1 to 3.



Note: System clock ϕ is $f(X_{CIN})/2$ in the low-speed mode.

Fig. 25 Structure of timer 123 mode register

SERIAL INTERFACE
Serial I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer (baud rate generator) is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode is selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register to “1”.
For clock synchronous serial I/O mode, the transmitter and the receiver must use the same clock as an operation clock.
When an internal clock is selected as an operation clock, transmit or receive is started by a write signal to the transmit buffer register.
When an external clock is selected as an operation clock, serial I/O1 becomes the state where transmit or receive can be performed by a write signal to the transmit buffer register. Transmit and receive are started by input of an external clock.

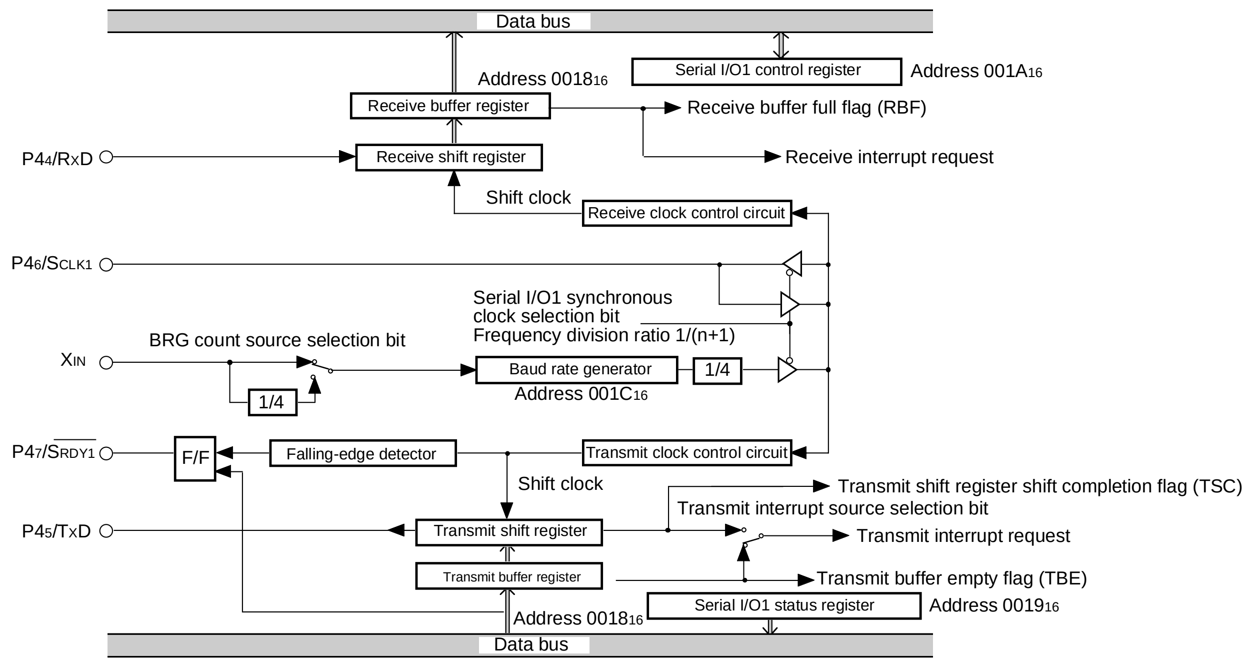
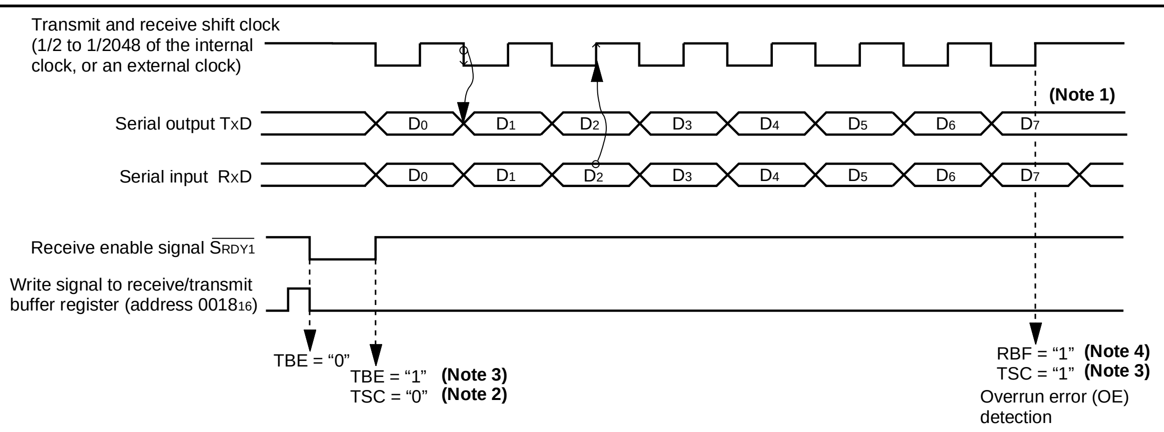


Fig. 26 Block diagram of clock synchronous serial I/O1



Notes
1 : After data transferring, the TxD pin keeps D7 output value.
2 : If data is written to the transmit buffer register when TSC = “0”, the transmit clock is generated continuously and serial data can be output continuously from the TxD pin.
3 : Select the serial I/O1 transmit interrupt request factor between when the transmit buffer register has emptied (TBE = “1”) or after the transmit shift operation has ended (TSC = “1”), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
4 : The serial I/O1 receive interrupt request occurs when the receive buffer full flag (RBF) becomes “1”.

Fig. 27 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) is selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register to “0”.

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer register, but the two buffers have the same address (0018_{16}) in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer, and receive data is read from the receive buffer.

The transmit buffer can also hold the next data to be transmitted during transmitting, and the receive buffer register can hold received one-byte data while the next one-byte data is being received.

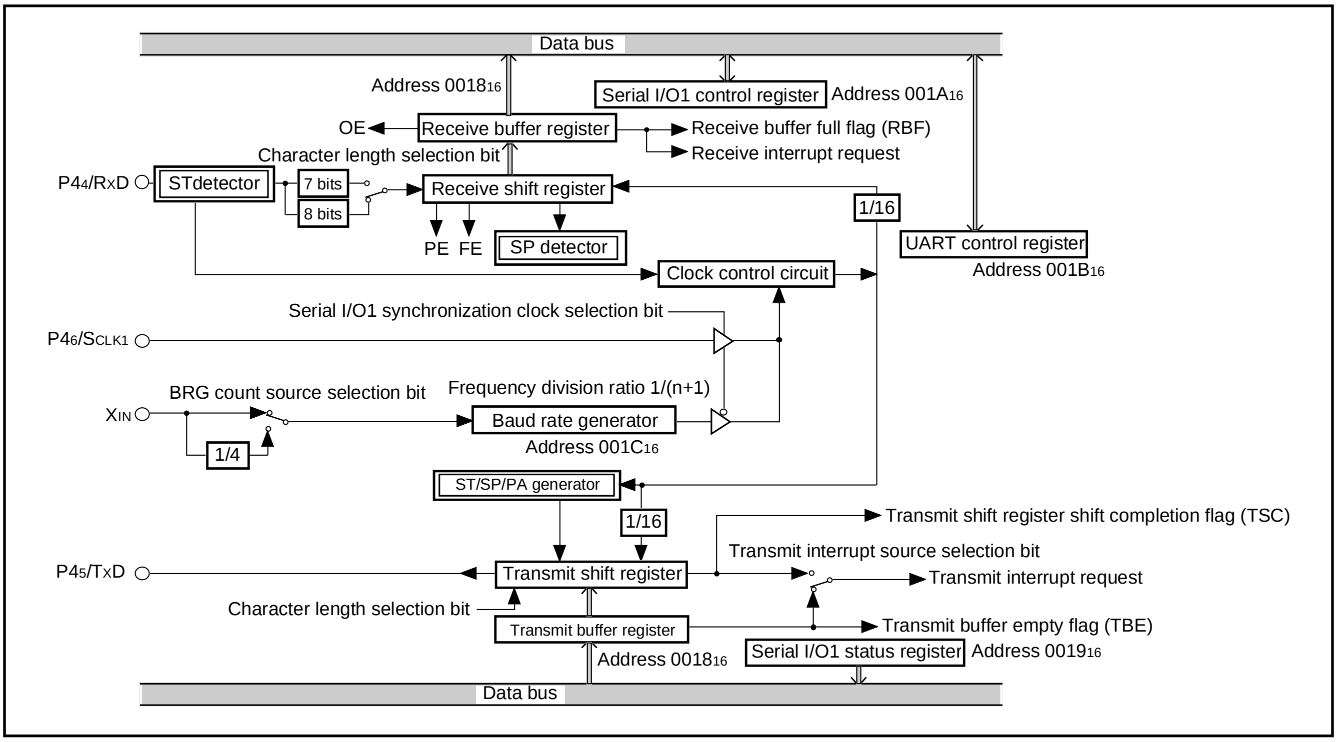
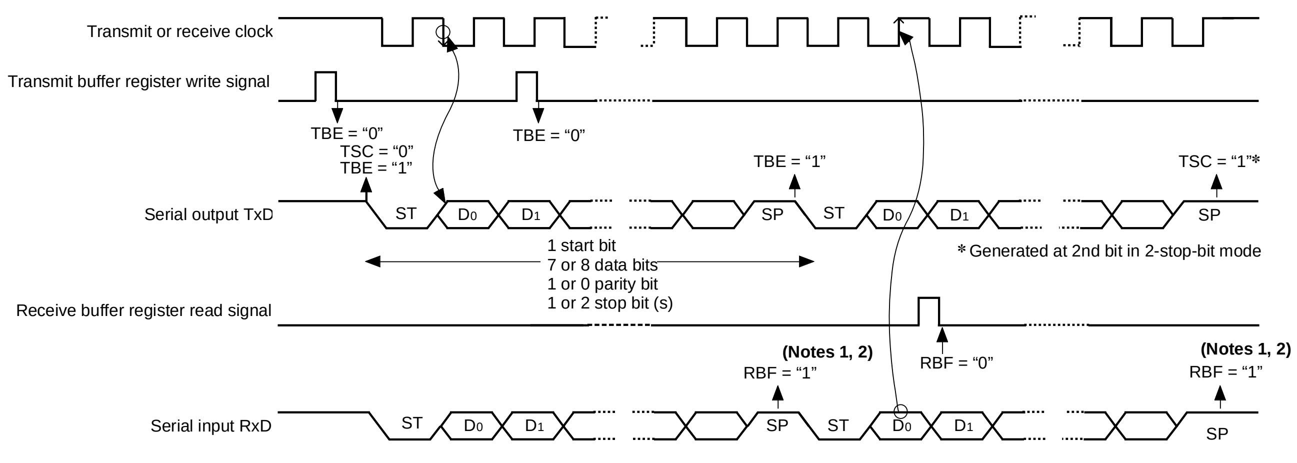


Fig. 28 Block diagram of UART serial I/O1



Notes 1 : Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit for reception).
2 : The serial I/O1 receive interrupt request occurs when the receive buffer full flag (RBF) becomes “1”.
3 : Select the serial I/O1 transmit interrupt request occurrence factor between when the transmit buffer register has emptied (TBE = “1”) or after the transmit shift operation has ended (TSC = “1”), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.

Fig. 29 Operation of UART serial I/O1 function

[Transmit Buffer/Receive Buffer Register (TB/RB)] 0018_{16}

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer register is write-only and the receive buffer register is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer register is “0”.

[Serial I/O1 Status Register (SIO1STS)] 0019_{16}

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is set to “0” when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set to “1”. A write signal to the serial I/O1 status register sets all the error flags (OE, PE, FE, and SE) (bit 3 to bit 6, respectively) to “0”. Writing “0” to the serial I/O1 enable bit (SIOE) also sets all the status flags to “0”, including the error flags.
All bits of the serial I/O1 status register are set to “0” at reset, but if the transmit enable bit of the serial I/O1 control register has been set to “1”, the transmit shift register shift completion flag and the transmit buffer empty flag become “1”.

[Serial I/O1 Control Register (SIO1CON)] $001A_{16}$

The serial I/O1 control register contains eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] $001B_{16}$

The UART control register consists of the bits which set the data format of a data transmit and receive, and the bit which sets the output structure of the $P4_5$/TxD pin.

[Baud Rate Generator (BRG)] $001C_{16}$

The baud rate generator is the 8-bit counter equipped with a reload register. Set the division value of the BRG count source to the baud rate generator.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

■Notes on serial I/O

When setting the transmit enable bit to “1”, the serial I/O1 transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronous with the transmission enabled, take the following sequence.
①Set the serial I/O1 transmit interrupt enable bit to “0” (disabled).
②Set the transmit enable bit to “1”.
③Set the serial I/O1 transmit interrupt request bit to “0” after 1 or more instructions have been executed.
④Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

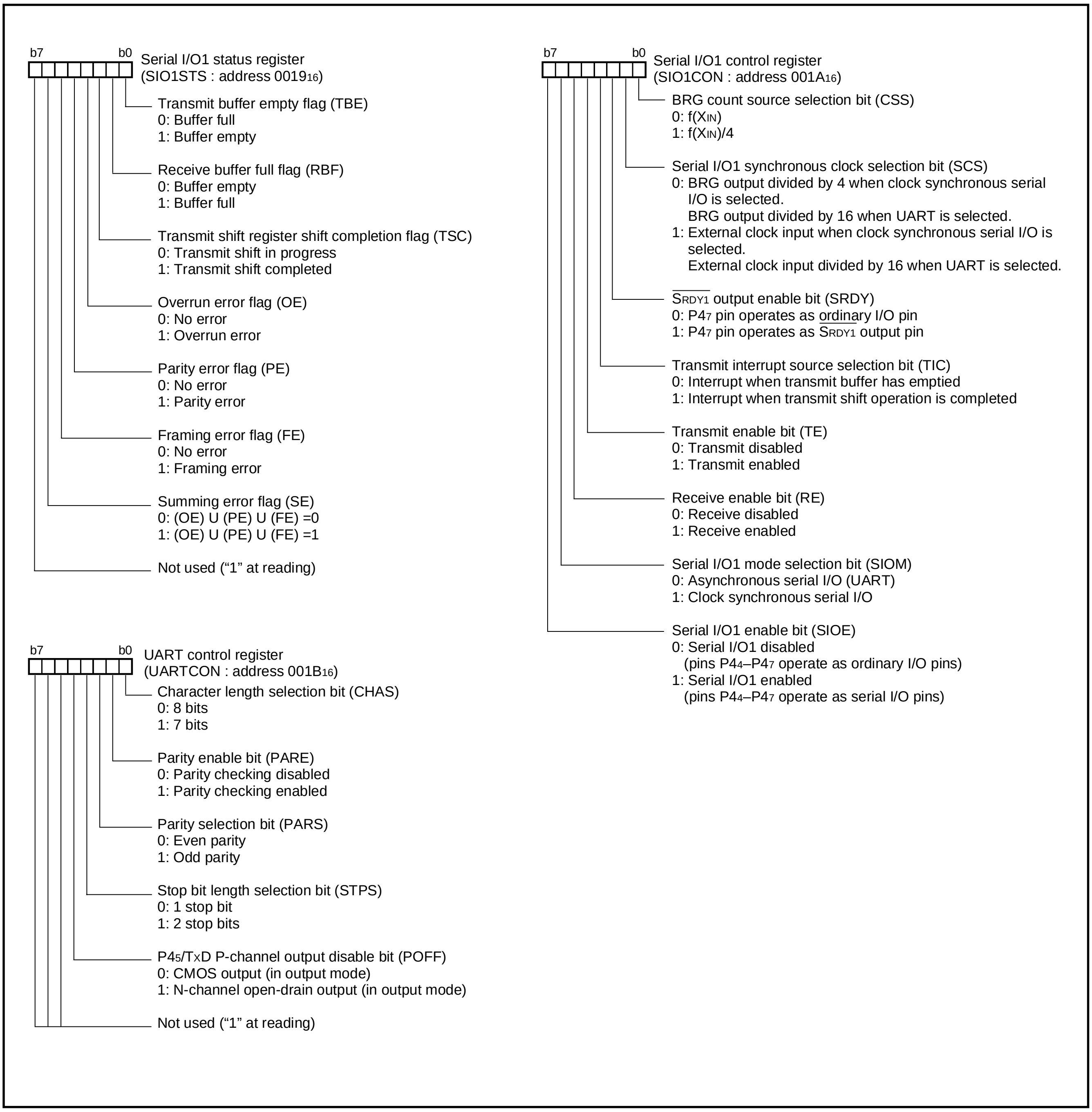


Fig. 30 Structure of serial I/O1 control registers

RENESAS

Serial I/O2

Serial I/O2 can be used only for clock synchronous serial I/O.
For serial I/O2, the transmitter and the receiver must use the same clock as a synchronous clock. When an internal clock is selected as a synchronous clock, the serial I/O2 is initialized and, transmit and receive is started by a write signal to the serial I/O2 register.
When an external clock is selected as an synchronous clock, the serial I/O2 counter is initialized by a write signal to the serial I/O2 register, serial I/O2 becomes the state where transmission or reception can be performed. Write to the serial I/O2 register while SCLK21 is "H" state when an external clock is selected as an synchronous clock.
Either P62/SCLK21 or P63/SCLK22 pin can be selected as an output pin of the synchronous clock. In this case, the pin that is not selected as an output pin of the synchronous clock functions as a I/O port.

[Serial I/O2 Control Register (SIO2CON)] 001D16

The serial I/O2 control register contains eight control bits for the serial I/O2 functions. After setting to this register, write data to the serial I/O2 register and start transmit and receive.

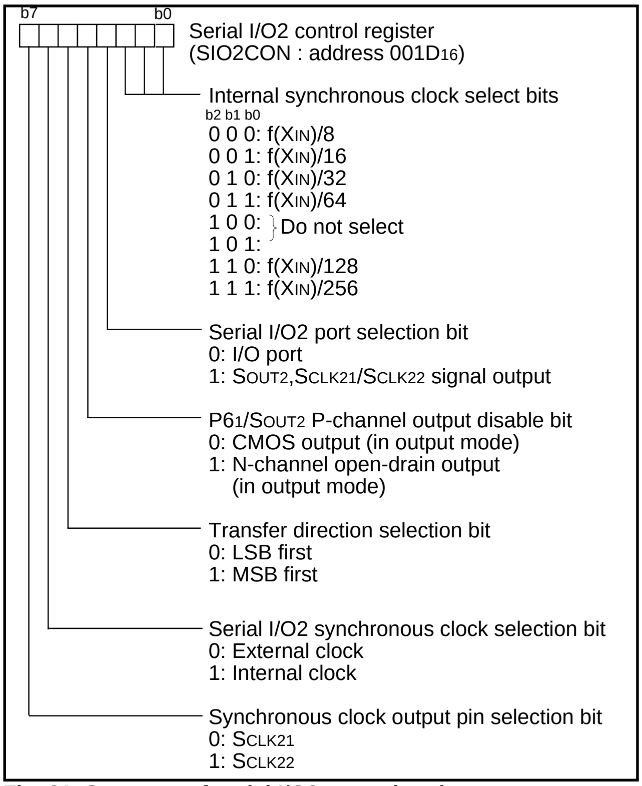


Fig. 31 Structure of serial I/O2 control register

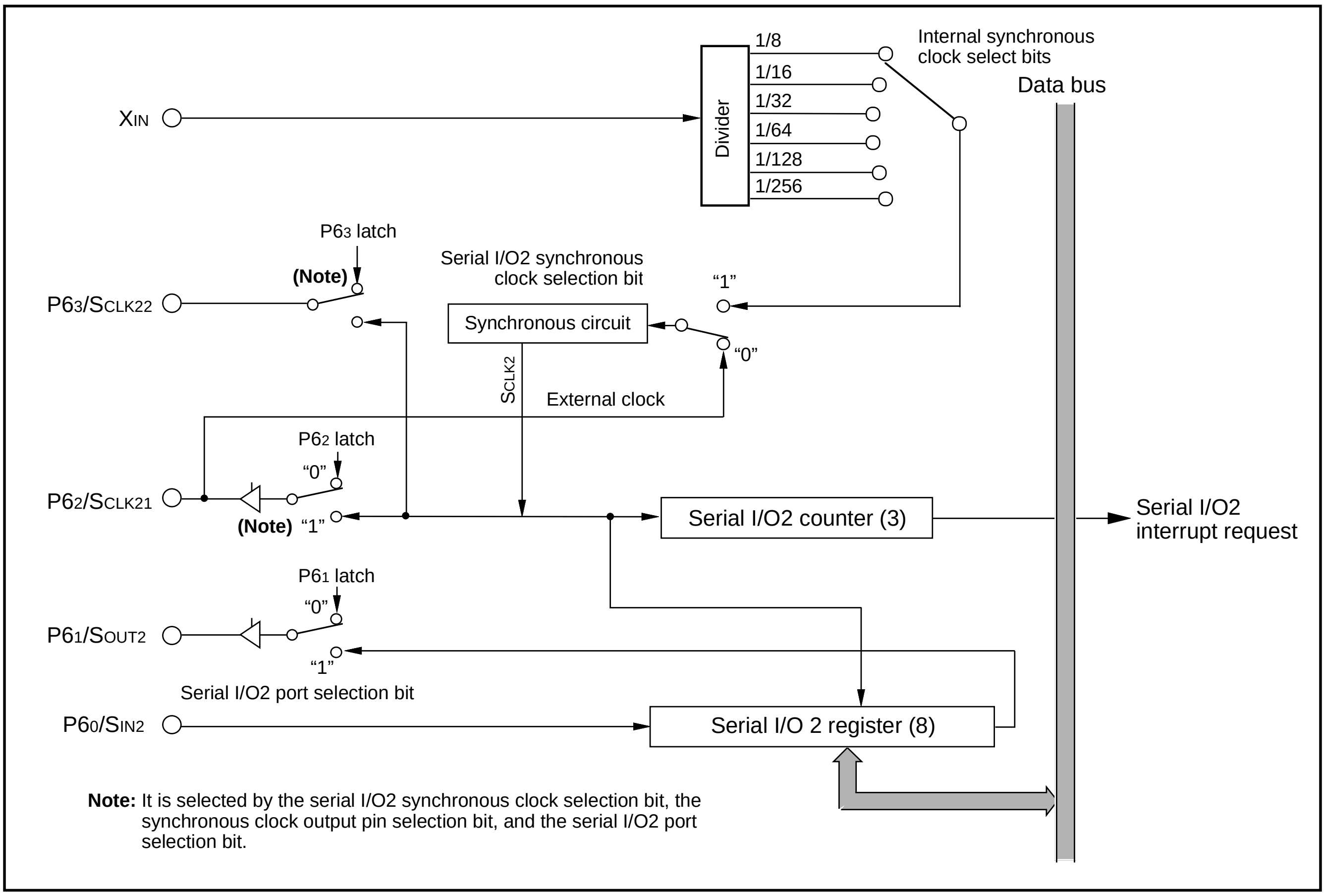


Fig. 32 Block diagram of serial I/O2 function

●Serial I/O2 Operating

The serial I/O2 counter is initialized to “7” by writing to the serial I/O2 register.

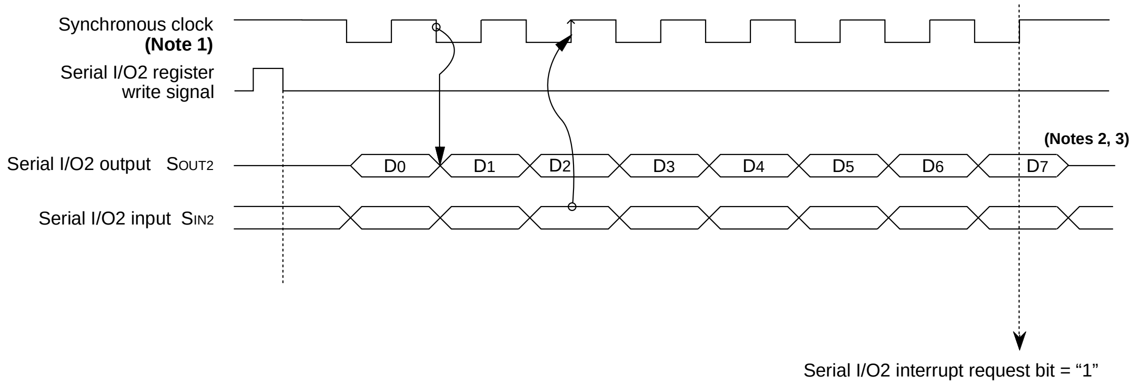
After writing, whenever a synchronous clock changes from “H” to “L”, data is output from the SOUT2 pin. Moreover, whenever a synchronous clock changes from “L” to “H”, data is taken in from the SIN2 pin, and 1 bit shift of the serial I/O2 register is carried out simultaneously.

When the internal clock is selected as a synchronous clock, it is as follows if a synchronous clock is counted 8 times.

- •Serial I/O2 counter = “0”
- •Synchronous clock stops in “H” state
- •Serial I/O2 interrupt request bit = “1”

The SOUT2 pin is in a high impedance state after transfer is completed.

When the external clock is selected as a synchronous clock, if a synchronous clock is counted 8 times, the serial I/O2 interrupt request bit is set to “1”, and the SOUT2 pin holds the output level of D7. However, if a synchronous clock continues being input, the shift of the serial I/O2 register is continued and transmission data continues being output from the SOUT2 pin.



Notes 1: When the internal clock is selected as the synchronous clock, the divide ratio can be selected by setting bits 0 to 2 of the serial I/O2 control register.
2: When the internal clock is selected as the synchronous clock, the SOUT2 pin goes to high impedance after transfer completion.
3: When the external clock is selected as the synchronous clock, the SOUT2 pin keeps D7 output level after transfer completion. However, if synchronous clocks input are carried on, the transmit data will be output continuously from the SOUT2 pin because shifts of serial I/O2 shift register is continued as long as synchronous clocks are input.

Fig. 33 Timing of serial I/O2 function

PULSE WIDTH MODULATION (PWM)

The 3826 group has a PWM function with an 8-bit resolution, using f(XIN) or f(XIN)/2 as a count source.

Data Setting

The PWM output pins are shared with ports $P5_0$ and $P5_1$. Set the PWM period by the PWM prescaler, and set the period during which the output pulse is an "H" by the PWM register.

If PWM count source is f(XIN) and the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

PWM period = 255 × (n+1)/f(XIN)
= 31.875 × (n+1) µs (when f(XIN) = 8 MHz)

Output pulse "H" period = PWM period × m/255
= 0.125 × (n+1) × m µs
(when f(XIN) = 8 MHz)

PWM Operation

When either bit 1 (PWM_0 function enable bit) or bit 2 (PWM_1 function enable bit) of the PWM control register or both bits are enabled, operation starts from initializing status, and pulses are output starting at "H". When one PWM output is enabled and that the other PWM output is enabled, PWM output which is enabled to output later starts pulse output from halfway of PWM period (see Figure 37).

When the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

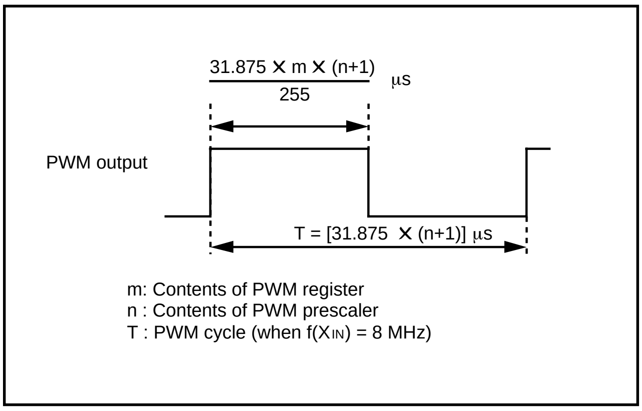


Fig. 34 Timing of PWM cycle

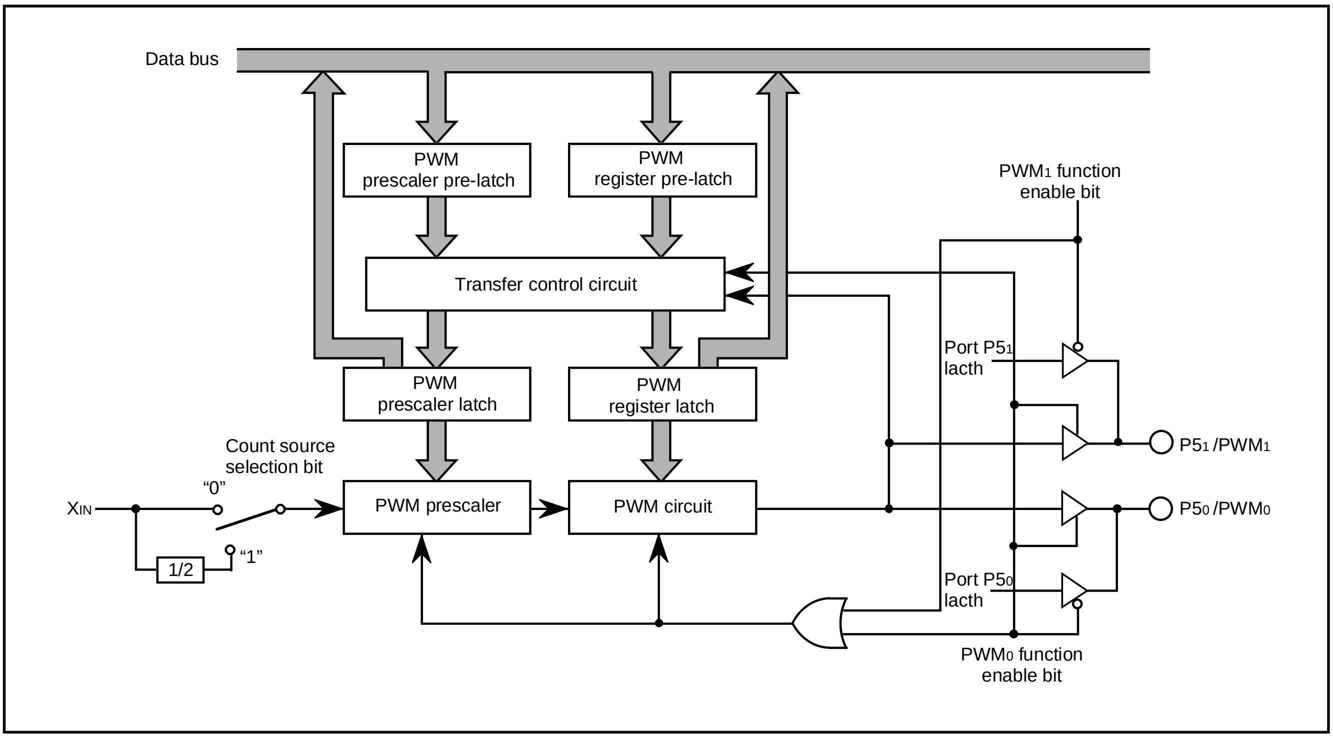


Fig. 35 Block diagram of PWM function

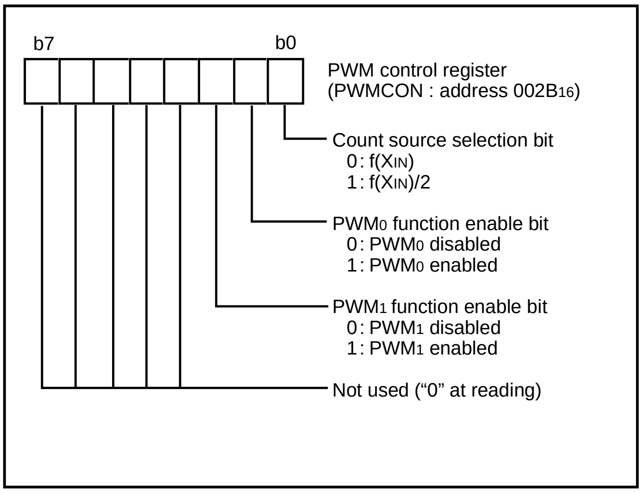


Fig. 36 Structure of PWM control register

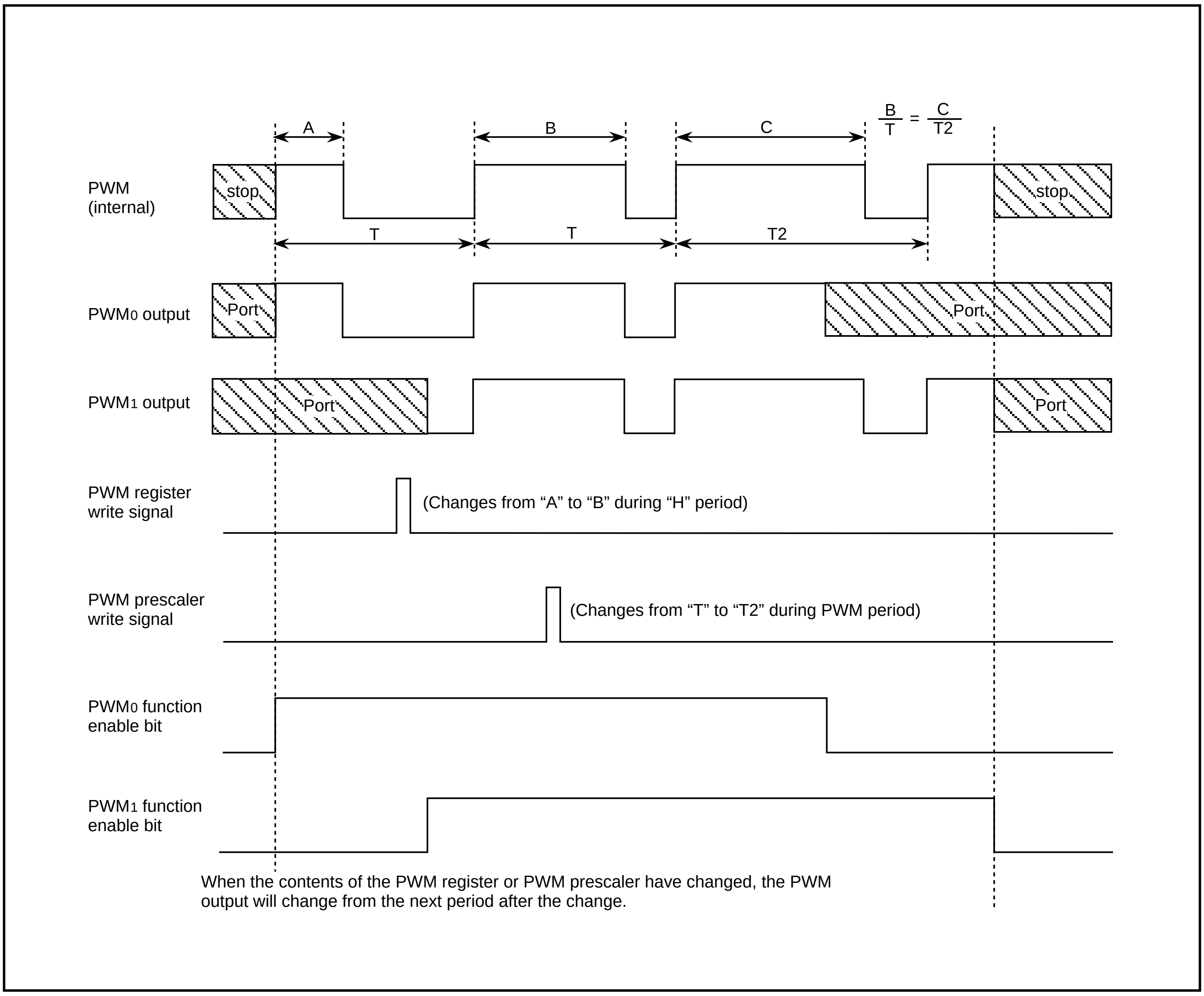


Fig. 37 PWM output timing when PWM register or PWM prescaler is changed

A/D CONVERTER
[AD Conversion Low-Order Register (ADL)] 0014_{16}
[AD Conversion High-Order Register (ADH)] 0035_{16}

The AD conversion registers are read-only registers that store the result of an A/D conversion. When reading this register during an A/D conversion, the previous conversion result is read.

The high-order 8 bits of a conversion result is stored in the AD conversion high-order register (address 0035_{16}), and the low-order 2 bits of the same result are stored in bit 7 and bit 6 of the AD conversion low-order register (address 0014_{16}).

Bit 0 of the AD conversion low-order register is the conversion mode selection bit. When this bit is set to “0”, that becomes the 10-bit A/D mode. When this bit is set to “1”, that becomes the 8-bit A/D mode.

[AD Control Register (ADCON)] 0034_{16}

The AD control register controls the A/D conversion process. Bits 0 to 2 of this register select specific analog input pins. Bit 3 indicates the completion of an A/D conversion. The value of this bit remains at “0” during an A/D conversion, then it is set to “1” when the A/D conversion is completed. Writing “0” to this bit starts the A/D conversion.

Bit 4 is the VREF input switch bit which controls connection of the resistor ladder and the reference voltage input pin (VREF). The resistor ladder is always connected to VREF when bit 4 is set to “1”. When bit 4 is set to “0”, the resistor ladder is cut off from VREF except for A/D conversion performed. When bit 5, which is the AD external trigger valid bit, is set to “1”, A/D conversion starts also by a falling edge of an ADT input. When using an A/D external trigger, set the $P5_7$/ADT pin to input mode (set “0” to bit 7 of port P5 direction register).

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF by 256 (when 8-bit A/D mode) or 1024 (when 10-bit A/D mode), and outputs the divided voltages.

Channel Selector

The channel selector selects one of the input ports $P6_7/AN_7$–$P6_0/AN_0$.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage and store the result in the AD conversion register. When an A/D conversion is completed, the control circuit sets the AD conversion completion bit and the A/D conversion interrupt request bit to “1”.

Note that because the comparator consists of a capacitor coupling, set f(X_{IN}) to 500 kHz or more during an A/D conversion. Use the clock divided from the main clock f(X_{IN}) as the system clock ϕ.

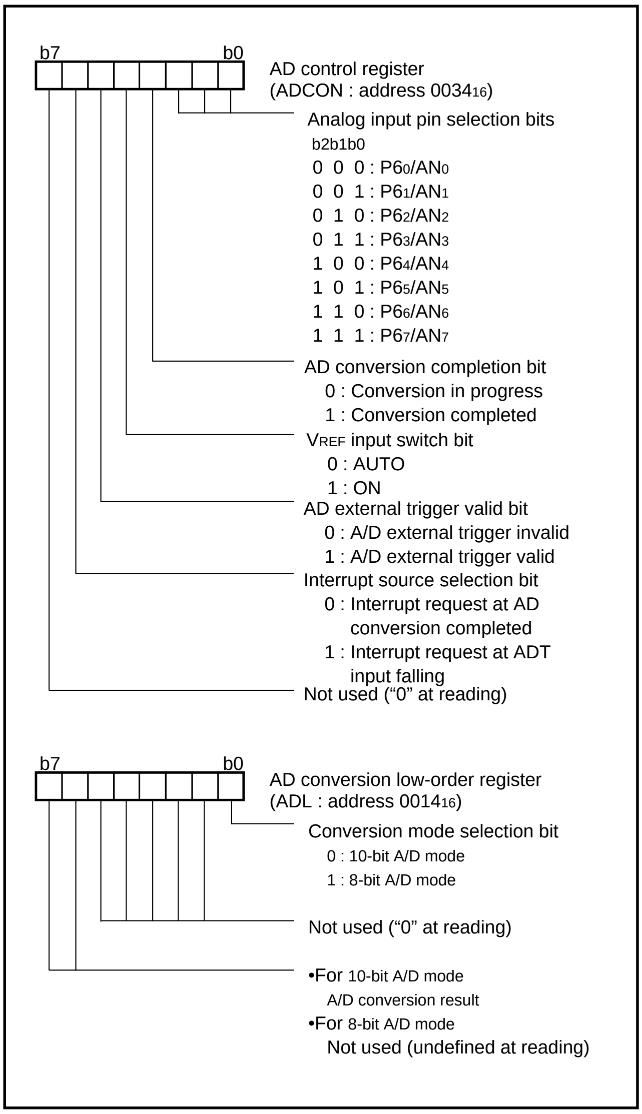


Fig. 38 Structure of A/D converter-related registers

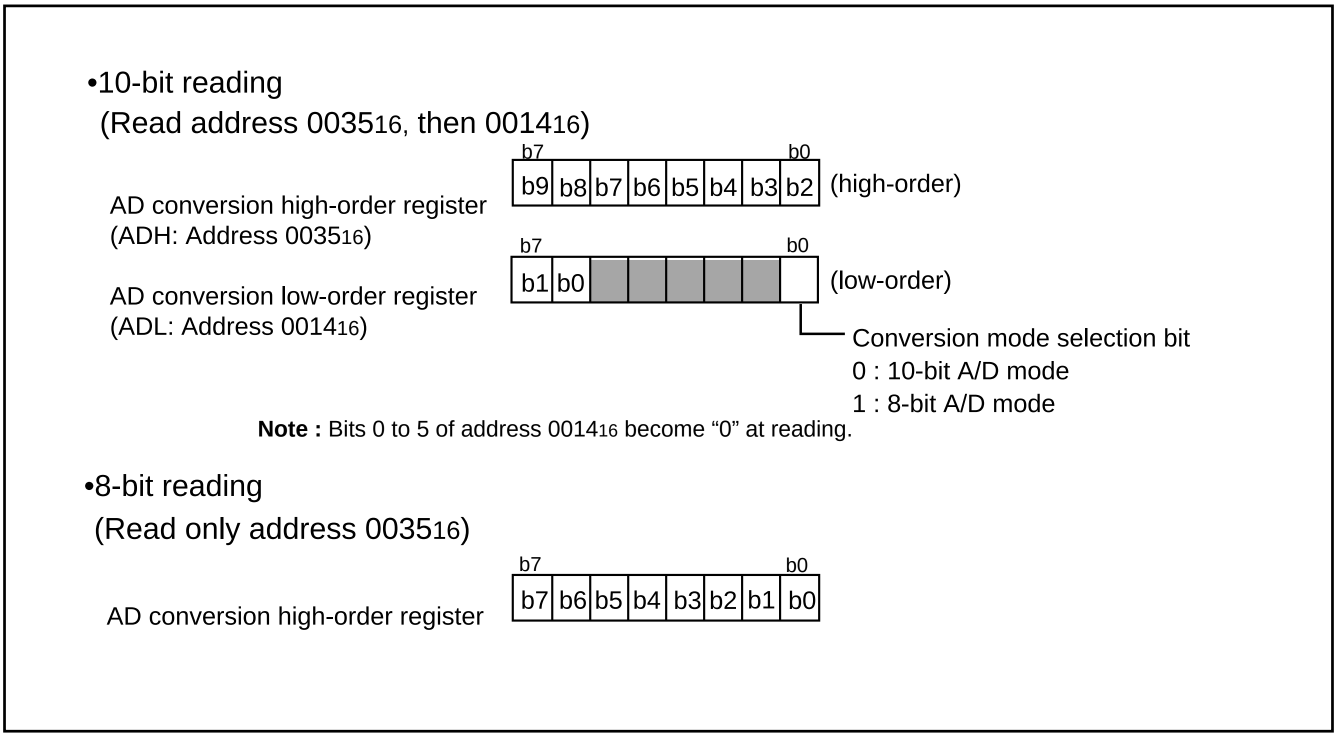


Fig. 39 Read of AD conversion register

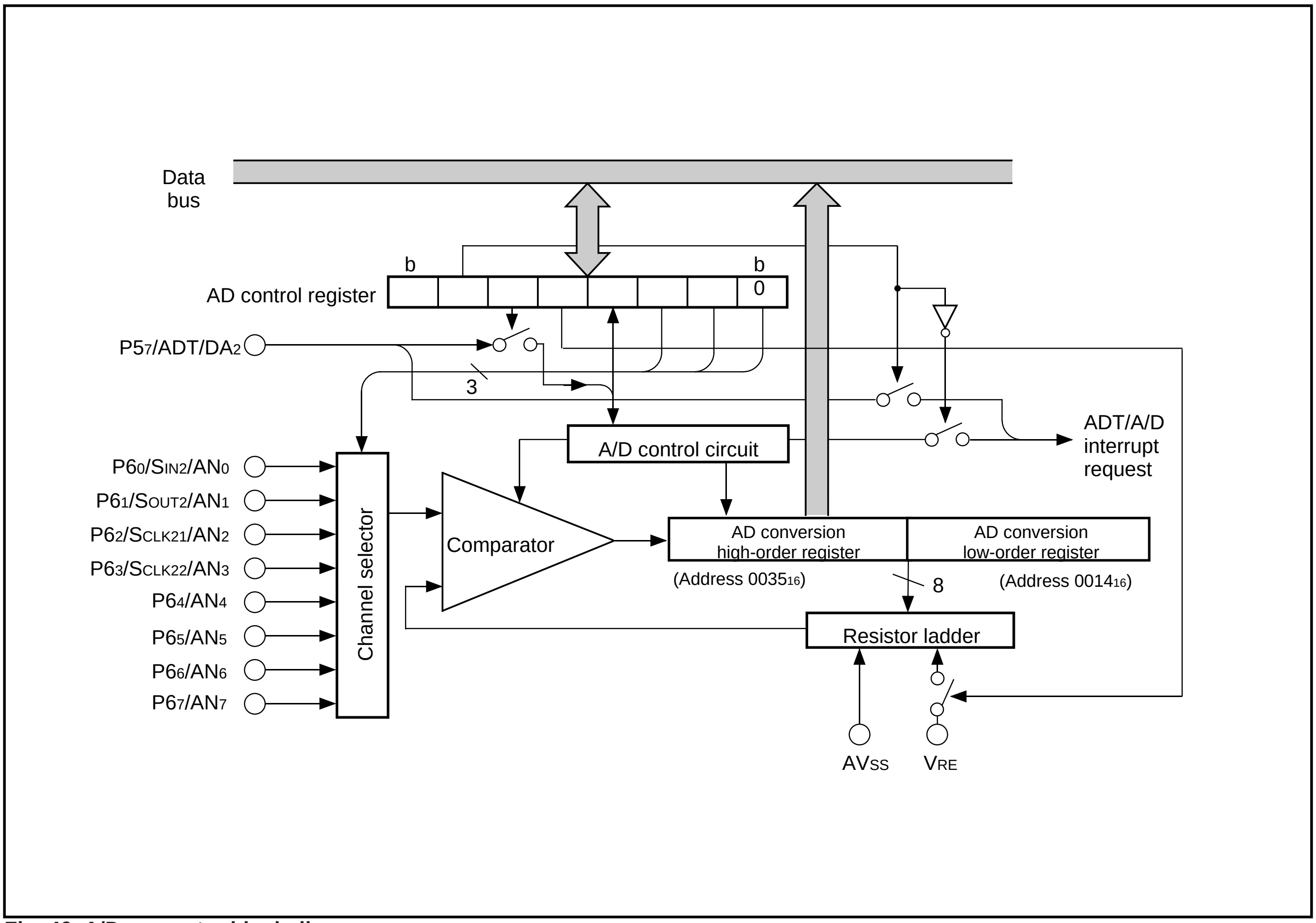


Fig. 40 A/D converter block diagram

D/A Converter

The 3826 group has a D/A converter with 8-bit resolution and 2 channels (DA_1, DA_2).
The D/A converter is started by setting the DTMF/DA_1 selection bit and the CTCSS/DA_2 selection bit to “0” and setting the value in the DA conversion register. When the DTMF/DA_1 output enable bit and the CTCSS/DA_2 output enable bit is set to “1”, the result of D/A conversion is output from the corresponding DA_1 pin or DA_2 pin.
When using the D/A converter, set the $P5_6$/DA_1 pin and the $P5_7$/DA_2 pin to input mode (set “0” to bits 6, 7 of port P5 direction register) and the pull-up resistor should be in the OFF state previously.
The output analog voltage V is determined by the value n (base 10) in the DA conversion register as follows:

$V = V_{REF} \times n/256$ (n=0 to 255)
Where V_{REF} is the reference voltage.

At reset, the DA conversion registers are set to “00_{16}”, the DTMF/DA_1 output enable bit and the CTCSS/DA_2 output enable bit are set to “0”, and the $P5_6$/DA_1 pin and the $P5_7$/DA_2 pin goes to high impedance state. The D/A converter is not buffered, so connect an external buffer when driving a low-impedance load.

■ Note on applied voltage to V_{REF} pin
When the $P5_6$/DA_1 pin and the $P5_7$/DA_2 pin are used as an I/O port, be sure to apply Vcc to V_{REF} pin.
When these pins are used as D/A conversion output pins, the Vcc level is recommended for the applied voltage to V_{REF} pin.
When the voltage below Vcc level is applied, the D/A conversion accuracy may be worse.

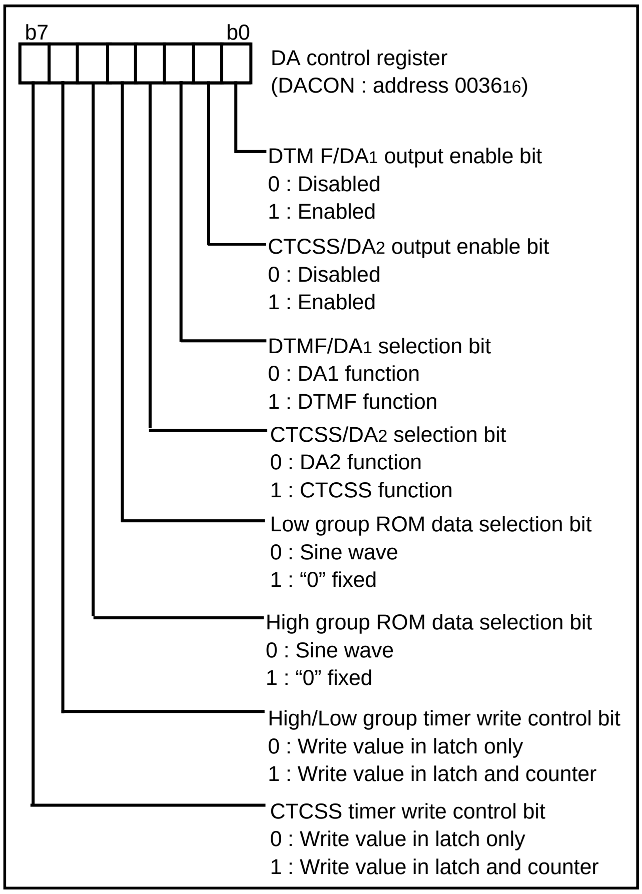
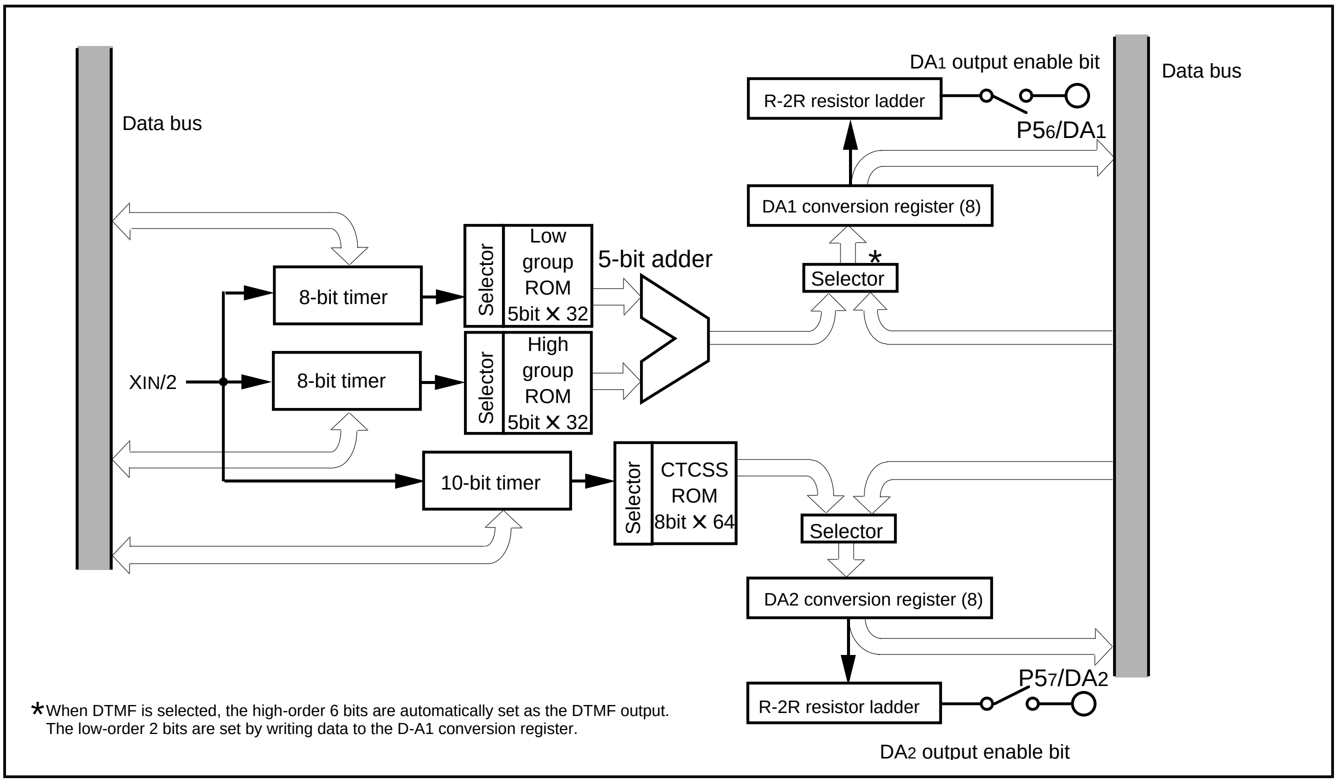


Fig. 41 Structure of DA control register



*When DTMF is selected, the high-order 6 bits are automatically set as the DTMF output. The low-order 2 bits are set by writing data to the D-A1 conversion register.

Fig. 42 Block diagram of D/A converter

DTMF Function (Dual Tone Multi Frequency)

DTMF function is used to output the result which generated automatically the waveform of sine wave of two kinds of different frequency, and added two kinds of this sine wave as an analog value.

DTMF output waveform can be output from DA_1 pin. DTMF waveform is output by setting "1" (enabled) to the DTMF/DA_1 output enable bit (bit 0 of address 0036_{16}), and setting "1" to the DTMF/DA_1 selection bit (bit 2 of address 0036_{16}). At this time, set "0" (input state) to the direction register of ports $P5_6$/DA_1 pin and pull-up resistor to be OFF state.

In order to set two kinds of frequency which generates DTMF waveform, write a value in the DTMF high group timer and the DTMF low group timer, respectively. The value written in each above-mentioned timer is n, the sine wave of the following frequency can be generated.

$$f = \frac{f(X_{IN})/2}{(n+1) \times 32} \text{ (Hz)}$$

Set "06_{16}" or more to the DTMF high group timer and the DTMF low group timer. After reset release, "06_{16}" is automatically set to them.

The digital value for one period of high group and low group output is shown in Figure 43.

DTMF output is automatically input to high-order 6 bits of the D/A1 conversion register as 6-bit D/A data. The low-order 2 bits of the D/A1 conversion register are fixed to the value written in the D/A1 conversion register.

Moreover, only the sine wave of high group can be output by setting "1" to the bit 4 of the D/A control register. By setting "1" to the bit 5 of the D/A control register similarly, only the sine wave of low group can be output. Writing to the DTMF high group timer and the DTMF low group timer can also be changed to "writing to latch and timer simultaneously" by setting "1" to the bit 6 of the D/A con trol register. "Writing to only latch" is set after reset release. If the D/A1 conversion register is read when the DTMF function is selected,the digital value of DTMF output can be read.

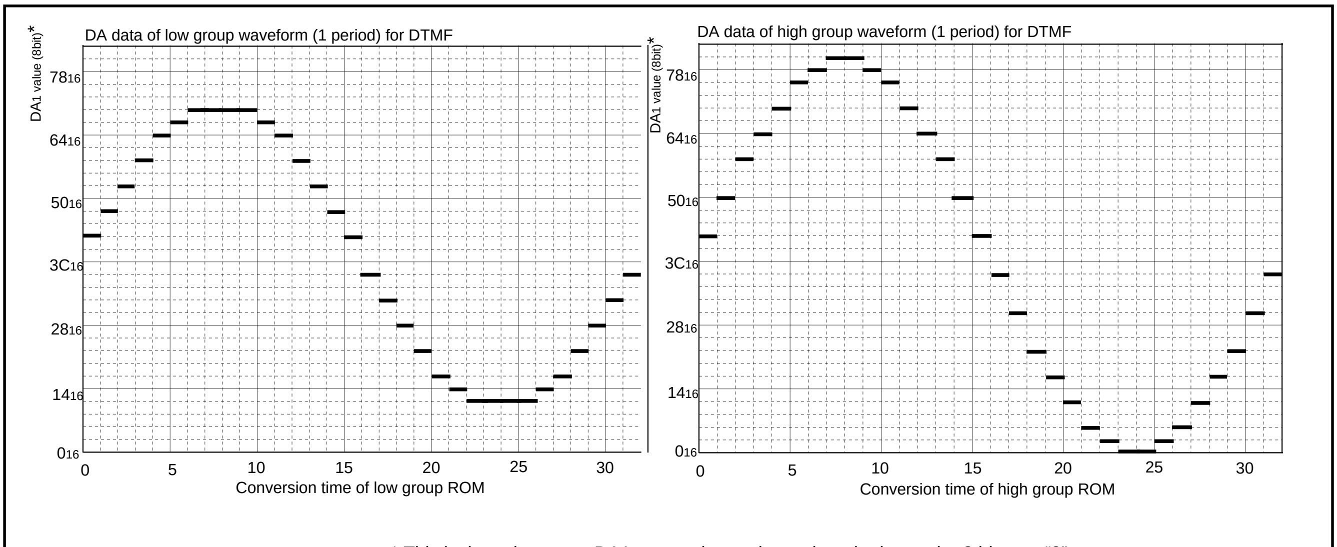


Fig. 43 Waveform data of high group and low group

Low Groupt Frequency, High Group Frequency

Low group frequency and high group frequency are as follows.

(1) Low group frequency
- 697 Hz
- 770 Hz
- 852 Hz
- 941 Hz

(2) High group frequency
- 1209 Hz
- 1336 Hz
- 1477 Hz
- 1633 Hz

Table 9 shows the example of frequency accuracy (at f(XIN)=4 MHz).

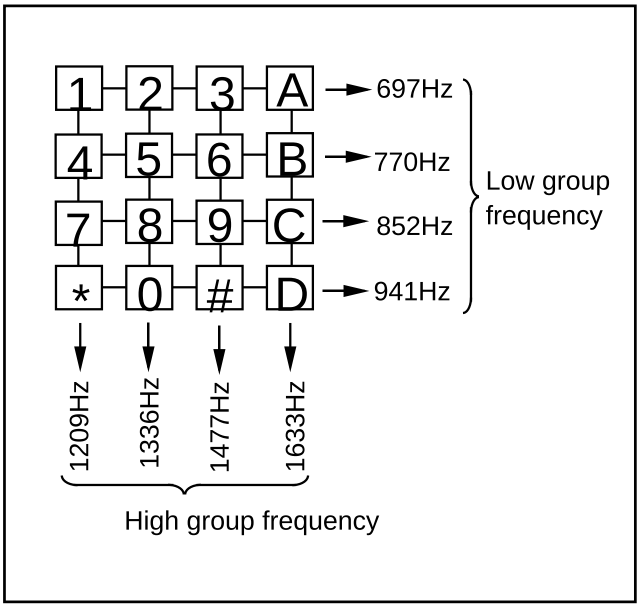


Fig. 44 Key matrix of telephone and rating frequency

Table 9 Example of frequency accuracy (at f(XIN) = 4 MHz)

Rating frequency (Hz)	n (Timer value)	Output frequency (Hz)	Error frequency (Hz)	Deviation (%)
697	89	694.4	–2.6	–0.367
770	80	771.6	1.6	0.208
852	72	856.2	4.2	0.488
941	65	946.9	5.9	0.630
1209	51	1201.9	–7.1	–0.580
1336	46	1329.7	–6.3	–0.460
1477	41	1488.1	11.1	0.750
1633	37	1644.7	11.7	0.720

CTCSS Function (Continuous Tone-Controlled Squelch System)

The CTCSS function is used to generate the sine wave of single frequency automatically. The CTCSS output waveform can be output from DA_2 pin. CTCSS waveform is outputted by setting “1” to the CTCSS/DA_2 output enable bit (bit 1 of address 0036_{16}), and setting “1” to the CTCSS/DA_2 selection bit (bit 3 of address 0036_{16}). In order to set the frequency of CTCSS output, value is written in the CTCSS timer. The CTCSS timer consists of a 10-bit timer. When writing a value to the CTCSS timer, write the low-order byte first.

When reading a value from the CTCSS timer, read the high-order byte first. By the value written in the CTCSS timer is n, the sine wave of the following frequency is generated.

$$f = \frac{f(X_{IN})/2}{(n+1) \times 64} \ (\text{Hz})$$

Set “006_{16}” or more to the CTCSS timer. “00_{16}” is automatically set to the high-order of the CTCSS timer and “06_{16}” is automatically set to the low-order of the CTCSS timer after reset release.

The amplitude of CTCSS output is obtained by the following formula.

$$C = \frac{Vcc}{2}$$

If the D/A2 conversion register is read when the CTCSS function is selected, the digital value of CTCSS output can be read.

Table 10 shows the example of frequency accuracy (at $f(X_{IN})$ = 4 MHz).

Table 10 Example of frequency accuracy (at $f(X_{IN})$ = 4 MHz)

Rating frequency (Hz)	n (Timer value)	Output frequency (Hz)]	Error frequency (Hz)	Deviation (%)
67.0	465	67.06	0.06	0.089
77.0	405	76.97	–0.03	–0.038
88.5	352	88.53	0.027	0.030
100.0	312	99.84	–0.16	–0.160
107.2	291	107.02	–0.18	–0.167
114.8	271	114.89	0.09	0.078
123.0	253	123.03	0.03	0.026
131.8	236	131.86	0.06	0.043
141.3	220	141.40	0.10	0.073
151.4	205	151.70	0.30	0.198
162.2	192	161.92	–0.28	–0.174
173.8	179	173.61	–0.19	–0.109
186.2	167	186.01	–0.19	–0.101
203.5	153	202.92	–0.58	–0.284
218.1	142	218.53	0.43	0.198
233.6	133	233.20	–0.39	–0.167
250.3	124	250.00	–0.30	–0.120

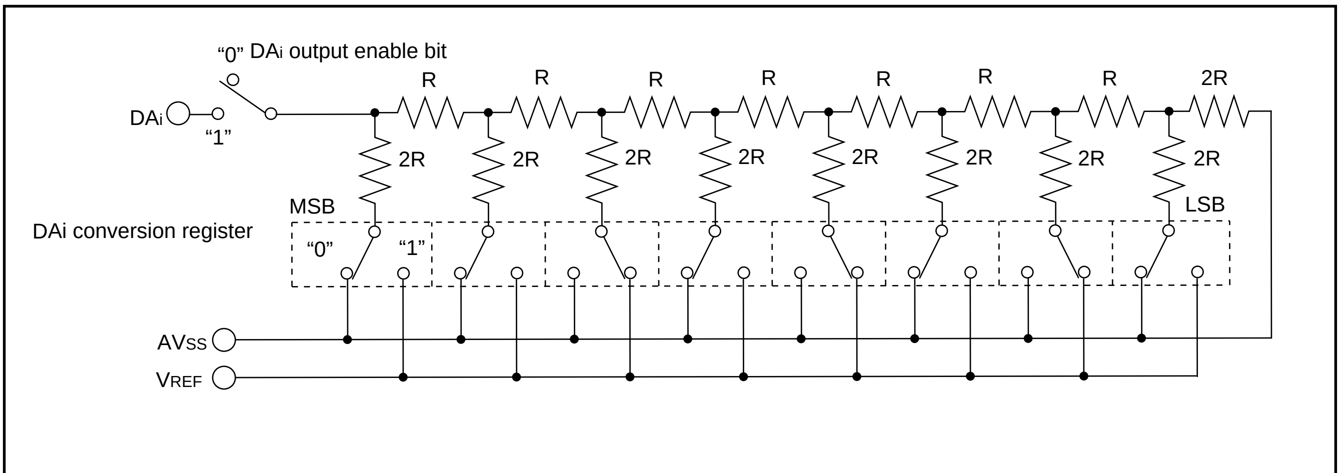


Fig. 45 Equivalent connection circuit of D/A converter

LCD DRIVE CONTROL CIRCUIT

The 3826 group has the Liquid Crystal Display (LCD) drive control circuit consisting of the following.

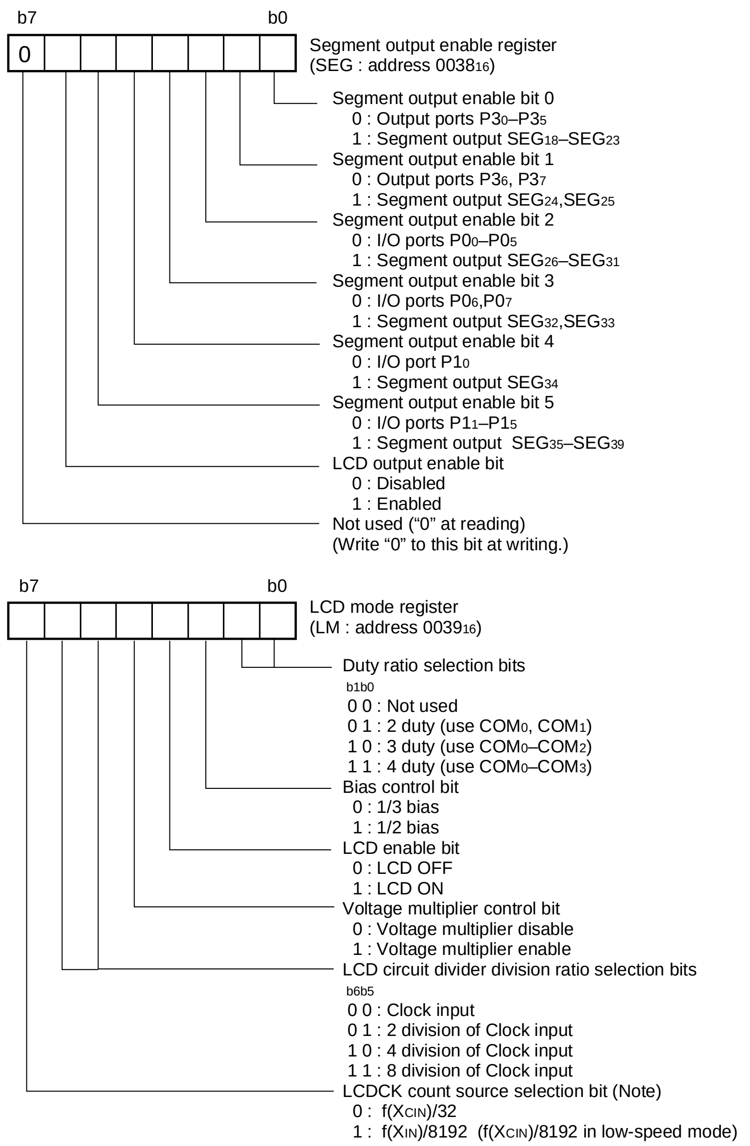
- LCD display RAM
- Segment output enable register
- LCD mode register
- Voltage multiplier
- Selector
- Timing controller
- Common driver
- Segment driver
- Bias control circuit

A maximum of 40 segment output pins and 4 common output pins can be used.

Up to 160 pixels can be controlled for LCD display. When the LCD enable bit is set to “1” (LCD ON) after data is set in the LCD mode register, the segment output enable register and the LCD display RAM, the LCD drive control circuit starts reading the display data automatically, performs the bias control and the duty ratio control, and displays the data on the LCD panel.

Table 11 Maximum number of display pixels at each duty ratio

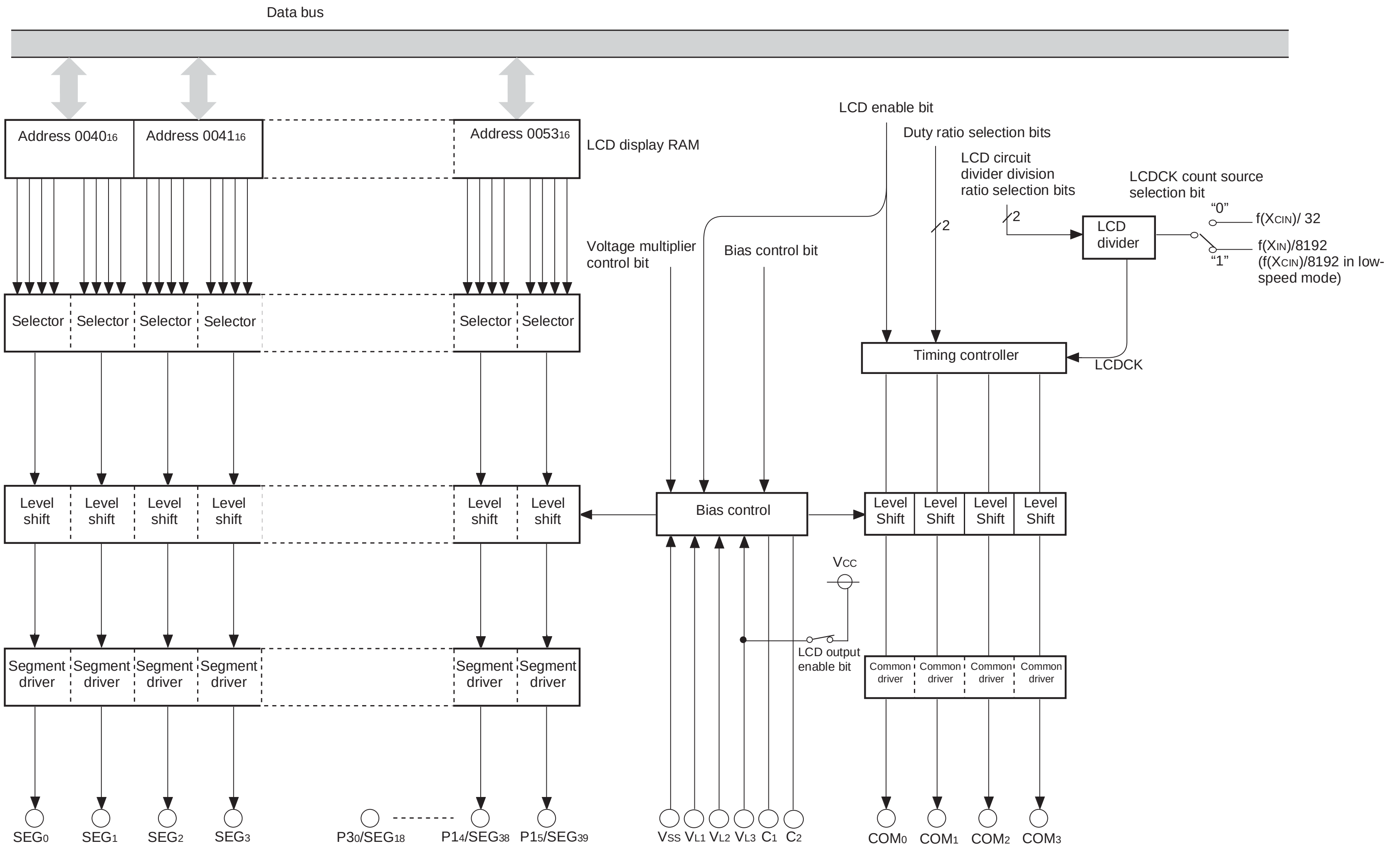
Duty ratio	Maximum number of display pixel
2	80 dots or 8 segment LCD 10 digits
3	120 dots or 8 segment LCD 15 digits
4	160 dots or 8 segment LCD 20 digits



Note : LCDCK is a clock for a LCD timing controller.

Fig. 46 Structure of segment output enable register and LCD mode register

Fig. 47 Block diagram of LCD controller/driver



Voltage Multiplier (3 Times)

The voltage multiplier performs threefold boosting. This circuit inputs a reference voltage for boosting from LCD power input pin V_{L1}.

Set each bit of the segment output enable register and the LCD mode register in the following order for operating the voltage multiplier.

1. Set the segment output enable bits (bits 0 to 5) of the segment output enable register to “0” or “1”.
2. Set the duty ratio selection bits (bits 0 and 1), the bias control bit (bit 2), the LCD circuit divider division ratio selection bits (bits 5 and 6), and the LCDCK count source selection bit (bit 7) of the LCD mode register to “0” or “1”.
3. Set the LCD output enable bit (bit 6) of the segment output enable register to “1” (enabled). Apply the limit voltage or less to the V_{L1} pin.
4. Set the voltage multiplier control bit (bit 4) of the LCD mode register to “1” (voltage multiplier enabled). However, be sure to select 1/3 bias for bias control.

When voltage is input to the V_{L1} pin during operating the voltage multiplier, voltage that is twice as large as V_{L1} occurs at the V_{L2} pin, and voltage that is three times as large as V_{L1} occurs at the V_{L3} pin.

■Notes on Voltage Multiplier

When using the voltage multiplier, apply the limit voltage or less to the V_{L1} pin, then set the voltage multiplier control bit to “1” (enabled).

When not using the voltage multiplier, set the LCD output enable bit to “1”, then apply proper voltage to the LCD power input pins (V_{L1}–V_{L3}). When the LCD output enable bit is set to “0” (disabled) (during reset is included), the V_{L3} pin is connected to V_{CC} inside of this microcomputer. When the voltage exceeding V_{CC} is applied to V_{L3}, apply V_{L3} voltage after setting the LCD output enable bit to “1” (enabled).

Bias Control and Applied Voltage to LCD Power Input Pins

To the LCD power input pins (V_{L1}–V_{L3}), apply the voltage shown in Table 12 according to the bias value.

Select a bias value by the bias control bit (bit 2 of the LCD mode register).

Table 12 Bias control and applied voltage to V_{L1}–V_{L3}

Bias value	Voltage value
1/3 bias	$V_{L3}=V_{LCD}$ $V_{L2}=2/3\ V_{LCD}$ $V_{L1}=1/3\ V_{LCD}$
1/2 bias	$V_{L3}=V_{LCD}$ $V_{L2}=V_{L1}=1/2\ V_{LCD}$

Note : V_{LCD} is the maximum value of supplied voltage for the LCD panel.

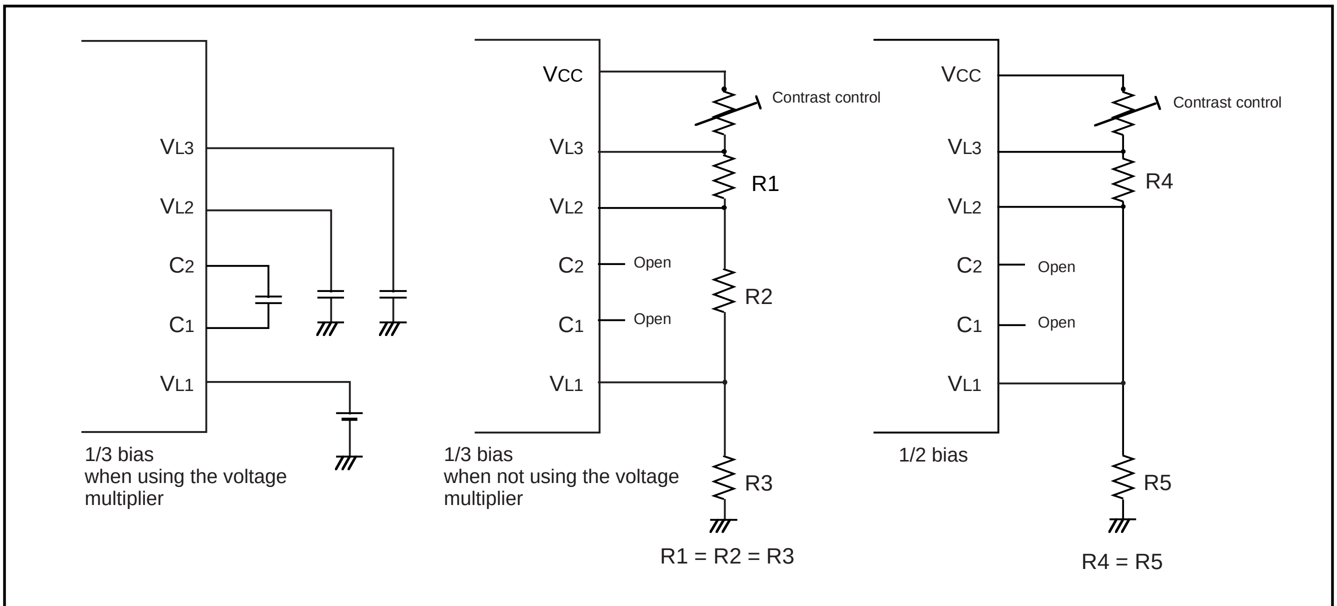


Fig. 48 Example of circuit at each bias

Common Pin and Duty Ratio Control

The common pins (COM$_0$–COM$_3$) to be used are determined by duty ratio.
Select duty ratio by the duty ratio selection bits (bits 0 and 1 of the LCD mode register).
After reset, the V$_{CC}$ (V$_{L3}$) voltage is output from the common pins.

Table 13 Duty ratio control and common pins used

Duty ratio	Duty ratio selection bits		Common pins used
	Bit 1	Bit 0	
2	0	1	COM$_0$, COM$_1$ (Note 1)
3	1	0	COM$_0$–COM$_2$ (Note 2)
4	1	1	COM$_0$–COM$_3$

Notes 1: COM$_2$ and COM$_3$ are open.
2: COM$_3$ is open.

Segment Signal Output Pins

Segment signal output pins are classified into the segment-only pins (SEG$_0$–SEG$_{17}$), the segment or output port pins (SEG$_{18}$–SEG$_{25}$), and the segment or I/O port pins (SEG$_{26}$–SEG$_{39}$).
Segment signals are output according to the bit data of the LCD RAM corresponding to the duty ratio. After reset, a V$_{CC}$ (=V$_{L3}$) voltage is output to the segment-only pins and the segment/output port pins are the high impedance condition and pulled up to V$_{CC}$ (=V$_{L3}$) voltage.
Also, the segment/I/O port pins (SEG$_{26}$–SEG$_{39}$) are set to input mode as I/O ports, and V$_{CC}$ (=V$_{L3}$) is applied to them by pull-up resistor.

LCD Display RAM

Addresses 0040$_{16}$ to 0053$_{16}$ are the designated RAM for the LCD display. When "1" are written to these addresses, the corresponding segments of the LCD display panel are turned on.

LCD Drive Timing

The frequency of internal signal LCDCK decided LCD drive timing and the frame frequency can be determined with the following equation:

$$f(\mathrm{LCDCK}) = \frac{\text{(frequency of count source for LCDCK)}}{\text{(divider division ratio for LCD)}}$$

$$\text{Frame frequency} = \frac{f(\mathrm{LCDCK})}{\text{duty ratio}}$$

Bit / Address	7	6	5	4	3	2	1	0
	COM$_3$	COM$_2$	COM$_1$	COM$_0$	COM$_3$	COM$_2$	COM$_1$	COM$_0$
0040$_{16}$	SEG$_1$				SEG$_0$			
0041$_{16}$	SEG$_3$				SEG$_2$			
0042$_{16}$	SEG$_5$				SEG$_4$			
0043$_{16}$	SEG$_7$				SEG$_6$			
0044$_{16}$	SEG$_9$				SEG$_8$			
0045$_{16}$	SEG$_{11}$				SEG$_{10}$			
0046$_{16}$	SEG$_{13}$				SEG$_{12}$			
0047$_{16}$	SEG$_{15}$				SEG$_{14}$			
0048$_{16}$	SEG$_{17}$				SEG$_{16}$			
0049$_{16}$	SEG$_{19}$				SEG$_{18}$			
004A$_{16}$	SEG$_{21}$				SEG$_{20}$			
004B$_{16}$	SEG$_{23}$				SEG$_{22}$			
004C$_{16}$	SEG$_{25}$				SEG$_{24}$			
004D$_{16}$	SEG$_{27}$				SEG$_{26}$			
004E$_{16}$	SEG$_{29}$				SEG$_{28}$			
004F$_{16}$	SEG$_{31}$				SEG$_{30}$			
0050$_{16}$	SEG$_{33}$				SEG$_{32}$			
0051$_{16}$	SEG$_{35}$				SEG$_{34}$			
0052$_{16}$	SEG$_{37}$				SEG$_{36}$			
0053$_{16}$	SEG$_{39}$				SEG$_{38}$			

Fig. 49 LCD display RAM map

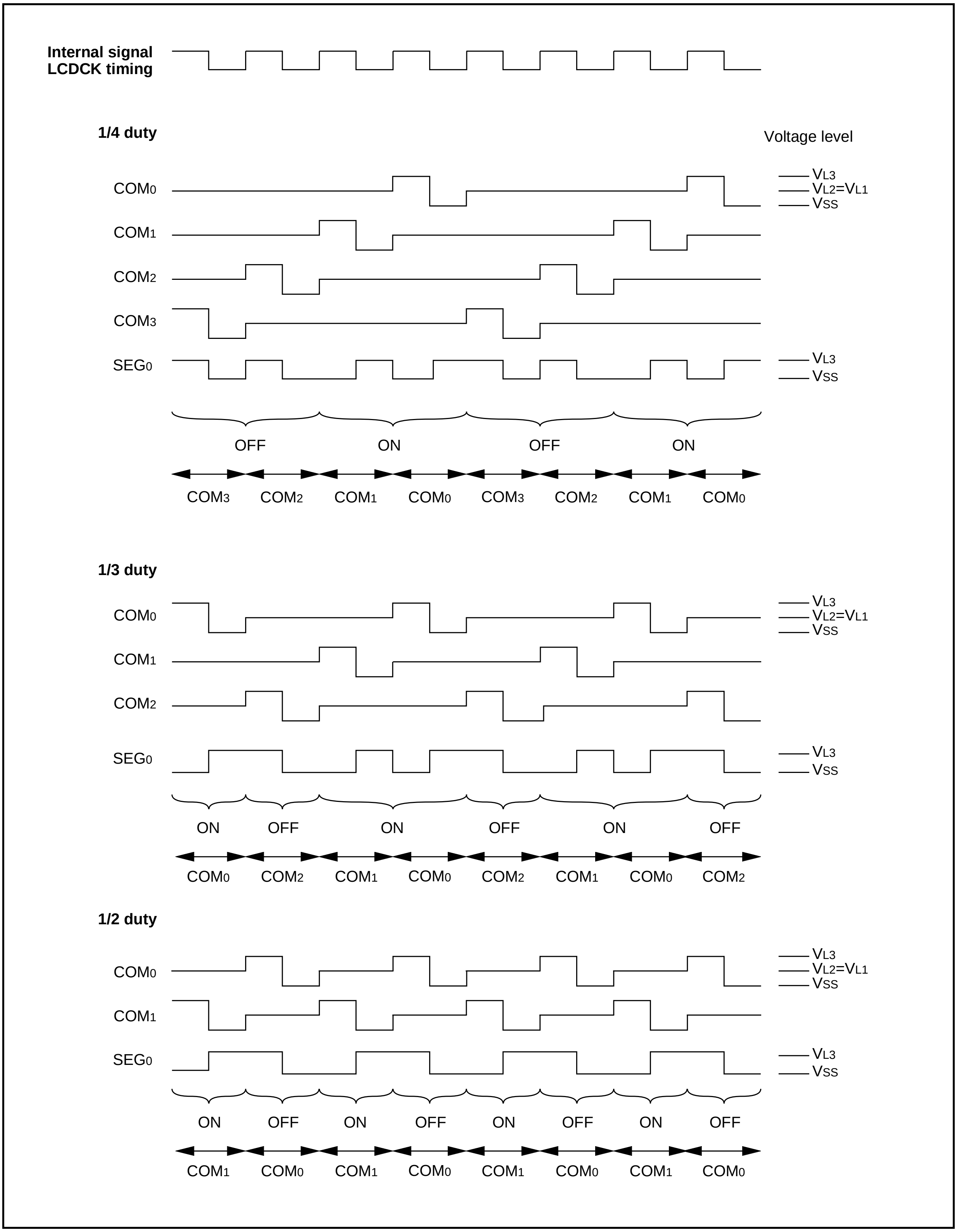


Fig. 50 LCD drive waveform (1/2 bias)

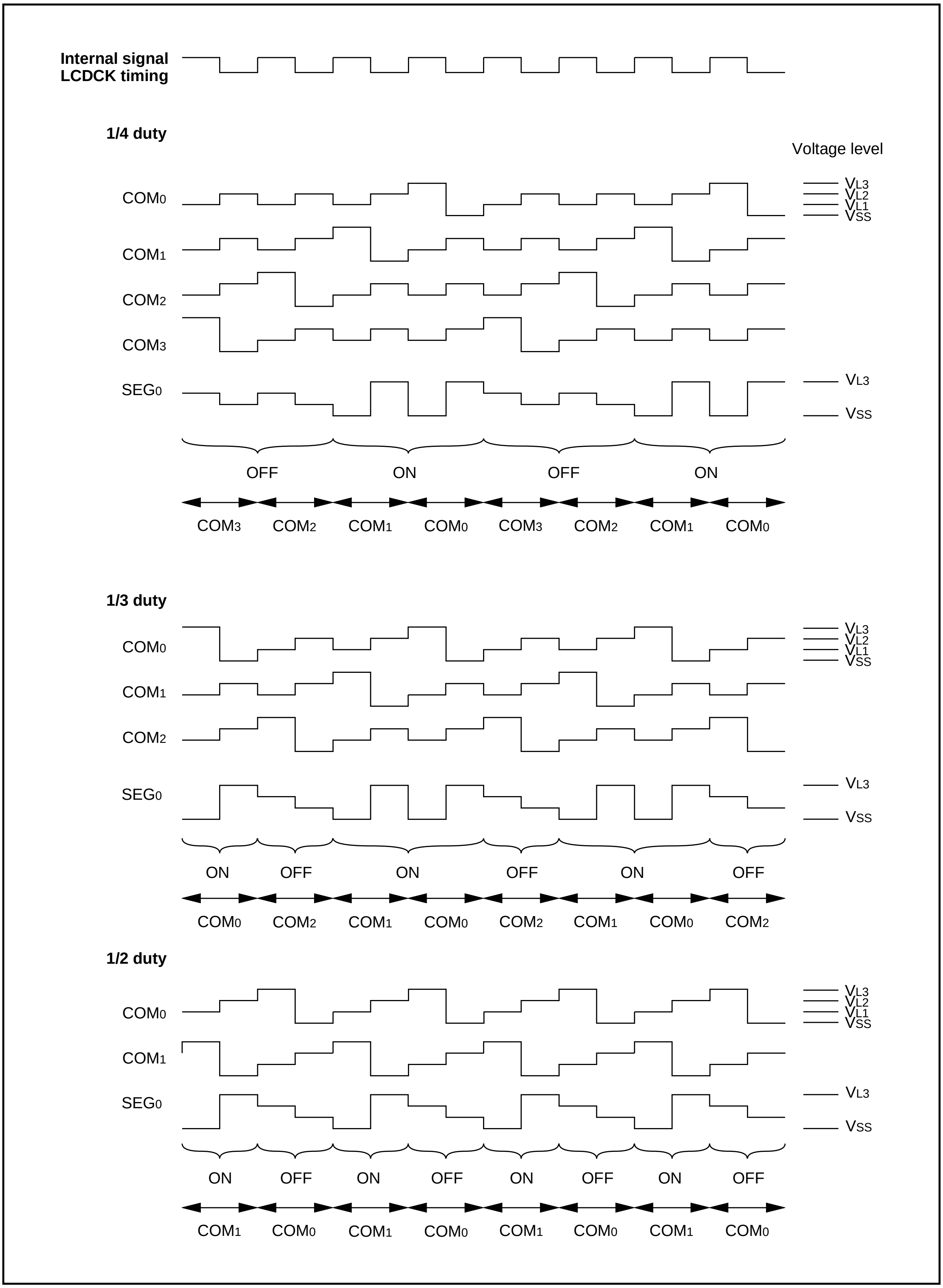


Fig. 51 LCD drive waveform (1/3 bias)

Watchdog Timer

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software runaway).

The watchdog timer consists of an 8-bit watchdog timer L and a 6-bit watchdog timer H. At reset or writing to the watchdog timer control register (address 0037_{16}), the watchdog timer is set to "$3FFF_{16}$". When any data is not written to the watchdog timer control register (address 0037_{16}) after reset, the watchdog timer is stopped. The watchdog timer starts to count down from "$3FFF_{16}$" by writing to the watchdog timer control register and an internal reset occurs at an underflow. Accordingly, when using the watchdog timer function, write the watchdog timer control register before an underflow. The watchdog timer does not function when writing to the watchdog timer control register has not been done after reset. When not using the watchdog timer, do not write to it. When the watchdog timer control register is read, the following values are read:

- value of high-order 6-bit counter
- value of STP instruction disable bit
- value of count source selection bit.

When the STP instruction disable bit is "0", the STP instruction is enabled. The STP instruction is disabled when this bit is set to "1". If the STP instruction which is disabled is executed, it is processed as an undefined instruction, so that a reset occurs internally.

This bit can be set to "1" but cannot be set to "0" by program. This bit is "0" after reset.

When the watchdog timer H count source selection bit is "0", the detection time is set to 8.19 s at f(XCIN) = 32 kHz and 32.768 ms at f(XIN) = 8 MHz.

When the watchdog timer H count source selection bit is "0", the detection time is set to 32 ms at f(XCIN) = 32 kHz and 128 µs at f(XIN) = 8 MHz. There is no difference in the detection time between the middle-speed mode and the high-speed mode.

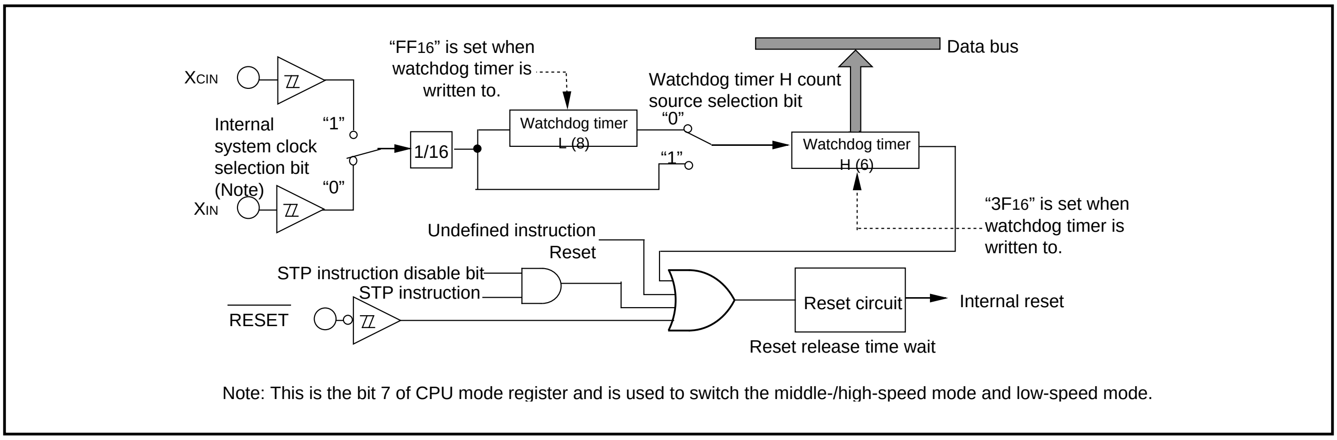


Fig. 52 Block diagram of watchdog timer

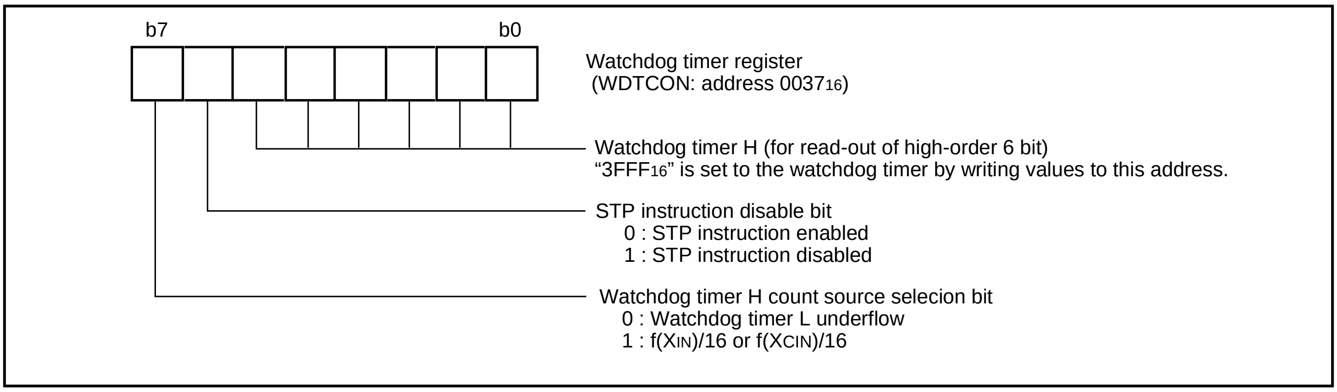


Fig. 53 Structure of watchdog timer control register

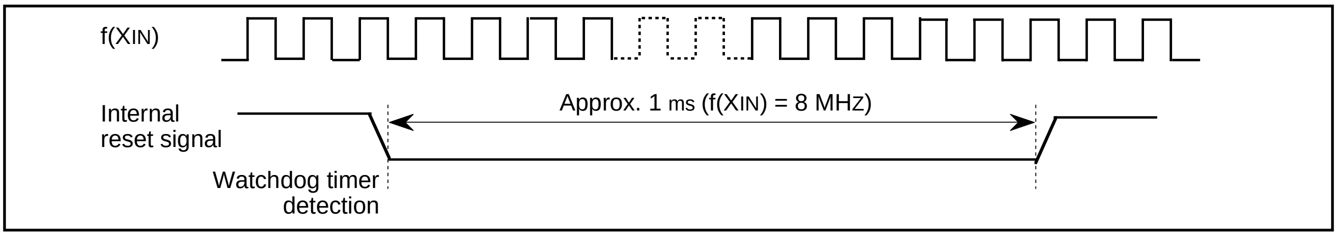


Fig. 54 Timing of reset output

TOUT/ϕ OUTPUT FUNCTION

The system clock ϕ or timer 2 divided by 2 (TOUT output) can be output from port P4₃ by setting the TOUT/ϕ output enable bit of the timer 123 mode register and the TOUT/ϕ output control register. Set the P4₃/ϕ/TOUT pin to output mode (set “1” to bit 3 of port P4 direction register) when outputting TOUT/ϕ.

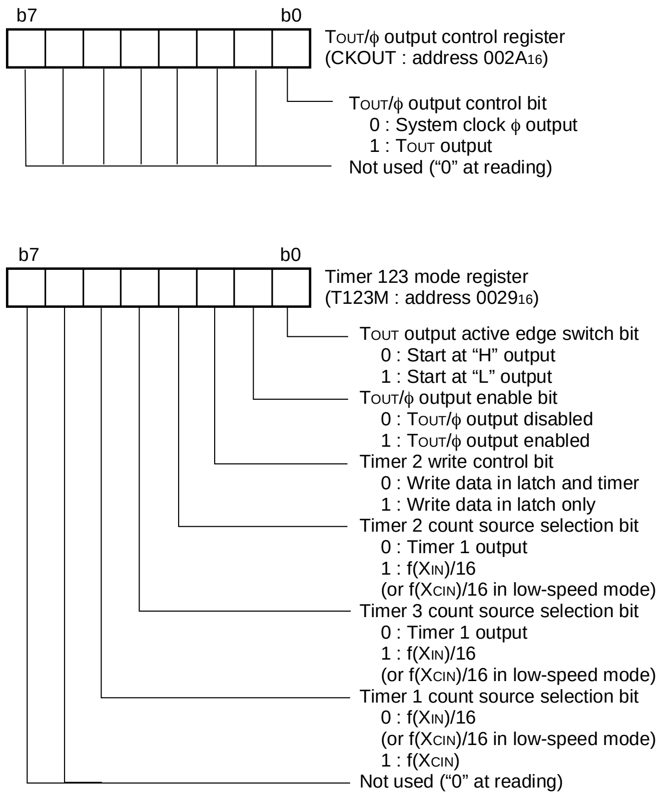


Fig. 55 Structure of TOUT/ϕ output-related registers

RESET CIRCUIT

When the power source voltage is within limits, and main clock XIN-XOUT is stable, or a stabilized clock is input to the XIN pin, if the RESET pin is held at an “L” level for 2 µs or more, the micro-computer is in an internal reset state. Then the RESET pin is returned to an “H” level, reset is released after approximate 8200 cycles of f(XIN), the program in address FFFD16 (high-order byte) and address FFFC16 (low-order byte). Make sure that the reset input voltage is less than 0.2 VCC(min.) for the power source voltage of VCC(min.).

*VCC(min.) = Minimum value of power supply voltage limits applied to VCC pin

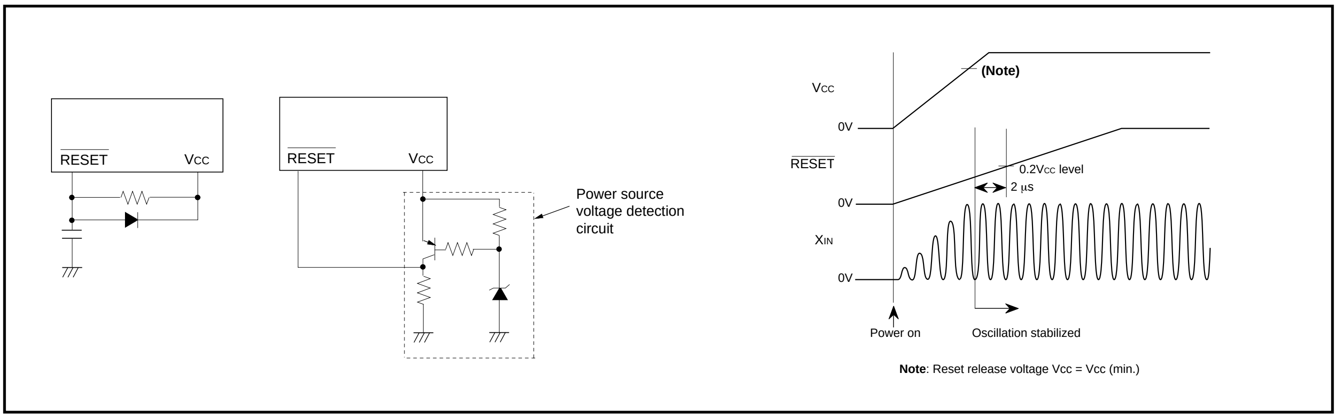


Fig. 56 Example of reset circuit

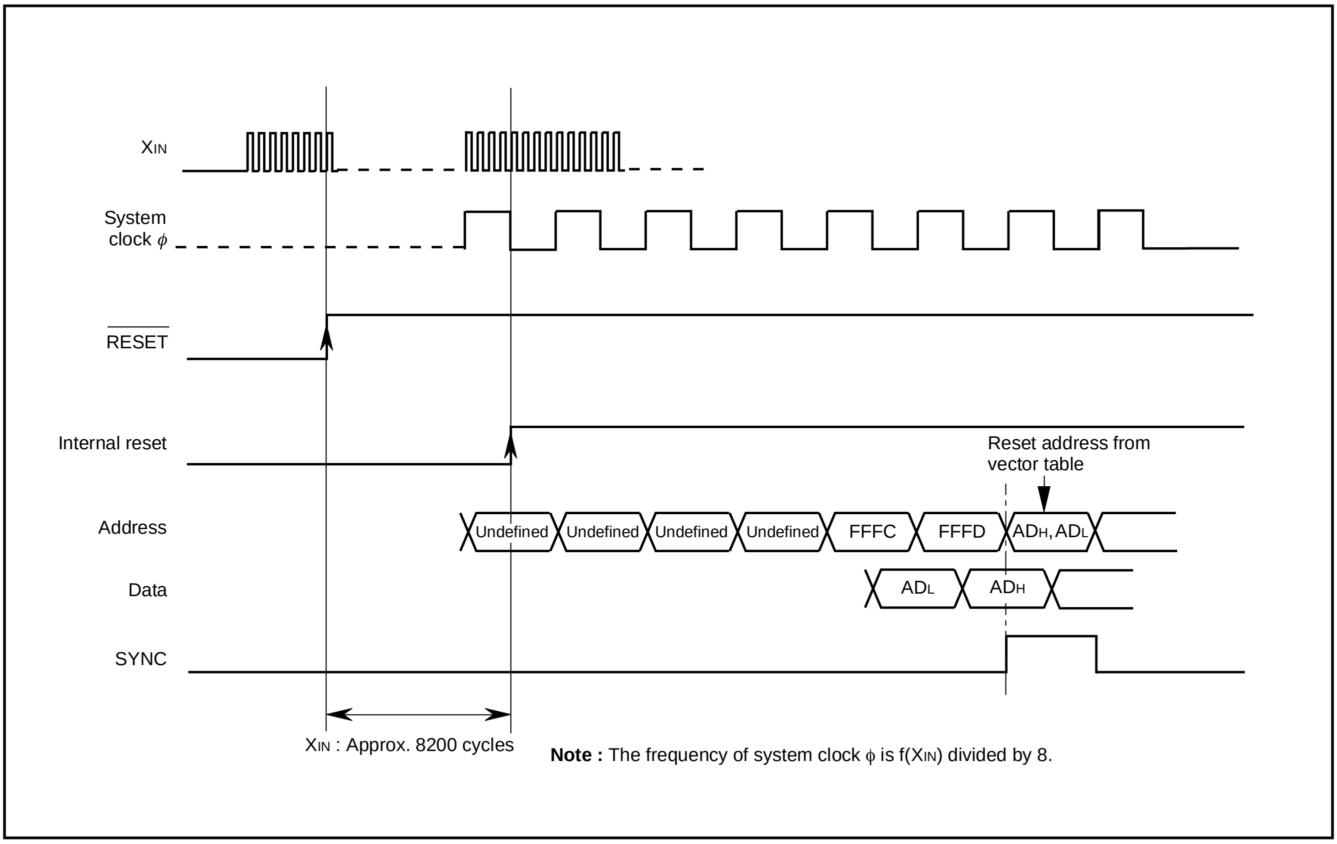


Fig. 57 Reset Sequence

		Address	Register contents
(1)	Port P0 direction register	0001_{16}	00_{16}
(2)	Port P1 direction register	0003_{16}	00_{16}
(3)	Port P2 direction register	0005_{16}	00_{16}
(4)	Port P3 output control register	0007_{16}	00_{16}
(5)	Port P4 direction register	0009_{16}	00_{16}
(6)	Port P5 direction register	$000B_{16}$	00_{16}
(7)	Port P6 direction register	$000D_{16}$	00_{16}
(8)	Port P7 direction register	$000F_{16}$	00_{16}
(9)	AD conversion low-order register	0014_{16}	× × 0 0 0 0 0 1
(10)	Key input control register	0015_{16}	00_{16}
(11)	PULL register A	0016_{16}	$3F_{16}$
(12)	PULL register B	0017_{16}	00_{16}
(13)	Serial I/O1 status register	0019_{16}	1 0 0 0 0 0 0 0
(14)	Serial I/O1 control register	$001A_{16}$	00_{16}
(15)	UART control register	$001B_{16}$	1 1 1 0 0 0 0 0
(16)	Serial I/O2 control register	$001D_{16}$	00_{16}
(17)	Timer X low-order register	0020_{16}	FF_{16}
(18)	Timer X high-order register	0021_{16}	FF_{16}
(19)	Timer Y low-order register	0022_{16}	FF_{16}
(20)	Timer Y high-order register	0023_{16}	FF_{16}
(21)	Timer 1 register	0024_{16}	FF_{16}
(22)	Timer 2 register	0025_{16}	01_{16}
(23)	Timer 3 register	0026_{16}	FF_{16}
(24)	Timer X mode register	0027_{16}	00_{16}
(25)	Timer Y mode register	0028_{16}	00_{16}
(26)	Timer 123 mode register	0029_{16}	00_{16}
(27)	T_{OUT}/ϕ output control register	$002A_{16}$	00_{16}
(28)	PWM control register	$002B_{16}$	00_{16}

		Address	Register contents
(29)	CTCSS timer (low-order)	$002E_{16}$	06_{16}
(30)	CTCSS timer (high-order)	$002F_{16}$	00_{16}
(31)	DTMF high group timer	0030_{16}	06_{16}
(32)	DTMF low group timer	0031_{16}	06_{16}
(33)	DA1 conversion register	0032_{16}	00_{16}
(34)	DA2 conversion register	0033_{16}	00_{16}
(35)	AD control register	0034_{16}	0 0 0 0 1 0 0 0
(36)	DA control register	0036_{16}	00_{16}
(37)	Watchdog timer control register	0037_{16}	0 0 1 1 1 1 1 1
(38)	Segment output enable register	0038_{16}	00_{16}
(39)	LCD mode register	0039_{16}	00_{16}
(40)	Interrupt edge selection register	$003A_{16}$	00_{16}
(41)	CPU mode register	$003B_{16}$	0 1 0 0 1 0 0 0
(42)	Interrupt request register 1	$003C_{16}$	00_{16}
(43)	Interrupt request register 2	$003D_{16}$	00_{16}
(44)	Interrupt control register 1	$003E_{16}$	00_{16}
(45)	Interrupt control register 2	$003F_{16}$	00_{16}
(46)	Processor status register	(PS)	× × × × × 1 × ×
(47)	Program counter	(PC_H)	Contents of address $FFFD_{16}$
		(PC_L)	Contents of address $FFFC_{16}$
(48)	Watchdog timer (high-order)		$3F_{16}$
(49)	Watchdog timer (low-order)		FF_{16}

Note: The contents of all other registers and RAM are undefined after reset, so they must be initialized by software.
× : Undefined

Fig. 58 Internal state of microcomputer immediately after reset

CLOCK GENERATING CIRCUIT

The 3826 group has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub-clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting an oscillator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the oscillator manufacturer's recommended values. A feed-back resistor exists on-chip (An external feed-back resistor may be needed depending on conditions.). However, an external feed-back resistor is needed between XCIN and XCOUT since a resistor does not exist between them.

To supply a clock signal externally, input it to the XIN pin and make the XOUT pin open. The sub-clock oscillation circuit cannot directly input clocks that are externally generated. Accordingly, be sure to cause an external oscillator to oscillate.

Immediately after poweron, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins go to high-impedance state.

Frequency Control

(1) Middle-speed mode

The clock input to the XIN pin is divided by 8 and it is used as the system clock ϕ.

After reset, this mode is selected.

(2) High-speed mode

The clock input to the XIN pin is divided by 2 and it is used as the system clock ϕ.

(3) Low-speed mode

- The clock input to the XCIN pin is divided by 2 and it is used as the system clock ϕ.
- A low-power consumption operation can be realized by stopping the main clock in this mode. To stop the main clock, set the main clock stop bit of the CPU mode register to "1".
  When the main clock is restarted, after setting the main clock stop bit to "0", set enough time for oscillation to stabilize by program.

Note: If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub clock to stabilize, especially immediately after poweron and at returning from stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency in the condition that f(XIN) > 3•f(XCIN).

Oscillation Control

(1) Stop mode

If the STP instruction is executed, the system clock ϕ stops at an "H" level, and main and sub clock oscillators stop.

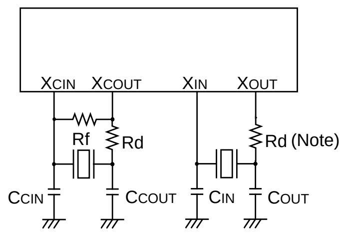
In this time, values set previously to timer 1 latch and timer 2 latch are loaded automatically to timer 1 and timer 2. Before the STP instruction, set the values to generate the wait time required for oscillation stabilization to timer 1 latch and timer 2 latch (low-order 8 bits are set to timer 1, high-order 8 bits are set to timer 2). Either f(XIN) or f(XCIN) divided by 16 is input to timer 1 as count source, and the output of timer 1 is connected to timer 2.

The bits of the timer 123 mode register except bit 4 are set to "0". Set the timer 1 and timer 2 interrupt enable bits to "0" before executing the STP instruction.

Oscillation restarts at reset or when an external interrupt is received, but the system clock ϕ is not supplied to the CPU until timer 2 underflows. This allows time for the clock circuit oscillation to stabilize when a ceramic resonator is used.

(2) Wait mode

If the WIT instruction is executed, only the system clock ϕ stops at an "H" state. The states of main clock and sub clock are the same as the state before the executing the WIT instruction, and oscillation does not stop. Since supply of internal clock ϕ is started immediately after the interrupt is received, the instruction can be executed immediately.



Notes : Insert a damping resistor if required.
The resistance will vary depending on the oscillator and the oscillation drive capacity setting.
Use the value recommended by the maker of the oscillator.
Also, if the oscillator manufacturer's data sheet specifies that a feedback resistor be added external to the chip though a feedback resistor exists on-chip, insert a feedback resistor between XIN and XOUT following the instruction.

Fig. 59 Oscillator circuit

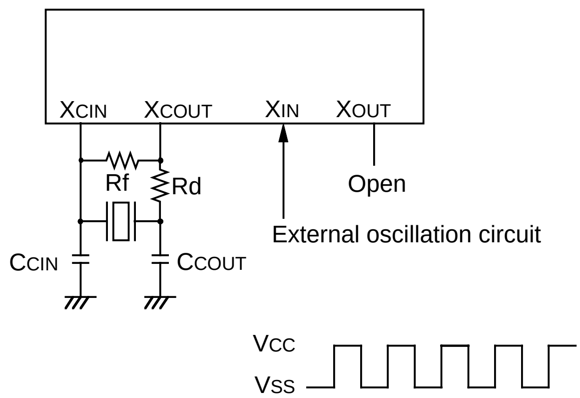
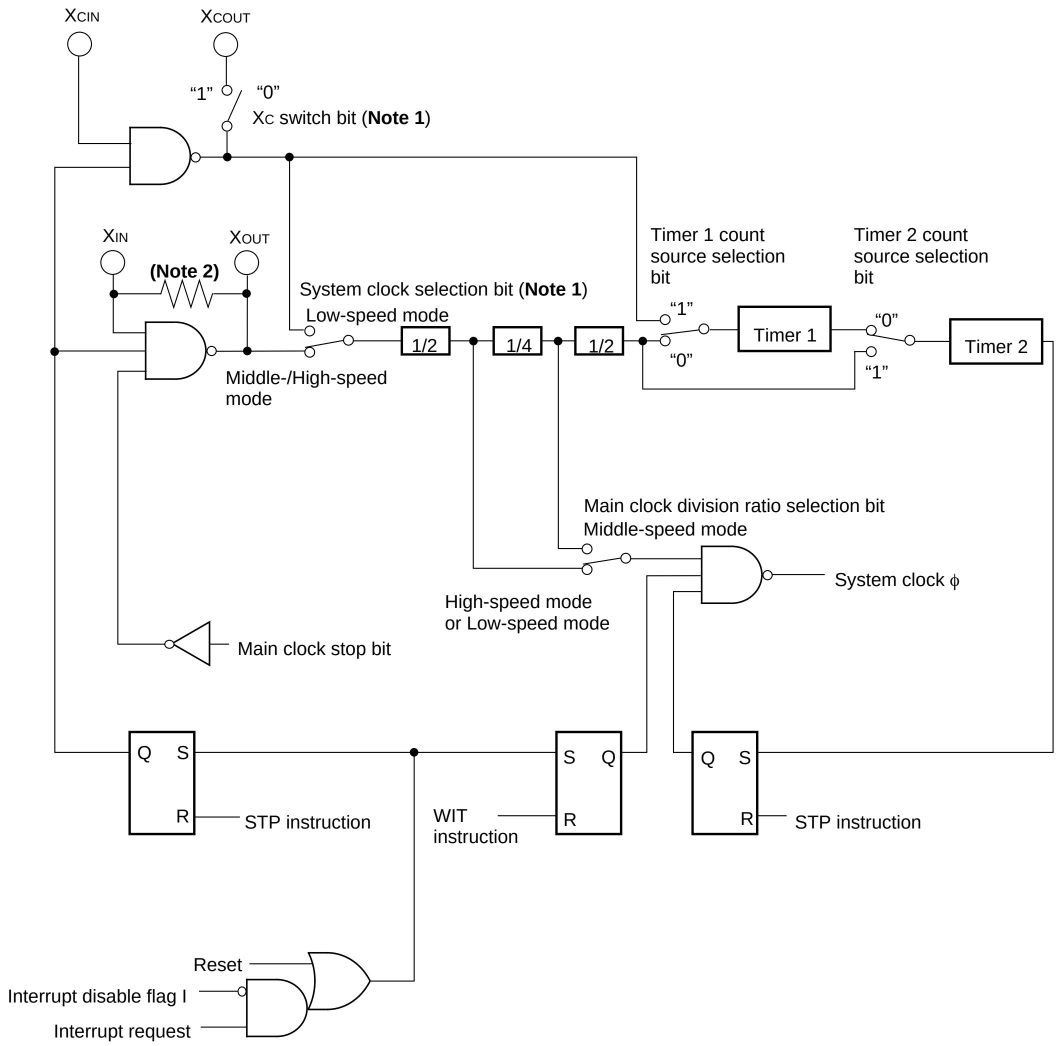
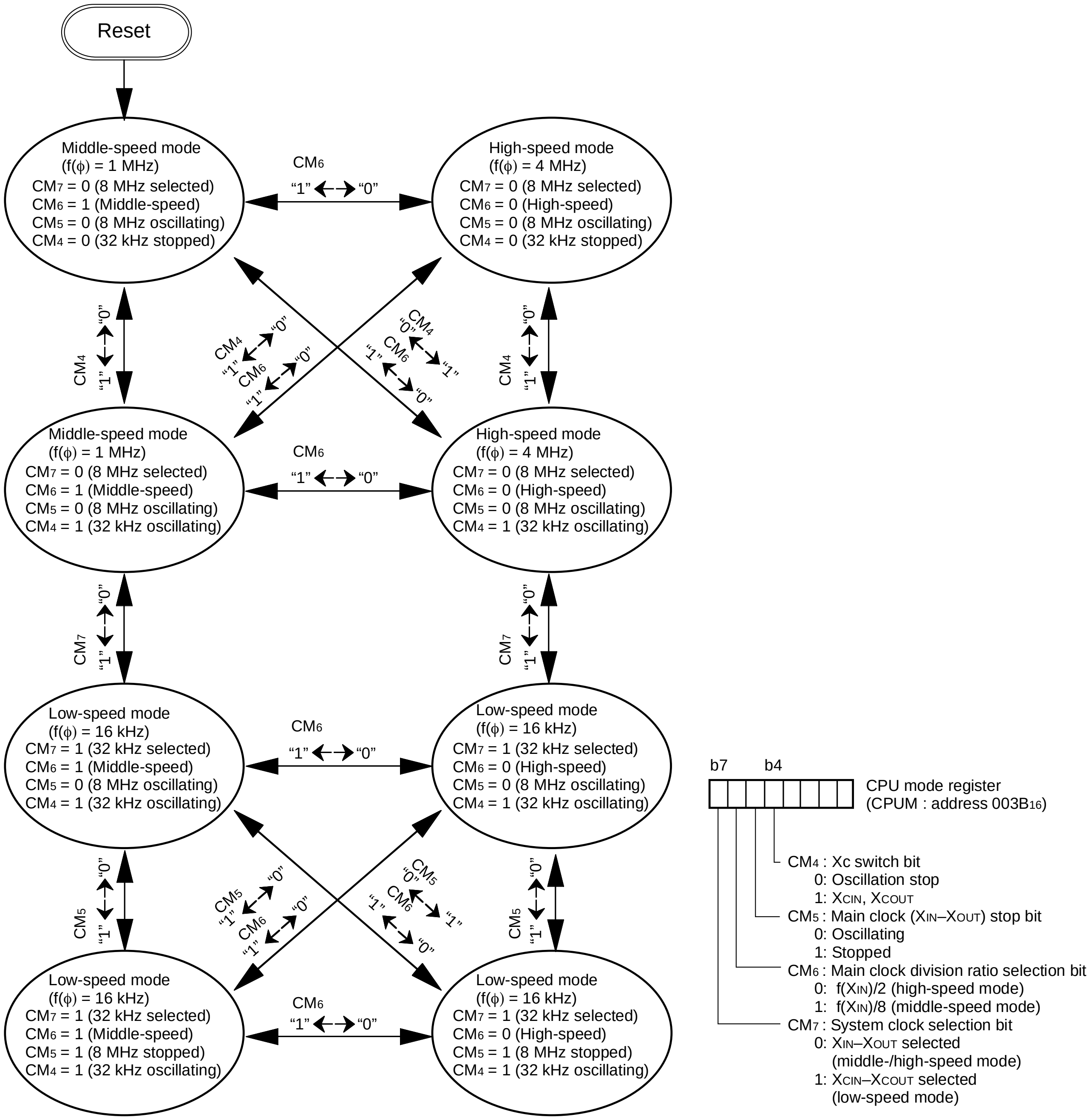


Fig. 60 External clock input circuit



Notes 1: When using the sub clock for the system clock φ, set the XC switch bit to "1".
2: Although a feed-back resistor exists on-chip, an external feed-back resistor may be needed depending on conditions.

Fig. 61 Clock generating circuit block diagram



Notes 1: Switch the mode according to the arrows shown between the mode blocks. (Do not switch between the mode directly without an arrow.)

2: The all modes can be switched to the stop mode or the wait mode and returned to the source mode when the stop mode or the wait mode is ended.

3: When the stop mode is ended, a delay time can be set by timer 1 and timer 2.

4: Timer and LCD operate in the wait mode.

5: Wait until oscillation stabilizes after oscillating the main clock before the switching from the low-speed mode to middle-/high-speed mode.

6: The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. φ indicates the system clock.

Fig. 62 State transitions of system clock

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags (T flag, D flag, etc.) which affect program execution.

Interrupt

When the contents of an interrupt request bits are changed by the program, execute a BBC or BBS instruction after at least one instruction. This is for preventing executing a BBC or BBS instruction to the contents before change.

Decimal Calculations

To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.

In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Multiplication and Division Instructions

The index mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
The execution of these instructions does not change the contents of the processor status register.

Ports

Use instructions such as LDM and STA, etc., to set the port direction registers.
The contents of the port direction registers cannot be read.
The following cannot be used:

- LDA instruction
- The memory operation instruction when the T flag is “1”
- The bit-test instruction (BBC or BBS, etc.)
- The read-modify-write instruction (calculation instruction such as ROR etc., bit manipulation instruction such as CLB or SEB etc.)
- The addressing mode which uses the value of a direction register as an index

Serial I/O

In clock synchronous serial I/O, if the receive side is using an external clock and it is to output the $\overline{\text{SRDY}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY}}$ output enable bit to “1”.
The TxD pin of serial I/O1 retains the level then after transmission is completed.
In serial I/O2 selecting an internal clock, the SOUT2 pin goes to high impedance state after transmission is completed.
In serial I/O2 selecting an external clock, the SOUT2 pin retains the level then after transmission is completed.

A/D Converter

The input to the comparator is combined by internal capacitors. Therefore, since conversion accuracy may be worse by losing of an electric charge when the conversion speed is not enough, make sure that f(XIN) is at least 500 kHz during an A/D conversion.
The normal operation of A/D conversion cannot be guaranteed when performing the next operation:

- When writing to CPU mode register during A/D conversion operation
- When writing to AD control register during A/D conversion operation
- When executing STP instruction or WIT instruction during A/D conversion operation

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the system clock ϕ by the number of cycles needed to execute an instruction.
The number of cycles required to execute an instruction is shown in the list of machine instructions.
The frequency of the system clock ϕ depends on the main clock division ratio selection bit and the system clock selection bit.

NOTES ON USE
Countermeasures Against Noise

(1) Shortest wiring length

① Wiring for $\overline{\text{RESET}}$ pin

Make the length of wiring which is connected to the $\overline{\text{RESET}}$ pin as short as possible. Especially, connect a capacitor across the $\overline{\text{RESET}}$ pin and the Vss pin with the shortest possible wiring (within 20 mm).

● Reason

The width of a pulse input into the $\overline{\text{RESET}}$ pin is determined by the timing necessary conditions. If noise having a shorter pulse width than the standard is input to the $\overline{\text{RESET}}$ pin, the reset is released before the internal state of the microcomputer is completely initialized. This may cause a program runaway.

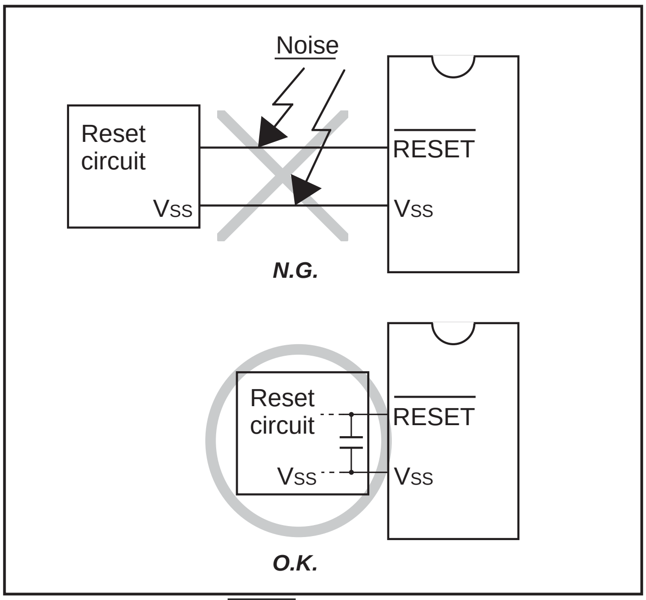


Fig. 63 Wiring for the $\overline{\text{RESET}}$ pin

② Wiring for clock input/output pins

- Make the length of wiring which is connected to clock I/O pins as short as possible.
- Make the length of wiring (within 20 mm) across the grounding lead of a capacitor which is connected to an oscillator and the Vss pin of a microcomputer as short as possible.
- Separate the Vss pattern only for oscillation from other Vss patterns.

● Reason

If noise enters clock I/O pins, clock waveforms may be deformed. This may cause a program failure or program runaway. Also, if a potential difference is caused by the noise between the Vss level of a microcomputer and the Vss level of an oscillator, the correct clock will not be input in the microcomputer.

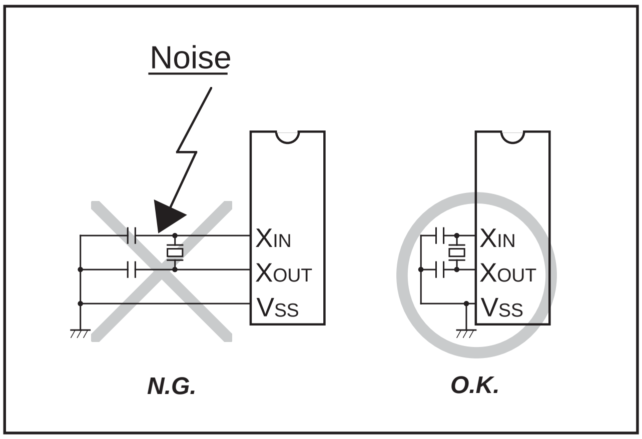


Fig. 64 Wiring for clock I/O pins

(2) Connection of bypass capacitor across Vss line and Vcc line

In order to stabilize the system operation and avoid the latch-up, connect an approximately 0.1 µF bypass capacitor across the Vss line and the Vcc line as follows:

- Connect a bypass capacitor across the Vss pin and the Vcc pin at equal length.
- Connect a bypass capacitor across the Vss pin and the Vcc pin with the shortest possible wiring.
- Use lines with a larger diameter than other signal lines for Vss line and Vcc line.
- Connect the power source wiring via a bypass capacitor to the Vss pin and the Vcc pin.

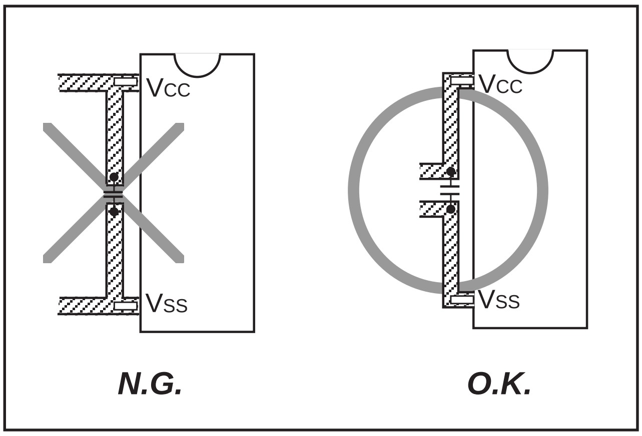


Fig. 65 Bypass capacitor across the Vss line and the Vcc line

(3) Oscillator concerns

In order to obtain the stabilized operation clock on the user system and its condition, contact the oscillator manufacturer and select the oscillator and oscillation circuit constants. Be careful especially when range of voltage or/and temperature is wide.
Also, take care to prevent an oscillator that generates clocks for a microcomputer operation from being affected by other signals.

① Keeping oscillator away from large current signal lines
Install a microcomputer (and especially an oscillator) as far as possible from signal lines where a current larger than the tolerance of current value flows.

● Reason
In the system using a microcomputer, there are signal lines for controlling motors, LEDs, and thermal heads or others. When a large current flows through those signal lines, strong noise occurs because of mutual inductance.

② Installing oscillator away from signal lines where potential levels change frequently
Install an oscillator and a connecting pattern of an oscillator away from signal lines where potential levels change frequently. Also, do not cross such signal lines over the clock lines or the signal lines which are sensitive to noise.

● Reason
Signal lines where potential levels change frequently (such as the CNTR pin signal line) may affect other lines at signal rising edge or falling edge. If such lines cross over a clock line, clock waveforms may be deformed, which causes a microcomputer failure or a program runaway.

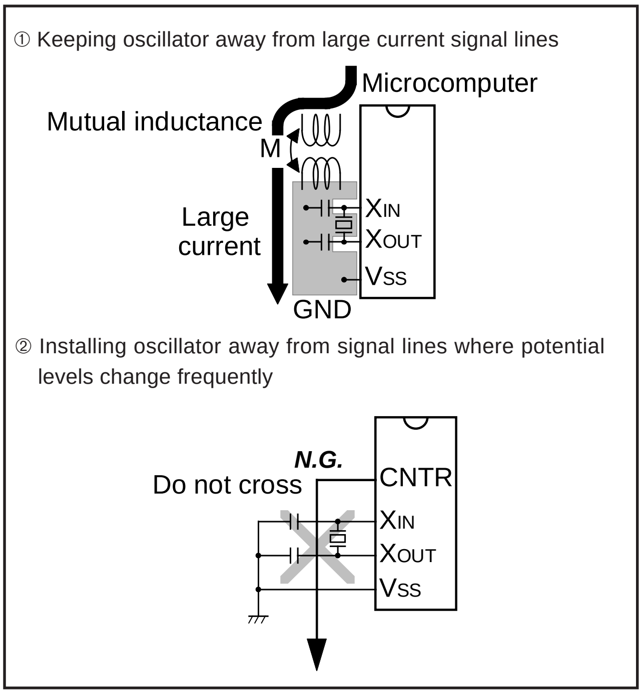


Fig. 66 Wiring for a large current signal line/Wiring of signal lines where potential levels change frequently

(4) Analog input

The analog input pin is connected to the capacitor of a comparator. Accordingly, sufficient accuracy may not be obtained by the charge/discharge current at the time of A/D conversion when the analog signal source of high-impedance is connected to an analog input pin. In order to obtain the A/D conversion result stabilized more, please lower the impedance of an analog signal source, or add the smoothing capacitor to an analog input pin.

(5) Difference of memory type and size

When Mask ROM and PROM version and memory size differ in one group, actual values such as an electrical characteristics, A-D conversion accuracy, and the amount of proof of noise incorrect operation may differ from the ideal values.
When these products are used switching, perform system evaluation for each product of every after confirming product specification.

(6) Wiring to VPP pin of One Time PROM version and EPROM version

Connect an approximately 5 kΩ resistor to the VPP pin the shortest possible in series.

Note: Even when a circuit which included an approximately 5 kΩ resistor is used in the Mask ROM version, the microcomputer operates correctly.

● Reason
The VPP pin of the PROM version is the power source input pin for the built-in PROM. When programming in the built-in PROM, the impedance of the VPP pin is low to allow the electric current for writing flow into the built-in PROM. Because of this, noise can enter easily. If noise enters the VPP pin, abnormal instruction codes or data are read from the built-in PROM, which may cause a program runaway.

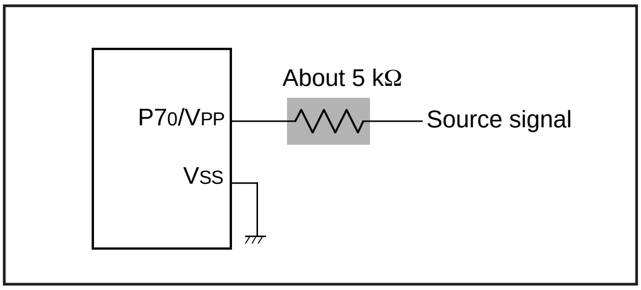


Fig. 67 Wiring for the VPP pin of One Time PROM

NOTES ON USE

Power Source Voltage

When the power source voltage value of a microcomputer is less than the value which is indicated as the recommended operating conditions, the microcomputer does not operate normally and may perform unstable operation.

In a system where the power source voltage drops slowly when the power source voltage drops or the power supply is turned off, reset a microcomputer when the power source voltage is less than the recommended operating conditions and design a system not to cause errors to the system by this unstable operation.

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM pro-grammer in the user ROM area.

Table 14 Special programming adapter

Package	Name of Programming Adapter
PRQP0100JB-A	PCA4738F-100A
PLQP0100KB-A	PCA4738G-100A
100D0	PCA4738L-100A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To en-sure proper operation after programming, the procedure shown in Figure 68 is recommended to verify programming.

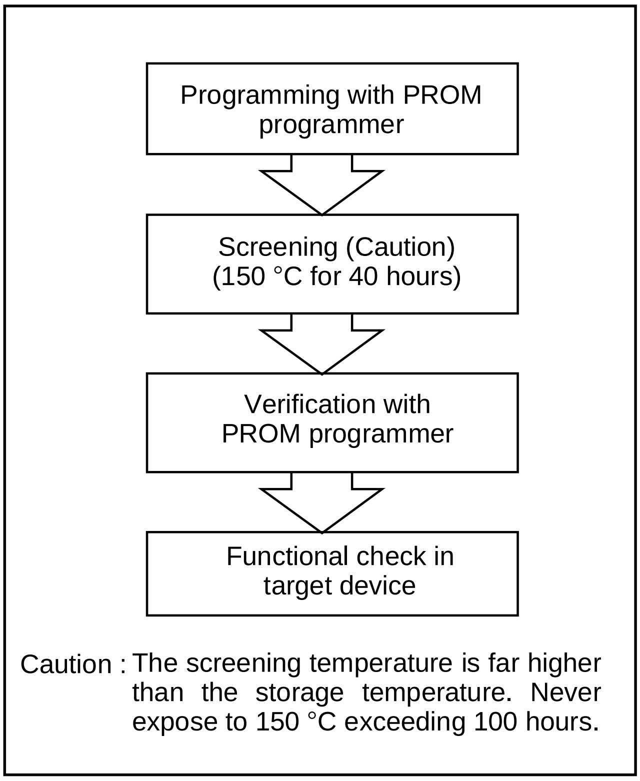


Fig. 68 State transitions of system clock

ELECTRICAL CHARACTERISTICS
ABSOLUTE MAXIMUM RATINGS

Table 15 Absolute maximum ratings

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. When an input voltage is measured, output transistors are cut off.	–0.3 to 7.0	V
V_I	Input voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage $P7_0$–$P7_7$		–0.3 to V_{CC} +0.3	V
V_I	Input voltage V_{L1}		–0.3 to V_{L2}	V
V_I	Input voltage V_{L2}		V_{L1} to V_{L3}	V
V_I	Input voltage V_{L3}		V_{L2} to 7.0	V
V_I	Input voltage C_1, C_2		–0.3 to 7.0	V
V_I	Input voltage $\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage C_1, C_2		–0.3 to 7.0	V
V_O	Output voltage $P0_0$–$P0_7$, $P1_0$–$P1_5$, $P3_0$–$P3_7$	At output port	–0.3 to V_{CC}	V
		At segment output	–0.3 to V_{L3}	V
V_O	Output voltage $P1_6$, $P1_7$, $P2_0$–$P2_7$, $P4_0$–$P4_7$, $P5_0$–$P5_7$, $P6_0$–$P6_7$, $P7_1$–$P7_7$		–0.3 to V_{CC} +0.3	V
V_O	Output voltage V_{L3}		–0.3 to 7.0	V
V_O	Output voltage V_{L2}, SEG_0–SEG_{17}		–0.3 to V_{L3}	V
V_O	Output voltage X_{OUT}		–0.3 to V_{CC} +0.3	V
Pd	Power dissipation	Ta = 25°C	300	mW
Topr	Operating temperature		–20 to 85	°C
Tstg	Storage temperature		–40 to 125	°C

RECOMMENDED OPERATING CONDITIONS

Table 16 Recommended operating conditions (1)

(V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage	High-speed mode f(X_{IN}) = 8 MHz	4.0	5.0	5.5	V
		Middle-speed mode f(X_{IN}) = 8 MHz	2.5	5.0	5.5	
		Low-speed mode	2.5	5.0	5.5	
V_{SS}	Power source voltage			0		V
V_{REF}	A/D, D/A conversion reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage			0		V
V_{IA}	Analog input voltage AN_0–AN_7		AV_{SS}		V_{CC}	V
V_{IH}	"H" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_3$, $P4_5$, $P4_7$, $P5_0$–$P5_3$, $P5_6$, $P6_1$, $P6_4$–$P6_7$, $P7_1$–$P7_7$	0.7 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$P2_0$–$P2_7$, $P4_1$, $P4_2$, $P4_4$, $P4_6$, $P5_4$, $P5_5$, $P5_7$, $P6_0$, $P6_2$, $P6_3$, $P7_0$	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	$\overline{RESET}$	0.8 V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage	X_{IN}	0.8 V_{CC}		V_{CC}	V
V_{IL}	"L" input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P4_0$, $P4_3$, $P4_5$, $P4_7$, $P5_0$–$P5_3$, $P5_6$, $P6_1$, $P6_4$–$P6_7$, $P7_1$–$P7_7$	0		0.3 V_{CC}	V
V_{IL}	"L" input voltage	$P2_0$–$P2_7$, $P4_1$, $P4_2$, $P4_4$, $P4_6$, $P5_4$, $P5_5$, $P5_7$, $P6_0$, $P6_2$, $P6_3$, $P7_0$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	$\overline{RESET}$	0		0.2 V_{CC}	V
V_{IL}	"L" input voltage	X_{IN}	0		0.2 V_{CC}	V

Table 17 Recommended operating conditions (2)
(V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
$\Sigma I_{OH(peak)}$	"H" total peak output current	P00–P07, P10–P17, P20–P27, P30–P37 **(Note 1)**			–20	mA
$\Sigma I_{OH(peak)}$	"H" total peak output current	P41–P47, P50–P57, P60–P67 **(Note 1)**			–20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	P00–P07, P10–P17, P20–P27, P30–P37 **(Note 1)**			20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	P41–P47, P50–P57, P60–P67 **(Note 1)**			20	mA
$\Sigma I_{OL(peak)}$	"L" total peak output current	P40, P71–P77 **(Note 1)**			80	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	P00–P07, P10–P17, P20–P27, P30–P37 **(Note 1)**			–10	mA
$\Sigma I_{OH(avg)}$	"H" total average output current	P41–P47, P50–P57, P60–P67 **(Note 1)**			–10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	P00–P07, P10–P17, P20–P27, P30–P37 **(Note 1)**			10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	P41–P47, P50–P57, P60–P67 **(Note 1)**			10	mA
$\Sigma I_{OL(avg)}$	"L" total average output current	P40, P71–P77 **(Note 1)**			40	mA
$I_{OH(peak)}$	"H" peak output current	P00–P07, P10–P15, P30–P37 **(Note 2)**			–1.0	mA
$I_{OH(peak)}$	"H" peak output current	P16, P17, P20–P27, P41–P47, P50–P57, P60–P67 **(Note 2)**			–5.0	mA
$I_{OL(peak)}$	"L" peak output current	P00–P07, P10–P15, P30–P37 **(Note 2)**			5.0	mA
$I_{OL(peak)}$	"L" peak output current	P16, P17, P20–P27, P41–P47, P50–P57, P60–P67 **(Note 2)**			10	mA
$I_{OL(peak)}$	"L" peak output current	P40, P71–P77 **(Note 2)**			20	mA
$I_{OH(avg)}$	"H" average output current	P00–P07, P10–P15, P30–P37 **(Note 3)**			–0.5	mA
$I_{OH(avg)}$	"H" average output current	P16, P17, P20–P27, P41–P47, P50–P57, P60–P67 **(Note 3)**			–2.5	mA
$I_{OL(avg)}$	"L" average output current	P00–P07, P10–P15, P30–P37 **(Note 3)**			2.5	mA
$I_{OL(avg)}$	"L" average output current	P16, P17, P20–P27, P41–P47, P50–P57, P60–P67 **(Note 3)**			5.0	mA
$I_{OL(avg)}$	"L" average output current	P40, P71–P77 **(Note 3)**			10	mA

Notes1: The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.
2: The peak output current is the peak current flowing in each port.
3: The average output current is an average value measured over 100 ms.

Table 18 Recommended operating conditions (3)
(V_{CC} = 2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
f(CNTR0) f(CNTR1)	Input frequency for timers X and Y (duty cycle 50%)	(4.0 V ≤ V_{CC} ≤ 5.5 V)			4.0	MHz
		(V_{CC} ≤ 4.0 V)			(2×V_{CC}) –4	MHz
f(X_{IN})	Main clock input oscillation frequency **(Note 1)**	High-speed mode (4.0 V ≤ V_{CC} ≤ 5.5 V)			8.0	MHz
		High-speed mode (2.5 V ≤ V_{CC} ≤ 4.0 V)			(4×V_{CC}) –8	MHz
		Middle-speed mode			8.0	MHz
f(X_{CIN})	Sub-clock input oscillation frequency **(Notes 1, 2)**			32.768	50	kHz

Notes1: When the oscillation frequency has a duty cycle of 50%.
2: When using the microcomputer in low-speed mode, make sure that the sub-clock input oscillation frequency on condition that f(X_{CIN}) < f(X_{IN})/3.

ELECTRICAL CHARACTERISTICS

Table 19 Electrical characteristics (1)

(V_{CC} =4.0 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	"H" output voltage P00–P07, P10–P15, P30–P37	I_{OH} = –1 mA	V_{CC}–2.0			V
		I_{OH} = –0.25 mA, V_{CC} = 2.5 V	V_{CC}–0.8			V
V_{OH}	"H" output voltage P16, P17, P20–P27, P41–P47, P50–P57, P60–P67	I_{OH} = –5 mA	V_{CC}–2.0			V
		I_{OH} = –1.5 mA	V_{CC}–0.5			V
		I_{OH} = –1.25 mA, V_{CC} = 2.5 V	V_{CC}–0.8			V
V_{OL}	"L" output voltage P00–P07, P10–P15, P30–P37	I_{OL} = 5 mA			2.0	V
		I_{OL} = 1.5 mA			0.5	V
		I_{OL} = 1.25 mA, V_{CC} = 2.5 V			0.8	V
V_{OL}	"L" output voltage P16, P17, P20–P27, P41–P47, P50–P57, P60–P67	I_{OL} = 10 mA			2.0	V
		I_{OL} = 3.0 mA			0.5	V
		I_{OL} = 2.5 mA, V_{CC} = 2.5 V			0.8	V
V_{OL}	"L" output voltage P40, P71–P77	I_{OL} = 10 mA			0.5	V
		I_{OL} = 5 mA, V_{CC} = 2.5 V			0.3	V
$V_{T+} – V_{T–}$	Hysteresis INT0–INT2, ADT, CNTR0, CNTR1, P20–P27			0.5		V
$V_{T+} – V_{T–}$	Hysteresis SCLK, RXD, SIN2			0.5		V
$V_{T+} – V_{T–}$	Hysteresis $\overline{\text{RESET}}$			0.5		V
I_{IH}	"H" input current P00–P07, P10–P17, P20–P27, P40–P47, P50–P57, P60–P67, P70–P77	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current $\overline{\text{RESET}}$	V_I = V_{CC}			5.0	µA
I_{IH}	"H" input current XIN	V_I = V_{CC}		4.0		µA
I_{IL}	"L" input current P00–P07,P10–P17, P20–P27,P41–P47, P50–P57, P60–P67	V_I = V_{SS}, Pull-ups "off"			–5.0	µA
		V_{CC} = 5 V, V_I = V_{SS}, Pull-ups "on"	–60.0	–120.0	–240.0	µA
		V_{CC} = 2.5 V, V_I = V_{SS}, Pull-ups "on"	–6.0	–25.0	–45.0	µA
I_{IL}	"L" input current P40, P70–P77				–5.0	µA
I_{IL}	"L" input current $\overline{\text{RESET}}$	V_I = V_{SS}			–5.0	µA
I_{IL}	"L" input current XIN	V_I = V_{SS}		–4.0		µA
I_{LOAD}	Output load current P30–P37	V_{CC} = 5.0 V, V_O = V_{CC}, Pullup ON, Output transistors "off"	–60.0	–120.0	–240.0	µA
		V_{CC} = 2.5 V,V_O = V_{CC}, Pullup ON, Output transistors "off"	–6.0	–25.0	–45.0	µA
I_{LEAK}	Output leak current P30–P37	V_O = V_{CC}, Pullup OFF, Output transistors "off"			5.0	µA
		V_O = V_{SS}, Pullup OFF, Output transistors "off"			–5.0	µA

Table 20 Electrical characteristics (2)
(V_{CC} =2.5 to 5.5 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{RAM}	RAM retention voltage	At clock stop mode		2.0		5.5	V
I_{CC}	Power source current	• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A/D converter in operating			6.4	13	mA
		• High-speed mode, V_{CC} = 5 V $f(X_{IN})$ = 8 MHz (in WIT state) $f(X_{CIN})$ = 32.768 kHz Output transistors “off” A/D converter stop			1.6	3.2	mA
		• Low-speed mode, V_{CC} = 5 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			35	70	µA
		• Low-speed mode, V_{CC} = 5 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			20	40	µA
		• Low-speed mode, V_{CC} = 3 V, Ta ≤ 55°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz Output transistors “off”			15	22	µA
		• Low-speed mode, V_{CC} = 3 V, Ta = 25°C $f(X_{IN})$ = stopped $f(X_{CIN})$ = 32.768 kHz (in WIT state) Output transistors “off”			4.5	9.0	µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	
V_{L1}	Power source voltage	When using voltage multiplier		1.3	1.8	2.3	V
I_{L1}	Power source current (V_{L1}) **(Note)**	V_{L1} = 1.8 V			4.0		µA

Note: When the voltage multiplier control bit of the LCD mode register (bit 4 at address 0039_{16}) is “1”.

A/D CONVERTER CHARACTERISTICS

Table 21 A/D converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85°C, f(X_{IN}) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)
8-bit A/D mode (when conversion mode selection bit (bit 0 of address 0014_{16}) is “1”)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 2.7 to 5.5 V			±2	LSB
t_{CONV}	Conversion time	f(X_{IN}) = 8 MHz			12.5 (Note)	µS
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Note: When the internal trigger is used in the middle-speed mode, the max. value of t_{CONV} is 14 µS.

Table 22 A/D converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85°C, f(X_{IN}) = 500 kHz to 8 MHz, in middle/high-speed mode unless otherwise noted)
10-bit A/D mode (when conversion mode selection bit (bit 0 of address 0014_{16}) is “0”)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				10	Bits
–	Absolute accuracy (excluding quantization error)	V_{CC} = V_{REF} = 2.7 to 5.5 V			±4	LSB
t_{CONV}	Conversion time	f(X_{IN}) = 8 MHz			15.5 (Note)	µS
R_{LADDER}	Ladder resistor		12	35	100	kΩ
I_{VREF}	Reference power source input current	V_{REF} = 5 V	50	150	200	µA
I_{IA}	Analog port input current				5.0	µA

Note: When the internal trigger is used in the middle-speed mode, the max. value of t_{CONV} is 17 µS.

D/A CONVERTER CHARACTERISTICS

Table 23 D/A converter characteristics

(V_{CC} = 2.7 to 5.5 V, V_{CC} = V_{REF}, V_{SS} = AV_{SS} = 0 V, Ta = –20 to 85°C, in middle/high-speed mode unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
–	Resolution				8	Bits
–	Absolute accuracy	V_{CC} = V_{REF} = 5 V			1.0	%
		V_{CC} = V_{REF} = 2.7 V			2.0	%
t_{su}	Setting time			3		µs
R_O	Output resistor		1	2.5	4	kΩ
I_{VREF}	Reference power source input current	**(Note)**			3.2	mA

Note: Using one D/A converter, with the value in the D/A conversion register of the other D/A converter being “00_{16}”, and excluding currents flowing through the A/D resistance ladder.

TIMING REQUIREMENTS

Table 24 Timing requirements 1

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	250			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	105			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	105			ns
$t_{wH(INT)}$	INT_0 to INT_2 input “H” pulse width	80			ns
$t_{wL(INT)}$	INT_0 to INT_2 input “L” pulse width	80			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time **(Note)**	800			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width **(Note)**	370			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width **(Note)**	370			ns
$t_{su(RxD-S_{CLK1})}$	Serial I/O1 input set up time	220			ns
$t_{h(S_{CLK1}-RxD)}$	Serial I/O1 input hold time	100			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time **(Note)**	1000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width **(Note)**	400			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width **(Note)**	400			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	200			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	200			ns

Note: When bit 6 of address $001A_{16}$ is “1”.
Divide this value by four when bit 6 of address $001A_{16}$ is “0”.

Table 25 Timing requirements 2

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits Min.	Limits Typ.	Limits Max.	Unit
$t_{w(\overline{RESET})}$	Reset input “L” pulse width	2			µs
$t_{c(X_{IN})}$	Main clock input cycle time (X_{IN} input)	125			ns
$t_{wH(X_{IN})}$	Main clock input “H” pulse width	45			ns
$t_{wL(X_{IN})}$	Main clock input “L” pulse width	40			ns
$t_{c(CNTR)}$	$CNTR_0$, $CNTR_1$ input cycle time	500/(V_{CC}-2)			ns
$t_{wH(CNTR)}$	$CNTR_0$, $CNTR_1$ input “H” pulse width	250/(V_{CC}-2)–20			ns
$t_{wL(CNTR)}$	$CNTR_0$, $CNTR_1$ input “L” pulse width	250/(V_{CC}-2)–20			ns
$t_{wH(INT)}$	INT_0 to INT_2 input “H” pulse width	230			ns
$t_{wL(INT)}$	INT_0 to INT_2 input “L” pulse width	230			ns
$t_{c(S_{CLK1})}$	Serial I/O1 clock input cycle time **(Note)**	2000			ns
$t_{wH(S_{CLK1})}$	Serial I/O1 clock input “H” pulse width **(Note)**	950			ns
$t_{wL(S_{CLK1})}$	Serial I/O1 clock input “L” pulse width **(Note)**	950			ns
$t_{su(RxD-S_{CLK1})}$	Serial I/O1 input set up time	400			ns
$t_{h(S_{CLK1}-RxD)}$	Serial I/O1 input hold time	200			ns
$t_{c(S_{CLK2})}$	Serial I/O2 clock input cycle time **(Note)**	2000			ns
$t_{wH(S_{CLK2})}$	Serial I/O2 clock input “H” pulse width **(Note)**	950			ns
$t_{wL(S_{CLK2})}$	Serial I/O2 clock input “L” pulse width **(Note)**	950			ns
$t_{su(S_{IN2}-S_{CLK2})}$	Serial I/O2 input set up time	400			ns
$t_{h(S_{CLK2}-S_{IN2})}$	Serial I/O2 input hold time	300			ns

Note: When bit 6 of address $001A_{16}$ is “1”.
Divide this value by four when bit 6 of address $001A_{16}$ is “0”.

SWITCHING CHARACTERISTICS

Table 26 Switching characteristics 1

(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output "H" pulse width	$t_C(S_{CLK1})/2-30$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output "L" pulse width	$t_C(S_{CLK1})/2-30$			ns
$t_d(S_{CLK1}-T_XD)$	Serial I/O1 output delay time **(Note 1)**			140	ns
$t_v(S_{CLK1}-T_XD)$	Serial I/O1 output valid time **(Note 1)**	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			30	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			30	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output "H" pulse width	$t_C(S_{CLK2})/2-160$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output "L" pulse width	$t_C(S_{CLK2})/2-160$			ns
$t_d(S_{CLK2}-S_{OUT2})$	Serial I/O2 output delay time			$0.2 \times t_C(S_{CLK2})$	ns
$t_v(S_{CLK2}-S_{OUT2})$	Serial I/O2 output valid time	0			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			40	ns
$t_r(CMOS)$	CMOS output rising time **(Note 2)**		10	30	ns
$t_f(CMOS)$	CMOS output falling time **(Note 2)**		10	30	ns

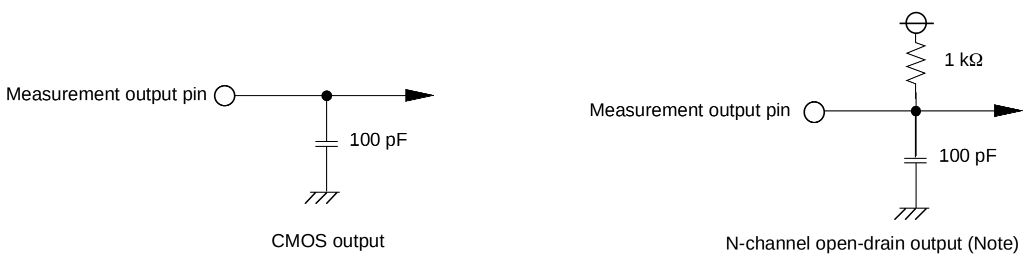
Notes1: When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: X_{OUT} and X_{COUT} pins are excluded.

Table 27 Switching characteristics 2

(V_{CC} = 2.5 to 4.0 V, V_{SS} = 0 V, Ta = –20 to 85°C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_{WH}(S_{CLK1})$	Serial I/O1 clock output "H" pulse width	$t_C(S_{CLK1})/2-50$			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock output "L" pulse width	$t_C(S_{CLK1})/2-50$			ns
$t_d(S_{CLK1}-T_XD)$	Serial I/O1 output delay time **(Note 1)**			350	ns
$t_v(S_{CLK1}-T_XD)$	Serial I/O1 output valid time **(Note 1)**	–30			ns
$t_r(S_{CLK1})$	Serial I/O1 clock output rising time			50	ns
$t_f(S_{CLK1})$	Serial I/O1 clock output falling time			50	ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock output "H" pulse width	$t_C(S_{CLK2})/2-240$			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock output "L" pulse width	$t_C(S_{CLK2})/2-240$			ns
$t_d(S_{CLK2}-S_{OUT2})$	Serial I/O2 output delay time			$0.2 \times t_C(S_{CLK2})$	ns
$t_v(S_{CLK2}-S_{OUT2})$	Serial I/O2 output valid time	0			ns
$t_f(S_{CLK2})$	Serial I/O2 clock output falling time			50	ns
$t_r(CMOS)$	CMOS output rising time **(Note 2)**		20	50	ns
$t_f(CMOS)$	CMOS output falling time **(Note 2)**		20	50	ns

Notes1: When the $P4_5/T_XD$ P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is "0".
2: X_{OUT} and X_{COUT} pins are excluded.



Note: When $P7_1$–$P7_7$, $P4_0$ and bit 4 of the UART control register (address $001B_{16}$) is "1" (N-channel open-drain output mode).

Fig. 69 Circuit for measuring output switching characteristics

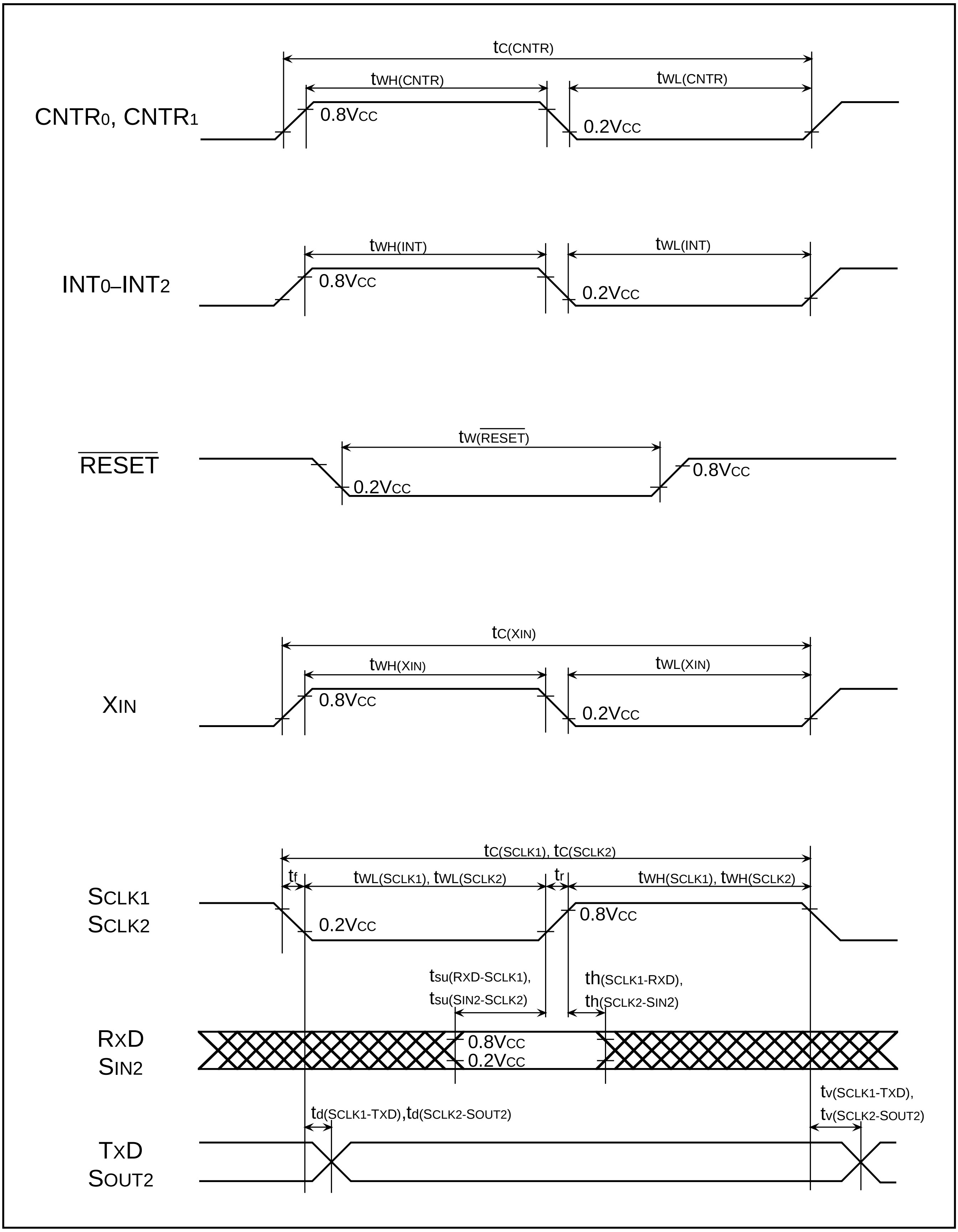
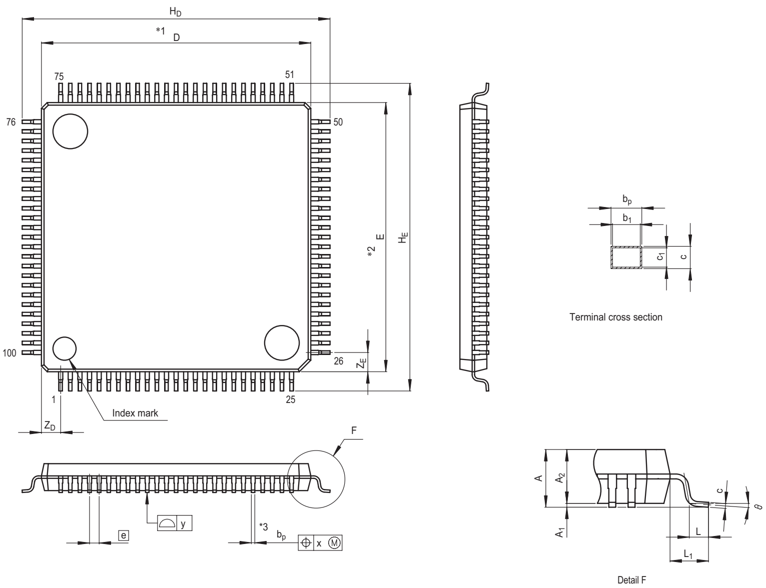


Fig. 70 Timing diagram

PACKAGE OUTLINE

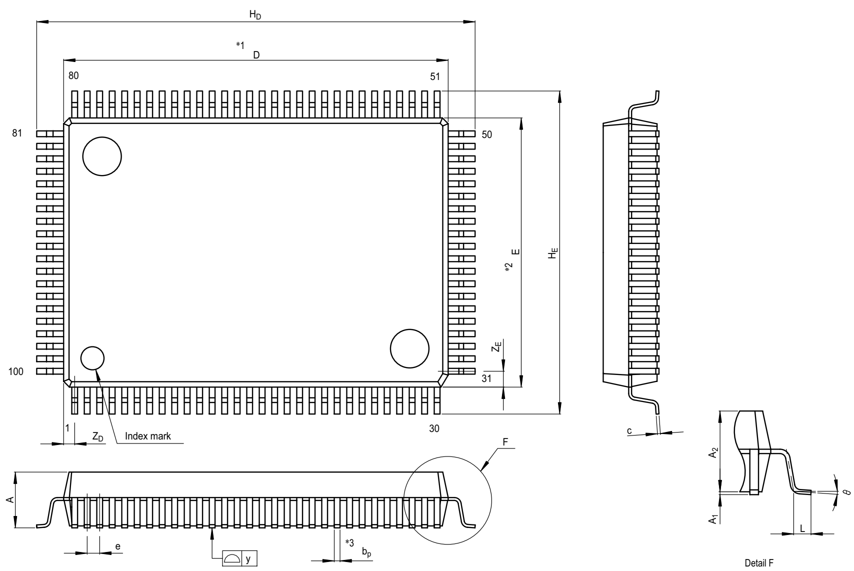
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
$\boxed{e}$	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-QFP100-14x20-0.65	PRQP0100JB-A	100P6S-A	1.6g



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.8	20.0	20.2
E	13.8	14.0	14.2
A_2	—	2.8	—
H_D	22.5	22.8	23.1
H_E	16.5	16.8	17.1
A	—	—	3.05
A_1	0	0.1	0.2
b_p	0.25	0.3	0.4
c	0.13	0.15	0.2
θ	0°	—	10°
e	0.5	0.65	0.8
y	—	—	0.10
Z_D	—	0.575	—
Z_E	—	0.825	—
L	0.4	0.6	0.8

3.3 Notes on use

3.3.1 Notes on programming

(1) Processor status register

① **Initializing of processor status register**

Flags which affect program execution must be initialized after a reset.
In particular, it is essential to initialize the T and D flags because they have an important effect on calculations.

● **Reason**

After a reset, the contents of the processor status register (PS) are undefined except for the I flag which is "1".

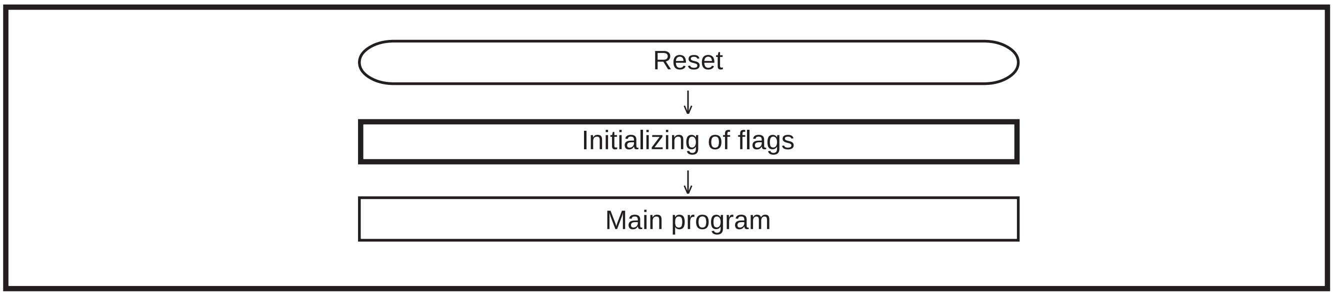


Fig. 3.3.1 Initialization of processor status register

② **How to reference the processor status register**

To reference the contents of the processor status register (PS), execute the **PHP** instruction once then read the contents of (S+1). If necessary, execute the **PLP** instruction to return the PS to its original status.

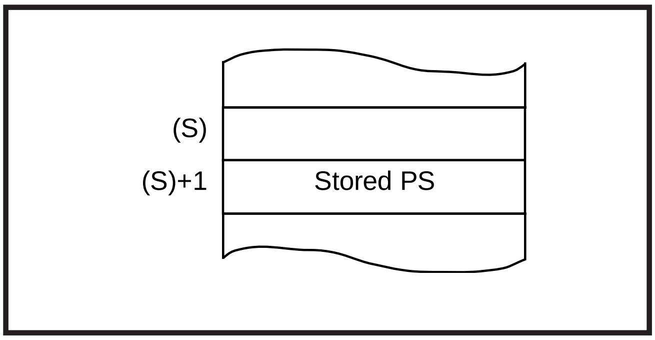


Fig. 3.3.3 Stack memory contents after PHP instruction execution

(2) Decimal calculations

■ Execution of decimal calculations

The **ADC** and **SBC** are the only instructions which will yield proper decimal notation, set the decimal mode flag (D) to "1" with the **SED** instruction. After executing the **ADC** or **SBC** instruction, execute another instruction before executing the **SEC**, **CLC**, or **CLD** instruction.

■ Notes on status flag in decimal mode

When decimal mode is selected, the values of three of the flags in the status register (the N, V, and Z flags) are invalid after a **ADC** or **SBC** instruction is executed.

The carry flag (C) is set to "1" if a carry is generated as a result of the calculation, or is cleared to "0" if a borrow is generated. To determine whether a calculation has generated a carry, the C flag must be initialized to "0" before each calculation. To check for a borrow, the C flag must be initialized to "1" before each calculation.

Set D flag to "1"

↓

ADC or **SBC** instruction

↓

NOP instruction

↓

SEC, **CLC**, or **CLD** instruction

Fig. 3.3.4 Status flag at decimal calculations

(3) Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

(4) JMP instruction

When using the **JMP** instruction in indirect addressing mode, do not specify the last address on a page as an indirect address.

(5) BRK instruction

When the BRK instruction is executed with the following conditions satisfied, the interrupt execution is started from the address of interrupt vector which has the highest priority.

- Interrupt request bit and interrupt enable bit are set to "1".
- Interrupt disable flag (I) is set to "1" to disable interrupt.

(6) Read-modify-write instruction

Do not execute a read-modify-write instruction to the read invalid address (memory and SFR). The read-modify-write instruction operates in the following sequence: read one-byte of data from memory, modify the data, write the data back to original memory. The following instructions are classified as the read-modify-write instructions in the 740 Family.

•Bit management instructions: CLB, SEB
•Shift and rotate instructions: ASL, LSR, ROL, ROR, RRF
•Add and subtract instructions: DEC, INC
•Logical operation instructions (1's complement): COM

Add and subtract/logical operation instructions (ADC, SBC, AND, EOR, and ORA) when T flag = "1" operate in the way as the read-modify-write instruction. Do not execute the read invalid memory and SFR.

[Reason]

When the read-modify-write instruction is executed to read invalid memory and SFR, the instruction may cause the following consequence: the instruction reads unspecified data from the memory due to the read invalid condition. Then the instruction modifies this unspecified data and writes the data to the memory. The result will be random data written to the memory or some unexpected event.

(7) Instruction execution time

Each instruction execution time is obtained from the cycle time of system clock ϕ multiplied by the number of instruction cycles listed in the machine instruction table. Note that the cycle time of system clock ϕ is defined by the system clock division ratio selection bit and the system clock selection bit.

3.3.2 Notes on I/O port

(1) Modifying output data with bit managing instruction

When the port latch of an I/O port is modified with the bit managing instruction **(Note)**, the value of the unspecified bit may be changed.

● **Reason**

I/O ports can be set to input or output mode in a bit unit. When reading or writing are performed to the port Pi (i = 0–7) register, the microcomputer operates as follows.

•Port in input mode
 -Read-access: reads pin's level (The contents of port latch and pin's level are unrelated.)
 -Write-access: writes data to port latch (The contents of port latch and pin's level are unrelated.)

•Port in output mode
 -Read-access: reads port latch (The contents of port latch and pin's level are unrelated.)
 -Write-access: writes data to port latch (The contents of port latch are output from the pin.)

The bit managing instructions are read-modify-write form instructions (refer to "3.3.1 Notes on programming (6)") for reading and writing data by a byte unit.
Therefore, when the bit managing instructions are executed to the port set to input mode, the instruction read the pin's states, modify the specification bit, and then write data to the port latch. At this time, if the contents of the original port latch are different from the pins's level, the contents of the port latch of bit which is not specified by instruction will change.
In addition to this, if the bit managing instructions are executed to the port Pi register in order to setting output data when port Pi is configured as a mixed input and output port, the contents of the port latch of bit in the input mode which is not specified by instruction may change.

Note: Bit managing instructions: SEB instruction, CLB instruction

(2) The port direction registers are write-only registers. Therefore, the following instructions cannot be used to this register:

•LDA instruction
•Memory operation instruction when T flag is "1"
•Instructions operating in addressing mode that modifies direction register
•Bit test instructions such as BBC and BBS
•Bit modification instructions such as CLB and SEB
•Arithmetic instructions using read-modify-write form instructions such as ROR

The LDM, STA instructions etc. are used for setting of the direction register.

(3) Pull-up Operation

When using each port which built in pull-up resistor as an output port, the pull-up control bit of corresponding port becomes invalid, and pull-up resistor is not connected.

● **Reason**

Pull-up control is effective only when each direction register is set to the input mode.

3.3.3 Termination of unused pins

(1) Terminate unused pins

Perform the following wiring at the shortest possible distance (20 mm or less) from microcomputer pins.

①**Output ports**

Open them.

②**Input ports**

Connect each pin to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ.

A for pins whose potential affects to operation modes such as the INTi pin or others, select the V_{CC} pin or the V_{SS} pin according to their operation mode.

③ **I/O ports**

Set the I/O ports for the input mode and connect each pin to V_{CC} or V_{SS} through each resistor of 1 kΩ to 10 kΩ. The port which can select a built-in pull-up resistor can also use the built-in pull-up resistor.

When using the I/O ports as the output mode, open them at “L” or “H”.

- When opening them in the output mode, the input mode of the initial status remains until the mode of the ports is switched over to the output mode by the program after reset. Thus, the potential at these pins is undefined and the power source current may increase in the input mode. With regard to an effects on the system, thoroughly perform system evaluation on the user side.
- Since the direction register setup may be changed because of a program runaway or noise, set direction registers by program periodically to increase the reliability of program.

(2) Termination remarks

■ Input ports

Do not open them.

● **Reason**

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination ② shown on the above.

■ I/0 ports setting as input mode

[1] Do not open in the input mode.

● **Reason**

- The power source current may increase depending on the first-stage circuit.
- An effect due to noise may be easily produced as compared with proper termination ③ shown on the above.

[2] I/O ports :

Do not connect to V_{CC} or V_{SS} directly.

● **Reason**

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur.

[3] I/O ports :

Do not connect multiple ports in a lump to V_{CC} or V_{SS} through a resistor.

● **Reason**

If the direction register setup changes for the output mode because of a program runaway or noise, a short circuit may occur between ports.

3.3.4 Notes on interrupts

(1) Unused interrupts

Set the interrupt enable bit for unused interrupts to “0” (disabled).

(2) Change of relevant register settings

When setting the followings, the interrupt request bit may be set to “1”.

•When switching external interrupt active edge

Related register: •Interrupt edge selection register (address $3A_{16}$)
•Timer X mode register (address 27_{16})
•Timer Y mode register (address 28_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated

Related register: •Interrupt source selection bit of AD control register (bit 6 of address 34_{16})

When not requiring for the interrupt occurrence synchronous with these setting, take the following sequence.

Set the corresponding interrupt enable bit to “0” (disabled) .

↓

Set the interrupt edge select bit, active edge switch bit, or the interrupt source select bit.

↓

NOP (One or more instructions)

↓

Set the corresponding interrupt request bit to “0” (no interrupt request issued).

↓

Set the corresponding interrupt enable bit to “1” (enabled).

Fig. 3.3.5 Sequence of changing relevant register

■ **Reason**

When setting the followings, the interrupt request bit of the corresponding interrupt may be set to “1”.

•When switching external interrupt active edge

Concerned register: INT_0 interrupt edge selection bit (bit 0 of Interrupt edge selection register (address $3A_{16}$))
INT_1 interrupt edge selection bit (bit 1 of Interrupt edge selection register (address $3A_{16}$))
INT_2 interrupt edge selection bit (bit 2 of Interrupt edge selection register (address $3A_{16}$))
$CNTR_0$ active edge switch bit (bit 6 of timer X mode register (address 27_{16}))
$CNTR_1$ active edge switch bit (bit 6 of timer Y mode register (address 28_{16}))

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated.

Concerned register: Interrupt source selection bit (bit 6 of AD control register (address 34_{16}))

(3) Check of interrupt request bit

When executing the **BBC** or **BBS** instruction to an interrupt request bit of an interrupt request register immediately after this bit is set to “0”, take the following sequence.

Set the interrupt request bit to “0” (no interrupt issued)

↓

NOP (one or more instructions)

↓

Execute the **BBC** or **BBS** instruction

Fig. 3.3.6 Sequence of check of interrupt request bit

■ **Reason**

If the BBC or BBS instruction is executed immediately after an interrupt request bit of an interrupt request register is cleared to “0”, the value of the interrupt request bit before being cleared to “0” is read.

3.3.5 Notes on timer

This clause describes notes for the various operation modes of Timer X, Timer Y, Timer 1, Timer 2, and Timer 3.

(1) Timer X

■For all modes

◆When reading and writing to the timer X high-order and low-order registers, be sure to read/write both the timer X high- and low-order registers.
When reading the timer X high-order and low-order registers, read the high-order register first.
When writing to the timer X high-order and low-order registers, write the low-order register first.
The timer X cannot perform the correct operation if the next operation is performed.
•Write operation to the high- or low-order register before reading the timer X low-order register
•Read operation from the high- or low-order register before writing to the timer X high-order register

◆When the operation "writing data only to the latch" is selected by the timer X write control bit (bit 0 of timer X mode register (address 27_{16})) is selected, a value is simultaneously set to the timer X and the timer X latch if the writing in the high-order register and the underflow of timer X are performed at the same timing. Unexpected value may be set in the high-order timer on this occasion.

■Pulse output mode

◆When reading port $P5_4$ (bit 4 of port P5 register (address $0A_{16}$)) in the pulse output mode, the pin state is read instead of the contents of the port latch.

■Real time port function

◆After reset is released, the port P5 direction register is set as the input mode and ports $P5_0$–$P5_7$ functions as regular ports. To use as the RTP function pin, set the corresponding bit of the port P5 direction register to the output mode.

■$CNTR_0$ active edge selection

◆The $CNTR_0$ active edge selection bit (bit 6 of timer X mode register) also effects the active edge of the generation of the $CNTR_0$ interrupt request.

(2) Timer Y

■For all modes

◆When reading and writing to the timer Y high-order and low-order registers, be sure to read/write both the timer Y high- and low-order registers.
When reading the timer Y high-order and low-order registers, read the high-order register first.
When writing to the timer Y high-order and low-order registers, write the low-order register first.
The timer Y cannot perform the correct operation if the next operation is performed.
•Write operation to the high- or low-order register before reading the timer Y low-order register
•Read operation from the high- or low-order register before writing to the timer Y high-order register

■$CNTR_1$ active edge selection

◆The $CNTR_1$ active edge selection bit (bit 6 of timer Y mode register (address 28_{16})) also effects the active edge of the generation of the $CNTR_1$ interrupt request. However, both edges are valid for the request generation regardless of the bit state in the continuous HL pulse-width measurement mode.

(3) Timers 1–3

Set the value of timer in the order of the timer 1 register, the timer 2 register, and the timer 3 register after the count source selection of timer 1 to 3.

<Reason>

•When the count source of timers 1 to 3 is changed, the timer counting value may become arbitrary value because a thin pulse is generated in count input of timer.

•If timer 1 output is selected as the count source of timer 2 or timer 3, when timer 1 is written, the counting value of timer 2 or timer 3 may become undefined value because a thin pulse is generated in timer 1 output.

(4) Timer 2

If the value is written in latch only, a value is simultaneously set to the timer 2 and the timer 2 latch when the writing in the high-order register and the underflow of timer 2 are performed at the same timing.

(5) All timers

■The count source for timers is effected by system clock ϕ which is selected by the system clock selection bit (bit 7 of CPU mode register (address $3B_{16}$)).

■Set the timer which is not used as follows:

•Stop the count (when using a timer with stop control)

•Set “0” to the corresponding interrupt enable bit

3.3.6 Notes on serial I/O1

(1) Writing to baud rate generator (BRG)

Write data to BRG while the transmission and reception operations are stopped.

(2) Setting procedure when using serial I/O1 transmit interrupt

When the serial I/O1 transmit interrupt is used, take the following sequence.

①Set the serial I/O1 transmit interrupt enable bit (bit 3 of interrupt control register 1 (address $3E_{16}$)) to “0” (disabled).

②Set the transmit enable bit (bit 4 of serial I/O1 control register (address $1A_{16}$)) to “1”.

③Set the serial I/O1 transmit interrupt request bit (bit 3 of interrupt request register 1 (address $3C_{16}$)) to “0” (no interrupt request issued) after 1 or more instruction has executed.

④Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

<Reason>

When the transmission enable bit is set to “1”, the transmit buffer empty flag (bit 0 of serial I/O1 status register (address 19_{16})) and the transmit shift register completion flag (bit 2 of serial I/O1 status register) are set to “1”.

Therefore, the serial I/O1 transmit interrupt request bit is set to “1” regardless of the state of the transmit interrupt source selection bit (bit 3 of serial I/O1 control register).

(3) Data transmission control with referring to transmit shift register completion flag

After the transmit data is written to the transmit buffer register (address 18_{16}), the transmit shift register completion flag changes from “1” to “0” with a delay of 0.5 to 1.5 shift clocks. When data transmission is controlled with referring to the flag after writing the data to the transmit buffer register, note the delay.

(4) Setting serial I/O1 control register again

Set the serial I/O1 control register again after the transmission and the reception circuits are reset by setting both the transmit enable bit and the receive enable bit to “0”.

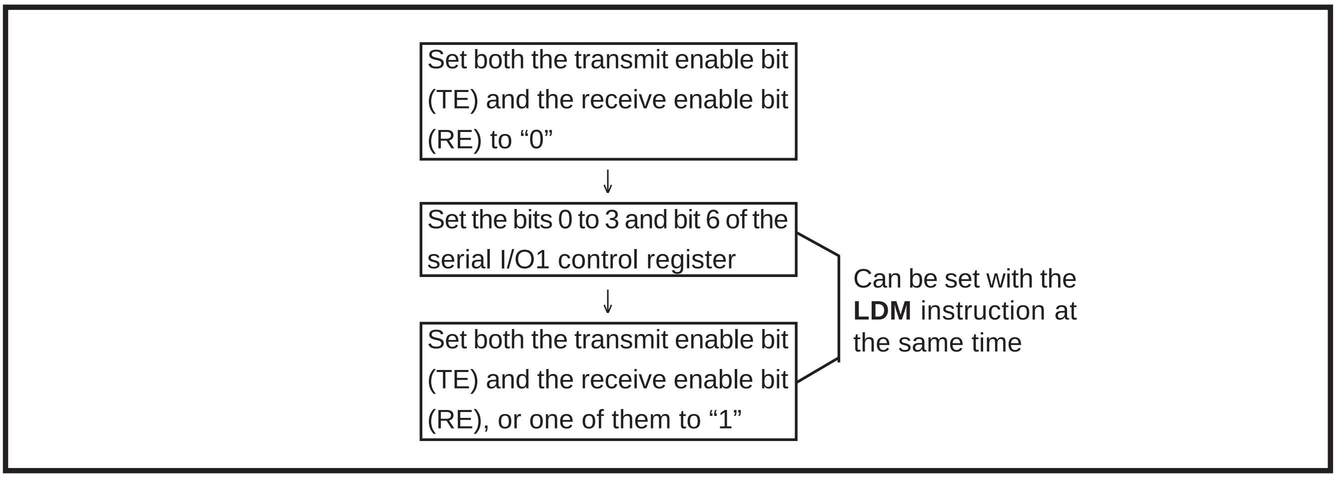


Fig. 3.3.7 Sequence of setting serial I/O1 control register again

(5) Pin state after transmit completion

The TxD pin holds the state of the last bit of the transmission after transmission completion. When the internal clock is selected for the transmit clock in the clock synchronous serial I/O mode, the S_{CLK1} pin holds “H”.

(6) Serial I/O1 enable bit during transmit operation

When the serial I/O1 enable bit (bit 7 of serial I/O1 control register) is set to “0” (serial I/O1 disabled) when data transmission is in progress, the transmission progress internally. However, the external data transfer is terminated because the pins become regular I/O ports. In addition to this, when data is written to the transmission buffer register, data transmission is started internally. When the serial I/O1 enable bit is set to “1”, the transmission is output to the TxD pin in the middle of the transfer.

(7) Transmission control when external clock is selected

When an external clock is used as the synchronous clock for data transmission, set the transmit enable bit to “1” at “H” of the S_{CLK1} input level. Also, write the transmit data to the transmit buffer register at “H” of the S_{CLK1} input level.

(8) Receive operation in clock synchronous serial I/O mode

When receiving data in the clock synchronous serial I/O mode, set not only the receive enable bit but also the transmit enable bit to “1”. Then write dummy data to the transmission buffer register. When the internal clock is selected as the synchronous clock, the synchronous clock is output at this point and the receive operation is started. When the external clock is selected as the transfer clock, the serial I/O becomes ready for data receive at this point and, when the external clock is input to the clock input pin, the receive operation is started. The $P4_5$/TxD pin outputs the dummy data written in the transmission buffer register.

(9) Transmit and receive operation in clock synchronous serial I/O mode

When stopping transmitting and receiving operations in the clock synchronous serial I/O mode, set the receive enable bit and the transmit enable bit to “0” simultaneously. If only one of them is stopped the receive or transmit operation may loose synchronization, causing a bit slippage.

3.3.7 Notes on serial I/O2

(1) Switching synchronous clock

When switching the synchronous clock by the serial I/O2 synchronous clock selection bit (bit 6 of serial I/O2 control register (address $1D_{16}$)), initialize the serial I/O2 counter (write data to serial I/O2 register (address $1F_{16}$)).

(2) Notes when selecting external clock

When an external clock is selected as the synchronous clock, the S_{OUT2} pin holds the output level of D_7 after transmission is completed. However, if the clock is input to the serial I/O continuously, the serial I/O2 register continue the shift operation and output data from the S_{OUT2} pin continuously. A write operation to the serial I/O2 register must be performed when the S_{CLK21} pin is “H”.

When the internal clock is selected as the synchronous clock, the S_{OUT2} pin holds the high-impedance state after transmission.

3.3.8 Notes on PWM output circuit

●"L" level output before starting PWM output

When at least one of two is set to "1" when both the PWM_0 function enable bit and the PWM_1 function enable bit are "0", "L" level is output from the corresponding PWM pin during the period shown below. Then, PWM output is started from "H" level.

•Count source selection bit = "0", where n is the value set in the prescaler

$$\frac{n + 1}{2 \cdot f(X_{IN})} \text{ sec.}$$

•Count source selection bit = "1", where n is the value set in the prescaler

$$\frac{n + 1}{f(X_{IN})} \text{ sec.}$$

●Change of PWM output

When the PWM prescaler and the PWM register are changed during PWM output, the PWM waveforms corresponding to updated data will be output from the next repetitive cycle. Figure 3.3.8 shows the change of PWM output.

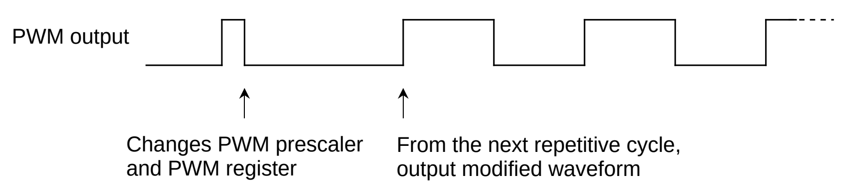


Fig. 3.3.8 Change of PWM output

3.3.9 Notes on A/D converter

(1) Analog input pin

Make the signal source impedance for analog input low, or equip an analog input pin with an external capacitor of 0.01 μF to 1 μF. Further, be sure to verify the operation of application products on the user side.

● **Reason**

An analog input pin includes the capacitor for analog voltage comparison. Accordingly, when signals from signal source with high impedance are input to an analog input pin, charge and discharge noise generates. This may cause the A/D conversion precision to be worse.

(2) Analog power source input pin AVss

The AVss pin is an analog power source input pin. Regardless of using the A/D conversion function or not, connect it as following :

• AVss : Connect to the Vss line

● **Reason**

If the AVss pin is opened, the microcomputer may have a failure because of noise or others.

(3) Reference voltage input pin V_{REF}

Connect an approximately 1000 pF capacitor across the AVss pin and the V_{REF} pin. Besides, connect the capacitor across the V_{REF} pin and the AVss pin at equal length as close as possible.

(4) Clock frequency during A/D conversion

Use the A/D converter in the following conditions:

• Select X_{IN}-X_{OUT} as system clock ϕ by the system clock selection bit (bit 7 of CPU mode register (address $3B_{16}$)). When selecting X_{CIN}-X_{COUT} as system clock ϕ, the A/D conversion function cannot be used.

• $f(X_{IN})$ is 500 kHz or more.

• Do not execute the STP or WIT instruction during A/D conversion.

● **Reason**

The comparator consists of a capacity coupling, and a charge of the capacity will be lost if the clock frequency is too low. This may cause the A/D conversion precision to be worse.

(5) When the falling edge is input to the ADT pin during A/D conversion at the time of A/D external trigger effective, the conversion processing is interrupted and the A/D conversion starts again. In addition, even if “0” is set to the AD conversion completion bit by the program during A/D conversion, re-conversion is not performed but the original conversion is continued.

(6) The A/D converter will not operate normally if one of the following operation is applied during the A/D conversion:

•Writing to CPU mode register
•Writing to AD control register
•Executing the STP instruction and WIT instruction

3.3.10 Notes on D/A converter

(1) Pin states at reset

The $P5_6/DA_1$ pin and the $P5_7/ADT/DA_2$ pin go to high impedance state at reset.

(2) Connecting low-impedance device

The DAi output pin have no buffer, so connect an external buffer when driving a low-impedance load.

(3) Reference voltage input pin V_{REF}

•When the $P5_6/DA_1$ pin and the $P5_7/ADT/DA_2$ pin are used as DAi output pins, the Vcc level is recommended for the applied voltage to the V_{REF} pin. When the voltage below Vcc level is applied, the D/A conversion accuracy may be worse.

•Connect an approximately 1000 pF capacitor across the AVss pin and the V_{REF} pin. Besides, connect the capacitor across the V_{REF} pin and the AVss pin at equal length as close as possible.

3.3.11 Notes on LCD drive control circuit

(1) Count source for LCDCK

The LCDCK count source selection bit (bit 7 of LCD mode register (address 39_{16})) is set to "0" after reset, selecting f(X_{CIN})/32. The sub clock has stopped after reset. Therefore, turn on LCD after starting the oscillation and stabilizing the oscillation. Select the LCDCK count source after the corresponding clock source becomes stable.

(2) STP instruction

When executing the STP instruction, execute the STP instruction after setting the LCD enable bit to "0". If the STP instruction is executed during LCD lighting, direct-current voltage will be applied to the LCD panel.

(3) When not using LCD

When not using an LCD, leave the LCD segment and common pins open. Connect the V_{L1} pin to Vss, and the V_{L2} and V_{L3} pins to Vcc.

(4) Using voltage multiplier circuit

When using the voltage multiplier, apply the limit voltage or less to the V_{L1} pin, then set the voltage multiplier control bit to "1" (enabled). If above the limit voltage is applied to the V_{L1} pin, current may flow in the voltage multiplier circuit at the time of the voltage multiplier circuit operation start. For the limit value, refer to "Electrical characteristics".

When not using the voltage multiplier, set the LCD output enable bit to "1", then apply proper voltage to the LCD power input pins (V_{L1}–V_{L3}).

When the LCD output enable bit is set to "0" (disabled), the Vcc voltage is applied to the V_{L3} pin inside of this microcomputer.

(5) LCD drive power supply

Power supply capacitor may be insufficient with the division resistance for LCD power supply, and the characteristic of the LCD panel. In this case, there is the method of connecting the bypass capacitor about 0.1–0.33 μF to V_{L1}–V_{L3} pins. The example of a strengthening measure of the LCD drive power supply is shown in Figure 3.3.9.

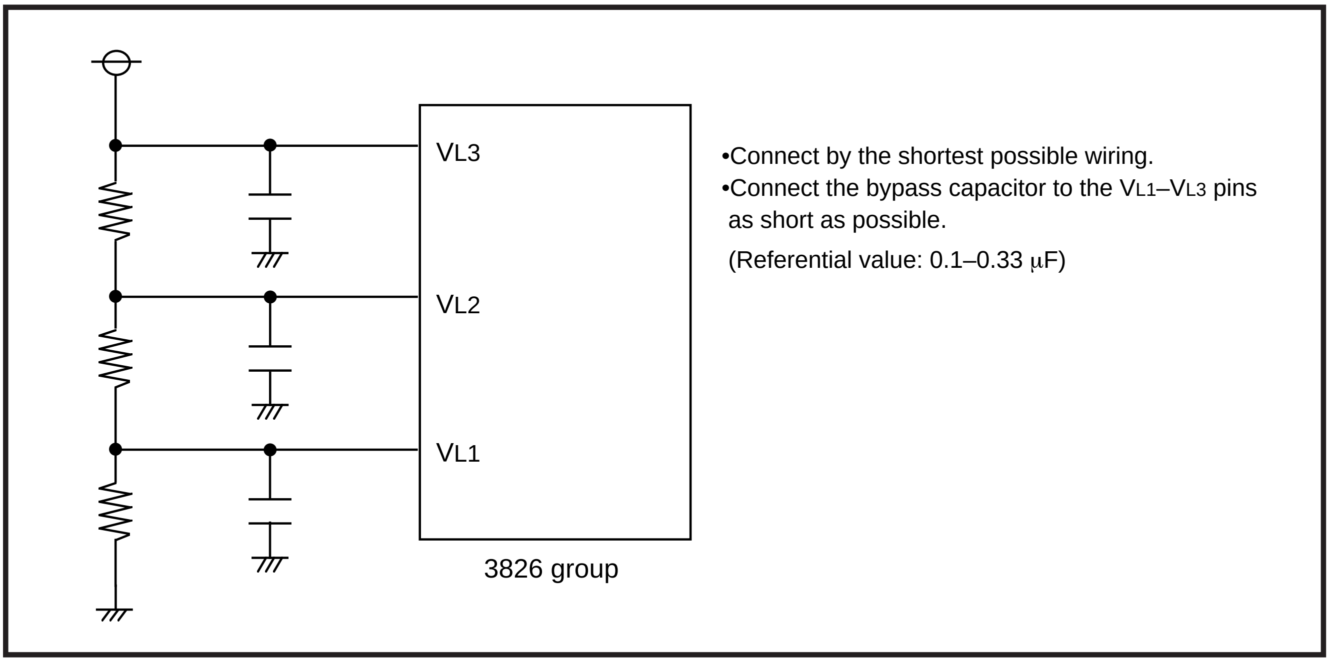


Fig. 3.3.9 Strengthening measure example of LCD drive power supply

(6) Data setting to LCD display RAM

When writing a data into the LCD display RAM during LCD being turned ON (LCD enable bit = “1”), write the confirmed data. Do not write temporarily on the LCD display RAM because this might cause the LCD display flickering. Figure 3.3.10 shows the write procedure for LCD display RAM when LCD is on.

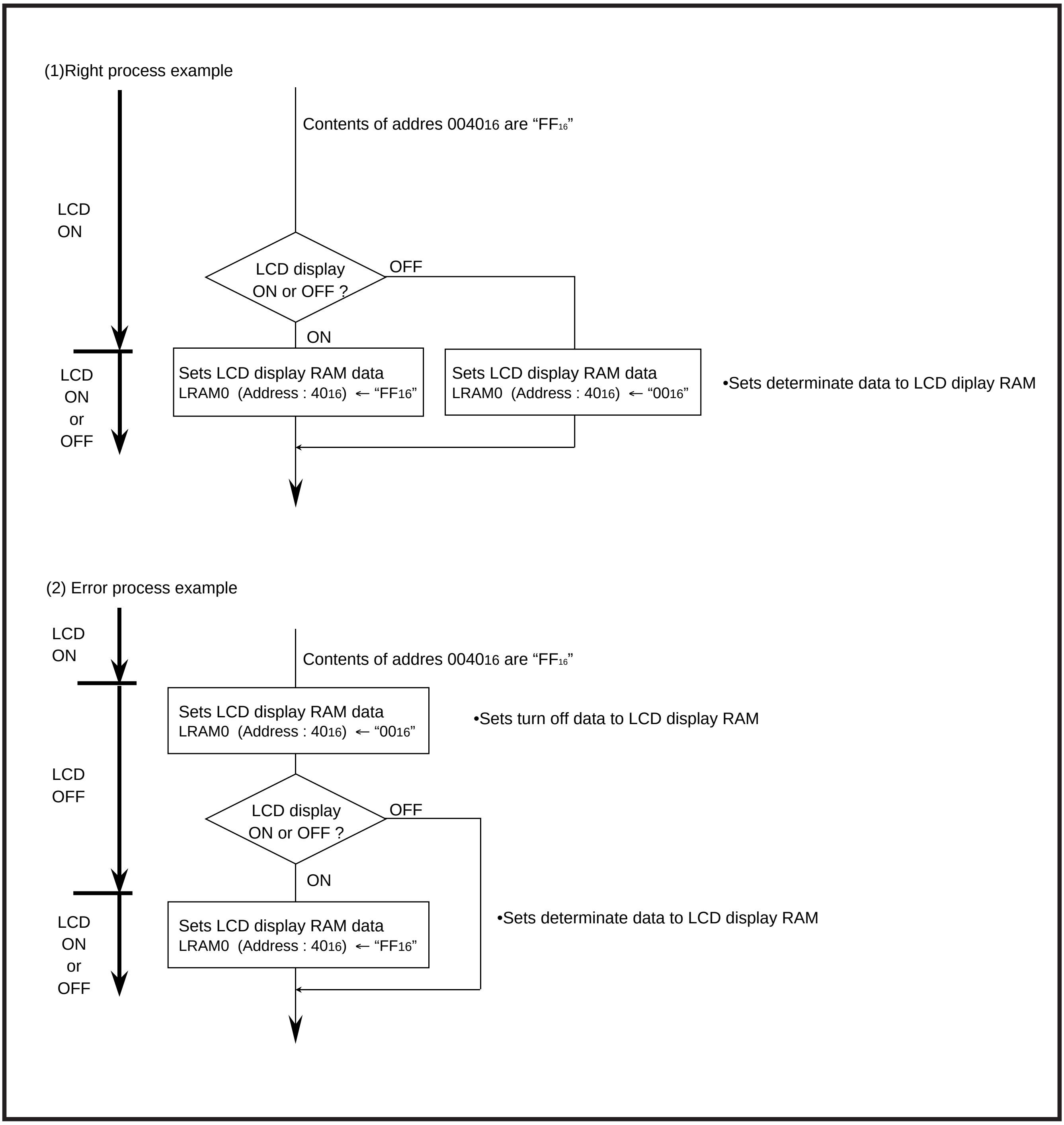


Fig. 3.3.10 Write procedure for LCD display RAM when LCD is on

3.3.12 Notes on watchdog timer

(1) The watchdog timer is operating during the wait mode. Write data to the watchdog timer control register to prevent timer underflow.

(2) The watchdog timer stops during the stop mode. However, the watchdog timer is running during the clock stabilization period and the watchdog timer control register must be written just before executing the STP instruction.

(3) The count source of the watchdog timer is affected by the system clock ϕ selected by the system clock selection bit (bit 7 of CPU mode register (address $3B_{16}$)).

3.3.13 Notes on reset circuit

(1) Reset input voltage control

Make sure that the reset input voltage is less than 0.2 Vcc for Vcc(min).

(2) Countermeasures for reset signal slow rising

In case where the $\overline{\text{RESET}}$ signal rise time is long, connect a ceramic capacitor or others across the $\overline{\text{RESET}}$ pin and the Vss pin. Use a 1000 pF or more capacitor for high frequency use. When connecting the capacitor, note the following:

•Make the length of the wiring which is connected to a capacitor as short as possible.

•Be sure to verify the operation of application products on the user side.

●Reason

If the several nanosecond or several ten nanosecond impulse noise enters the $\overline{\text{RESET}}$ pin, it may cause a microcomputer failure.

(3) Port state immediately after reset

Table 3.3.1 shows the each pin state during $\overline{\text{RESET}}$ pin is "L".

Table 3.3.1 Each pin state during $\overline{\text{RESET}}$ pin is "L"

Pin name	Pin state
P0, P1 (SEG_{26}–SEG_{39})	Input mode (with pull-up)
P2, $P4_1$–$P4_7$, P5, P6	Input mode (high-impedance)
P3 (SEG_{18}–SEG_{25})	Pulled up to Vcc level
$P7_0$	High-impedance
$P4_0$, $P7_1$–$P7_7$	Input mode (high-impedance)
SEG_0–SEG_{17}	Vcc level output
COM_0–COM_3	Vcc level output

3.3.14 Notes on clock generating circuit

●Mode transition

Both the main clock (X_{IN}-X_{OUT}) and sub-clock (X_{CIN}-X_{COUT}) need time for the oscillations to stabilize. The mode transition between middle-/high-speed and low-speed mode must be performed after the corresponding clock becomes stable. The sub-clock, needs extra time to stabilize particularly when executing operations after power-on and stop mode. The main and sub clocks require the following condition for mode transition.

$$f(X_{IN}) > 3 \times f(X_{CIN})$$

3.3.15 Notes on standby function

(1) Once the STP instruction is disabled by the STP instruction disable bit (bit 6 of watchdog timer control register (address 37_{16})), the microcomputer cannot be return to the STP instruction enable state.

(2) When using the standby function, note the following.
The power dissipation may increase depending on functions and pin states.
Take the following countermeasures for reduce the power dissipation.

■Countermeasures for reduce power dissipation

•Input ports: Fix to “H” or “L” externally
•Output ports: Fix to level that avoid leak-current.
(Example: Fix the pin to “H“ when the circuit which current flows and LED turns on at “L” output.)
•A/D input pins: Fix to “H” or “L” externally
•PWMi function enable bits (bits 1 and 2 of PWM control register (address $2B_{16}$)): “0”
•LCD enable bit: “0”
•Complete A/D conversion
(Confirm the AD conversion completion bit (bit 3 of AD control register (address 34_{16})) is “1”)
•V_{REF} input switch bit (bit 4 of AD control register): “0”
•D/Ai conversion register (addresses 32_{16}, 33_{16}): “00_{16}”

(3) **When using stop mode**

■Operation after restoration by occurrence of interrupt request

•All the timer 123 mode register bits are automatically set to “0” except for bit 4.
•When an interrupt request occurs in the stop mode, the stop mode is released and the clock stopped by STP starts the oscillation. The oscillation stabilizing time of main clock is secured to restoration from the stop mode when both the main and sub clocks are oscillating and the main clock is set for the system clock when executing the STP instruction. Note that the oscillation of sub clock may not be stable after main clock oscillation being stable.

■When LCD display

Execute the STP instruction after turning LCD to OFF by setting the LCD enable bit (bit 3 of LCD mode register (address 39_{16})) to “0”. If the STP instruction is executed while the LCD is ON, direct voltage will be applied to the LCD panel.

■Watchdog timer

The watchdog timer stops during the stop mode but operates during the oscillation stabilizing time. Therefore, the watchdog timer control register must be written just before executing the STP instruction to prevent its underflow.

(4) When using wait mode

■Restoration by reset input

When the sub clock is selected as the system clock and the main clock is stopped at the time WIT instruction is executed, if the $\overline{RESET}$ pin input level is set to “L”, the sub clock oscillation stops and the main clock oscillation starts. Oscillation is unstable at first and requires an oscillation stabilizing time. Retain the $\overline{RESET}$ pin input level at “L” until the oscillation is stabilized. After the oscillation has stabilized, retain the $\overline{RESET}$ pin at “L” for 2 μs or more in order to set the internal reset state.

■Watchdog timer

The watchdog timer operates during the wait mode. The watchdog timer control register must be written to prevent its underflow.

REVISION HISTORY	3826 Group (One Time PROM version) Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep 06, 2006	–	First edition issued
			This datasheet describes only 3826 Group One Time PROM version (60K version of ROM).
			The change point from past 3826 Group datasheet (MEJ02B0083-0102Z) is described to the revision history as your information though it is a first edition.
		–	Improvement term union of sentence expressions.
		–	Terms are united. (Union terms: A/D converter, D/A converter, serial interface, etc.)
			Package type: 100P6S-A → PRQP0100JB-A, 100P6Q-A → PLQP0100KB-A
		–	DESCRIPTION: Revised for One Time PROM and EPROM vertions.
		1	FEATURES: Power source voltage, power dissipation reviced and 10-bit A/D mode added.
			APPLICATIONS: cordless phone, wireless application, household appliances, added
		2	Fig. 2 and Fig.3 Pin configurations: One Time PROM version name described.
		6	Fig. 4 Part numbering: Description for RAM size added.
		7	Fig. 5 Memory expansion plan: One Time PROM and EPROM versions added.
			Table 3 Support products: One Time PROM and EPROM versions added.
		13	Fig. 10 SFR:
			0014_{16}: Reserved area → AD convertion low-order register (ADL)
			0035_{16}: AD conversion register (AD) → AD conversion high-order register (ADH)
		14	Fig. 11 Structure of port P0 direction register, port P1 direction register added.
			Fig. 12 Structure of port P3 output control register added
		25	Fig. 21 Structure of key input control register added
		35	● Serial I/O2 Operating: added
		38	A/D CONVERTER: AD → ADH, ADL
			Fig. 38 Structure of A/D converter-related registers: added.
		39	Fig. 39 Read of AD conversion register: added.
			Fig. 40 A/D converter block diagram: AD convertion register → ADL, ADH
		43	Fig. 45 Equivalent connection circuit of D/A converter added.
		46	Fig. 48 Example of circuit at each bias revised.
		52	Fig. 56 Example of reset circuit revised.
		53	Fig. 58 AD conversion low-order register (0014_{16}) added.
		54	CLOCK GENERATING CIRCUIT: Underline part changed and ( ) added
			<u>A feed-back resistor exists on-chip</u> (An external feed-back resistor may be needed depending on conditions.). However, an external feed-back resistor is needed between X_{CIN} and X_{COUT} since a resistor does not exist between them.
			Fig. 59 Oscillator circuit: Rd and note added
		55	Fig. 61 Clock generating circuit block diagram: note 2 added
		56	Fig. 62d State transitions of system clock: revised

REVISION HISTORY	3826 Group (One Time PROM version) Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Sep 06, 2006	58, 59	NOTE ON USE: Countermeasures Against Noise added
		60	NOTE ON USE: Power Source Voltage: added
			DATA REQUIRED FOR MASK ORDERS: eliminated
		61 to 68	Ratings of One Time PROM version described.
		69	PACKAGE OUTLINE: changed
		77 to 88	3.3 Notes on use: added

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