100V Constant-Current and Constant-Voltage Controller with Dual Current Sense

FEATURES

- **3000:1 True Color PWM™ Dimming**
- **Wide Input Voltage Range: 6V to 100V**
- **Current Monitoring Up to 100V**
- **High Side PMOS Disconnect and PWM Switch Driver**
- Constant-Current and Constant-Voltage Regulation
- Dual Current Sense Amplifiers with Reporting
- C/10 Detection for Battery and SuperCap Charging
- Linear Current Sense Threshold Programming
- Short-Circuit Protection
- Adjustable Frequency: 100kHz to 1MHz
- Frequency Synchronization
- Programmable Open LED Protection with $\overline{\text{VMODE}}$ Flag
- Programmable Undervoltage Lockout with Hysteresis
- Soft-Start with Programmable Fault Restart Timer
- Low Shutdown Current: <1µA
- Available in 28-Lead TSSOP Package

APPLICATIONS

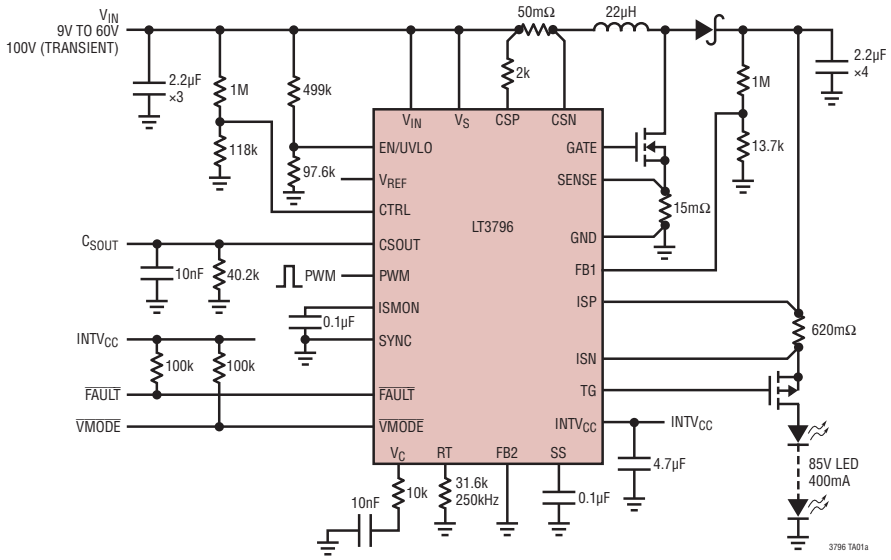
- High Power LED, High Voltage LED
- Battery and SuperCap Chargers
- Accurate Current Limited Voltage Regulators

DESCRIPTION

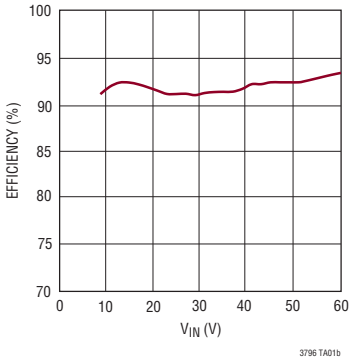
The LT®3796 is a DC/DC controller designed to regulate a constant-current or constant-voltage and is ideal for driving LEDs. It drives a low side external N-channel power MOSFET from an internal regulated 7.7V supply. The fixed frequency and current mode architecture result in stable operation over a wide range of supply and output voltages. Two ground referred voltage FB pins serve as the input for several LED protection features, and also allow the converter to operate as a constant-voltage source. The LT3796 features a programmable threshold output sense amplifier with rail-to-rail common mode range. The LT3796 also includes a separate high side current sensing amplifier that is gain configurable with two resistors. The TG pin inverts and level shifts the PWM signal to drive the gate of the external PMOS. The PWM input provides LED dimming ratios of up to 3000:1, and the CTRL input provides additional analog dimming capability.

TYPICAL APPLICATION

Boost LED Driver with Input Current Monitor



Efficiency vs V_{IN}

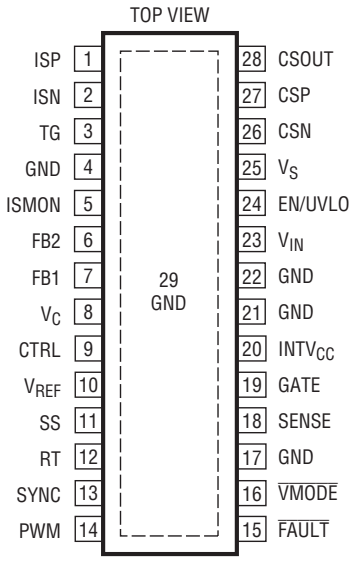


ABSOLUTE MAXIMUM RATINGS

(Note 1)

V_{IN}, V_S 100V
EN/UVLO 100V
ISP, ISN 100V
TG, GATE ..... Note 3
CSP, CSN 100V
V_S - CSP, V_S - CSN ..... –0.3V to 4V
$INTV_{CC}$ (Note 2) ..... 8.6V, V_{IN} + 0.3V
PWM, $\overline{VMODE}$, $\overline{FAULT}$ 12V
FB1, FB2, SYNC 8V
CTRL 15V
SENSE 0.5V
ISMON, CSOUT 5V
V_C, V_{REF}, SS 3V
RT 2V
Operating Junction Temperature Range (Note 4)
LT3796E/LT3796I ..... –40 to 125°C
LT3796H ..... –40 to 150°C
Storage Temperature Range ..... –65 to 150°C

PIN CONFIGURATION



FE PACKAGE
T_{JMAX} = 150°C, θ_{JA} = 30°C/W, θ_{JC} = 10°C/W
EXPOSED PAD (PIN 29) IS GND, MUST BE SOLDERED TO PCB

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LT3796EFE#PBF	LT3796EFE#TRPBF	LT3796FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3796IFE#PBF	LT3796IFE#TRPBF	LT3796FE	28-Lead Plastic TSSOP	–40°C to 125°C
LT3796HFE#PBF	LT3796HFE#TRPBF	LT3796FE	28-Lead Plastic TSSOP	–40°C to 150°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
For more information on tape and reel specifications, go to: http://www.linear.com/tapeandreel/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 24V, EN/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN} Minimum Operating Voltage	V_{IN} Tied to $INTV_{CC}$				6	V
V_{IN} Shutdown I_Q	EN/UVLO = 0V, PWM = 0V EN/UVLO = 1.15V, PWM = 0V				1 12	µA µA
V_{IN} Operating I_Q (Not Switching)	R_T = 82.5k to GND, FB1 = 1.5V			2.5	3	mA
V_{REF} Voltage	–100µA ≤ I_{REF} ≤ 10µA	●	1.97	2.015	2.06	V
V_{REF} Pin Line Regulation	6V < V_{IN} < 100V			1.5		m%/V
V_{REF} Pin Load Regulation	–100µA < I_{REF} < 0µA			10		m%/µA
SENSE Current Limit Threshold		●	100	113	125	mV
SENSE Input Bias Current	Current Out of Pin			60		µA
SS Sourcing Current	SS = 0V			28		µA
SS Sinking Current	ISP – ISN = 1V, SS = 2V			2.8		µA
Error Amplifier						
Full Scale LED Current Sense Threshold ($V_{(ISP-ISN)}$)	ISP = 48V, CTRL ≥ 1.2V ISP = 0V, CTRL ≥ 1.2V	● ●	243 243	250 250	257 257	mV mV
9/10th LED Current Sense Threshold ($V_{(ISP-ISN)}$)	CTRL = 1V, ISP = 48V CTRL = 1V, ISP = 0V	● ●	220 220	225 225	230 230	mV mV
1/2 LED Current Sense Threshold ($V_{(ISP-ISN)}$)	CTRL = 0.6V, ISP = 48V CTRL = 0.6V, ISP = 0V	● ●	119 119	125 125	131 131	mV mV
1/10th LED Current Sense Threshold ($V_{(ISP-ISN)}$)	CTRL = 0.2V, ISP = 48V CTRL = 0.2V, ISP = 0V	● ●	16 16	25 25	32 32	mV mV
ISP/ISN Current Monitor Voltage (V_{ISMON})	$V_{(ISP-ISN)}$ = 250mV, ISP = 48V, –50µA < I_{ISMON} < 0 µA $V_{(ISP-ISN)}$ = 250mV, ISP = 0V, –50µA < I_{ISMON} < 0 µA	● ●	0.96 0.96	1 1	1.04 1.04	V V
ISP/ISN Over Current Protection Threshold ($V_{(ISP-ISN)}$)	ISN = 48V ISN = 0V	● ●	360 360	375 375	390 390	mV mV
CTRL Input Bias Current	Current Out of Pin, CTRL = 1.2V			50	200	nA
ISP/ISN Current Sense Amplifier Input Common Mode Range			0		100	V
ISP/ISN Input Current Bias Current (Combined)	PWM = 5V (Active), ISP = 48V PWM = 0V (Standby), ISP = 48V			700 0	 0.1	µA µA
ISP/ISN Current Sense Amplifier g_m	$V_{(ISP-ISN)}$ = 250mV			400		µs
V_C Output Impedance				2000		kΩ
V_C Standby Input Bias Current	PWM = 0V		–20		20	nA
FB1, FB2 Regulation Voltage (V_{FB})	ISP = ISN = 48V ISP = ISN = 48V	●	1.230 1.238	1.250 1.250	1.270 1.264	V V
FB1 Amplifier g_m			800	1000	1200	µS
FB2 Amplifier g_m			130	170	210	µS
FB1, FB2 Pin Input Bias Current	FB = V_{FB}			100	200	nA
FB1 Open LED Threshold	$\overline{VMODE}$ Falling, ISP = ISN = 48V		V_{FB} – 70mV	V_{FB} – 60mV	V_{FB} – 50mV	V
C/10 Comparator Threshold ($V_{(ISP-ISN)}$)	$\overline{VMODE}$ Falling, FB1 = 1.5V, ISP = 48V $\overline{VMODE}$ Falling, FB1 = 1.5V, ISN = 0V			25 25		mV mV
FB1 Overvoltage Threshold	$\overline{FAULT}$ Falling		V_{FB} + 35mV	V_{FB} + 50mV	V_{FB} + 60mV	V
FB2 Overvoltage Threshold	TG Rising		V_{FB} + 35mV	V_{FB} + 50mV	V_{FB} + 60mV	V
V_C Current Mode Gain ($\Delta V_{VC}/\Delta V_{SENSE}$)				4.2		V/V

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 24V, EN/UVLO = 24V, CTRL = 2V, PWM = 5V, unless otherwise noted.

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Current Sense Amplifier (CSA)						
Power Supply Voltage Range (V_S)		●	3		100	V
CSA Input Voltage Common Mode Range (V_{CSP} and V_{CSN})		●	2.5		100	V
CSOUT Maximum Output Current	CSOUT = 10kΩ to GND	●			200	µA
Input Voltage Offset ($V_{(CSP-CSN)}$)	V_{SNS} = 100mV, V_S = 48V (Note 5)	●	–3	0	3	mV
CSP, CSN Input Bias Current	V_{SNS} = 0mV, R_{IN1} = R_{IN2} = 1k (Note 5)			100		nA
CSP, CSN Input Current Offset	V_{SNS} = 0mV, R_{IN1} = R_{IN2} = 1k (Note 5)			0		nA
V_S Supply Current	V_S = 48V			80		µA
Input Step Response (to 50% of Output Step)	ΔV_{SENSE} = 100mV Step, R_{IN1} = R_{IN2} = 1k, R_{OUT} = 10k			1		µs
Linear Regulator						
$INTV_{CC}$ Regulation Voltage		●	7.4	7.7	8	V
Dropout (V_{IN}– $INTV_{CC}$)	I_{INTVCC} = –20mA, V_{IN} = 6V			400		mV
$INTV_{CC}$ Current Limit	V_{IN} = 100V, $INTV_{CC}$ = 6V V_{IN} = 12V, $INTV_{CC}$ = 6V		20 85			mA mA
$INTV_{CC}$ Shutdown Bias Current if Externally Driven to 7V	EN/UVLO = 0V, $INTV_{CC}$ = 7V			10		µA
$INTV_{CC}$ Undervoltage Lockout			3.8	4	4.1	V
$INTV_{CC}$ Undervoltage Lockout Hysteresis				150		mV
Oscillator						
Switching Frequency	R_T = 82.5k R_T = 19.6k R_T = 6.65k	● ● ●	85 340 900	105 400 1000	125 480 1150	kHz kHz kHz
Minimum Off-Time	(Note 6)			190		ns
Minimum On-Time	(Note 6)			210		ns
LOGIC Input/Outputs						
PWM Input Threshold Rising		●	0.96	1	1.04	V
PWM Pin Bias Current				10		µA
EN/UVLO Threshold Voltage Falling		●	1.185	1.220	1.250	V
EN/UVLO Rising Hysteresis				20		mV
EN/UVLO Input Low Voltage	I_{VIN} Drops Below 1µA		0.4			V
EN/UVLO Pin Bias Current Low	EN/UVLO = 1.15V		2.5	3	3.8	µA
EN/UVLO Pin Bias Current High	EN/UVLO = 1.30V			40	200	nA
$\overline{VMODE}$ OUTPUT Low	$I_{\overline{VMODE}}$ = 0.5mA				300	mV
$\overline{FAULT}$ OUTPUT Low	$I_{\overline{FAULT}}$ = 0.5mA				300	mV
SYNC Pin Resistance to GND				40		kΩ
SYNC Input Low Threshold			0.4			V
SYNC Input High Threshold					1.5	V

ELECTRICAL CHARACTERISTICS

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PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Gate Driver						
t_r NMOS GATE Driver Output Rise Time	C_L = 3300pF, 10% to 90%			20		ns
t_f NMOS GATE Driver Output Fall Time	C_L = 3300pF, 10% to 90%			18		ns
NMOS GATE Output Low (V_{OL})					0.05	V
NMOS GATE Output High (V_{OH})			$INTV_{CC}$ – 0.05			V
t_r Top GATE Driver Output Rise Time	C_L = 300pF			50		ns
t_f Top GATE Driver Output Fall Time	C_L = 300pF			100		ns
Top Gate On Voltage (V_{ISP}-V_{TG})	ISP = 48V			7	8	V
Top Gate Off Voltage (V_{ISP}-V_{TG})	PWM = 0V, ISP = 48V			0	0.3	V

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: Operating maximum for $INTV_{CC}$ is 8V.

Note 3: Do not apply a positive or negative voltage source to TG and GATE pins, otherwise permanent damage may occur.

Note 4: The LT3796E is guaranteed to meet specified performance from 0°C to 125°C. Specifications over the –40°C to 125°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LT3796I is guaranteed to meet performance specifications over the –40°C to 125°C operating temperature range. The LT3796H is guaranteed over the full –40°C to 150° C operating junction temperature range. High junction temperatures degrade operating lifetimes. Operating lifetime is derated at junction temperatures greater than 125°C.

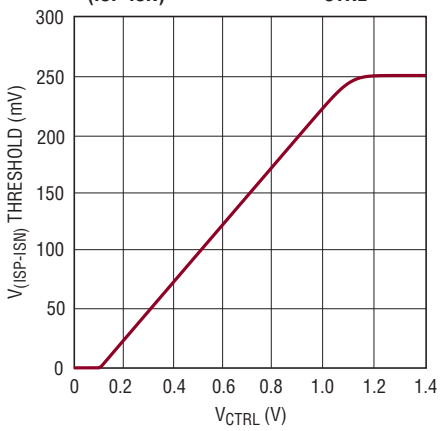
Note 5: Measured in servo. See Figure 9 for details.

Note 6: See Duty Cycle Considerations in the Applications Information section.

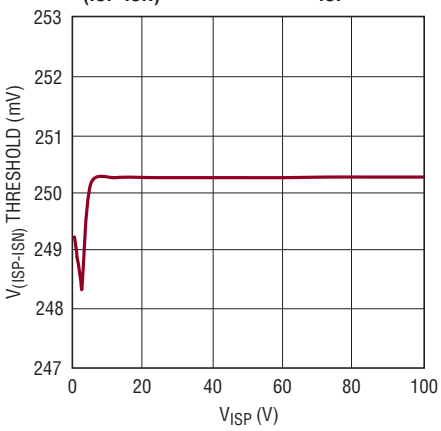
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

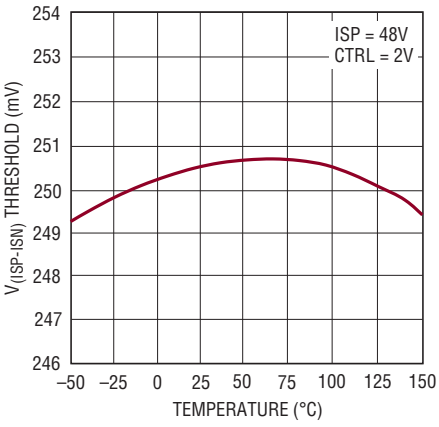
$V_{(ISP-ISN)}$ Threshold vs V_{CTRL}



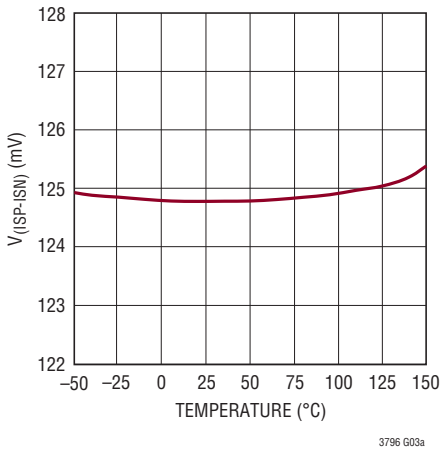
$V_{(ISP-ISN)}$ Threshold vs V_{ISP}



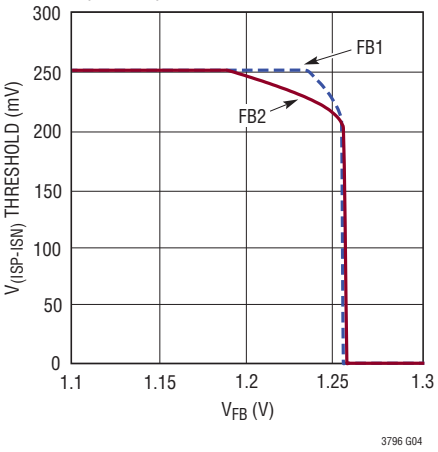
$V_{(ISP-ISN)}$ Full-Scale Threshold vs Temperature



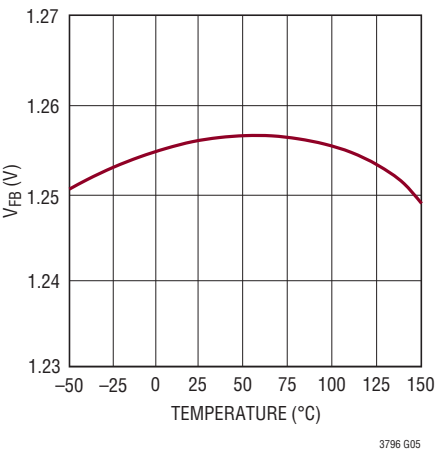
$V_{(ISP-ISN)}$ Threshold at CTRL = 0.6V vs Temperature



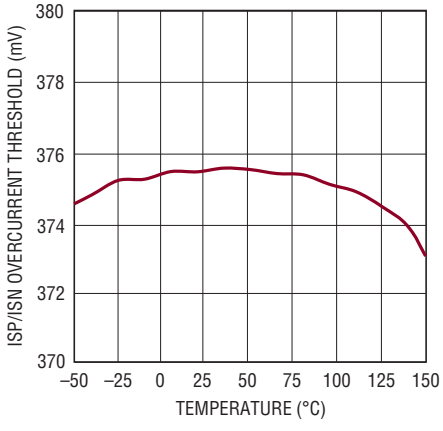
$V_{(ISP-ISN)}$ Threshold vs FB Voltage



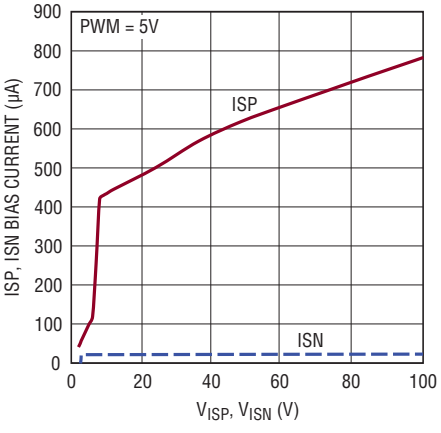
V_{FB} vs Temperature



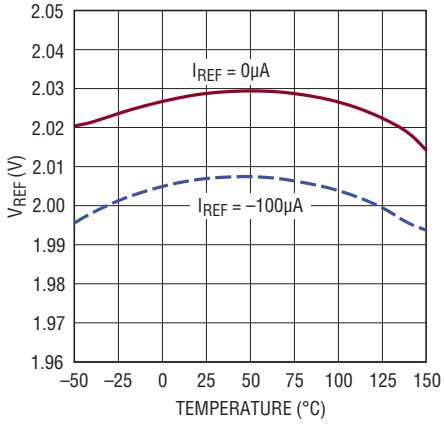
ISP/ISN Overcurrent Protection Threshold vs Temperature



ISP/ISN Input Bias Current vs V_{ISP}, V_{ISN}



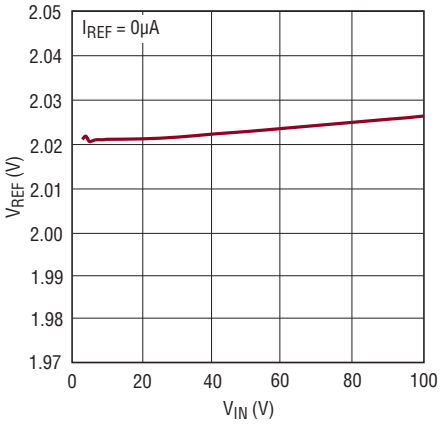
V_{REF} Voltage vs Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

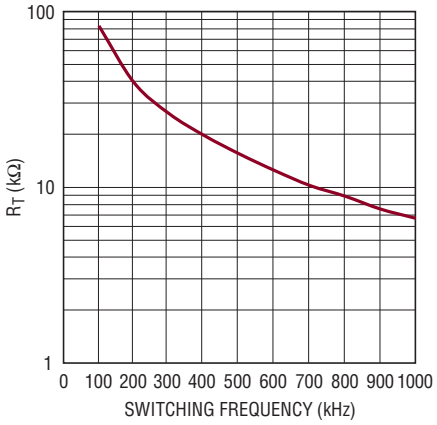
T_A = 25°C, unless otherwise noted.

V_{REF} vs V_{IN}



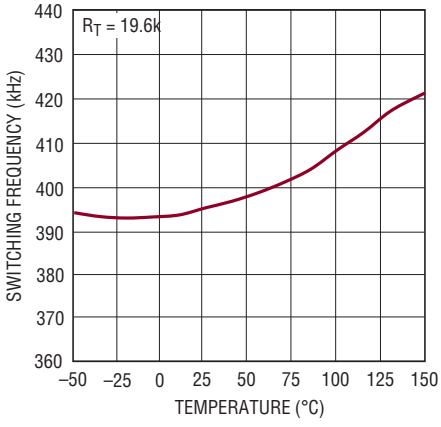
3796 G09

R_T vs Switching Frequency



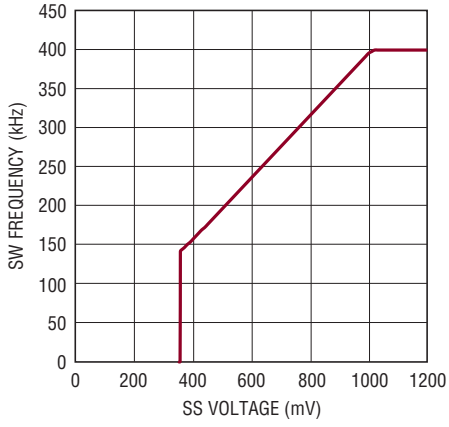
3796 G10

Switching Frequency vs Temperature



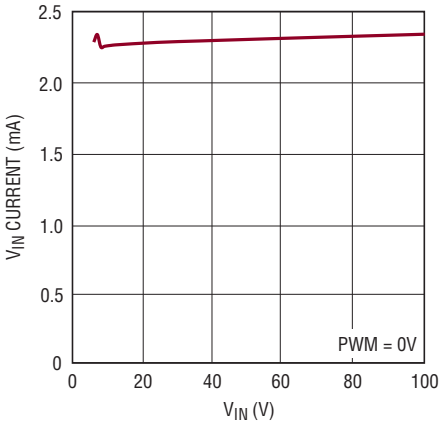
3796 G11

Switching Frequency vs SS Voltage



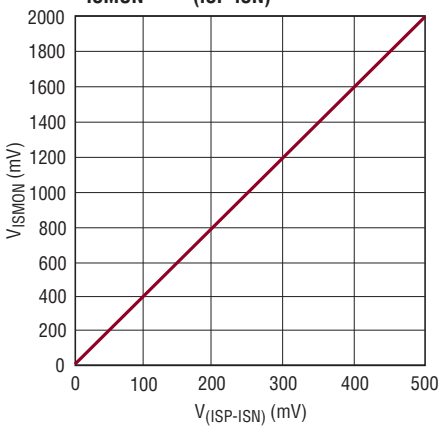
3796 G11a

Quiescent Current vs V_{IN}



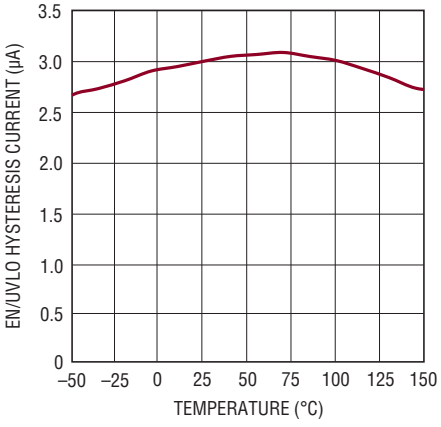
3796 G12

V_{ISMON} vs $V_{(ISP-ISN)}$



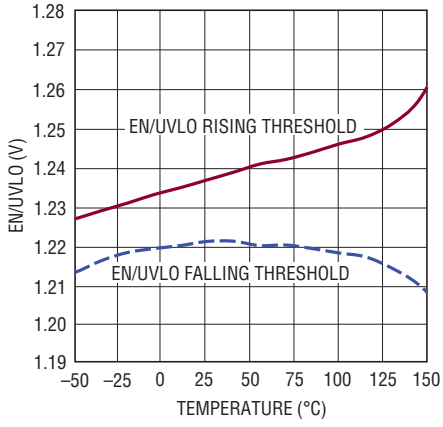
3796 G13

EN/UVLO Hysteresis Current vs Temperature



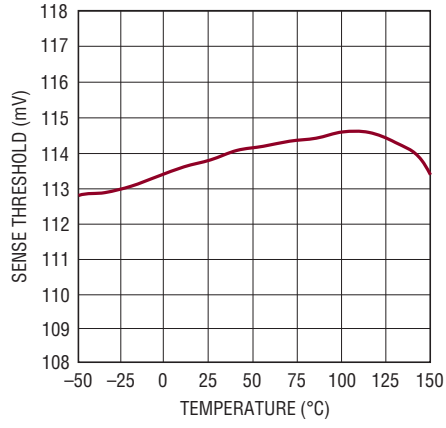
3796 G14

EN/UVLO Falling/Rising Threshold vs Temperature



3796 G15

SENSE Current Limit Threshold vs Temperature

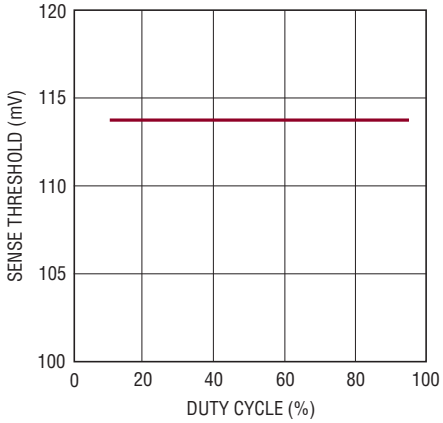


3796 G16

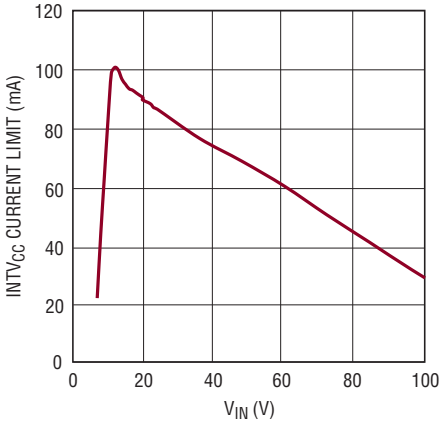
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

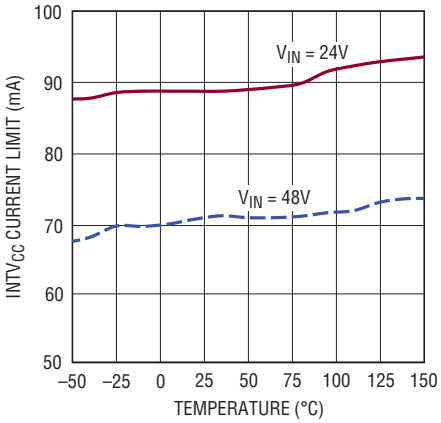
SENSE Current Limit Threshold vs Duty Cycle



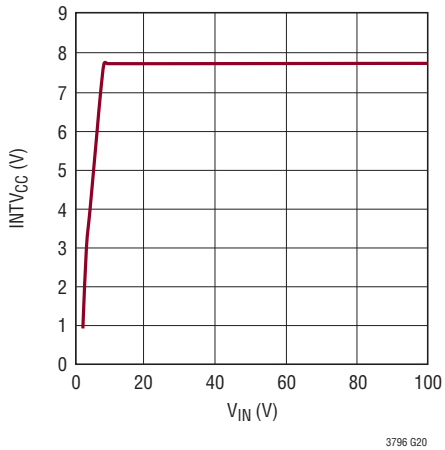
$INTV_{CC}$ Current Limit vs V_{IN}



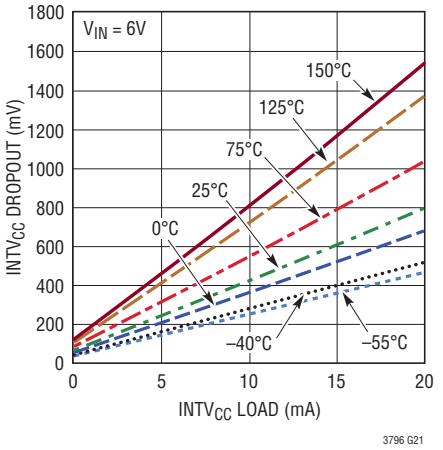
$INTV_{CC}$ Current Limit vs Temperature



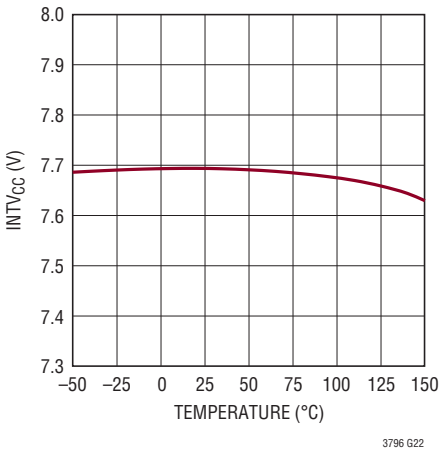
$INTV_{CC}$ vs V_{IN}



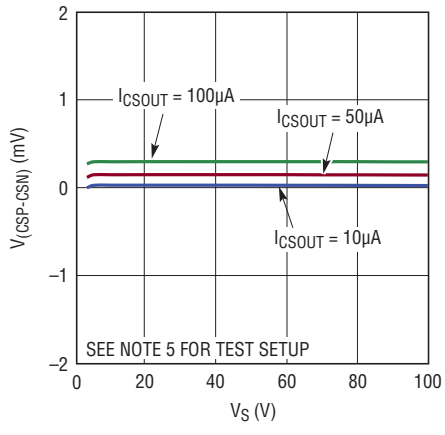
$INTV_{CC}$ Dropout Voltage vs Current, Temperature



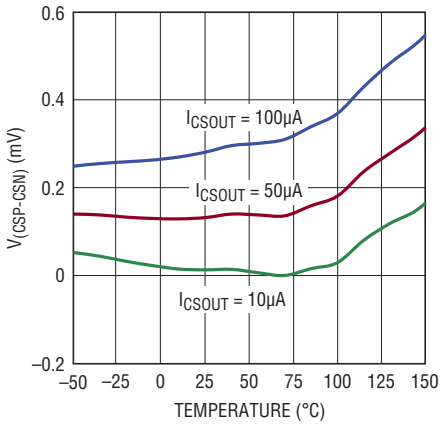
$INTV_{CC}$ vs Temperature



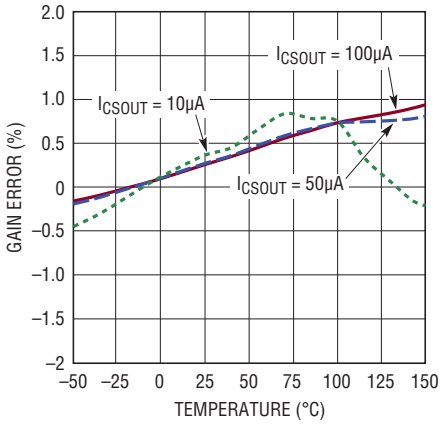
$V_{(CSP-CSN)}$ Offset Voltage with Different I_{CSOUT} vs V_S



$V_{(CSP-CSN)}$ Offset Voltage vs Temperature



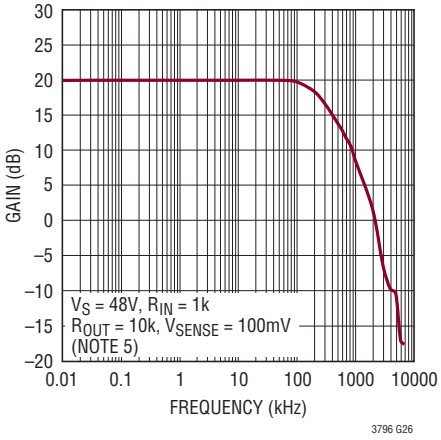
Current Sense Amplifier Gain Error vs Temperature



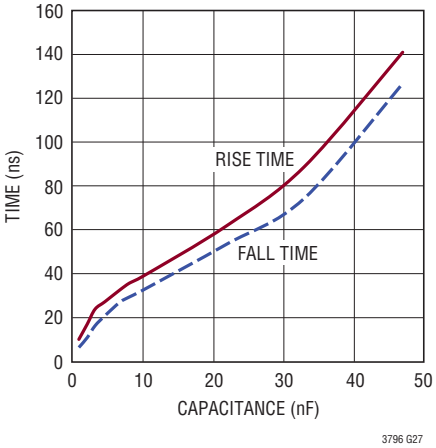
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

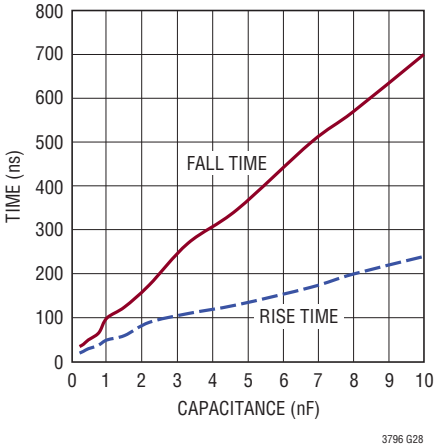
Current Sense Amplifier Gain vs Frequency



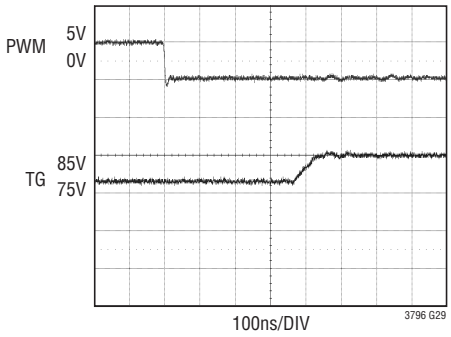
NMOS Gate Rise/Fall Time vs Capacitance



Top Gate (PMOS) Rise/Fall Time vs Capacitance

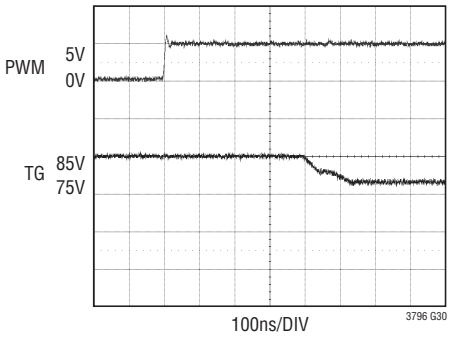


Top Gate Driver Rising Edge



PMOS VISHAY SILICONIX Si7113DN

Top Gate Driver Falling Edge



PMOS VISHAY SILICONIX Si7113DN

PIN FUNCTIONS

ISP (Pin 1): Connection Point for the Positive Terminal of the Current Feedback Resistor (R_{LED}). Also serves as positive rail for TG pin driver.

ISN (Pin 2): Connection Point for the Negative Terminal of the Current Feedback Resistor (R_{LED}).

TG (Pin 3): Top Gate Driver Output. An inverted PWM signal drives series PMOS device between V_{ISP} and (V_{ISP} – 7V) if V_{ISP} > 7V. An internal 7V clamp protects the PMOS gate by limiting VGS. Leave TG unconnected if not used.

GND (Pins 4, 17, 21, 22, Exposed Pad Pin 29): Ground. These pins also serve as current sense input for control loop, sensing negative terminal of current sense resistor in the source of the N-channel MOSFET. Solder the exposed pad directly to ground plane.

ISMON (Pin 5): ISP/ISN Current Report Pin. The LED current sensed by ISP/ISN inputs is reported as $V_{ISMON} = I_{LED} \bullet R_{LED} \bullet 4$. Leave ISMON pin unconnected if not used. When PWM is low, ISMON is driven to ground. Bypass with a 47nF capacitor or higher if needed.

FB2 (Pin 6): Voltage Loop Feedback 2 Pin. This pin is connected to the internal transconductance amplifier positive input node. The internal transconductance amplifier with output V_C regulates FB2 to 1.25V through the DC/DC converter. If FB2 is driven above 1.3V, the TG pin is pulled high to turn off the external PMOS and GATE pin is driven to GND to turn off the external N-channel MOSFET. Connect to GND if not used.

FB1 (Pin 7): Voltage Loop Feedback 1 Pin. FB1 is intended for constant-voltage regulation or for LED protection/open LED detection. The internal transconductance amplifier with output V_C regulates FB1 to 1.25V (nominal) through the DC/DC converter. If the FB1 input is regulating the loop and $V_{(ISP-ISN)}$ is less than 25mV (normal), the $\overline{VMODE}$ pull-down is asserted. This action may signal an open LED fault. If FB1 is driven above the 1.3V (by an external power supply spike, for example), the $\overline{FAULT}$ pull-down is asserted, the GATE pin is pulled low to turn off the external N-channel MOSFET and the TG pin is driven high to protect the LEDs from an overcurrent event. Do not leave the FB1 pin open. If not used, connect FB1 to GND.

V_C (Pin 8): Transconductance Error Amplifier Output Pin. Used to stabilize the control loop with an RC network. This pin is high impedance when PWM is low, a feature that stores the demand current state variable for the next PWM high transition. Connect a capacitor between this pin and GND; a resistor in series with the capacitor is recommended for fast transient response. Do not leave this pin open.

CTRL (Pin 9): Current Sense Threshold Adjustment Pin. Regulating threshold $V_{(ISP-ISN)}$ is $0.25 \bullet V_{CTRL}$ plus an offset for 0.1V < V_{CTRL} < 1V. For V_{CTRL} > 1.2V the current sense threshold is constant at the full-scale value of 250mV. For 1V < V_{CTRL} < 1.2V, the dependence of the current sense threshold upon V_{CTRL} transitions from a linear function to a constant value, reaching 98% of full-scale value by V_{CTRL} = 1.1V. Connect CTRL to V_{REF} for the 250mV default current threshold. Do not leave this pin open. Pull CTRL pin to GND for zero LED current.

V_{REF} (Pin 10): Voltage Reference Output Pin. Typically 2.015V. This pin drives a resistor divider for the CTRL pin, either for analog dimming or for temperature limit/compensation of LED load. It can supply up to 100µA.

SS (Pin 11): Soft-Start Pin. This pin modulates oscillator frequency and compensation pin voltage (V_C) clamp. The soft-start interval is set with an external capacitor. The pin has a 28µA (typical) pull-up current source to an internal 2.5V rail. This pin can be used as fault timer. Provided the SS pin has exceeded 1.7V, the pull-up current source is disabled and a 2.8µA pull-down current enabled when any one of the following fault conditions happen:

1. LED overcurrent
2. $INTV_{CC}$ undervoltage
3. Thermal limit

The SS pin must be discharged below 0.2V to reinitiate a soft-start cycle. Switching is disabled until SS is recharged.

RT (Pin 12): Switching Frequency Adjustment Pin. Set the frequency using a resistor to GND (for resistor values, see the Typical Performance curve or Table 2). Do not leave the RT pin open.

PIN FUNCTIONS

SYNC (Pin 13): The SYNC pin is used to synchronize the internal oscillator to an external logic level signal. If SYNC is used, the R_T resistor should be chosen to program an internal switching frequency 20% slower than the SYNC pulse frequency. Gate turn-on occurs a fixed delay after the rising edge of SYNC. Use a 50% duty cycle waveform to drive this pin. If not used, tie this pin to GND.

PWM (Pin 14): PWM Input Signal Pin. A signal low turns off switching, idles the oscillator, disconnects the V_C pin from all internal loads, and makes the TG pin high.

$\overline{\text{FAULT}}$ (Pin 15): An open-collector pull-down on $\overline{\text{FAULT}}$ asserts when any of the following conditions happen: 1. FB1 overvoltage (V_{FB1} > 1.3V), 2. $INTV_{CC}$ undervoltage, 3. LED overcurrent ($V_{(ISP-ISN)}$ > 375mV), or 4. Thermal shutdown. If all faults are removed, $\overline{\text{FAULT}}$ flag returns high. Fault status is only updated during PWM high state and latched during PWM low state. $\overline{\text{FAULT}}$ remains asserted until the SS pin is discharged below 0.2V for cases 2, 3 and 4 above.

$\overline{\text{VMODE}}$ (Pin 16): An open-collector pull-down on $\overline{\text{VMODE}}$ asserts if the FB1 input is above 1.19V (typical), and $V_{(ISP-ISN)}$ is less than 25mV (typical). To function, the pin requires an external pull-up resistor. $\overline{\text{VMODE}}$ status is updated only during PWM high state and latched during PWM low state.

SENSE (Pin 18): The current sense input for the control loop. Kelvin connect this pin to the positive terminal of the switch current sense resistor, R_{SENSE}, in the source of the N-channel MOSFET. The negative terminal of the current sense resistor should be Kelvin connected to the GND plane of the IC.

GATE (Pin 19): N-Channel MOSFET Gate Driver Output. Switches between $INTV_{CC}$ and GND. It is driven to GND during shutdown, fault or idle states.

$INTV_{CC}$ (Pin 20): Regulated Supply for Internal Loads, GATE Driver and Top Gate (PMOS) Driver. Supplied from V_{IN} and regulates to 7.7V (typical). $INTV_{CC}$ must be bypassed with a 4.7µF capacitor placed close to the pin. Connect $INTV_{CC}$ directly to V_{IN} if V_{IN} is always less than or equal to 7V.

V_{IN} (Pin 23): Input Supply Pin. Must be locally bypassed with a 0.22µF (or larger) capacitor placed close to the IC.

EN/UVLO (Pin 24): Enable and Undervoltage Lockout Pin. An accurate 1.22V falling threshold with externally programmable hysteresis detects when power is OK to enable switching. Rising hysteresis is generated by the external resistor divider and an accurate internal 3µA pull-down current. Above the threshold (but below 6V), EN/UVLO input bias current is sub-µA. Below the falling threshold, a 3µA pull-down current is enabled so the user can define the hysteresis with the external resistor selection. An undervoltage condition resets soft-start. Tie to 0.4V, or less, to disable the device and reduce V_{IN} quiescent current below 1µA.

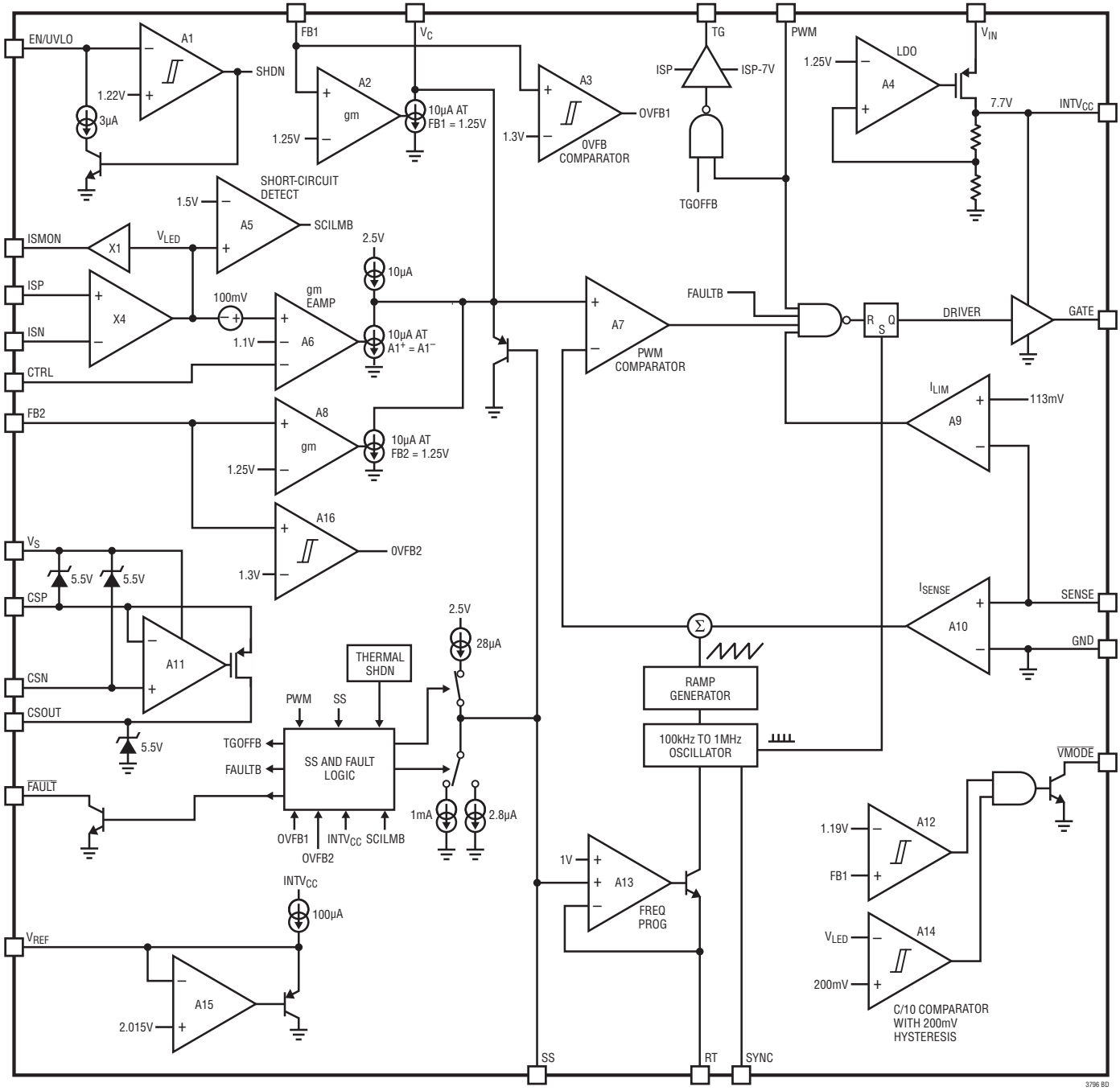
V_S (Pin 25): Current Sense Amplifier Power Supply Pin. This pin supply current to the current sense amplifier and can operate from 3V to 100V.

CSN (Pin 26): Negative Current Sense Input Terminal. CSN remains functional for voltages up to 100V. Typically connected to V_S and CSP as shown in Figure 9.

CSP (Pin 27): Positive Current Sense Input Terminal. The internal sense amplifier sinks current from CSP to regulate it to the same potential as CSN. A resistor (R_{IN1}) tied from V_{IN} to CSP sets the output current $I_{CSOUT} = V_{SNS}/R_{IN1}$. V_{SNS} is the voltage developed across R_{SNS}. See Figure 9.

CSOUT (Pin 28): Current Sense Amplifier Output. CSOUT pin sources the current that is drawn from CSP. Typically is output to an external resistor to GND.

BLOCK DIAGRAM



LT3796 Block Diagram

OPERATION

The LT3796 is a constant-frequency, current mode controller with a low side NMOS gate driver. The operation of the LT3796 is best understood by referring to the Block Diagram. In normal operation, with the PWM pin low, the GATE pin is driven to GND, the TG pin is pulled high to ISP to turn off the PMOS disconnect switch, the V_C pin goes high impedance to store the previous switching state on the external compensation capacitor, and the ISP and ISN pin bias currents are reduced to leakage levels. When the PWM pin transitions high, the TG pin transitions low after a short delay. At the same time, the internal oscillator wakes up and generates a pulse to set the PWM latch, turning on the external power N-channel MOSFET switch (GATE goes high). A voltage input proportional to the switch current, sensed by an external current sense resistor between the SENSE and GND input pins, is added to a stabilizing slope compensation ramp and the resulting switch current sense signal is fed into the negative terminal of the PWM comparator. The current in the external inductor increases steadily during the time the switch is on. When the switch current sense voltage exceeds the output of the error amplifier, labeled V_C, the latch is reset and the switch is turned off. During the switch off phase, the inductor current decreases. At the completion of each oscillator cycle, internal signals such as slope compensation return to their starting points and a new cycle begins with the set pulse from the oscillator. Through this repetitive action, the PWM control algorithm establishes a switch duty cycle to regulate a current or voltage in the load. The V_C signal is integrated over many switching cycles and is an amplified version of the difference between the LED current sense voltage, measured between ISP and ISN, and the target difference voltage set by the CTRL pin. In this manner, the error amplifier sets the correct peak switch current level to keep the LED current in regulation. If the error amplifier output increases, more current is demanded in the switch; if it decreases, less current is demanded. The switch current is monitored during the on phase and the voltage across the SENSE pin is not allowed to exceed the current limit threshold of 113mV (typical). If the SENSE pin exceeds the current limit threshold, the SR latch is reset regardless of the output state of the PWM comparator. Likewise, any fault condition, i.e. FB1 overvoltage (V_{FB1} > 1.3V), LED over current, or $INTV_{CC}$ undervoltage ($INTV_{CC}$ < 4V), the GATE pin is pulled down to GND immediately.

In voltage feedback mode, the operation is similar to that described above, except the voltage at the V_C pin is set by the amplified difference of the internal reference of 1.25V (nominal) and the FB1 and FB2 pins. If FB1 and FB2 are both lower than the reference voltage, the switch current increases; if FB1 or FB2 is higher than the reference voltage, the switch demand current decreases. The LED current sense feedback interacts with the voltage feedback so that neither FB1 or FB2 exceeds the internal reference and the voltage between ISP and ISN does not exceed the threshold set by the CTRL pin. For accurate current or voltage regulation, it is necessary to be sure that under normal operating conditions, the appropriate loop is dominant. To deactivate the voltage loop entirely, FB1 and FB2 can be connected to GND. To deactivate the LED current loop entirely, the ISP and ISN should be tied together and the CTRL input tied to V_{REF}.

Two LED specific functions featured on the LT3796 are controlled by the voltage feedback FB1 pin. First, when the FB1 pin exceeds a voltage 60mV lower (–5%) than the FB1 regulation voltage and $V_{(ISP-ISN)}$ is less than 25mV (typical), the pull-down driver on the $\overline{VMODE}$ pin is activated. This function provides a status indicator that the load may be disconnected and the constant-voltage feedback loop is taking control of the switching regulator. When the FB1 pin exceeds the FB1 regulation voltage by 50mV (4% typical), the $\overline{FAULT}$ pin is activated.

LT3796 features a PMOS disconnect switch driver. The PMOS disconnect switch can be used to improve the PWM dimming ratio, and operate as fault protection as well. Once a fault condition is detected, the TG pin is pulled high to turnoff the PMOS switch. The action isolates the LED array from the power path, preventing excessive current from damaging the LEDs.

A standalone current sense amplifier is integrated in the LT3796. It can work as input current limit or open LED protection. The detailed information can be found in the Application Information section.

APPLICATIONS INFORMATION

$INTV_{CC}$ Regulator Bypassing and Operation

The $INTV_{CC}$ pin requires a capacitor for stable operation and to store the charge for the large GATE switching currents. Choose a 10V rated low ESR, X7R or X5R ceramic capacitor for best performance. A 4.7µF ceramic capacitor is adequate for many applications. Place the capacitor close to the IC to minimize the trace length to the $INTV_{CC}$ pin and also to the power ground.

An internal current limit on the $INTV_{CC}$ output protects the LT3796 from excessive on-chip power dissipation. The minimum value of this current limit should be considered when choosing the switching N-channel MOSFET and the operating frequency. I_{INTVCC} can be calculated from the following equation:

$$I_{INTVCC} = Q_G \bullet f_{OSC}$$

Careful choice of a lower Q_G MOSFET allows higher switching frequencies, leading to smaller magnetics. The $INTV_{CC}$ pin has its own undervoltage disable (UVLO) set to 4V (typical) to protect the external FETs from excessive power dissipation caused by not being fully enhanced. If the $INTV_{CC}$ pin drops below the UVLO threshold, the GATE pin is forced to 0V, TG pin is pulled high and the soft-start pin will be reset. If the input voltage, V_{IN}, will not exceed 7V, then the $INTV_{CC}$ pin should be connected to the input supply. Be aware that a small current (typically 10µA) loads the $INTV_{CC}$ in shutdown. If V_{IN} is normally above, but occasionally drops below the $INTV_{CC}$ regulation voltage, then the minimum operating V_{IN} is close to 6V. This value is determined by the dropout voltage of the linear regulator and the 4V $INTV_{CC}$ undervoltage lockout threshold mentioned above.

Programming the Turn-On and Turn-Off Thresholds with the EN/UVLO Pin

The falling UVLO value can be accurately set by the resistor divider. A small 3µA pull-down current is active when EN/UVLO is below the threshold. The purpose of this current is to allow the user to program the rising hysteresis. The following equations should be used to determine the values of the resistors:

$$V_{IN(FALLING)} = 1.22 \bullet \frac{R1+R2}{R2}$$

$$V_{IN(RISING)} = V_{IN(FALLING)} + 3\mu A \bullet R1$$

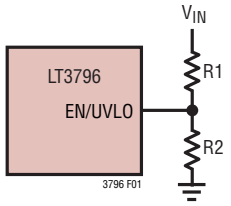


Figure 1.

LED Current Programming

The LED current is programmed by placing an appropriate value current sense resistor R_{LED} between the ISP and ISN pins. Typically, sensing of the current should be done at the top of the LED string. If this option is not available, then the current may be sensed at the bottom of the string. The CTRL pin should be tied to a voltage higher than 1.2V to get the full-scale 250mV (typical) threshold across the sense resistor. The CTRL pin can also be used to dim the LED current to zero, although relative accuracy decreases with the decreasing voltage sense threshold. When the CTRL pin voltage is less than 1V, the LED current is:

$$I_{LED} = \frac{V_{CTRL} - 100mV}{R_{LED} \bullet 4}, \; 0.1V < V_{CTRL} \leq 1V$$

$$I_{LED} = 0, \; V_{CTRL} = 0V$$

When the CTRL pin voltage is between 1V and 1.2V, the LED current varies with CTRL, but departs from the previous equation by an increasing amount as the CTRL voltage increases. Ultimately above 1.2V, the LED current no

APPLICATIONS INFORMATION

longer varies with CTRL. The typical $V_{(ISP-ISN)}$ threshold vs CTRL is listed in the Table 1.

Table 1. $V_{(ISP-ISN)}$ Threshold vs CTRL

V_{CTRL} (V)	$V_{(ISP-ISN)}$ (mV)
1	225
1.05	236
1.1	244.5
1.15	248.5
1.2	250

When CTRL is higher than 1.2V, the LED current is regulated to:

$$I_{LED} = \frac{250mV}{R_{LED}}$$

The CTRL pin should not be left open (tie to V_{REF} if not used). The CTRL pin can also be used in conjunction with a thermistor to provide overtemperature protection for the LED load, or with a resistor divider to V_{IN} to reduce output power and switching current when V_{IN} is low. The presence of a time varying differential voltage signal (ripple) across ISP and ISN at the switching frequency is expected. The amplitude of this signal is increased by high LED load current, low switching frequency and/or a smaller value output filter capacitor.

Programming Output Voltage (Constant-Voltage Regulation) or Open LED/Overvoltage Threshold

The LT3796 has two voltage feedback pins, FB1 and FB2. Either one can be used for a boost or SEPIC application. The difference between these two pins is FB1 has a comparator that senses when FB1 exceeds V_{FB} – 60mV ($\overline{VMODE}$ threshold) and asserts the $\overline{VMODE}$ output if $V_{(ISP-ISN)}$ is less than 25mV. This indicates that the output is in voltage regulation mode and not current regulation. FB2 does not have this extra comparator. The output voltage can be set by selecting the values of R3 and R4 (see Figure 2) according to the following equation:

$$V_{OUT} = 1.25 \bullet \frac{R3+R4}{R4}$$

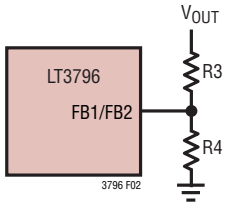


Figure 2. Feedback Resistor Connections for Boost and SEPIC Applications

For a boost type LED driver, set the resistor from the output to the FB1 pin such that the expected V_{FB1} during normal operation does not exceed 1.15V. For an LED driver of buck mode or a buck-boost mode configuration, the FB voltage is typically level shifted to a signal with respect to GND as illustrated in Figure 3. The output can be expressed as:

$$V_{OUT} = 1.25 \bullet \frac{R5}{R8} \bullet \frac{R6+R7}{R6}$$

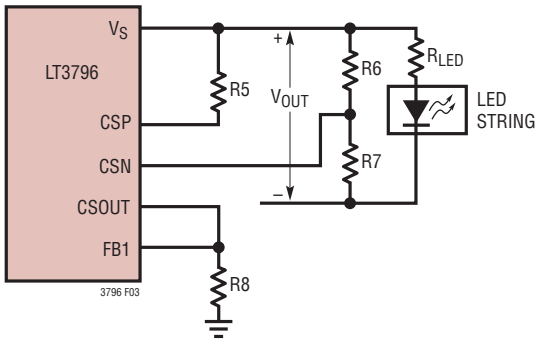


Figure 3. Feedback Resistor Connection for Buck Mode or Buck-Boost Mode LED Driver

APPLICATIONS INFORMATION

Open LED Detection

The LT3796 provides an open-collector status pin, $\overline{VMODE}$, that pulls low when the FB1 pin is above 1.19V and $V_{(ISP-ISN)}$ is less than 25mV. If the open LED clamp voltage is programmed correctly using the resistor divider, then the FB1 pin should never exceed 1.15V when LEDs are connected, therefore, the only way for the FB1 pin to be within 60mV of the 1.25V regulation voltage is for an open LED event to have occurred.

LED Over Current Protection Feature

The ISP and ISN pins have a short-circuit protection feature independent of the LED current sense feature. This feature prevents the development of excessive switching currents and protects the power components. The short-circuit protection threshold (375mV, typ) is designed to be 50% higher than the default LED current sense threshold. Once the LED over current is detected, the GATE pin is driven to GND to stop switching, and TG pin is pulled high to disconnect the LED array from the power path.

A typical LED short-circuit protection scheme for boost or buck-boost mode converter is shown in Figure 4. The Schottky diode D2 should be put close to the drain of M2 on the board. It protects the LED+ node from swinging well below ground when being shorted to ground through a long cable. Usually, the internal protection loop takes about 1µs to respond. Including PNP helper Q1 is recommended to limit the transient short-circuit current.

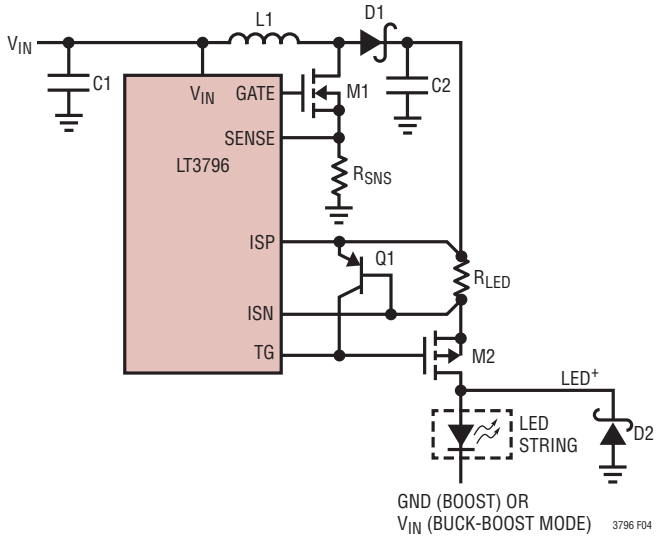


Figure 4. The Simplified LED Short-Circuit Protection Schematic for Boost/Buck-Boost Mode LED Driver

With the PNP helper, the short-circuit current can be limited to 2A, whereas the short-circuit current can reach to 20A without the PNP helper as shown in Figure 5 and Figure 6 respectively. Refer to boost LED driver with output short-circuit protection and LED current monitor for the test schematic. Note that the impedance of the short-circuit cable affects the peak current.

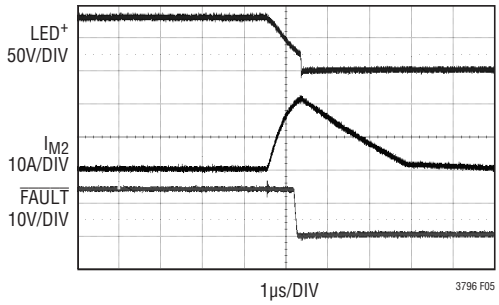


Figure 5. Short-circuit Current without PNP Helper

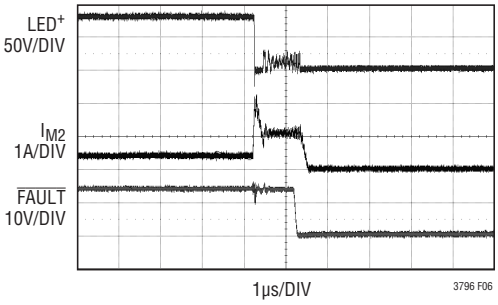


Figure 6. Short-circuit Current with PNP Helper

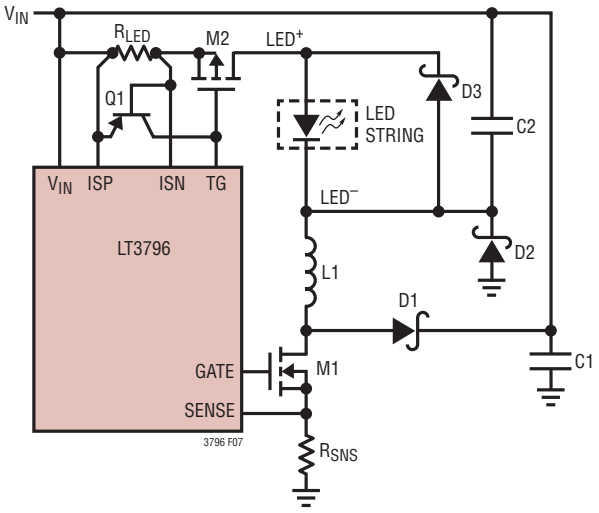


Figure 7. The Simplified LED Short-Circuit Protection Schematic for Buck Mode Converter

APPLICATIONS INFORMATION

Similar to boost, Schottky diodes D2, D3 and PNP transistor Q1 are recommended to protect short-circuit event in the buck mode.

PWM Dimming Control for Brightness

There are two methods to control the LED current for dimming using the LT3796. One method uses the CTRL pin to adjust the current regulated in the LEDs. A second method uses the PWM pin to modulate the LED current between zero and full current to achieve a precisely programmed average current, without the possibility of color shift that occurs at low current in LEDs. To make PWM dimming more accurate, the switch demand current is stored on the V_C node during the quiescent phase when PWM is low. This feature minimizes recovery time when the PWM signal goes high. To further improve the recovery time, a disconnect switch should be used in the LED current path to prevent the output capacitor from discharging during the PWM signal low phase. The minimum PWM on or off time depends on the choice of operating frequency through the RT input. For best current accuracy, the minimum PWM high time should be at least three switching cycles (3µs for f_{SW} = 1MHz).

A low duty cycle PWM signal can cause excessive start-up times if it were allowed to interrupt the soft-start sequence. Therefore, once start-up is initiated by PWM > 1V, it will ignore a logical disable by the external PWM input signal. The device will continue to soft-start with switching and TG enabled until either the voltage at SS reaches the 1.0V level, or the output current reaches one-fourth of the full-scale current. At this point the device will begin following the dimming control as designated by PWM. If at any time an output overcurrent is detected, GATE and TG will be disabled even as SS continues to charge.

Programming the Switching Frequency

The RT frequency adjust pin allows the user to program the switching frequency from 100kHz to 1MHz to optimize efficiency/performance or external component size. Higher frequency operation yields smaller component size but increases switching losses and gate driving current, and may not allow sufficiently high or low duty cycle operation. Lower frequency operation gives better performance at the cost of larger external component size. For an appropriate R_T resistor value see Table 2. An external resistor from the RT pin to GND is required—do not leave this pin open.

Table 2. Typical Switching Frequency vs R_T Value (1% Resistor)

f_{osc}(kHz)	R_T(kΩ)
1000	6.65
900	7.50
800	8.87
700	10.2
600	12.4
500	15.4
400	19.6
300	26.1
200	39.2
100	82.5

Frequency Synchronization

The LT3796 switching frequency can be synchronized to an external clock using the SYNC pin. For proper operation, the R_T resistor should be chosen for a switching frequency 20% lower than the external clock frequency. The SYNC pin is disabled during the soft-start period. Observation of the following guidelines about the SYNC waveform will ensure proper operation of this feature. Driving SYNC with a 50% duty cycle waveform is always a good choice, otherwise, maintain the duty cycle between 20% and 60%. When using both PWM and SYNC features, the PWM signal rising edge must have the aligned rising edges to achieve the optimized high PWM dimming ratio. If the SYNC pin is not used, it should be connected to GND.

Duty Cycle Considerations

Switching duty cycle is a key variable defining converter operation, therefore, its limits must be considered when programming the switching frequency for a particular application. The fixed minimum on-time and minimum

APPLICATIONS INFORMATION

off-time (see Figure 8) and the switching frequency define the minimum and maximum duty cycle of the switch, respectively. The following equations express the minimum/ maximum duty cycle:

Min Duty Cycle = minimum on-time • switching frequency

Max Duty Cycle = 1 – minimum off-time • switching frequency

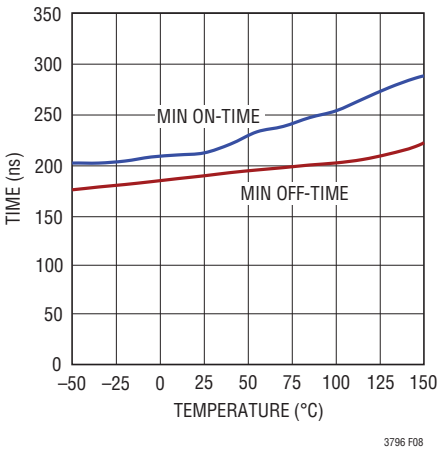


Figure 8. Typical Minimum On- and Off-Time vs Temperature

When calculating the operating limits, the typical values for on/off-time in the data sheet should be increased by at least 100ns to allow margin for PWM control latitude, GATE rise/fall times and SW node rise/fall times.

Setting Input Current Limit

The LT3796 has a standalone current sense amplifier. It can be used to limit the input current. As shown in Figure 9, the input current signal is converted to voltage output at CSOUT pin. When the CSOUT voltage exceeds FB2 regulation voltage, the GATE is pulled low, and the converter stops switching. The input current limit is calculated as follows:

$$I_{IN} = 1.25 \bullet \frac{R_{IN1}}{R_{OUT} \bullet R_{SNS}}$$

For buck applications, filter components, $R_{IN2(OPT)}$ and C_{OPT}, are recommended to be placed close to LT3796 to suppress the substantial transient signal or noise at across CSN and CSP pins. For boost and buck-boost applications, $R_{IN2(OPT)}$ and C_{OPT} are not required.

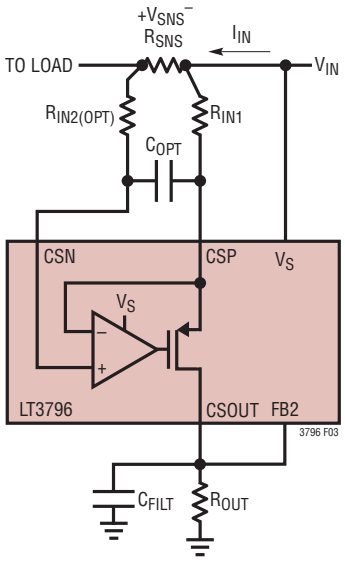


Figure 9. Setting Input Current Limit

Thermal Considerations

The LT3796 is rated to a maximum input voltage of 100V. Careful attention must be paid to the internal power dissipation of the IC at higher input voltages to ensure that a junction temperature of 150°C is not exceeded. This junction limit is especially important when operating at high ambient temperatures. The majority of the power dissipation in the IC comes from the supply current needed to drive the gate capacitance of the external power N-channel MOSFET. This gate drive current can be calculated as:

$$I_{GATE} = f_{SW} \bullet Q_G$$

A low Q_G power MOSFET should always be used when operating at high input voltages, and the switching frequency should also be chosen carefully to ensure that the IC does not exceed a safe junction temperature. The internal junction temperature, T_J of the IC can be estimated by:

$$T_J = T_A + [V_{IN} \bullet (I_Q + f_{SW} \bullet Q_G) \bullet \theta_{JA}]$$

where T_A is the ambient temperature, I_Q is the V_{IN} operating current of the part (2.5mA typical) and θ_{JA} is the package thermal impedance (30°C/W for the TSSOP package). For example, an application with $T_{A(MAX)}$ = 85°C, $V_{IN(MAX)}$ = 60V, f_{SW} = 400kHz, and having a N-channel MOSFET with

APPLICATIONS INFORMATION

Q_G = 20nC, the maximum IC junction temperature will be approximately:

T_J = 85°C + [60V • (2.5mA + 400kHz • 20nC) • 30°C/W]

≈ 104°C

The exposed pad on the bottom of the package must be soldered to a ground plane. This ground should then be connected to an internal copper ground plane with thermal vias placed directly under the package to spread out the heat dissipated by the IC.

It is best if the copper plane is extended on either the top or bottom layer of the PCB to have the maximum exposure to air. Internal ground layers do not dissipate thermals as much as top and bottom layer copper does. See recommended layout as an example.

Input Capacitor Selection

The input capacitor supplies the transient input current for the power inductor of the converter and must be placed and sized according to the transient current requirements. The switching frequency, output current and tolerable input voltage ripple are key inputs to estimating the capacitor value. An X7R type ceramic capacitor is usually the best choice since it has the least variation with temperature and DC bias. Typically, boost and SEPIC converters require a lower value capacitor than a buck mode converter. Assuming that a 100mV input voltage ripple is acceptable, the required capacitor value for a boost converter can be estimated as follows ($T_{SW} = 1/f_{OSC}$):

$$C_{IN}(\mu F) = I_{LED}(A) \bullet \frac{V_{LED}}{V_{IN}} \bullet T_{SW}(\mu s) \bullet \frac{1\mu F}{A \bullet \mu s \bullet 2.8}$$

Therefore, a 2.2µF capacitor is an appropriate selection for a 400kHz boost regulator with 12V input, 48V output and 500mA load.

With the same V_{IN} voltage ripple of less than 100mV, the input capacitor for a buck converter can be estimated as follows:

$$C_{IN}(\mu F) = I_{LED}(A) \bullet \frac{V_{LED}(V_{IN} - V_{LED})}{V_{IN}^2} \bullet T_{SW}(\mu s) \bullet \frac{10\mu F}{A \bullet \mu s}$$

A 10µF input capacitor is an appropriate selection for a 400kHz buck mode converter with 24V input, 12V output and 1A load.

In the buck mode configuration, the input capacitor has large pulsed currents due to the current returned through the Schottky diode when the switch is off. It is important to place the capacitor as close as possible to the Schottky diode and to the GND return of the switch (i.e., the sense resistor). It is also important to consider the ripple current rating of the capacitor. For best reliability, this capacitor should have low ESR and ESL and have an adequate ripple current rating. The RMS input current for a buck mode LED driver is:

$$I_{IN(RMS)} = I_{LED} \bullet \sqrt{(1-D)D}$$

$$D = \frac{V_{LED}}{V_{IN}}$$

where D is the switch duty cycle.

Table 3. Recommended Ceramic Capacitor Manufacturers

MANUFACTURER	WEB
TDK	www.tdk.com
Kemet	www.kemet.com
Murata	www.murata.com
Taiyo Yuden	www.t-yuden.com
AVX	www.avx.com

Output Capacitor Selection

The selection of the output capacitor depends on the load and converter configuration, i.e., step-up or step-down and the operating frequency. For LED applications, the equivalent resistance of the LED is typically low and the output filter capacitor should be sized to attenuate the current ripple. Use of an X7R type ceramic capacitor is recommended.

To achieve the same LED ripple current, the required filter capacitor is larger in the boost and buck-boost mode applications than that in the buck mode applications. Lower operating frequencies will require proportionately higher capacitor values.

APPLICATIONS INFORMATION

Power MOSFET Selection

For applications operating at high input or output voltages, the power N-channel MOSFET switch is typically chosen for drain voltage V_{DS} rating and low gate charge Q_G. Consideration of switch on-resistance, $R_{DS(ON)}$, is usually secondary because switching losses dominate power loss. The $INTV_{CC}$ regulator on the LT3796 has a fixed current limit to protect the IC from excessive power dissipation at high V_{IN}, so the MOSFET should be chosen so that the product of Q_G at 7.7V and switching frequency does not exceed the $INTV_{CC}$ current limit. For driving LEDs be careful to choose a switch with a V_{DS} rating that exceeds the threshold set by the FB pin in case of an open load fault. Several MOSFET vendors are listed in Table 4. The MOSFETs used in the application circuits in this data sheet have been found to work well with the LT3796. Consult factory applications for other recommended MOSFETs.

Table 4. MOSFET Manufacturers

VENDOR	WEB
Vishay Siliconix	www.vishay.com
Fairchild	www.fairchildsemi.com
International Rectifier	www.irf.com
Infineon	www.infineon.com

High Side PMOS Disconnect Switch Selection

A high side PMOS disconnect switch with a minimum V_{TH} of –1V to –2V is recommended in most LT3796 applications to optimize or maximize the PWM dimming ratio and protect the LED string from excessive heating during fault conditions as well. The PMOS disconnect switch is typically selected for drain-source voltage V_{DS}, and continuous drain current I_D. For proper operations, V_{DS} rating must exceed the open LED regulation voltage set by the FB1 pin, and I_D rating should be above I_{LED}.

Schottky Rectifier Selection

The power Schottky diode conducts current during the interval when the switch is turned off. Select a diode rated for the maximum SW voltage. If using the PWM feature for dimming, it is important to consider diode leakage, which increases with the temperature, from the output during the PWM low interval. Therefore, choose the Schottky diode with sufficiently low leakage current. Table 5 has some recommended component vendors.

Table 5. Schottky Rectifier Manufacturers

VENDOR	WEB
On Semiconductor	www.onsemi.com
Diodes, Inc	www.diodes.com
Central Semiconductor	www.centralsemi.com
Rohm Semiconductor	www.rohm.com

Sense Resistor Selection

The resistor, R_{SENSE}, between the source of the external N-channel MOSFET and GND should be selected to provide adequate switch current to drive the application without exceeding the 113mV (typical) current limit threshold on the SENSE pin of LT3796. For buck mode applications, select a resistor that gives a switch current at least 30% greater than the required LED current. For buck mode, select a resistor according to:

$$R_{SENSE(BUCK)} \leq \frac{0.07V}{I_{LED}}$$

For buck-boost mode, select a resistor according to:

$$R_{SENSE(BUCK-BOOST)} \leq \frac{V_{IN} \bullet 0.07V}{(V_{IN}+V_{LED})I_{LED}}$$

For boost, select a resistor according to:

$$R_{SENSE(BOOST)} \leq \frac{V_{IN} \bullet 0.07V}{V_{LED} \bullet I_{LED}}$$

The placement of R_{SENSE} should be close to the source of the NMOS FET and GND of the LT3796. The SENSE input to LT3796 should be a Kelvin connection to the positive terminal of R_{SENSE}.

70mV is used in the equations above to give some margin below the 113mV (typical) sense current limit threshold.

APPLICATIONS INFORMATION

Inductor Selection

The inductor used with the LT3796 should have a saturation current rating appropriate to the maximum switch current selected with the R_{SENSE} resistor. Choose an inductor value based on operating frequency, input and output voltage to provide a current mode signal on SENSE of approximately 20mV magnitude. The following equations are useful to estimate the inductor value ($T_{SW} = 1/f_{OSC}$):

$$L_{BUCK} = \frac{T_{SW} \bullet R_{SENSE} \bullet V_{LED}(V_{IN} - V_{LED})}{V_{IN} \bullet 0.02V}$$

$$L_{BUCK,\,BOOST} = \frac{T_{SW} \bullet R_{SENSE} \bullet V_{LED} \bullet V_{IN}}{(V_{LED} + V_{IN}) \bullet 0.02V}$$

$$L_{BOOST} = \frac{T_{SW} \bullet R_{SENSE} \bullet V_{IN}\,(V_{LED} - V_{IN})}{V_{LED} \bullet 0.02V}$$

Table 6 provides some recommended inductor vendors.

Table 6. Inductor Manufacturers

VENDOR	WEB
Sumida	www.sumida.com
Würth Elektronik	www.we-online.com
Coiltronics	www.cooperet.com
Vishay	www.vishay.com
Coilcraft	www.coilcraft.com

Loop Compensation

The LT3796 uses an internal transconductance error amplifier whose V_C output compensates the control loop. The external inductor, output capacitor and the compensation resistor and capacitor determine the loop stability. The inductor and output capacitor are chosen based on performance, size and cost. The compensation resistor and capacitor at V_C are selected to optimize control loop response and stability. For typical LED applications, a 22nF compensation capacitor at V_C is adequate, and a series resistor should always be used to increase the slew rate on the V_C pin to maintain tighter regulation of LED current during fast transients on the input supply to the converter.

Soft-Start Capacitor Selection

For many applications, it is important to minimize the inrush current at start-up. The built-in soft-start circuit significantly reduces the start-up current spike and output voltage overshoot. The soft-start interval is set by the soft-start capacitor selection according to the equation:

$$T_{SS} = C_{SS} \bullet \frac{2V}{28\mu A}$$

A typical value for the soft-start capacitor is 0.1µF. The soft-start pin reduces the oscillator frequency and the maximum current in the switch. Soft-start also operates as fault protection, which forces the converter into hiccup or latchoff mode. Detailed information is provided in the Fault Protection: Hiccup Mode and Latchoff Mode section.

Fault Protection: Hiccup Mode and Latchoff Mode

If an LED overcurrent condition, $INTV_{CC}$ undervoltage, or thermal limit happens, an open-drain pull-down on $\overline{FAULT}$ asserts. The TG pin is pulled high to disconnect the LED array from the power path, and the GATE pin is driven low. If the soft-start pin is charging and still below 1.7V, then it will continue to do so with a 28µA source. Once above 1.7V, the pull-up source is disabled and a 2.8µA pull-down is activated. While the SS pin is discharging, the GATE is forced low. When SS pin is discharged below 0.2V, a new cycle is initiated. This is referred as hiccup mode operation. If the fault still exists when SS crosses below 0.2V, then a full SS charge/discharge cycle has to complete before switching is enabled and the $\overline{FAULT}$ flag is deasserted.

If a resistor is placed between V_{REF} pin and SS pin to hold SS pin higher than 0.2V during a fault, then the LT3796 will enter latchoff mode with GATE pin low, TG pin high and $\overline{FAULT}$ pin low. To exit latchoff mode, the EN/UVLO pin must be toggled low to high.

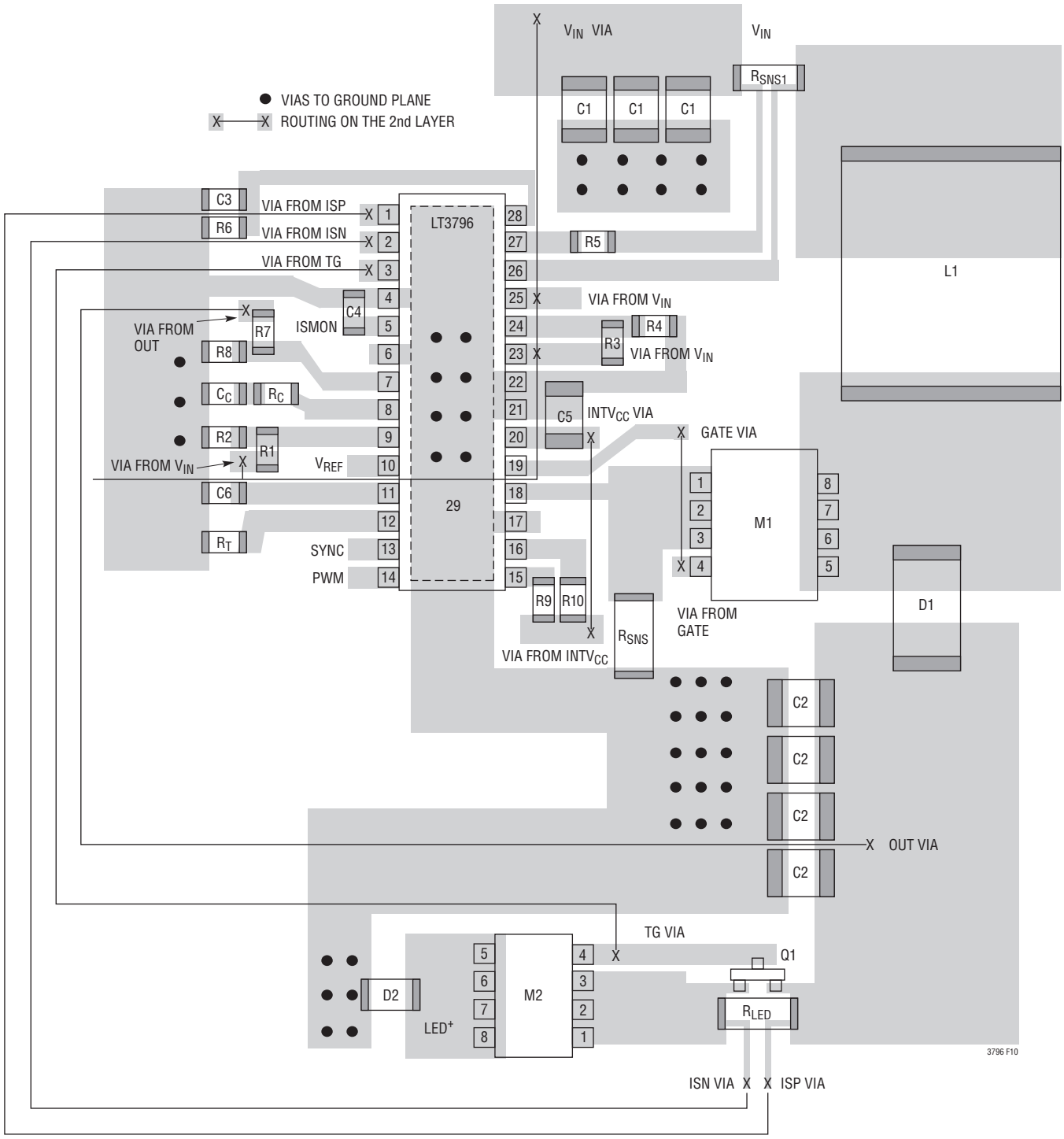
APPLICATIONS INFORMATION

Board Layout

The high speed operation of the LT3796 demands careful attention to board layout and component placement. The exposed pad of the package is the GND terminal of the IC and is also important for thermal management of the IC. It is crucial to achieve a good electrical and thermal contact between the exposed pad and the ground plane of the board. To reduce electromagnetic interference (EMI), it is important to minimize the area of the high dV/dt switching node between the inductor, switch drain and anode of the Schottky rectifier. Use a ground plane under the switching node to eliminate interplane coupling to sensitive signals. The lengths of the high dI/dt traces: 1) from the switch node through the switch and sense resistor to GND, and 2) from the switch node through the Schottky rectifier and filter capacitor to GND should be minimized. The ground points of these two switching current traces should come to a common point then connect to the ground plane under the LT3796. Likewise, the ground terminal of the bypass capacitor for the $INTV_{CC}$ regulator should be placed near the GND of the switching path. Typically, this requirement results in the external switch being closest to the IC, along with the $INTV_{CC}$ bypass capacitor. The ground for the compensation network and other DC control signals should be star connected to the underside of the IC. Do not extensively route high impedance signals such as FB1, FB2, RT and V_C, as they may pick up switching noise. Since there is a small variable DC input bias current to the ISN and ISP inputs, resistance in series with these pins should be minimized to avoid creating an offset in the current sense threshold. Likewise, minimize resistance in series with the SENSE input to avoid changes (most likely reduction) to the switch current limit threshold.

Figure 10 is a suggested two sided layout for a boost converter. Note that the 4-layer layout is recommended for best performance. Please contact the factory for the reference layout design.

APPLICATIONS INFORMATION

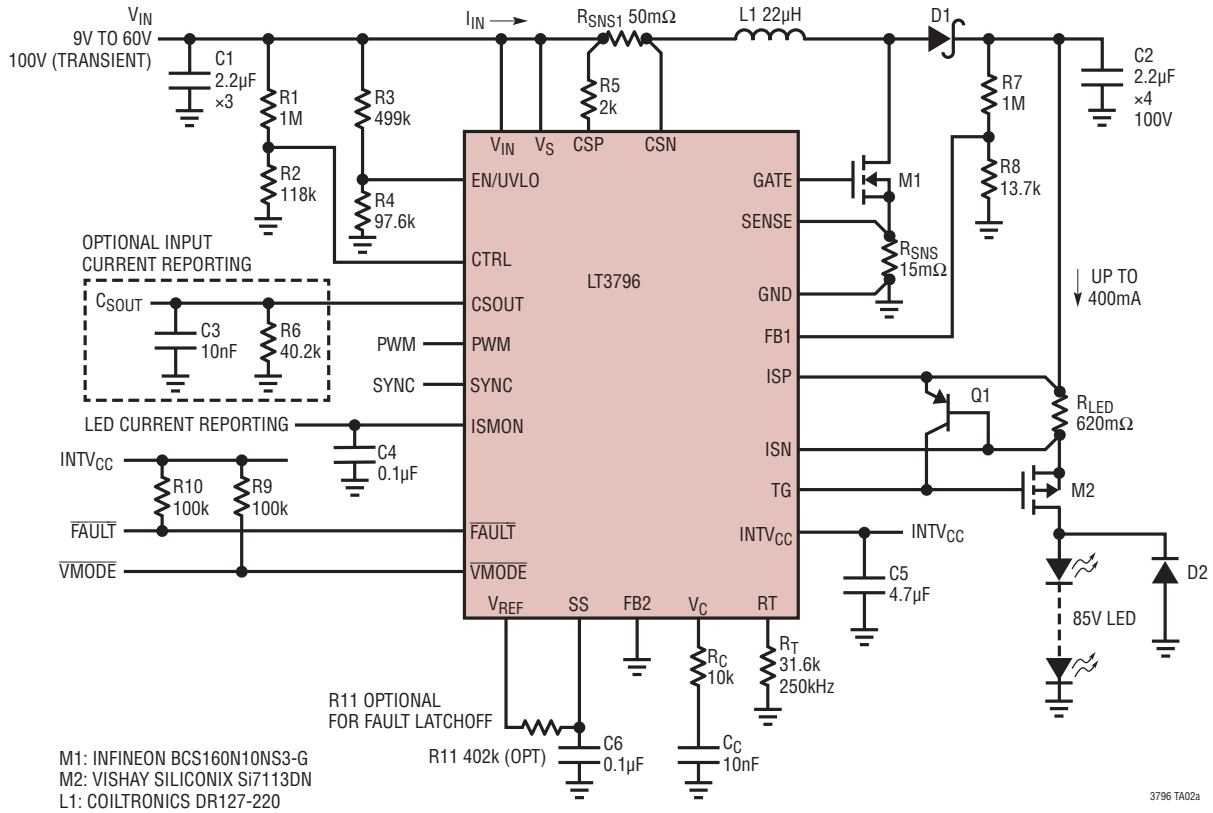


COMPONENT DESIGNATIONS REFER TO BOOST LED DRIVER WITH OUTPUT SHORT CIRCUIT PROTECTION AND LED CURRENT MONITOR

Figure 10. Boost Converter Suggested Layout

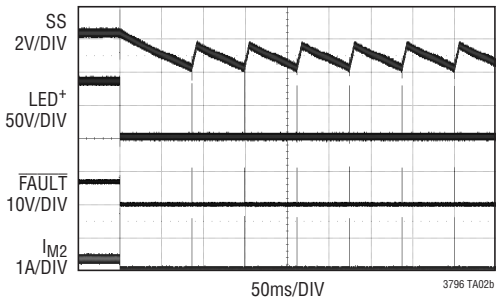
TYPICAL APPLICATIONS

Boost LED Driver with Output Short Circuit Protection and LED Current Monitor

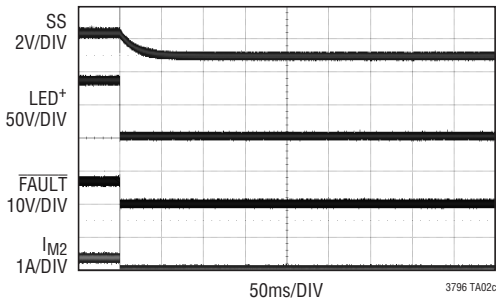


M1: INFINEON BCS160N10NS3-G
M2: VISHAY SILICONIX Si7113DN
L1: COILTRONICS DR127-220
D1: DIODES INC PDS5100
D2: VISHAY ES1C
Q1: ZETEX FMMT589
LED: CREE XLAMP XR-E

Fault (Short LED) Protection without R11: Hiccup Mode

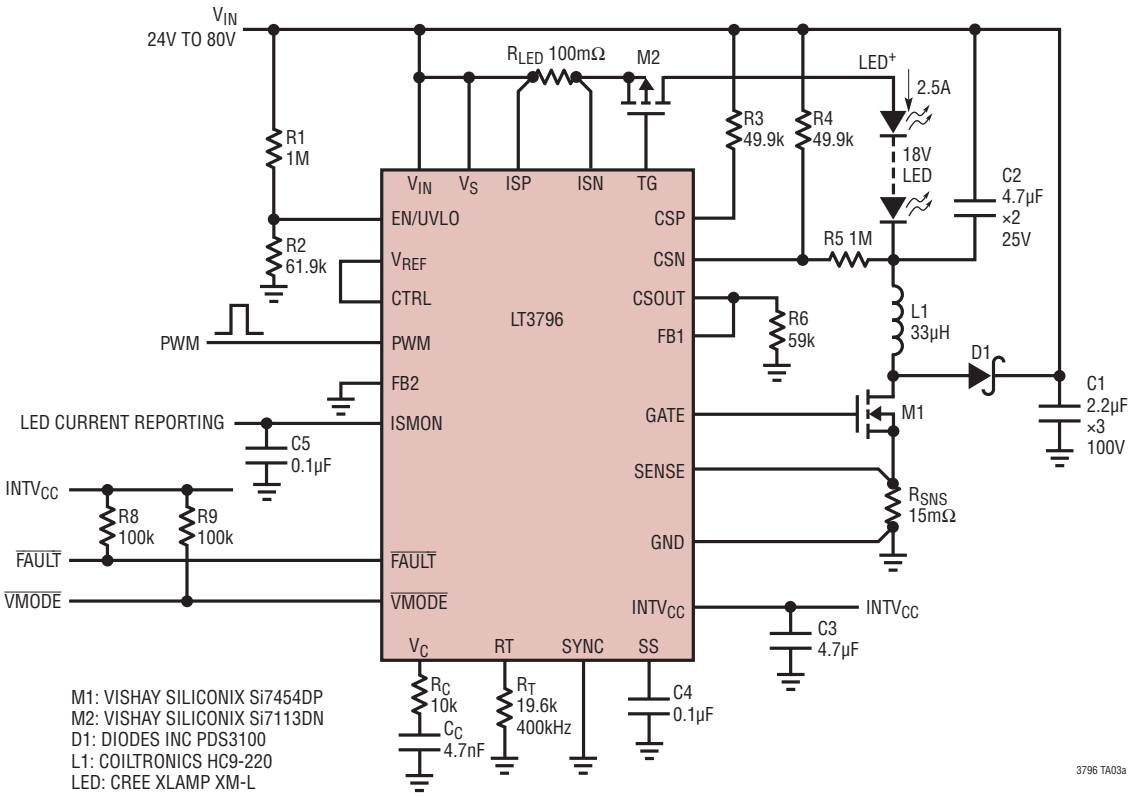


Fault (Short LED) Protection with R11: Latchoff Mode

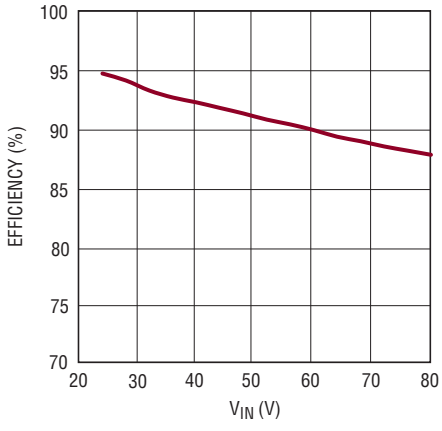


TYPICAL APPLICATIONS

Buck LED Driver with Open LED Flag and LED Current Reporting

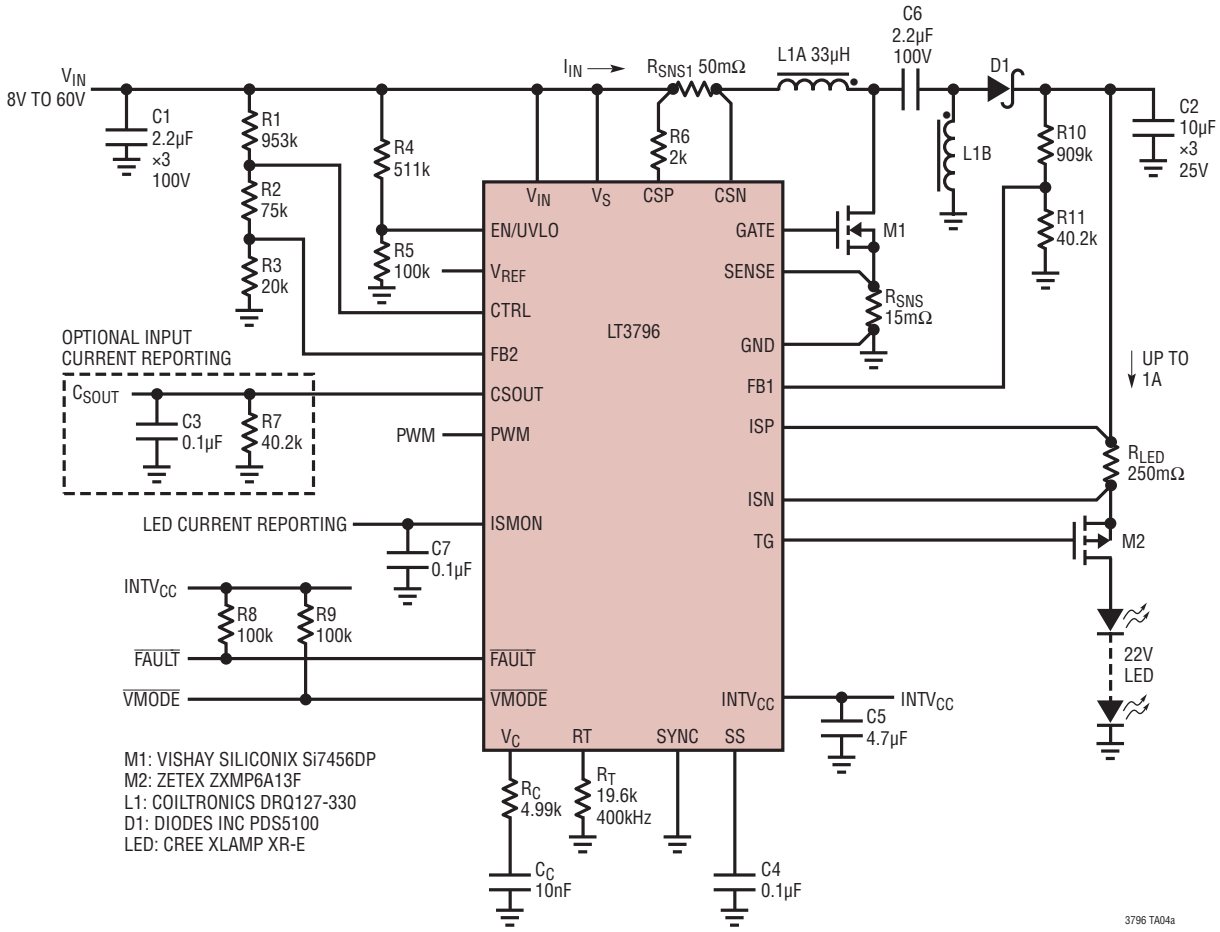


Efficiency vs V_{IN}

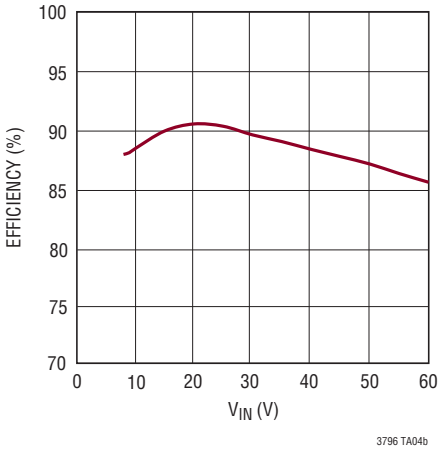


TYPICAL APPLICATIONS

SEPIC LED Driver Using FB2 for Input Overvoltage Protection

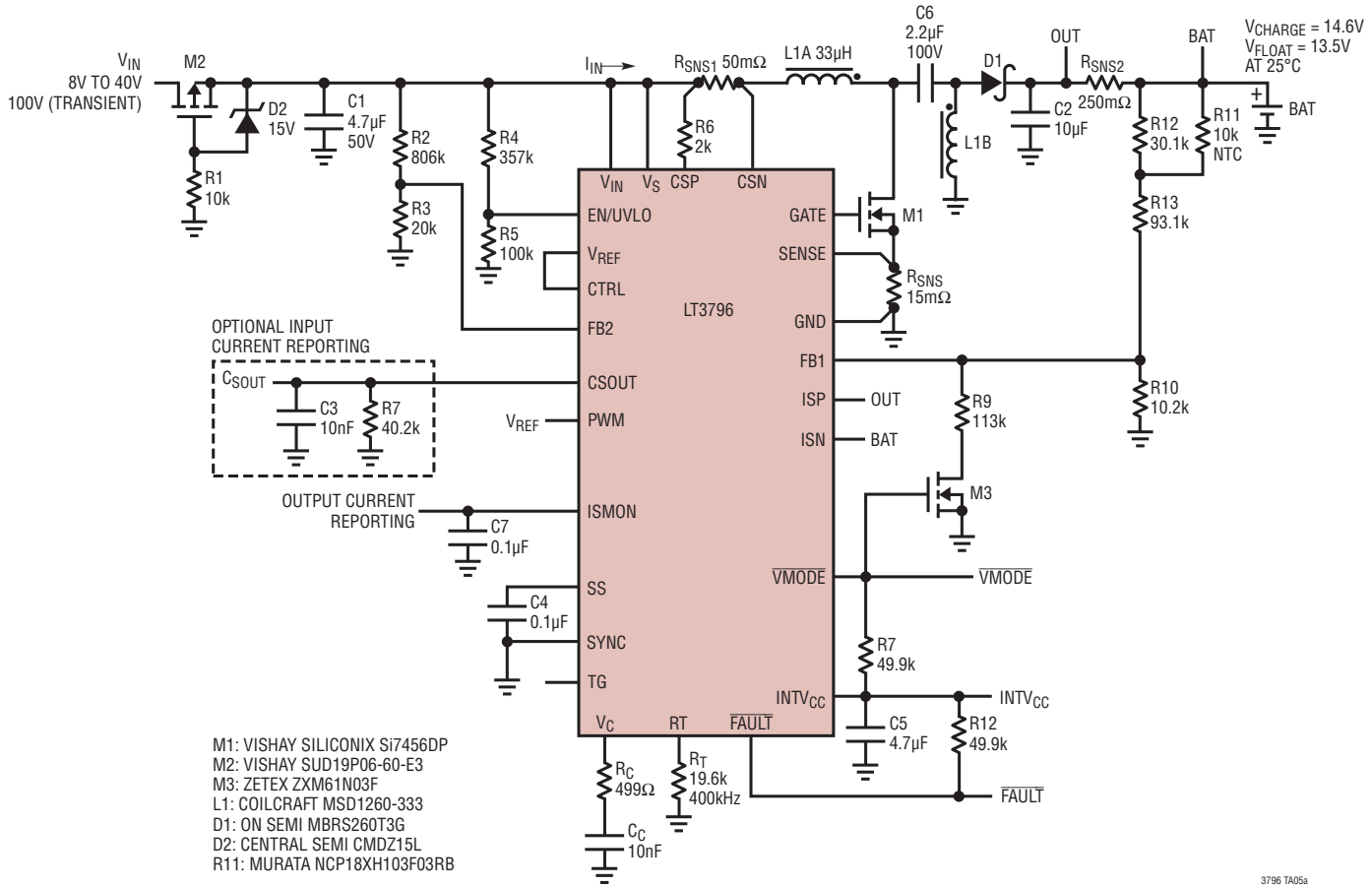


Efficiency vs V_{IN}

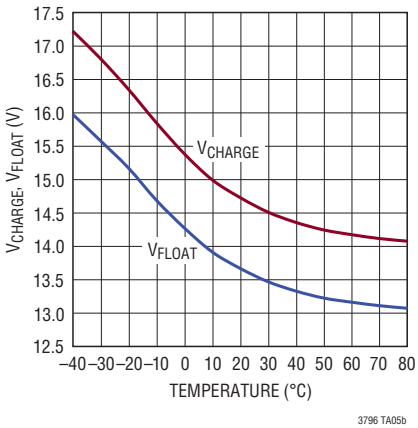


TYPICAL APPLICATIONS

SEPIC Sealed Lead Acid (SLA) Battery Charger

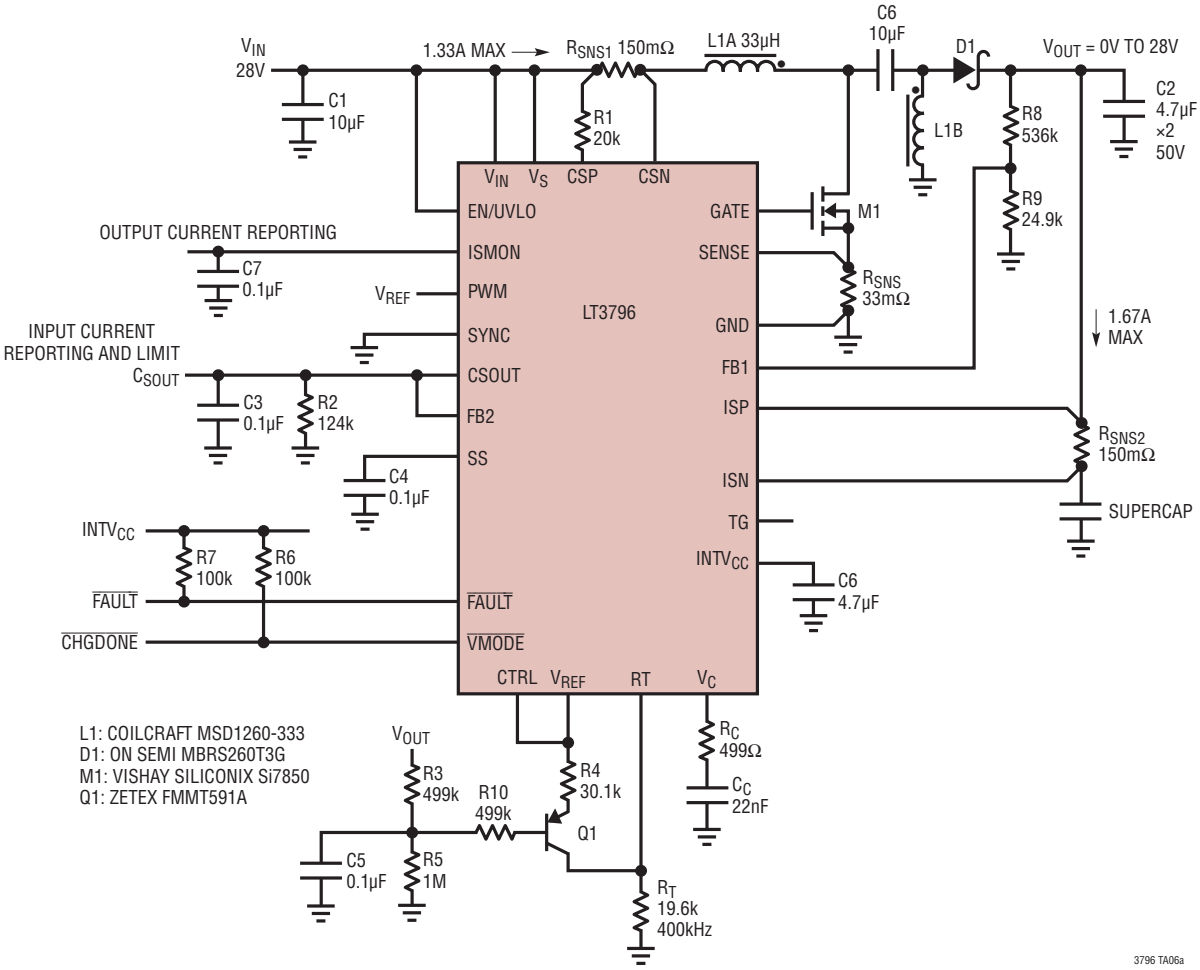


VCHARGE, VFLOAT vs Temperature

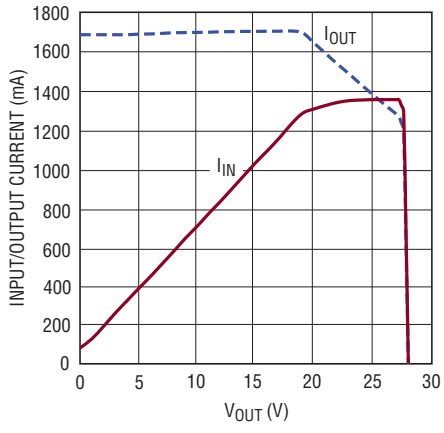


TYPICAL APPLICATIONS

28V_{IN} to 28V SuperCap Charger with Input Current Limit and Charge Done Flag

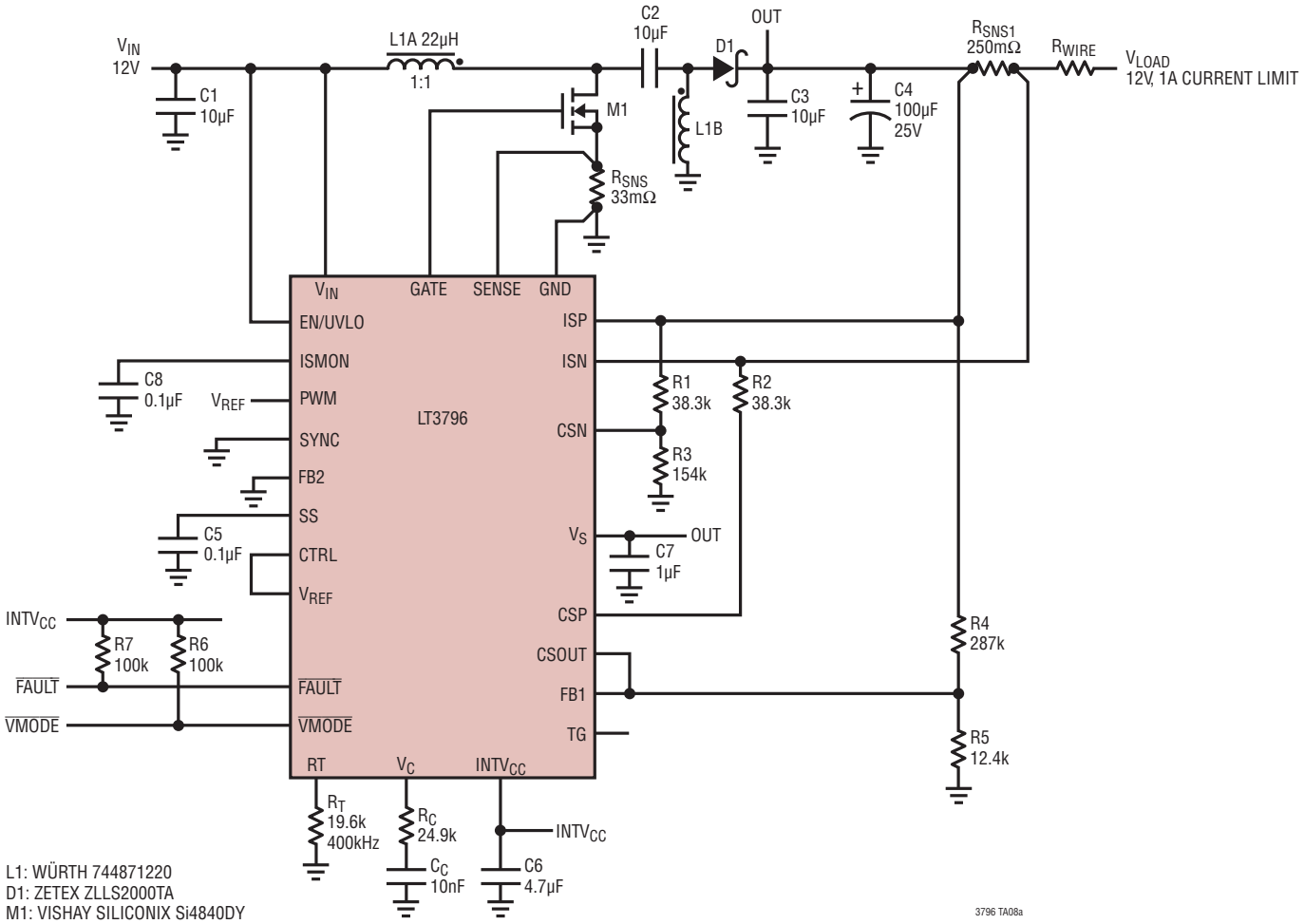


Input and Output Current vs Output Voltage



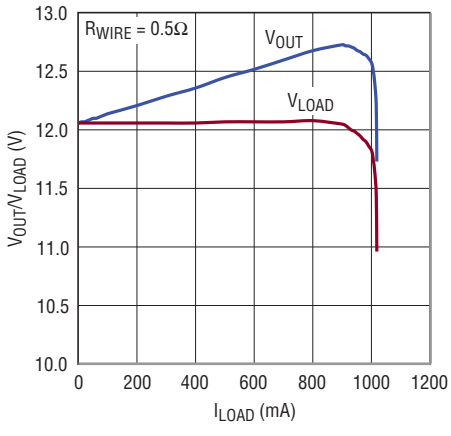
TYPICAL APPLICATIONS

SEPIC Converter with R_{WIRE} Compensation and Output Current Limit

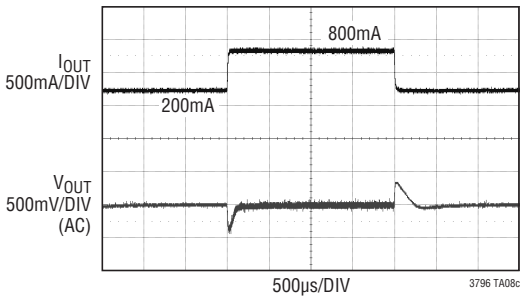


L1: WÜRTH 744871220
D1: ZETEX ZLLS2000TA
M1: VISHAY SILICONIX Si4840DY

Line Impedance Compensation

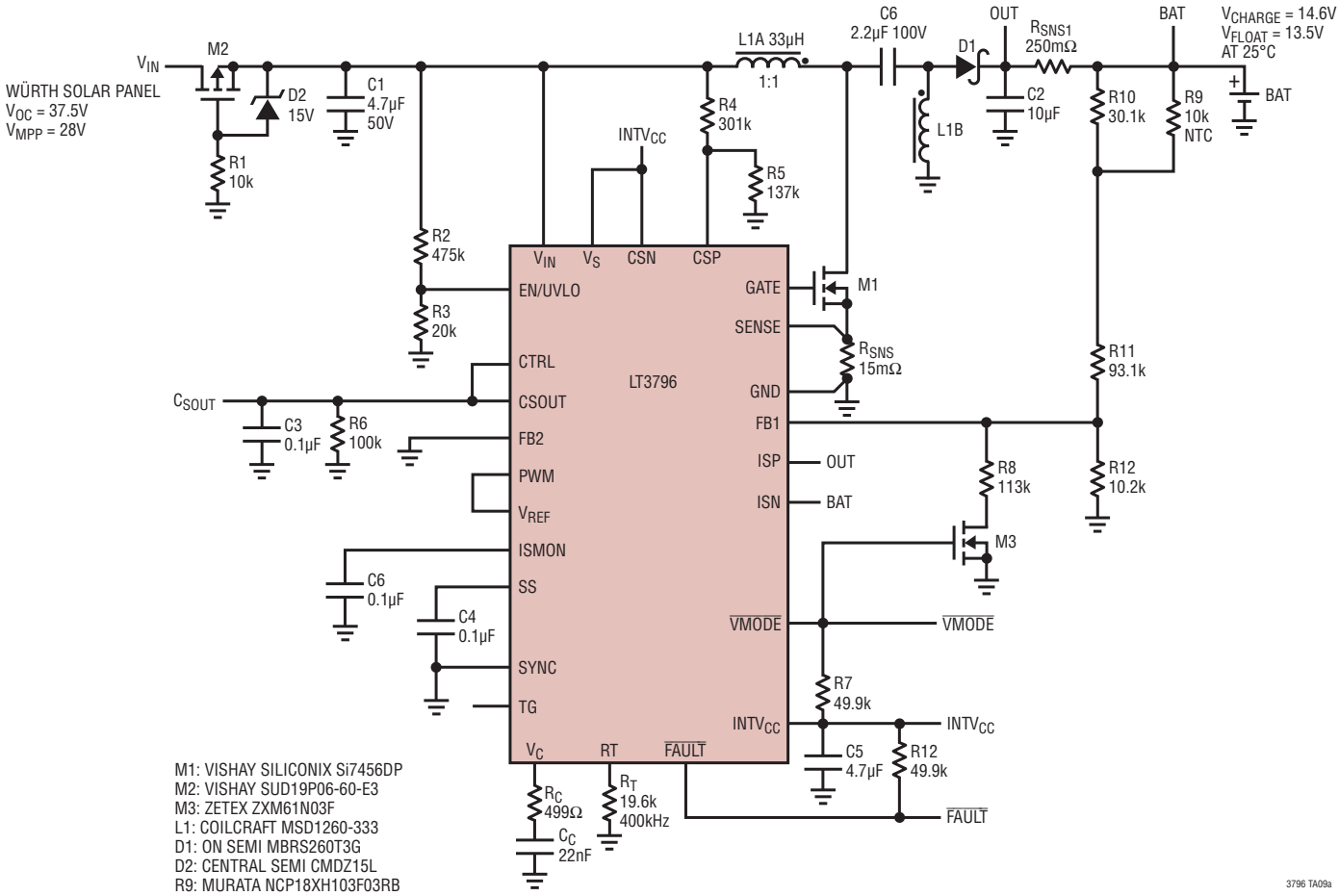


Load Step Response

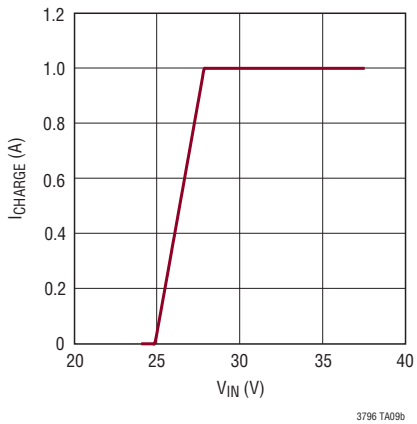


TYPICAL APPLICATIONS

Solar Panel Driven SLA Battery Charger with Maximum Power Point Tracking



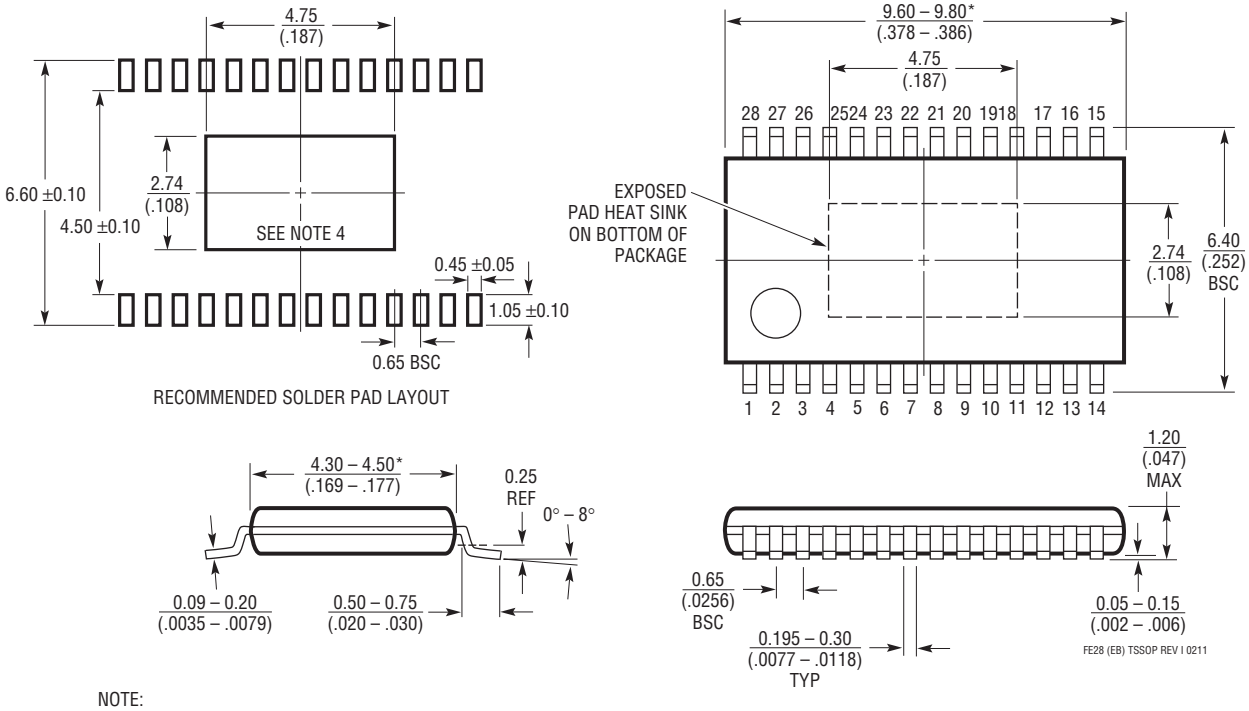
ICHARGE vs VIN



PACKAGE DESCRIPTION

Please refer to http://www.linear.com/designtools/packaging/ for the most recent package drawings.

FE Package
28-Lead Plastic TSSOP (4.4mm)
(Reference LTC DWG # 05-08-1663 Rev I)
Exposed Pad Variation EB

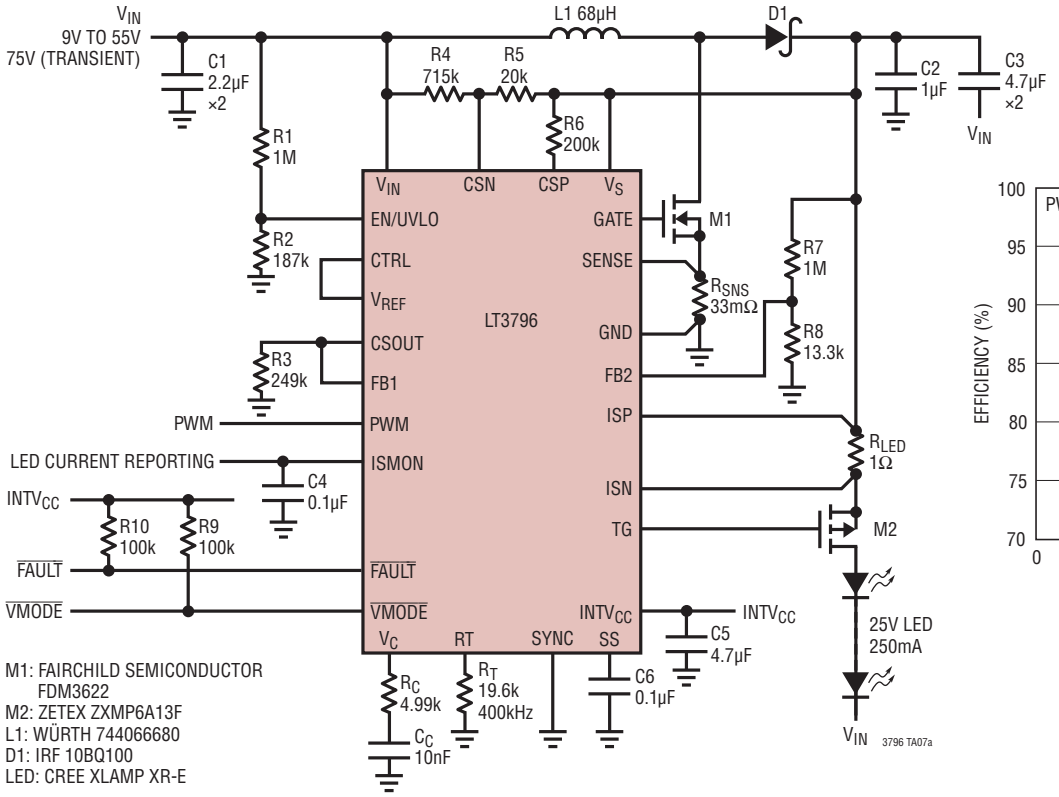


NOTE:
1. CONTROLLING DIMENSION: MILLIMETERS
2. DIMENSIONS ARE IN $\frac{\text{MILLIMETERS}}{\text{(INCHES)}}$
3. DRAWING NOT TO SCALE
4. RECOMMENDED MINIMUM PCB METAL SIZE FOR EXPOSED PAD ATTACHMENT

*DIMENSIONS DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.150mm (.006") PER SIDE

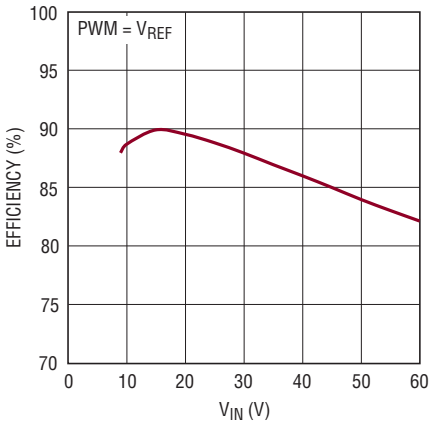
TYPICAL APPLICATION

Buck-Boost Mode LED Driver with Open LED Clamp and Output Voltage Limit



M1: FAIRCHILD SEMICONDUCTOR
FDM3622
M2: ZETEX ZXMP6A13F
L1: WÜRTH 744066680
D1: IRF 10BQ100
LED: CREE XLAMP XR-E

Efficiency vs V_{IN}



RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LT3791	60V, Synchronous Buck-Boost 1MHz LED Controller	V_{IN}: 4.7V to 60V, V_{OUT} Range: 0V to 60V, True Color PWM, Analog = 100:1, I_{SD} < 1µA, TSSOP-38E Package
LT3755/LT3755-1 LT3755-2	High Side 60V, 1MHz LED Controller with True Color 3,000:1 PWM Dimming	V_{IN}: 4.5V to 40V, V_{OUT} Range: 5V to 60V, True Color PWM, Analog = 3000:1, I_{SD} < 1µA, 3mm × 3mm QFN-16, MSOP-16E Packages
LT3756/LT3756-1 LT3756-2	High Side 100V, 1MHz LED Controller with True Color 3,000:1 PWM Dimming	V_{IN}: 6V to 100V, V_{OUT} Range: 5V to 100V, True Color PWM, Analog = 3000:1, I_{SD} < 1µA, 3mm × 3mm QFN-16, MSOP-16E Packages
LT3743	Synchronous Step-Down 20A LED Driver with Three-State LED Current Control	V_{IN}: 5.5V to 36V, V_{OUT} Range: 5.5V to 35V, True Color PWM, Analog = 3000:1, I_{SD} < 1µA, 4mm × 5mm QFN-28, TSSOP-28E Packages
LTC3780	High Efficiency, Synchronous, 4-Switch Buck-Boost Controller	V_{IN}: 4V to 36V, V_{OUT} Range: 0.8V to 30V, I_{SD} < 55µA, SSOP-24, QFN-32 Packages
LTC3789	High Efficiency, Synchronous, 4-Switch Buck-Boost Controller	V_{IN}: 4V to 38V, V_{OUT} Range: 0.8V to 38V, I_{SD} < 40µA, 4mm × 5mm QFN-28, SSOP-28 Packages
LT3517	1.3A, 2.5MHz High Current LED Driver with 3,000:1 Dimming	V_{IN}: 3V to 30V, True Color PWM, Analog = 3000:1, I_{SD} < 1µA, 4mm × 4mm QFN-16 Package
LT3518	2.3A, 2.5MHz High Current LED Driver with 3,000:1 Dimming	V_{IN}: 3V to 30V, True Color PWM, Analog = 3000:1, I_{SD} < 1µA, 4mm × 4mm QFN-16 Package
LT3474/LT3474-1	36V, 1A (ILED), 2MHz, Step-Down LED Driver	V_{IN}: 4V to 36V, V_{OUT} Range = 13.5V, True Color PWM = 400:1, I_{SD} < 1µA, TSSOP-16E Package
LT3475/LT3475-1	Dual 1.5A(ILED), 36V, 2MHz, Step-Down LED Driver	V_{IN}: 4V to 36V, V_{OUT} Range = 13.5V, True Color PWM, Analog = 3000:1, I_{SD} < 1µA, TSSOP-20E Package

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LT 0412 • PRINTED IN USA