3851 Group (Built-in 24 KB or more ROM)

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER

REJ03B0066-0101Z
Rev.1.01
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DESCRIPTION

The 3851 group (built-in 24 KB or more ROM) is the 8-bit microcomputer based on the 740 family core technology.

The 3851 group (built-in 24 KB or more ROM) is designed for the household products and office automation equipment and includes serial I/O functions, 8-bit timer, I^2C-BUS interface, and A-D converter.

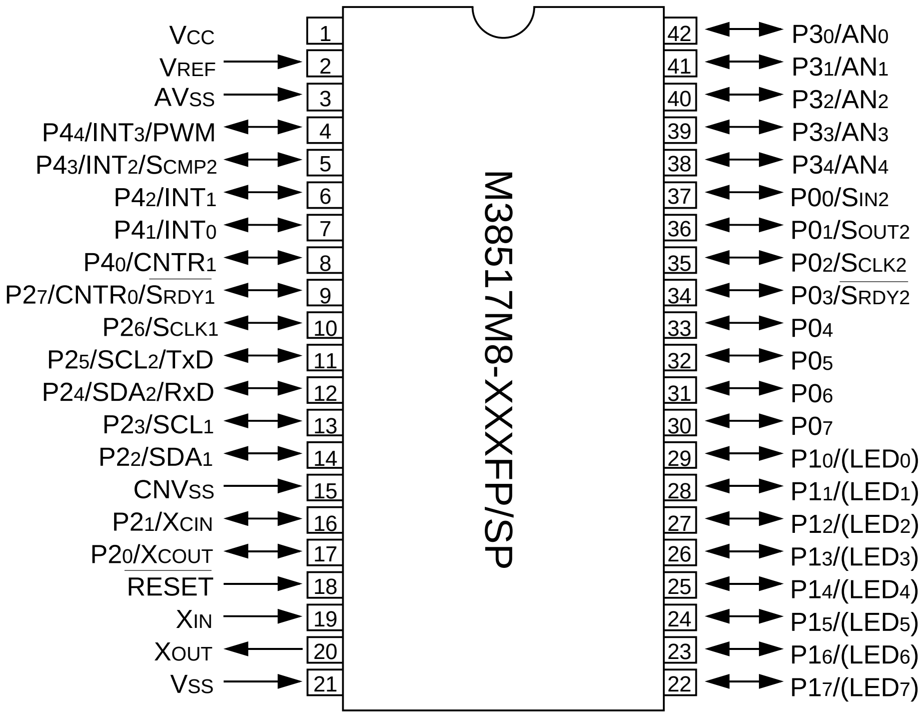
FEATURES

- Basic machine-language instructions 71
- Minimum instruction execution time .... 0.5 µs
  (at 8 MHz oscillation frequency)
- Memory size
  ROM .... 24K to 32K bytes
  RAM .... 640 to 1K bytes
- Programmable input/output ports 34
- Interrupts .... 17 sources, 16 vectors
- Timers .... 8-bit X 4
- Serial I/O1 .... 8-bit X 1(UART or Clock-synchronized)
- Serial I/O2 .... 8-bit X 1(Clock-synchronized)
- Multi-master I^2C-BUS interface .... 1 channel
- PWM .... 8-bit X 1
- A-D converter ....10-bit X 5 channels
- Watchdog timer .... 16-bit X 1
- Clock generating circuit .... Built-in 2 circuits
  (connect to external ceramic resonator or quartz-crystal oscillator)
- Power source voltage
  In high-speed mode .... 4.0 to 5.5 V
  (at 8 MHz oscillation frequency)
  In middle-speed mode .... 2.7 to 5.5 V
  (at 8 MHz oscillation frequency)
  In low-speed mode.. 2.7 to 5.5 V
  (at 32 kHz oscillation frequency)
- Power dissipation
  In high-speed mode .... 34 mW
  (at 8 MHz oscillation frequency, at 5 V power source voltage)
  In low-speed mode
  Except M38517F8FP/SP .... 60 µW
  M38517F8FP/SP .... 450 µW
  (at 32 kHz oscillation frequency, at 3 V power source voltage)
- Operating temperature range ....–20 to 85°C

APPLICATION

Office automation equipment, FA equipment, Household products, Consumer electronics, etc.

PIN CONFIGURATION (TOP VIEW)



Package type : FP .... 42P2R-A/E (42-pin plastic-molded SSOP)
Package type : SP .... 42P4B (42-pin plastic-molded SDIP)

Fig. 1 M38517M8-XXXFP/SP pin configuration

FUNCTIONAL BLOCK

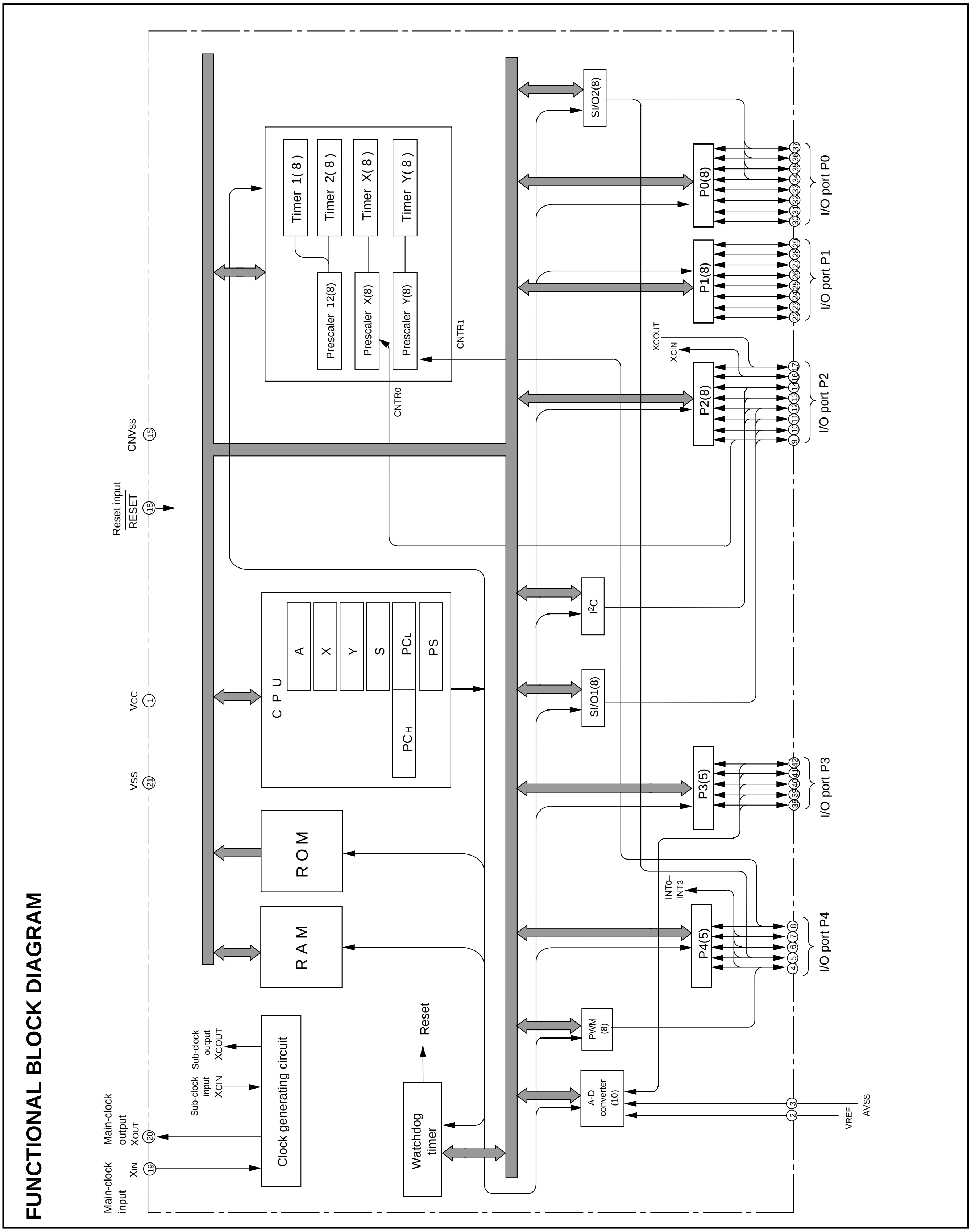


Fig.2 Functional block diagram

Table 1 Pin description

Pin	Name	Functions	Function except a port function
Vcc, Vss	Power source	•Apply voltage of 2.7 V – 5.5 V to Vcc, and 0 V to Vss.	
CNVss	CNVss input	•This pin controls the operation mode of the chip. •Normally connected to Vss.	
VREF	Reference voltage input	•Reference voltage input pin for A-D converter.	
AVss	Analog power source input	•Analog power source input pin for A-D converter. •Connect to Vss.	
$\overline{\text{RESET}}$	Reset input	•Reset input pin for active “L”.	
XIN	Clock input	•Input and output pins for the clock generating circuit. •Connect a ceramic resonator or quartz-crystal oscillator between the XIN and XOUT pins to set the oscillation frequency. •When an external clock is used, connect the clock source to the XIN pin and leave the XOUT pin open.	
XOUT	Clock output		
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/$\overline{\text{SRDY2}}$	I/O port P0	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •CMOS 3-state output structure. •P10 to P17 (8 bits) are enabled to output large current for LED drive.	• Serial I/O2 function pin
P04–P07			
P10–P17	I/O port P1		
P20/XCOUT P21/XCIN	I/O port P2	•8-bit CMOS I/O port. •I/O direction register allows each pin to be individually programmed as either input or output. •CMOS compatible input level. •P22 to P25 can be switched between CMOS compatible input level or SMBUS input level in the I^{2}C-BUS interface function. •P20, P21, P24 to P27: CMOS3-state output structure. •P24, P25: N-channel open-drain structure in the I^{2}C-BUS interface function. •P22, P23: N-channel open-drain structure.	• Sub-clock generating circuit I/O pins (connect a resonator)
P22/SDA1 P23/SCL1			• I^{2}C-BUS interface function pins
P24/SDA2/RxD P25/SCL2/TxD			• I^{2}C-BUS interface function pin/ Serial I/O1 function pins
P26/SCLK1			• Serial I/O1 function pin
P27/CNTR0/ $\overline{\text{SRDY1}}$			• Serial I/O1 function pin/Timer X function pin
P30/AN0–P34/AN4	I/O port P3	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• A-D converter input pin
P40/CNTR1	I/O port P4	•8-bit CMOS I/O port with the same function as port P0. •CMOS compatible input level. •CMOS 3-state output structure.	• Timer Y function pin
P41/INT0 P42/INT1			• Interrupt input pins
P43/INT2/SCMP2			• Interrupt input pin • SCMP2 output pin
P44/INT3/PWM			• Interrupt input pin • PWM output pin

PART NUMBERING

Product name M3851 4 M 6 – XXX SP

Package type
SP : 42P4B
FP : 42P2R-A/E
SS : 42S1B-A

ROM number
Omitted in One Time PROM version shipped in blank, EPROM version, and flash memory version.

– : standard
Omitted in One Time PROM version shipped in blank, EPROM version, and flash memory version.

ROM/PROM/Flash memory size

1 : 4096 bytes	9 : 36864 bytes
2 : 8192 bytes	A : 40960 bytes
3 : 12288 bytes	B : 45056 bytes
4 : 16384 bytes	C : 49152 bytes
5 : 20480 bytes	D : 53248 bytes
6 : 24576 bytes	E : 57344 bytes
7 : 28672 bytes	F : 61440 bytes
8 : 32768 bytes	

The first 128 bytes and the last 2 bytes of ROM are reserved areas ; they cannot be used as a user's ROM area.
However, they can be programmed or erased in the flash memory version, so that the users can use them.

Memory type
M : Mask ROM version
E : EPROM or One Time PROM version
F : Flash memory version

RAM size

0 : 192 bytes	5 : 768 bytes
1 : 256 bytes	6 : 896 bytes
2 : 384 bytes	7 : 1024 bytes
3 : 512 bytes	8 : 1536 bytes
4 : 640 bytes	9 : 2048 bytes

Fig. 3 Part numbering

GROUP EXPANSION

Renesas plans to expand the 3851 group (built-in 24 KB or more ROM) as follows.

Memory Type

Support for mask ROM, One Time PROM, and flash memory versions.

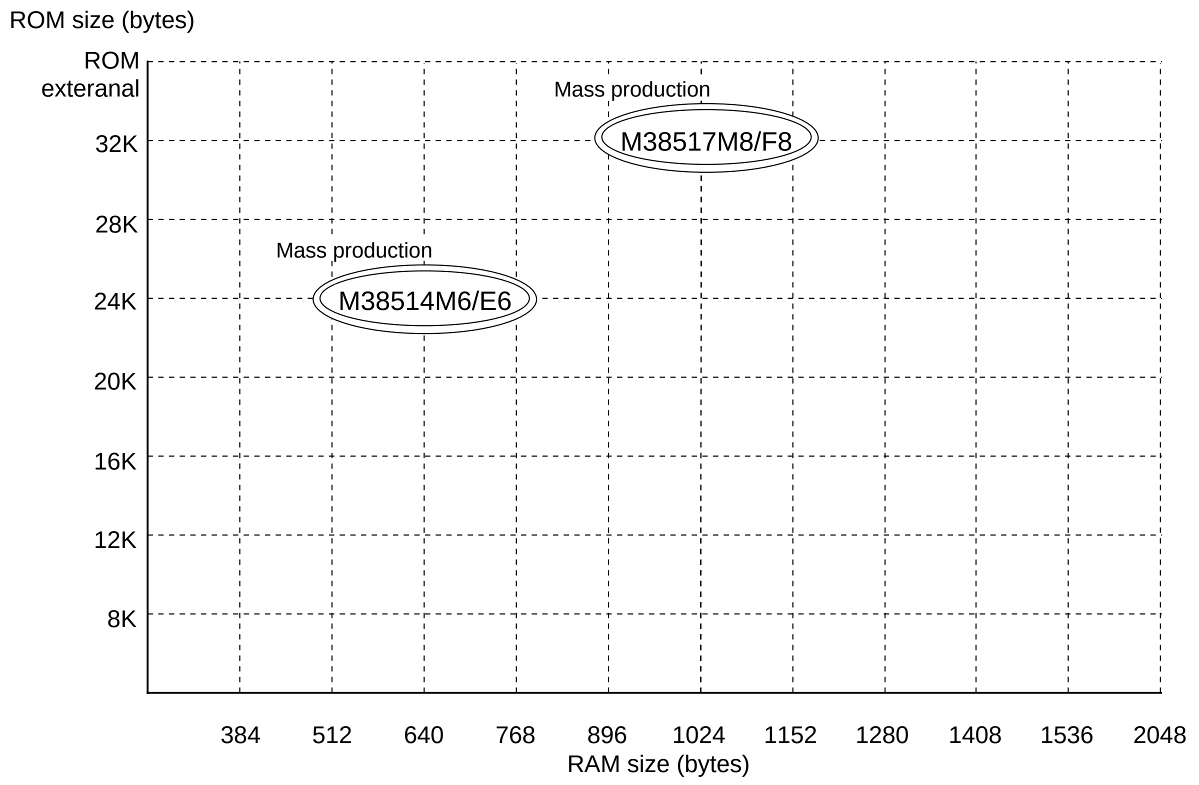
Memory Size

Flash memory size .... 32 K bytes
Mask ROM size .... 24 K to 32 K bytes
One Time PROM size .... 24 K bytes
RAM size .... 640 to 1 K bytes

Packages

42P4B .... 42-pin shrink plastic-molded DIP
42P2R-A/E .... 42-pin plastic-molded SSOP
42S1B-A .... 42-pin shrink ceramic DIP (EPROM version)

Memory Expansion Plan



Products under development or planning: the development schedule and specification may be revised without notice.
The development of planning products may be stopped.

Fig. 4 Memory expansion plan

Currently planning products are listed below.

Table 2 Support products

Product name	ROM size (bytes) ROM size for User in ( )	RAM size (bytes)	Package	Remarks
M38514M6-XXXSP	24576 (24446)	640	42P4B	Mask ROM version
M38514E6-XXXSP				One Time PROM version
M38514E6SP				One Time PROM version (blank)
M38514E6SS			42S1B-A	EPROM version
M38514M6-XXXFP			42P2R-A/E	Mask ROM version
M38514E6-XXXFP				One Time PROM version
M38514E6FP				One Time PROM version (blank)

Table 3 3851 group (built-in 16 KB ROM) and 3851 group (built-in 24 KB or more ROM) corresponding products

3851 group (built-in 16 KB ROM)	3851 group (built-in 24 KB or more ROM)
M38513M4-XXXFP/SP	M38514M6-XXXFP/SP
M38513E4-XXXFP/SP	M38514E6-XXXFP/SP
M38513E4FP/SP	M38514E6FP/SP
M38513E4SS	M38514E6SS
	M38517M8-XXXFP/SP
	M38517F8FP/SP

Table 4 Differences between 3851 group (built-in 16 KB ROM) and 3851 group (built-in 24 KB or more ROM)

	3851 group (built-in 16 KB ROM)	3851 group (built-in 24 KB or more ROM)
Serial I/O	1: Serial I/O (UART or Clock-synchronized)	2: Serial I/O1 (UART or Clock-synchronized) Serial I/O2 (Clock-synchronized)
A-D converter	Unserviceable in low-speed mode	Serviceable in low-speed mode
Large current port	5: $P1_3$–$P1_7$	8: $P1_0$–$P1_7$

Notes on differences between 3851 group (built-in 16 KB ROM), 3851 group (built-in 24 KB or more ROM)

(1) The absolute maximum ratings of 3851 group (built-in 24 KB or more ROM) is smaller than that of 3851 group (built-in 16 KB ROM).

•Power source voltage Vcc = –0.3 to 6.5 V

•CNVss input voltage

V_I = –0.3 to Vcc +0.3 V (M38514M6, M38517M8)

VI = –0.3 to 6.5 V (M38517F8)

(2) The oscillation circuit constants of X_{IN}-X_{OUT}, X_{CIN}-X_{COUT} may be some differences between 3851 group (built-in 16 KB ROM) and 3851 group (built-in 24 KB or more ROM).

(3) Do not write any data to the reserved area and the reserved bit. (Do not change the contents after reset.)

(4) Fix bit 3 of the CPU mode register to “1”.

(5) Be sure to perform the termination of unused pins.

FUNCTIONAL DESCRIPTION
CENTRAL PROCESSING UNIT (CPU)

The 3851 group uses the standard 740 Family instruction set. Refer to the table of 740 Family addressing modes and machine instructions or the 740 Family Software Manual for details on the instruction set.

Machine-resident 740 Family instructions are as follows:

The FST and SLW instructions cannot be used.

The STP, WIT, MUL, and DIV instructions can be used.

[Accumulator (A)]

The accumulator is an 8-bit register. Data operations such as data transfer, etc., are executed mainly through the accumulator.

[Index Register X (X)]

The index register X is an 8-bit register. In the index addressing modes, the value of the OPERAND is added to the contents of register X and specifies the real address.

[Index Register Y (Y)]

The index register Y is an 8-bit register. In partial instruction, the value of the OPERAND is added to the contents of register Y and specifies the real address.

[Stack Pointer (S)]

The stack pointer is an 8-bit register used during subroutine calls and interrupts. This register indicates start address of stored area (stack) for storing registers during subroutine calls and interrupts.

The low-order 8 bits of the stack address are determined by the contents of the stack pointer. The high-order 8 bits of the stack address are determined by the stack page selection bit. If the stack page selection bit is “0” , the high-order 8 bits becomes “00_{16}”. If the stack page selection bit is “1”, the high-order 8 bits becomes “01_{16}”.

The operations of pushing register contents onto the stack and popping them from the stack are shown in Figure 6.

Store registers other than those described in Figure 6 with program when the user needs them during interrupts or subroutine calls.

[Program Counter (PC)]

The program counter is a 16-bit counter consisting of two 8-bit registers PC_H and PC_L. It is used to indicate the address of the next instruction to be executed.

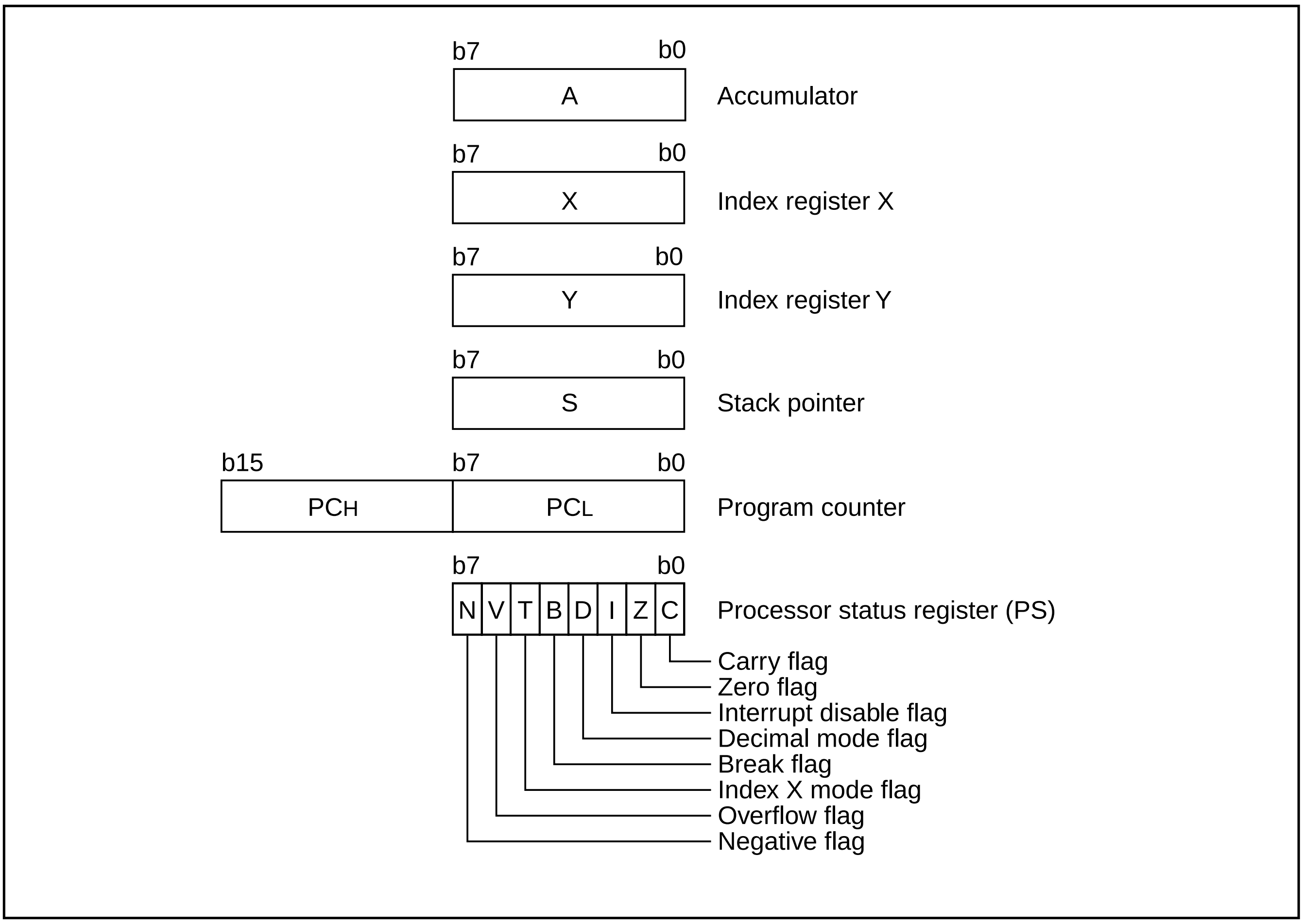


Fig. 5 740 Family CPU register structure

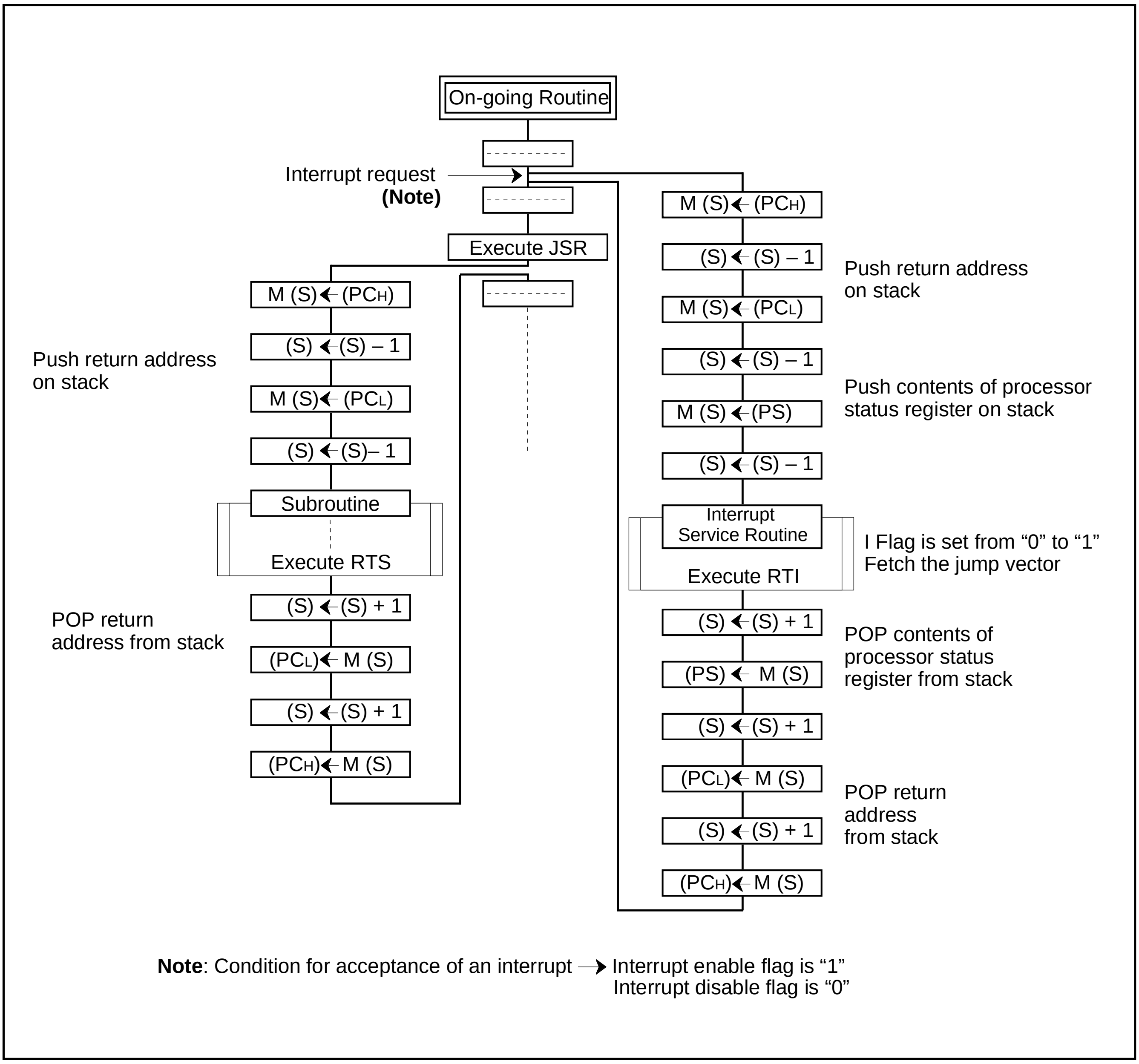


Fig. 6 Register push and pop at interrupt generation and subroutine call

Table 5 Push and pop instructions of accumulator or processor status register

	Push instruction to stack	Pop instruction from stack
Accumulator	PHA	PLA
Processor status register	PHP	PLP

[Processor status register (PS)]

The processor status register is an 8-bit register consisting of 5 flags which indicate the status of the processor after an arithmetic operation and 3 flags which decide MCU operation. Branch operations can be performed by testing the Carry (C) flag , Zero (Z) flag, Overflow (V) flag, or the Negative (N) flag. In decimal mode, the Z, V, N flags are not valid.

•Bit 0: Carry flag (C)
The C flag contains a carry or borrow generated by the arithmetic logic unit (ALU) immediately after an arithmetic operation. It can also be changed by a shift or rotate instruction.

•Bit 1: Zero flag (Z)
The Z flag is set if the result of an immediate arithmetic operation or a data transfer is "0", and cleared if the result is anything other than "0".

•Bit 2: Interrupt disable flag (I)
The I flag disables all interrupts except for the interrupt generated by the BRK instruction.
Interrupts are disabled when the I flag is "1".

•Bit 3: Decimal mode flag (D)
The D flag determines whether additions and subtractions are executed in binary or decimal. Binary arithmetic is executed when this flag is "0"; decimal arithmetic is executed when it is "1". Decimal correction is automatic in decimal mode. Only the ADC and SBC instructions can be used for decimal arithmetic.

•Bit 4: Break flag (B)
The B flag is used to indicate that the current interrupt was generated by the BRK instruction. The BRK flag in the processor status register is always "0". When the BRK instruction is used to generate an interrupt, the processor status register is pushed onto the stack with the break flag set to "1".

•Bit 5: Index X mode flag (T)
When the T flag is "0", arithmetic operations are performed between accumulator and memory. When the T flag is "1", direct arithmetic operations and direct data transfers are enabled between memory locations.

•Bit 6: Overflow flag (V)
The V flag is used during the addition or subtraction of one byte of signed data. It is set if the result exceeds +127 to -128. When the BIT instruction is executed, bit 6 of the memory location operated on by the BIT instruction is stored in the overflow flag.

•Bit 7: Negative flag (N)
The N flag is set if the result of an arithmetic operation or data transfer is negative. When the BIT instruction is executed, bit 7 of the memory location operated on by the BIT instruction is stored in the negative flag.

Table 6 Set and clear instructions of each bit of processor status register

	C flag	Z flag	I flag	D flag	B flag	T flag	V flag	N flag
Set instruction	SEC	–	SEI	SED	–	SET	–	–
Clear instruction	CLC	–	CLI	CLD	–	CLT	CLV	–

[CPU Mode Register (CPUM)] $003B_{16}$

The CPU mode register contains the stack page selection bit, etc.
The CPU mode register is allocated at address $003B_{16}$.

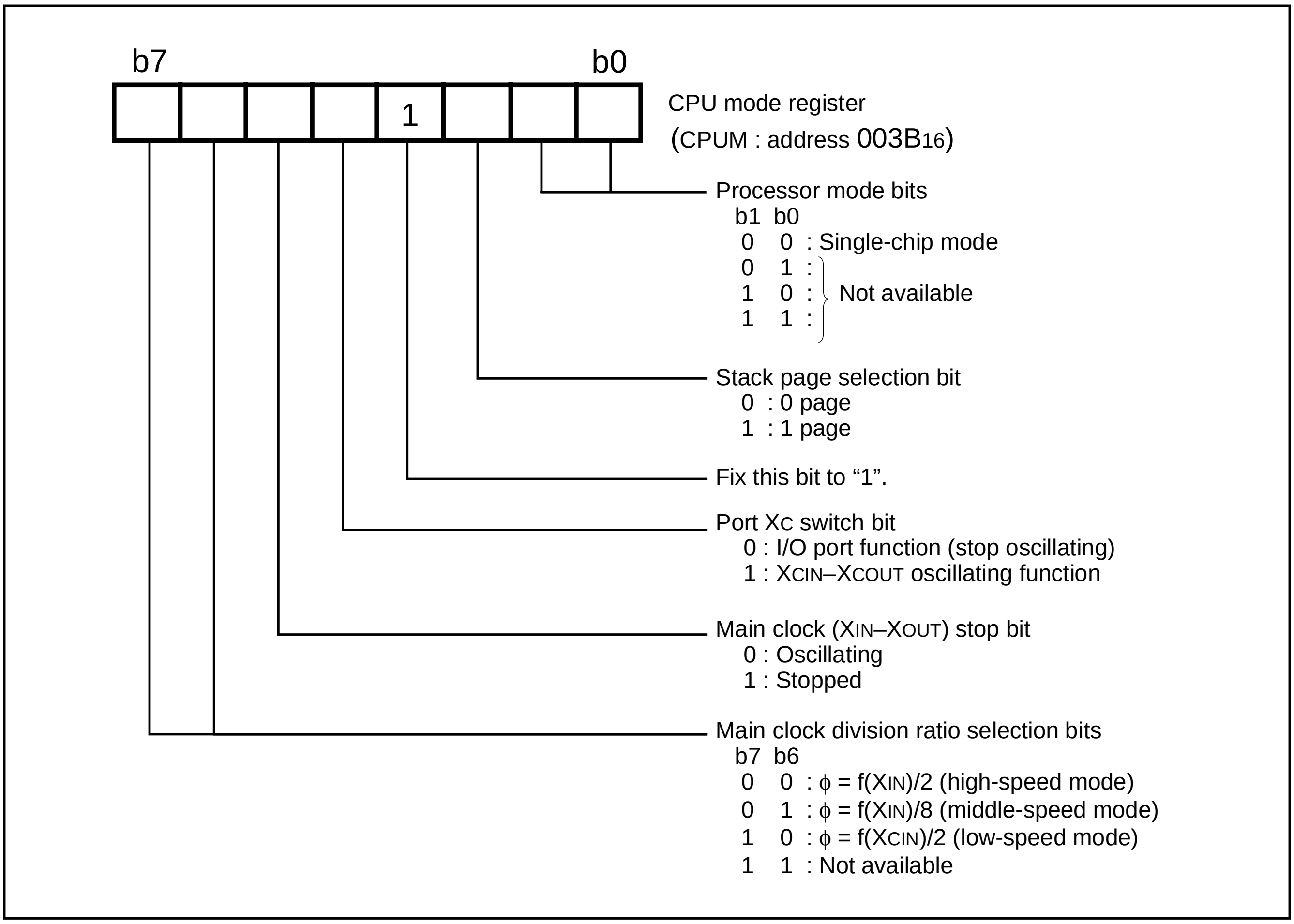


Fig. 7 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The Special Function Register area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

The first 128 bytes and the last 2 bytes of ROM are reserved for device testing and the rest is user area for storing programs.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

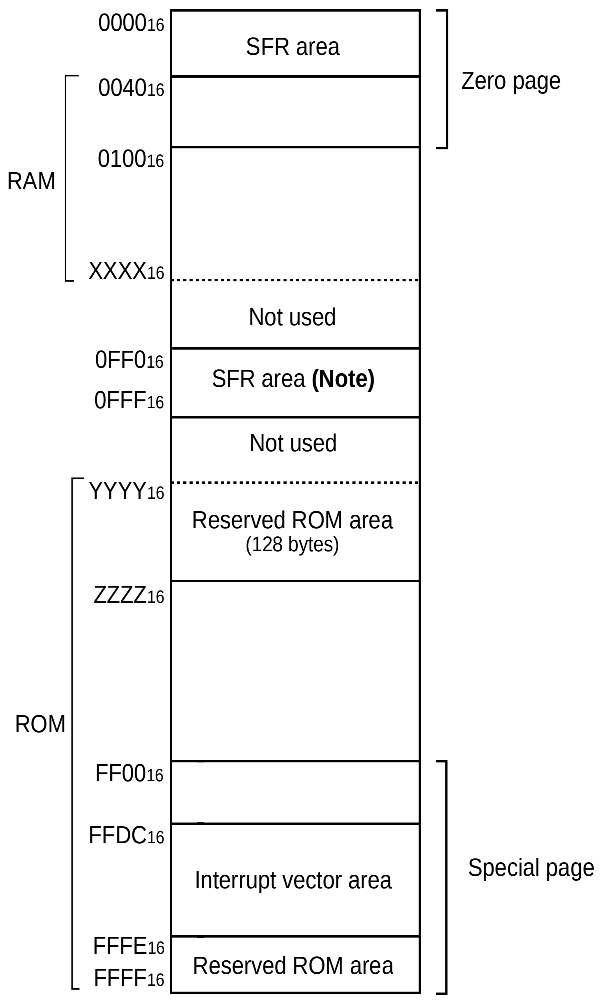
Access to this area with only 2 bytes is possible in the special page addressing mode.

RAM area

RAM size (bytes)	Address XXXX$_{16}$
192	00FF$_{16}$
256	013F$_{16}$
384	01BF$_{16}$
512	023F$_{16}$
640	02BF$_{16}$
768	033F$_{16}$
896	03BF$_{16}$
1024	043F$_{16}$
1536	063F$_{16}$
2048	083F$_{16}$

ROM area

ROM size (bytes)	Address YYYY$_{16}$	Address ZZZZ$_{16}$
4096	F000$_{16}$	F080$_{16}$
8192	E000$_{16}$	E080$_{16}$
12288	D000$_{16}$	D080$_{16}$
16384	C000$_{16}$	C080$_{16}$
20480	B000$_{16}$	B080$_{16}$
24576	A000$_{16}$	A080$_{16}$
28672	9000$_{16}$	9080$_{16}$
32768	8000$_{16}$	8080$_{16}$
36864	7000$_{16}$	7080$_{16}$
40960	6000$_{16}$	6080$_{16}$
45056	5000$_{16}$	5080$_{16}$
49152	4000$_{16}$	4080$_{16}$
53248	3000$_{16}$	3080$_{16}$
57344	2000$_{16}$	2080$_{16}$
61440	1000$_{16}$	1080$_{16}$



Note: Flash memory version only

Fig. 8 Memory map diagram

Address	Register	Address	Register
0000_{16}	Port P0 (P0)	0020_{16}	Prescaler 12 (PRE12)
0001_{16}	Port P0 direction register (P0D)	0021_{16}	Timer 1 (T1)
0002_{16}	Port P1 (P1)	0022_{16}	Timer 2 (T2)
0003_{16}	Port P1 direction register (P1D)	0023_{16}	Timer XY mode register (TM)
0004_{16}	Port P2 (P2)	0024_{16}	Prescaler X (PREX)
0005_{16}	Port P2 direction register (P2D)	0025_{16}	Timer X (TX)
0006_{16}	Port P3 (P3)	0026_{16}	Prescaler Y (PREY)
0007_{16}	Port P3 direction register (P3D)	0027_{16}	Timer Y (TY)
0008_{16}	Port P4 (P4)	0028_{16}	Timer count source selection register (TCSS)
0009_{16}	Port P4 direction register (P4D)	0029_{16}	
$000A_{16}$		$002A_{16}$	
$000B_{16}$		$002B_{16}$	I^2C data shift register (S0)
$000C_{16}$		$002C_{16}$	I^2C address register (S0D)
$000D_{16}$		$002D_{16}$	I^2C status register (S1)
$000E_{16}$		$002E_{16}$	I^2C control register (S1D)
$000F_{16}$		$002F_{16}$	I^2C clock control register (S2)
0010_{16}		0030_{16}	I^2C start/stop condition control register (S2D)
0011_{16}		0031_{16}	Reserved ✻
0012_{16}	Reserved ✻	0032_{16}	
0013_{16}	Reserved ✻	0033_{16}	
0014_{16}	Reserved ✻	0034_{16}	A-D control register (ADCON)
0015_{16}	Serial I/O2 control register 1 (SIO2CON1)	0035_{16}	A-D conversion low-order register (ADL)
0016_{16}	Serial I/O2 control register 2 (SIO2CON2)	0036_{16}	A-D conversion high-order register (ADH)
0017_{16}	Serial I/O2 register (SIO2)	0037_{16}	Reserved ✻
0018_{16}	Transmit/Receive buffer register (TB/RB)	0038_{16}	MISRG
0019_{16}	Serial I/O1 status register (SIOSTS)	0039_{16}	Watchdog timer control register (WDTCON)
$001A_{16}$	Serial I/O1 control register (SIOCON)	$003A_{16}$	Interrupt edge selection register (INTEDGE)
$001B_{16}$	UART control register (UARTCON)	$003B_{16}$	CPU mode register (CPUM)
$001C_{16}$	Baud rate generator (BRG)	$003C_{16}$	Interrupt request register 1 (IREQ1)
$001D_{16}$	PWM control register (PWMCON)	$003D_{16}$	Interrupt request register 2 (IREQ2)
$001E_{16}$	PWM prescaler (PREPWM)	$003E_{16}$	Interrupt control register 1 (ICON1)
$001F_{16}$	PWM register (PWM)	$003F_{16}$	Interrupt control register 2 (ICON2)
		$0FFD_{16}$	Reserved
		$0FFE_{16}$	Flash memory control register 1 (FMCR)
		$0FFF_{16}$	Reserved

✻ Reserved : Do not write any data to this addresses, because these areas are reserved.

Fig. 9 Memory map of special function register (SFR)

I/O PORTS

The I/O ports have direction registers which determine the input/output direction of each individual pin. Each bit in a direction register corresponds to one pin, and each pin can be set to be input port or output port.

When “0” is written to the bit corresponding to a pin, that pin becomes an input pin. When “1” is written to that bit, that pin becomes an output pin.

If data is read from a pin which is set to output, the value of the port output latch is read, not the value of the pin itself. Pins set to input are floating. If a pin set to input is written to, only the port output latch is written to and the pin remains floating.

Table 7 I/O port function

Pin	Name	Input/Output	I/O Structure	Non-Port Function	Related SFRs	Ref.No.
P00/SIN2 P01/SOUT2 P02/SCLK2 P03/$\overline{\text{SRDY2}}$	Port P0	Input/output, individual bits	CMOS compatible input level CMOS 3-state output	Serial I/O2 function I/O	Serial I/O2 control register	(1) (2) (3) (4)
P04–P07						(5)
P10–P17	Port P1					
P20/XCOUT P21/XCIN	Port P2			Sub-clock generating circuit	CPU mode register	(6) (7)
P22/SDA1 P23/SCL1			CMOS compatible input level CMOS/SMBUS input level (when selecting I^{2}C-BUS interface function) N-channel open-drain output	I^{2}C-BUS interface function I/O	I^{2}C control register	(8) (9)
P24/SDA2/RxD P25/SCL2/TxD			CMOS compatible input level CMOS/SMBUS input level (when selecting I^{2}C-BUS interface function) CMOS 3-state output N-channel open-drain output (when selecting I^{2}C-BUS interface function)	I^{2}C-BUS interface function I/O Serial I/O1 function I/O	I^{2}C control register Serial I/O1 control register	(10) (11)
P26/SCLK1			CMOS compatible input level CMOS 3-state output	Serial I/O1 function I/O	Serial I/O1 control register	(12)
P27/CNTR0/$\overline{\text{SRDY1}}$				Serial I/O1 function I/O Timer X function I/O	Serial I/O1 control register Timer XY mode register	(13)
P30/AN0–P34/AN4	Port P3			A-D conversion input	A-D control register	(14)
P40/CNTR1	Port P4			Timer Y function I/O	Timer XY mode register	(15)
P41/INT0 P42/INT1				External interrupt input	Interrupt edge selection register	(16)
P43/INT2/SCMP2				External interrupt input SCMP2 output	Interrupt edge selection register Serial I/O2 control register	(17)
P44/INT3/PWM				External interrupt input PWM output	Interrupt edge selection register PWM control register	(18)

Note: When reading bit 5, 6, or 7 of ports P3 and P4, the contents are undefined.

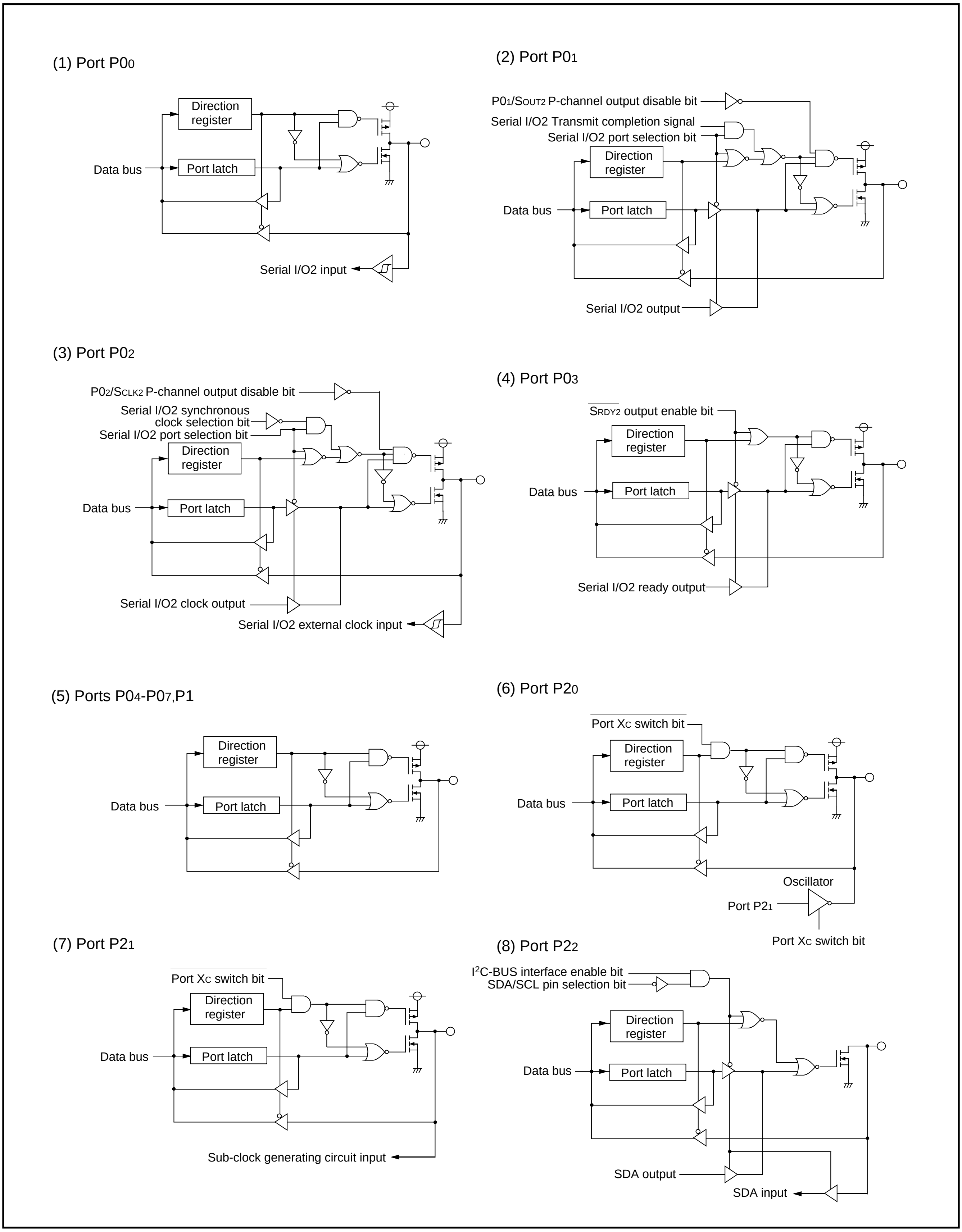


Fig. 10 Port block diagram (1)

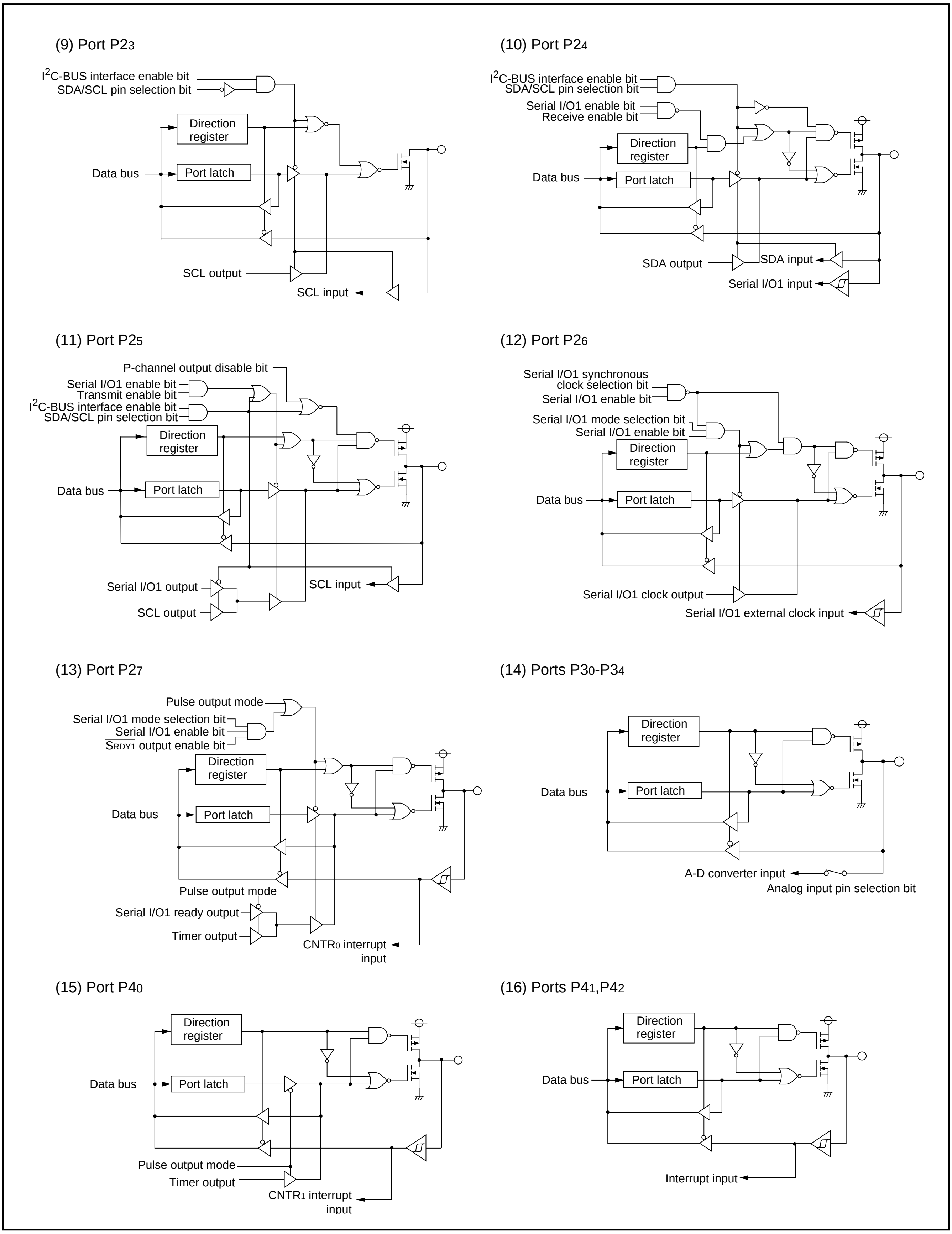


Fig. 11 Port block diagram (2)

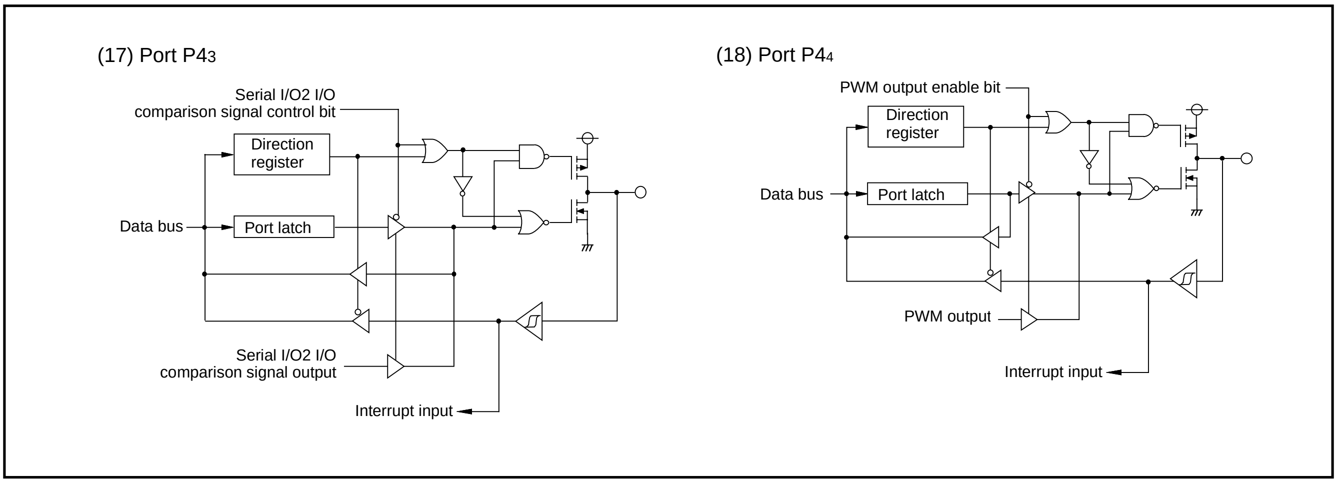


Fig. 12 Port block diagram (3)

INTERRUPTS

Interrupts occur by 17 : seven external, nine internal, and one software.

Interrupt Control

Each interrupt is controlled by an interrupt request bit, an interrupt enable bit, and the interrupt disable flag except for the software interrupt set by the BRK instruction. An interrupt occurs if the corresponding interrupt request and enable bits are “1” and the interrupt disable flag is “0”.
Interrupt enable bits can be set or cleared by software.
Interrupt request bits can be cleared by software, but cannot be set by software.
The BRK instruction cannot be disabled with any flag or bit. The I (interrupt disable) flag disables all interrupts except the BRK instruction interrupt.
When several interrupts occur at the same time, the interrupts are received according to priority.

Interrupt Operation

By acceptance of an interrupt, the following operations are automatically performed:

1. The contents of the program counter and the processor status register are automatically pushed onto the stack.
2. The interrupt disable flag is set and the corresponding interrupt request bit is cleared.
3. The interrupt jump destination address is read from the vector table into the program counter.

■Notes

When setting the followings, the interrupt request bit may be set to “1”.

•When setting external interrupt active edge
Related register: Interrupt edge selection register (address $003A_{16}$)
Timer XY mode register (address 0023_{16})

•When switching interrupt sources of an interrupt vector address where two or more interrupt sources are allocated
Related register: Interrupt edge selection register (address $003A_{16}$)

When not requiring for the interrupt occurrence synchronized with these setting, take the following sequence.

(1) Set the corresponding interrupt enable bit to “0” (disabled).
(2) Set the interrupt edge select bit or the interrupt source select bit.
(3) Set the corresponding interrupt request bit to “0” after 1 or more instructions have been executed.
(4) Set the corresponding interrupt enable bit to “1” (enabled).

Table 8 Interrupt vector addresses and priority

Interrupt Source	Priority	Vector Addresses **(Note 1)**		Interrupt Request Generating Conditions	Remarks
		High	Low		
Reset (Note 2)	1	FFFD$_{16}$	FFFC$_{16}$	At reset	Non-maskable
INT$_0$	2	FFFB$_{16}$	FFFA$_{16}$	At detection of either rising or falling edge of INT$_0$ input	External interrupt (active edge selectable)
SCL, SDA	3	FFF9$_{16}$	FFF8$_{16}$	At detection of either rising or falling edge of SCL or SDA input	External interrupt (active edge selectable)
INT$_1$	4	FFF7$_{16}$	FFF6$_{16}$	At detection of either rising or falling edge of INT$_1$ input	External interrupt (active edge selectable)
INT$_2$	5	FFF5$_{16}$	FFF4$_{16}$	At detection of either rising or falling edge of INT$_2$ input	External interrupt (active edge selectable)
INT$_3$	6	FFF3$_{16}$	FFF2$_{16}$	At detection of either rising or falling edge of INT$_3$ input	External interrupt (active edge selectable)
Serial I/O2				At completion of serial I/O2 data reception/transmission	Switch by Serial I/O2/INT$_3$ interrupt source bit
I^{2}C	7	FFF1$_{16}$	FFF0$_{16}$	At completion of data transfer	
Timer X	8	FFEF$_{16}$	FFEE$_{16}$	At timer X underflow	
Timer Y	9	FFED$_{16}$	FFEC$_{16}$	At timer Y underflow	
Timer 1	10	FFEB$_{16}$	FFEA$_{16}$	At timer 1 underflow	STP release timer underflow
Timer 2	11	FFE9$_{16}$	FFE8$_{16}$	At timer 2 underflow	
Serial I/O1 reception	12	FFE7$_{16}$	FFE6$_{16}$	At completion of serial I/O1 data reception	Valid when serial I/O is selected
Serial I/O1 transmission	13	FFE5$_{16}$	FFE4$_{16}$	At completion of serial I/O1 transfer shift or when transmission buffer is empty	Valid when serial I/O is selected
CNTR$_0$	14	FFE3$_{16}$	FFE2$_{16}$	At detection of either rising or falling edge of CNTR$_0$ input	External interrupt (active edge selectable)
CNTR$_1$	15	FFE1$_{16}$	FFE0$_{16}$	At detection of either rising or falling edge of CNTR$_1$ input	External interrupt (active edge selectable)
A-D converter	16	FFDF$_{16}$	FFDE$_{16}$	At completion of A-D conversion	
BRK instruction	17	FFDD$_{16}$	FFDC$_{16}$	At BRK instruction execution	Non-maskable software interrupt

Notes 1: Vector addresses contain interrupt jump destination addresses.
2: Reset function in the same way as an interrupt with the highest priority.

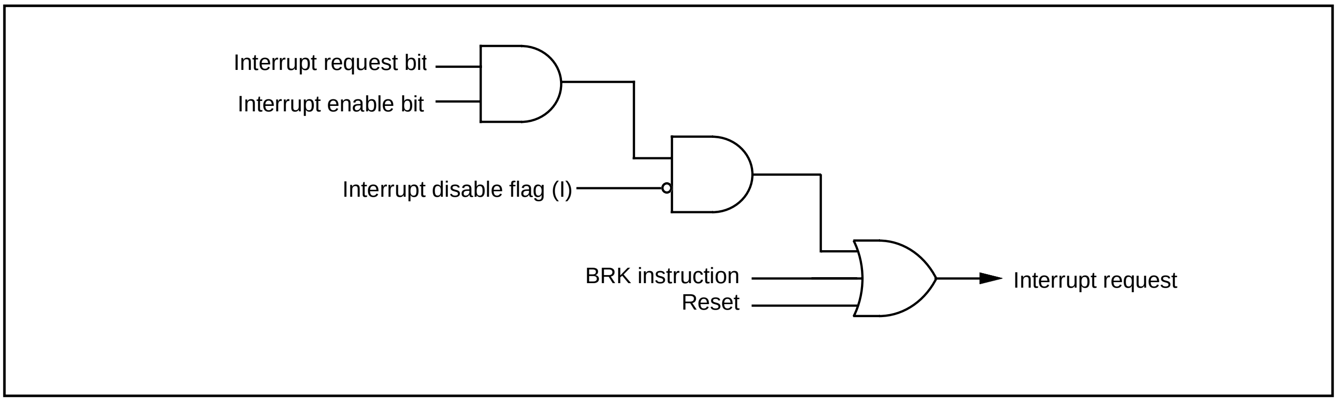


Fig. 13 Interrupt control

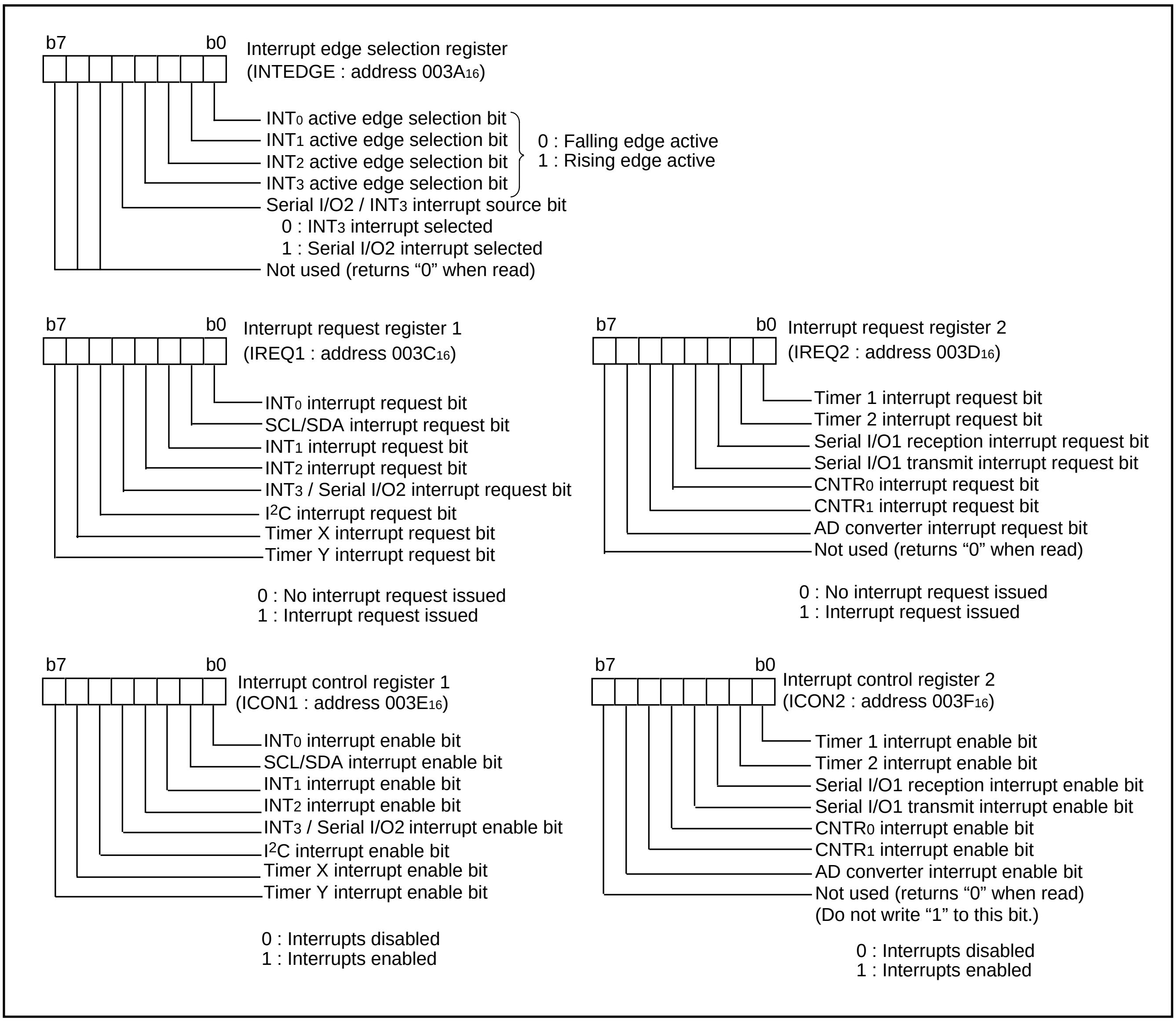


Fig. 14 Structure of interrupt-related registers

TIMERS

The 3851 group (built-in 24 KB or more ROM) has four timers: timer X, timer Y, timer 1, and timer 2.

The division ratio of each timer or prescaler is given by 1/(n + 1), where n is the value in the corresponding timer or prescaler latch.

All timers are count down. When the timer reaches "00_{16}", an underflow occurs at the next count pulse and the corresponding timer latch is reloaded into the timer and the count is continued. When a timer underflows, the interrupt request bit corresponding to that timer is set to "1".

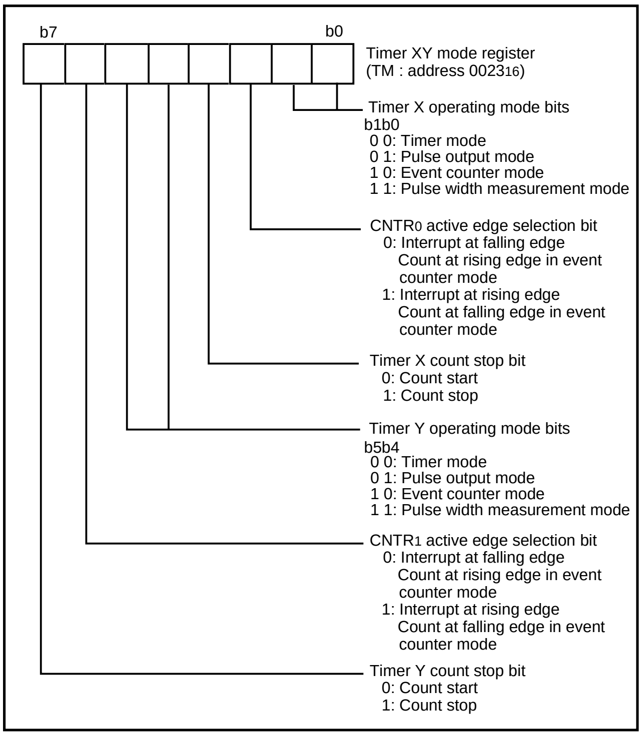


Fig. 15 Structure of timer XY mode register

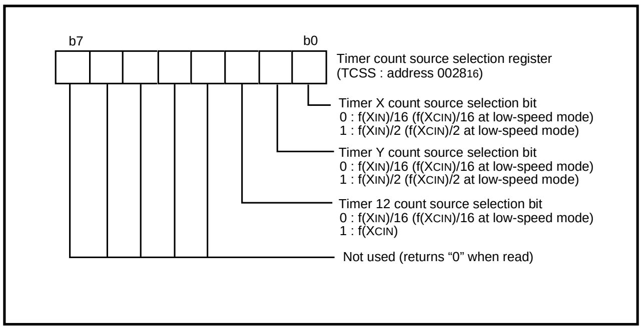


Fig. 16 Structure of timer count source selection register

Timer 1 and Timer 2

The count source of prescaler 12 is the oscillation frequency which is selected by timer 12 count source selection bit. The output of prescaler 12 is counted by timer 1 and timer 2, and a timer underflow sets the interrupt request bit.

Timer X and Timer Y

Timer X and Timer Y can each select in one of four operating modes by setting the timer XY mode register.

(1) Timer Mode

The timer counts the count source selected by Timer count source selection bit.

(2) Pulse Output Mode

The timer counts the count source selected by Timer count source selection bit. Whenever the contents of the timer reach "00_{16}", the signal output from the $CNTR_0$ (or $CNTR_1$) pin is inverted. If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", output begins at " H".

If it is "1", output starts at "L". When using a timer in this mode, set the corresponding port $P2_7$ (or port $P4_0$) direction register to output mode.

(3) Event Counter Mode

Operation in event counter mode is the same as in timer mode, except that the timer counts signals input through the $CNTR_0$ or $CNTR_1$ pin.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the rising edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

When the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the falling edge of the $CNTR_0$ (or $CNTR_1$) pin is counted.

(4) Pulse Width Measurement Mode

If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "0", the timer counts the selected signals by the count source selection bit while the $CNTR_0$ (or $CNTR_1$) pin is at "H". If the $CNTR_0$ (or $CNTR_1$) active edge selection bit is "1", the timer counts it while the $CNTR_0$ (or $CNTR_1$) pin is at "L".

The count can be stopped by setting "1" to the timer X (or timer Y) count stop bit in any mode. The corresponding interrupt request bit is set each time a timer underflows.

■Note

When switching the count source by the timer 12, X and Y count source bits, the value of timer count is altered in unconsiderable amount owing to generating of a thin pulses in the count input signals.

Therefore, select the timer count source before set the value to the prescaler and the timer.

When timer X/timer Y underflow while executing the instruction which sets "1" to the timer X/timer Y count stop bits, the timer X/timer Y interrupt request bits are set to "1". Timer X/Timer Y interrupts are received if these interrupts are enabled at this time.

The timing which interrupt is accepted has a case after the instruction which sets "1" to the count stop bit, and a case after the next instruction according to the timing of the timer underflow. When this interrupt is unnecessary, set "0" (disabled) to the interrupt enable bit and then set "1" to the count stop bit.

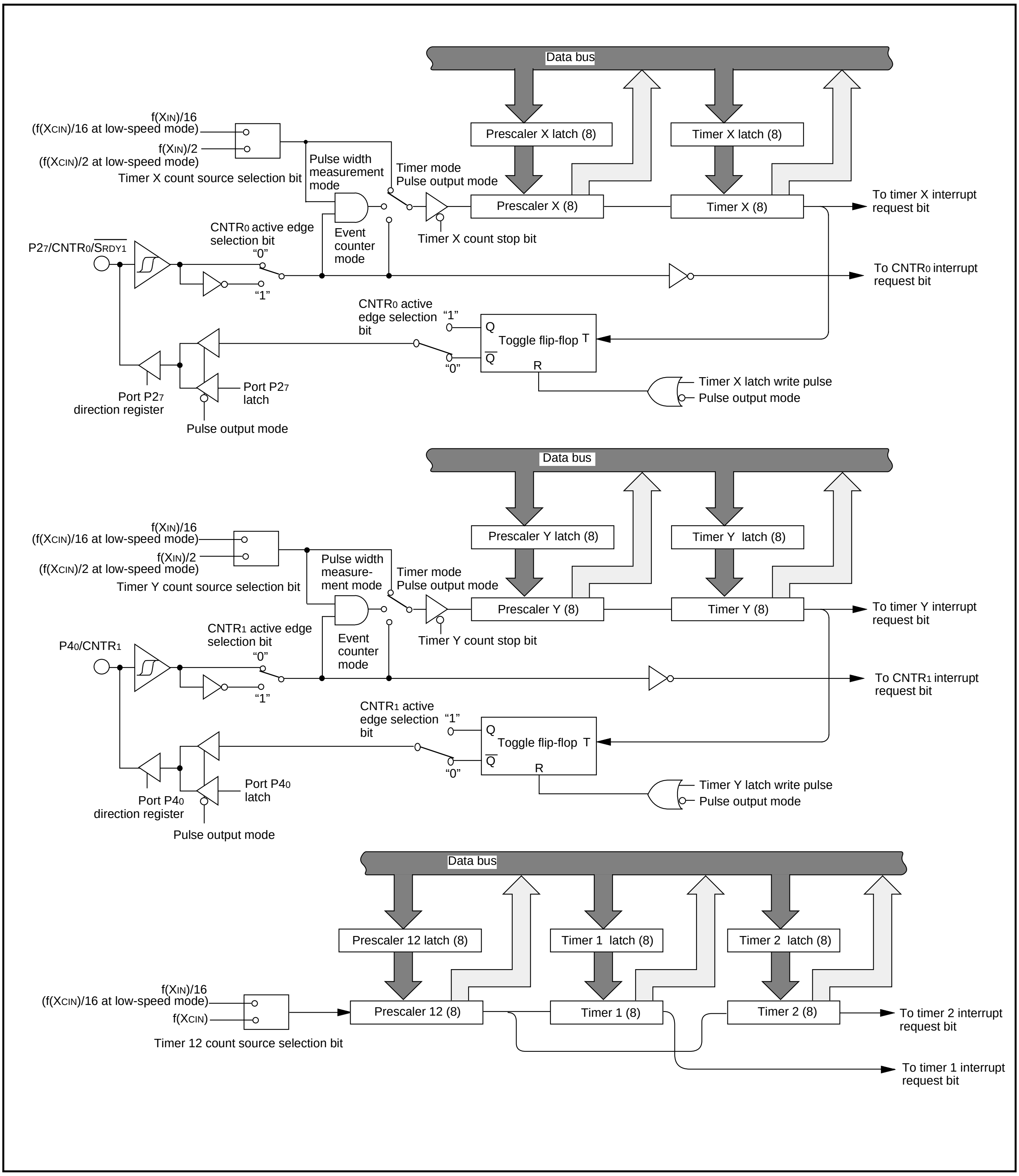


Fig. 17 Block diagram of timer X, timer Y, timer 1, and timer 2

SERIAL I/O

●SERIAL I/O1

Serial I/O1 can be used as either clock synchronous or asynchronous (UART) serial I/O. A dedicated timer is also provided for baud rate generation.

(1) Clock Synchronous Serial I/O Mode

Clock synchronous serial I/O mode can be selected by setting the serial I/O1 mode selection bit of the serial I/O1 control register (bit 6 of address $001A_{16}$) to “1”.

For clock synchronous serial I/O, the transmitter and the receiver must use the same clock. If an internal clock is used, transfer is started by a write signal to the TB/RB.

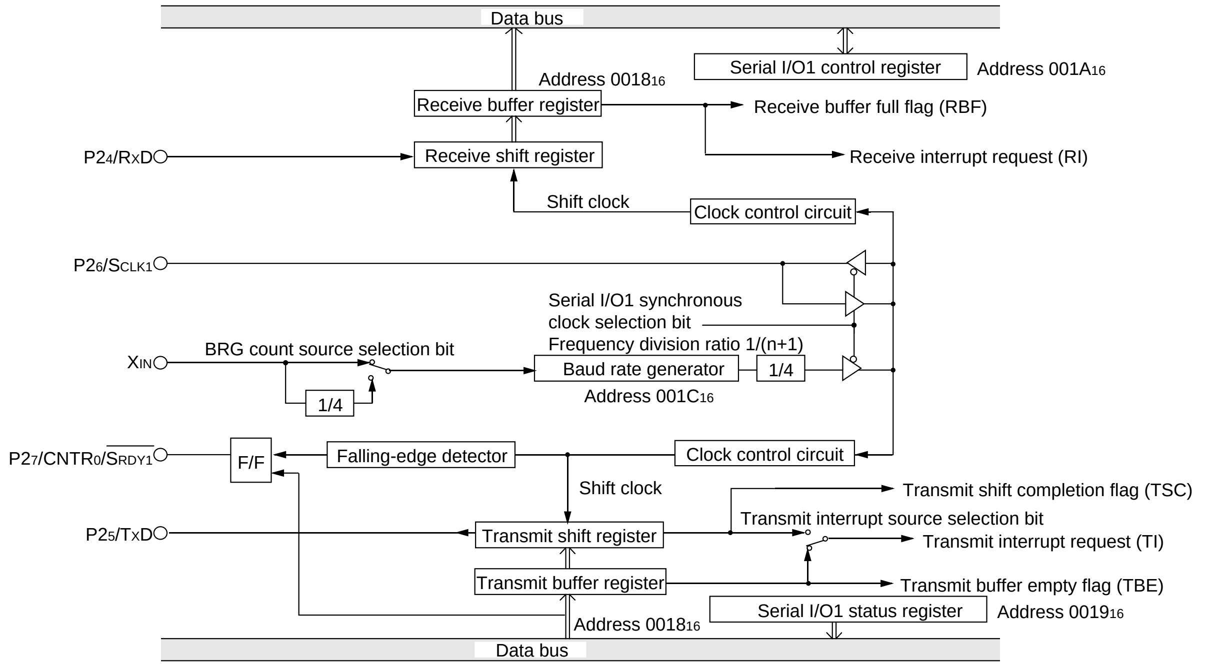
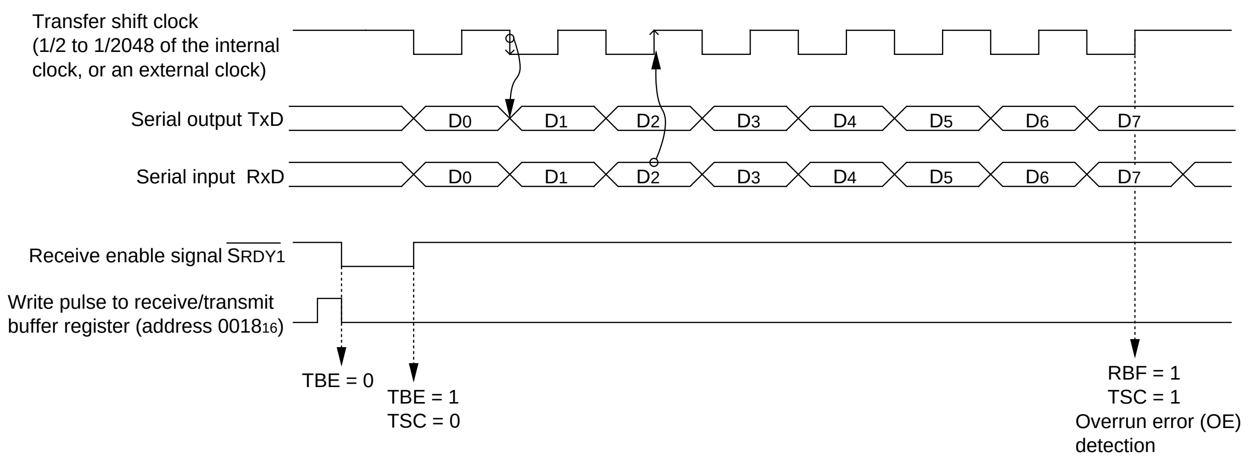


Fig. 18 Block diagram of clock synchronous serial I/O1



Notes 1: As the transmit interrupt (TI), either when the transmit buffer has emptied (TBE=1) or after the transmit shift operation has ended (TSC=1), by setting the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.

2: If data is written to the transmit buffer register when TSC=0, the transmit clock is generated continuously and serial data is output continuously from the TxD pin.

3: The receive interrupt (RI) is set when the receive buffer full flag (RBF) becomes “1” .

Fig. 19 Operation of clock synchronous serial I/O1 function

(2) Asynchronous Serial I/O (UART) Mode

Clock asynchronous serial I/O mode (UART) can be selected by clearing the serial I/O1 mode selection bit (b6) of the serial I/O1 control register to "0".

Eight serial data transfer formats can be selected, and the transfer formats used by a transmitter and receiver must be identical.

The transmit and receive shift registers each have a buffer, but the two buffers have the same address in memory. Since the shift register cannot be written to or read from directly, transmit data is written to the transmit buffer register, and receive data is read from the receive buffer register.

The transmit buffer register can also hold the next data to be transmitted, and the receive buffer register can hold a character while the next character is being received.

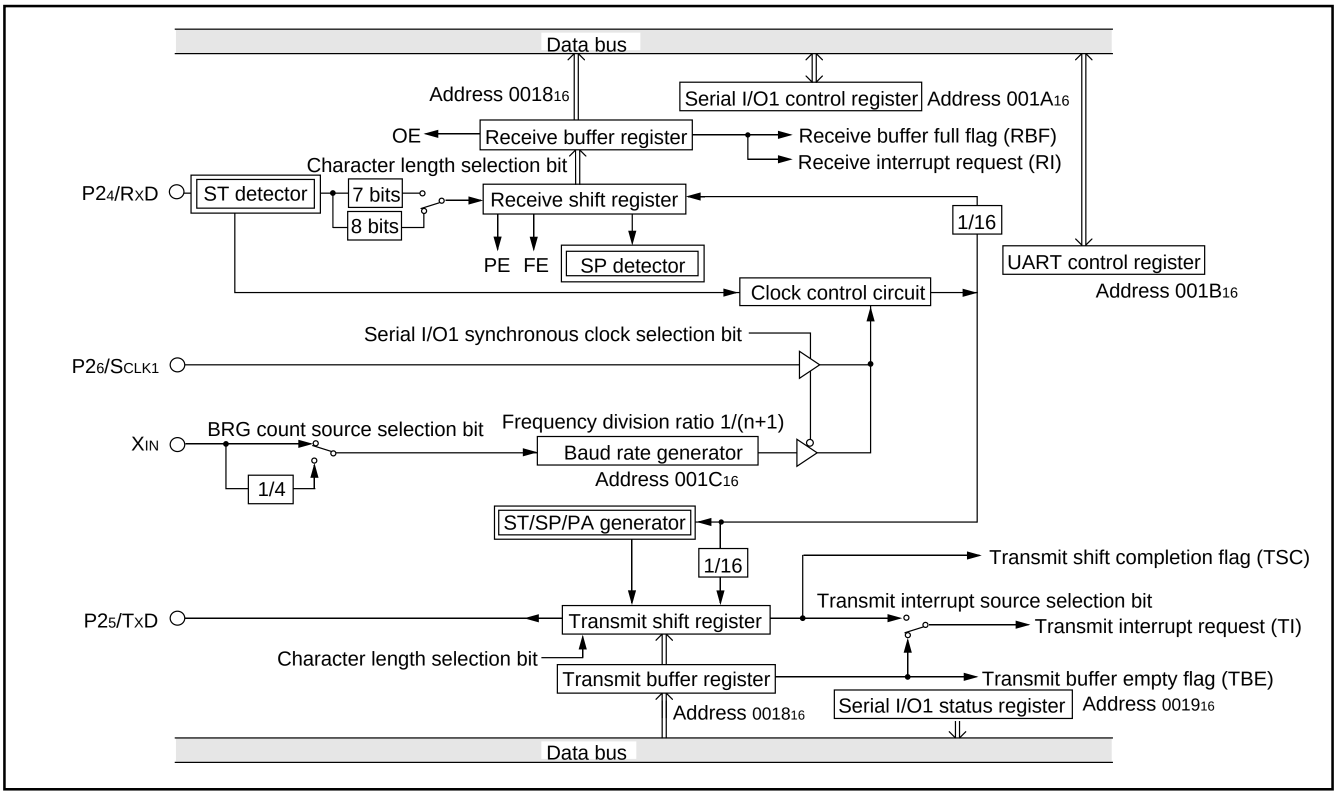
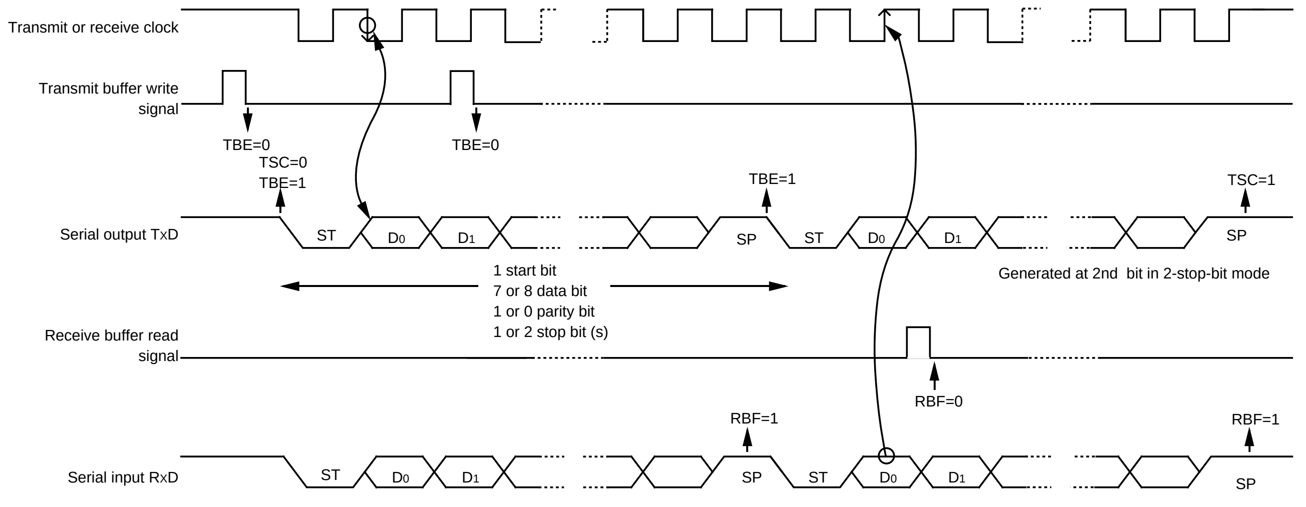


Fig. 20 Block diagram of UART serial I/O1



Notes 1: Error flag detection occurs at the same time that the RBF flag becomes “1” (at 1st stop bit, during reception).
2: As the transmit interrupt (TI), when either the TBE or TSC flag becomes “1”, can be selected to occur depending on the setting of the transmit interrupt source selection bit (TIC) of the serial I/O1 control register.
3: The receive interrupt (RI) is set when the RBF flag becomes “1”.
4: After data is written to the transmit buffer when TSC=1, 0.5 to 1.5 cycles of the data shift cycle is necessary until changing to TSC=0.

Fig. 21 Operation of UART serial I/O1 function

[Transmit Buffer Register/Receive Buffer Register (TB/RB)] 0018_{16}

The transmit buffer register and the receive buffer register are located at the same address. The transmit buffer is write-only and the receive buffer is read-only. If a character bit length is 7 bits, the MSB of data stored in the receive buffer is “0”.

[Serial I/O1 Status Register (SIOSTS)] 0019_{16}

The read-only serial I/O1 status register consists of seven flags (bits 0 to 6) which indicate the operating status of the serial I/O1 function and various errors.
Three of the flags (bits 4 to 6) are valid only in UART mode.
The receive buffer full flag (bit 1) is cleared to “0” when the receive buffer register is read.
If there is an error, it is detected at the same time that data is transferred from the receive shift register to the receive buffer register, and the receive buffer full flag is set. A write to the serial I/O1 status register clears all the error flags OE, PE, FE, and SE (bit 3 to bit 6, respectively). Writing “0” to the serial I/O1 enable bit SIOE (bit 7 of the serial I/O1 control register) also clears all the status flags, including the error flags.
Bits 0 to 6 of the serial I/O1 status register are initialized to “0” at reset, but if the transmit enable bit (bit 4) of the serial I/O1 control register has been set to “1”, the transmit shift completion flag (bit 2) and the transmit buffer empty flag (bit 0) become “1”.

[Serial I/O1 Control Register (SIOCON)] $001A_{16}$

The serial I/O1 control register consists of eight control bits for the serial I/O1 function.

[UART Control Register (UARTCON)] $001B_{16}$

The UART control register consists of four control bits (bits 0 to 3) which are valid when asynchronous serial I/O is selected and set the data format of an data transfer and one bit (bit 4) which is always valid and sets the output structure of the $P2_5$/TxD pin.

[Baud Rate Generator (BRG)] $001C_{16}$

The baud rate generator determines the baud rate for serial transfer.
The baud rate generator divides the frequency of the count source by 1/(n + 1), where n is the value written to the baud rate generator.

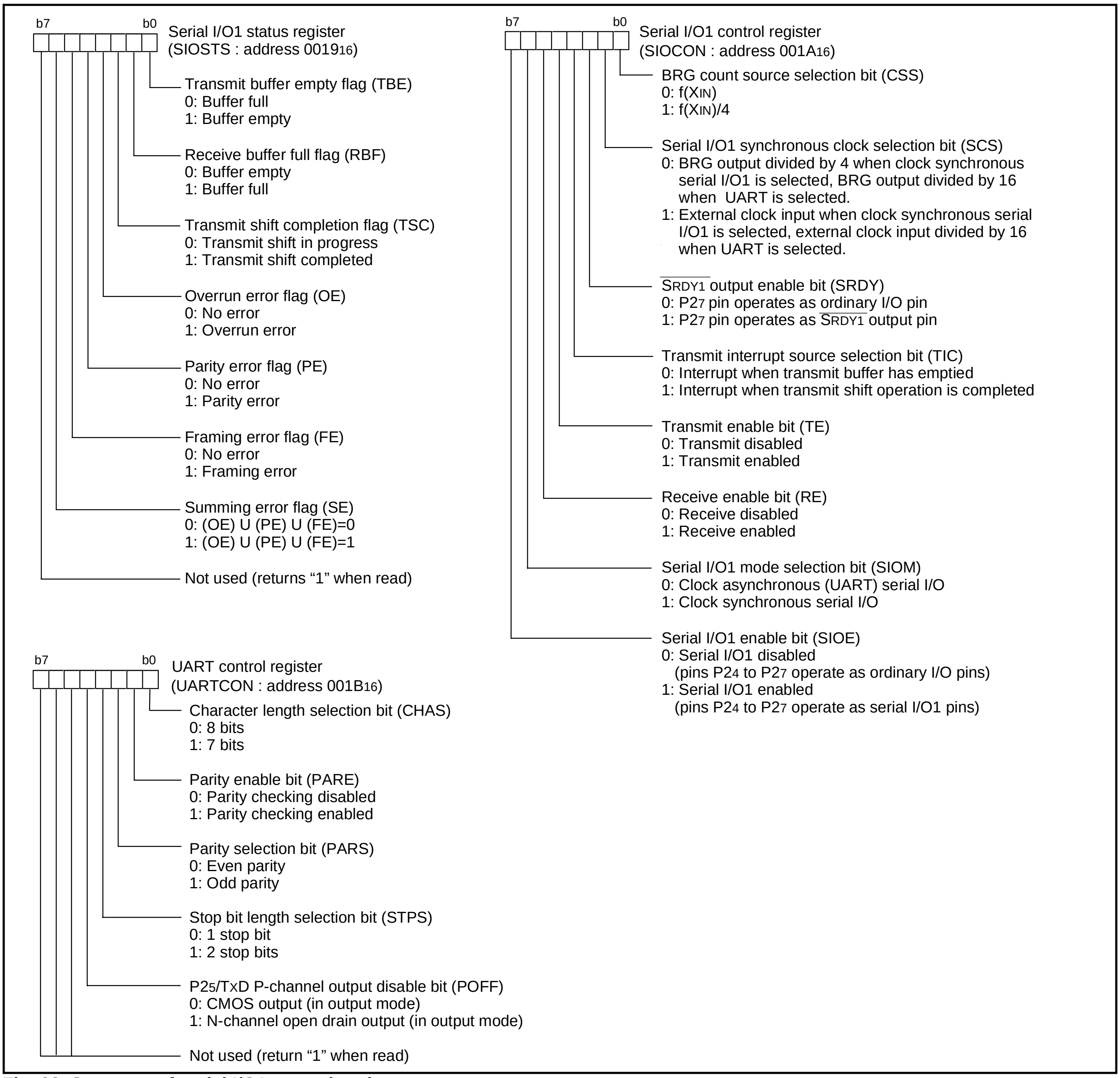


Fig. 22 Structure of serial I/O1 control registers

■Notes on serial I/O1

1. When using the serial I/O1, clear the I^2C-BUS interface enable bit to “0” or the SDA/SCL interrupt pin selection bit to “0”.
2. When setting the transmit enable bit of serial I/O1 to “1”, the serial I/O1 transmit interrupt request bit is automatically set to “1”. When not requiring the interrupt occurrence synchronized with the transmission enabled, take the following sequence.
   (1) Set the serial I/O1 transmit interrupt enable bit to “0” (disabled).
   (2) Set the transmit enable bit to “1”.
   (3) Set the serial I/O1 transmit interrupt request bit to “0” after 1 or more instructions have been executed.
   (4) Set the serial I/O1 transmit interrupt enable bit to “1” (enabled).

●SERIAL I/O2

The serial I/O2 can be operated only as the clock synchronous type. As a synchronous clock for serial transfer, either internal clock or external clock can be selected by the serial I/O2 synchronous clock selection bit (b6) of serial I/O2 control register 1.

The internal clock incorporates a dedicated divider and permits selecting 6 types of clock by the internal synchronous clock selection bits (b2, b1, b0) of serial I/O2 control register 1.

Regarding SOUT2 and SCLK2 being output pins, either CMOS output format or N-channel open-drain output format can be selected by the P01/SOUT2, P02/SCLK2 P-channel output disable bit (b7) of serial I/O2 control register 1.

When the internal clock has been selected, a transfer starts by a write signal to the serial I/O2 register (address 0017_{16}). After completion of data transfer, the level of the SOUT2 pin goes to high impedance automatically but bit 7 of the serial I/O2 control register 2 is not set to “1” automatically.

When the external clock has been selected, the contents of the serial I/O2 register is continuously sifted while transfer clocks are input. Accordingly, control the clock externally. Note that the SOUT2 pin does not go to high impedance after completion of data transfer.

To cause the SOUT2 pin to go to high impedance in the case where the external clock is selected, set bit 7 of the serial I/O2 control register 2 to “1” when SCLK2 is “H” after completion of data transfer. After the next data transfer is started (the transfer clock falls), bit 7 of the serial I/O2 control register 2 is set to “0” and the SOUT2 pin is put into the active state.

Regardless of the internal clock to external clock, the interrupt request bit is set after the number of bits (1 to 8 bits) selected by the optional transfer bit is transferred. In case of a fractional number of bits less than 8 bits as the last data, the received data to be stored in the serial I/O2 register becomes a fractional number of bits close to MSB if the transfer direction selection bit of serial I/O2 control register 1 is LSB first, or a fractional number of bits close to LSB if the transfer direction selection bit is MSB first. For the remaining bits, the previously received data is shifted.

At transmit operation using the clock synchronous serial I/O, the SCMP2 signal can be output by comparing the state of the transmit pin SOUT2 with the state of the receive pin SIN2 in synchronization with a rise of the transfer clock. If the output level of the SOUT2 pin is equal to the input level to the SIN2 pin, “L” is output from the SCMP2 pin. If not, “H” is output. At this time, an INT2 interrupt request can also be generated. Select a valid edge by bit 2 of the interrupt edge selection register (address $003A_{16}$).

[Serial I/O2 Control Registers 1, 2 (SIO2CON1 / SIO2CON2)] 0015_{16}, 0016_{16}

The serial I/O2 control registers 1 and 2 are containing various selection bits for serial I/O2 control as shown in Figure 23.

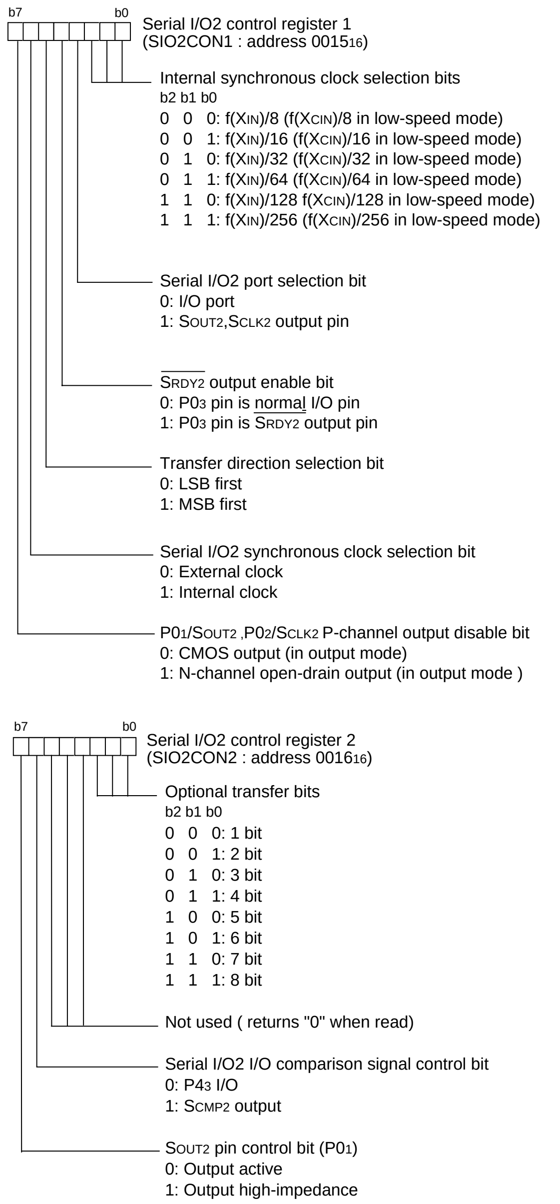
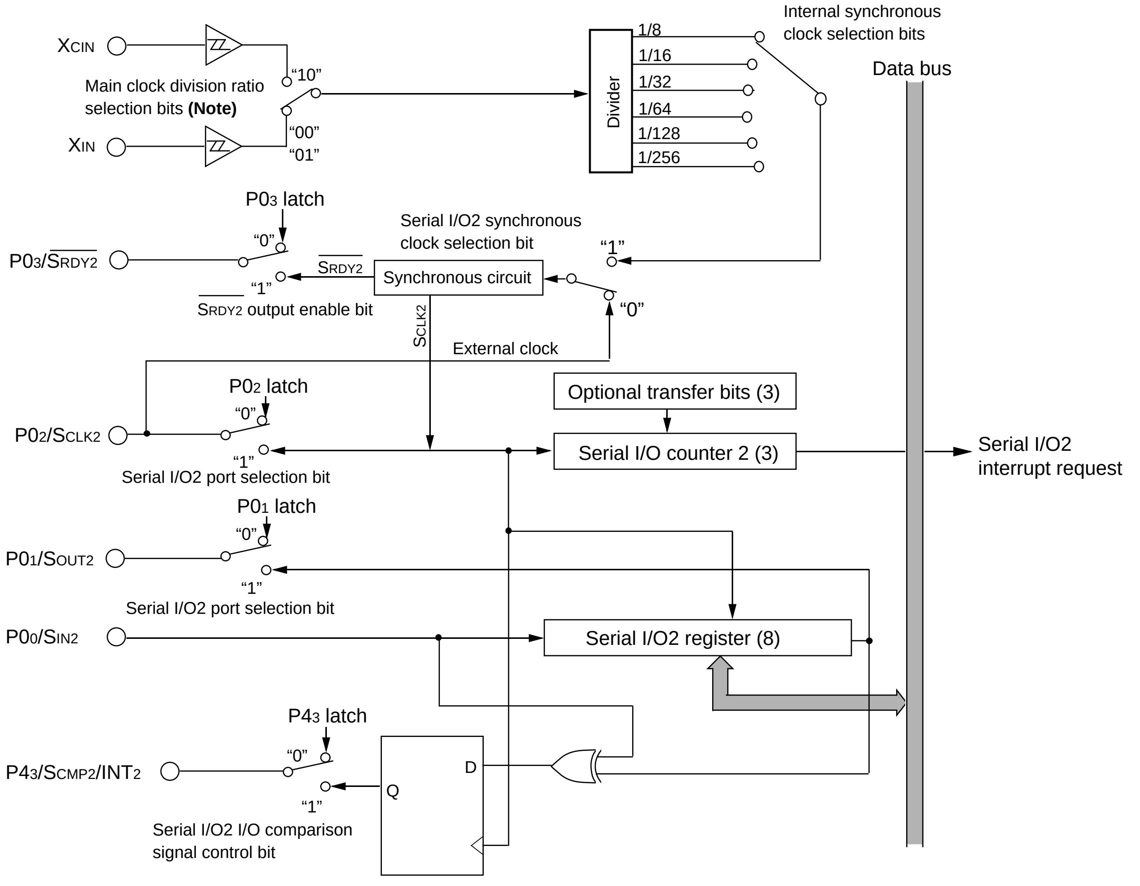
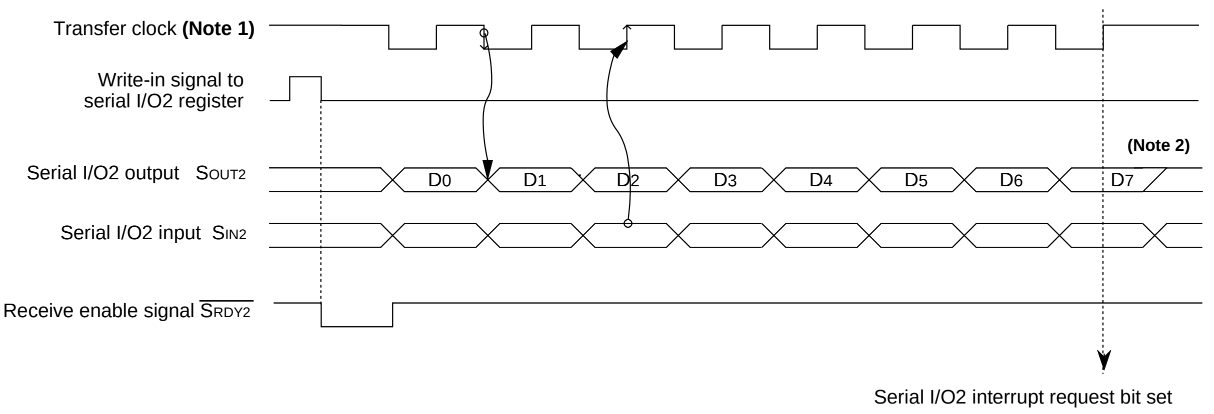


Fig. 23 Structure of Serial I/O2 control registers 1, 2



Note: Either high-speed, middle-speed or low-speed mode is selected by bits 6 and 7 of CPU mode register.

Fig. 24 Block diagram of Serial I/O2



Notes 1: When the internal clock is selected as a transfer clock, the f(XIN) clock division (f(XCIN) in low-speed mode) can be selected by setting bits 0 to 2 of serial I/O2 control register 1.
2: When the internal clock is selected as a transfer clock, the SOUT2 pin has high impedance after transfer completion.

Fig. 25 Timing chart of Serial I/O2

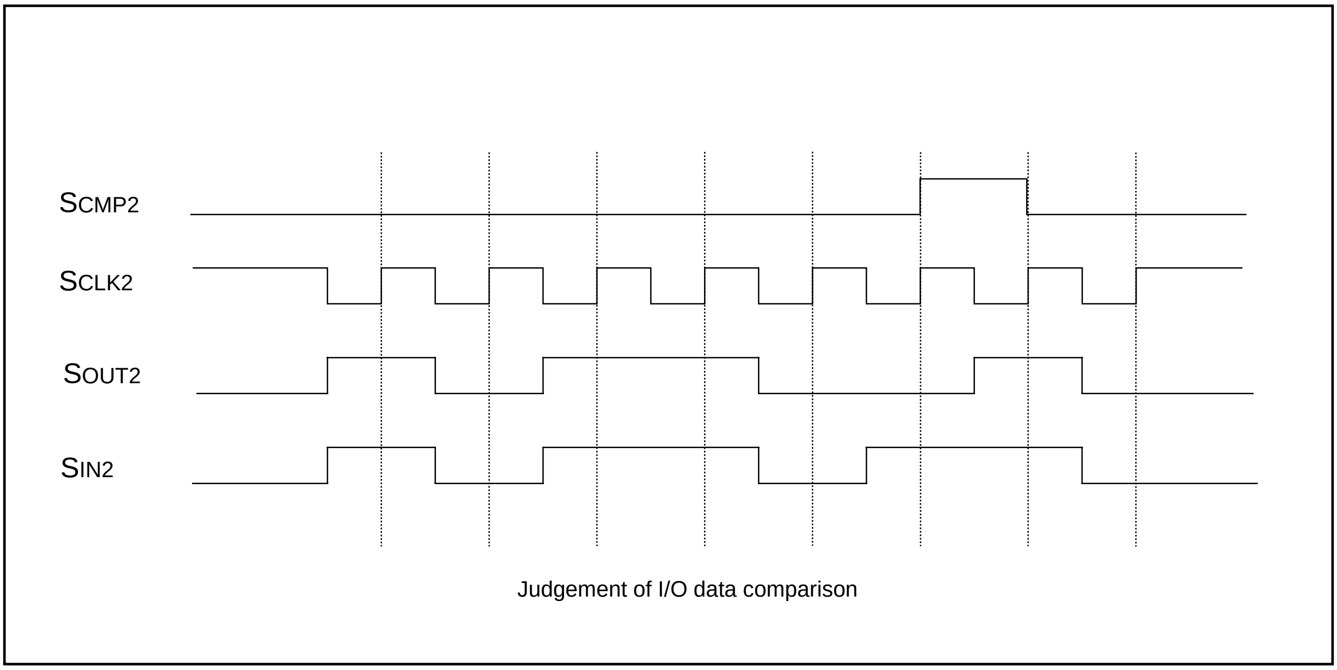


Fig. 26 SCMP2 output operation

MULTI-MASTER I^{2}C-BUS INTERFACE

The multi-master I^{2}C-BUS interface is a serial communications circuit, conforming to the Philips I^{2}C-BUS data transfer format. This interface, offering both arbitration lost detection and a synchronous functions, is useful for the multi-master serial communications.
Figure 27 shows a block diagram of the multi-master I^{2}C-BUS interface and Table 9 lists the multi-master I^{2}C-BUS interface functions.
This multi-master I^{2}C-BUS interface consists of the I^{2}C address register, the I^{2}C data shift register, the I^{2}C clock control register, the I^{2}C control register, the I^{2}C status register, the I^{2}C start/stop condition control register and other control circuits.
When using the multi-master I^{2}C-BUS interface, set 1 MHz or more to ϕ.

Note: Renesas Technology Corporation assumes no responsibility for infringement of any third-party's rights or originating in the use of the connection control function between the I^{2}C-BUS interface and the ports SCL_1, SCL_2, SDA_1 and SDA_2 with the bit 6 of I^{2}C control register ($002E_{16}$).

Table 9 Multi-master I^{2}C-BUS interface functions

Item	Function
Format	In conformity with Philips I^{2}C-BUS standard: 10-bit addressing format 7-bit addressing format High-speed clock mode Standard clock mode
Communication mode	In conformity with Philips I^{2}C-BUS standard: Master transmission Master reception Slave transmission Slave reception
SCL clock frequency	16.1 kHz to 400 kHz (at ϕ= 4 MHz)

System clock ϕ = $f(X_{IN})/2$ (high-speed mode)
ϕ = $f(X_{IN})/8$ (middle-speed mode)

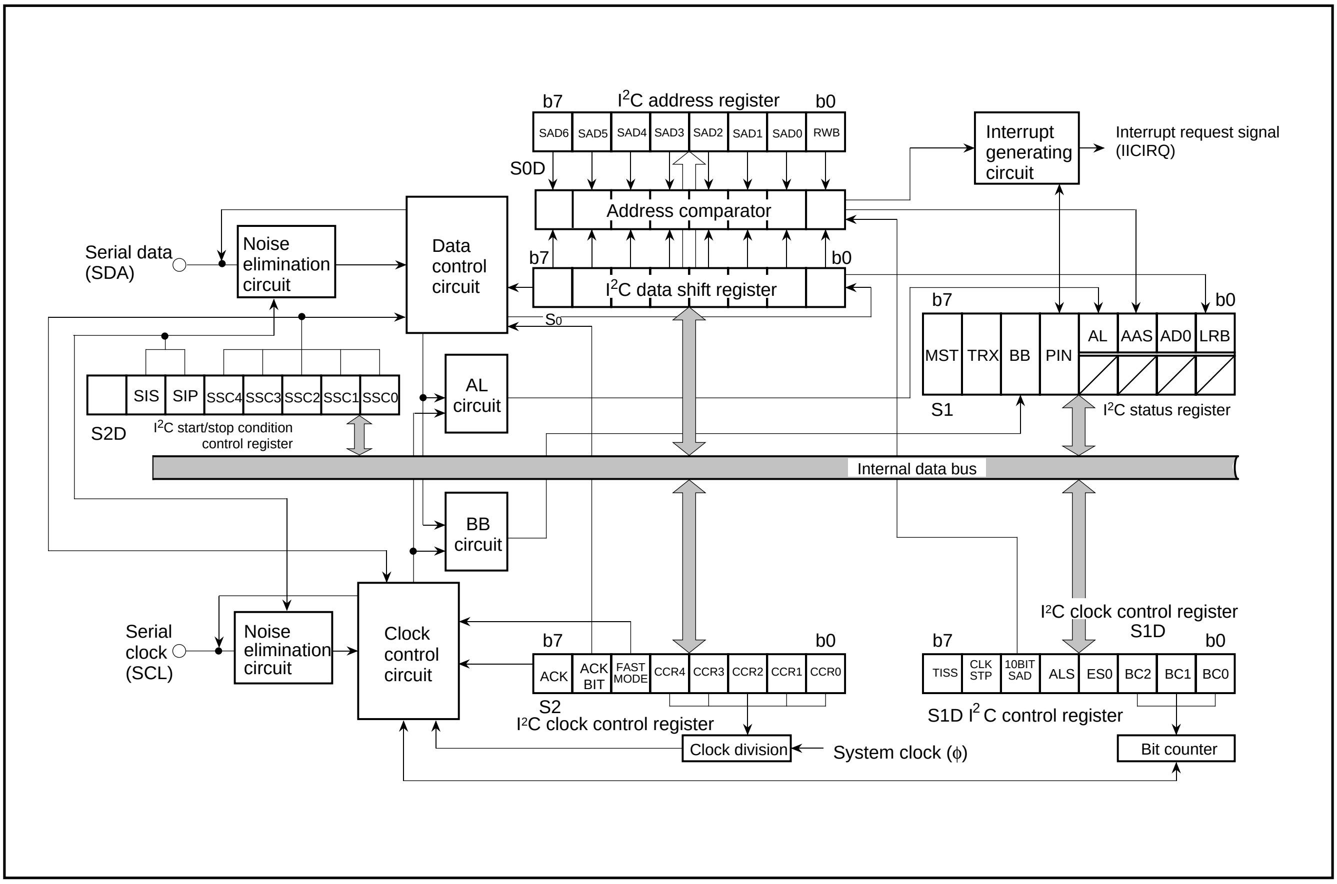


Fig. 27 Block diagram of multi-master I^{2}C-BUS interface

✻ : Purchase of Renesas Technology Corporation's I^{2}C components conveys a license under the Philips I^{2}C Patent Rights to use these components an I^{2}C system, provided that the system conforms to the I^{2}C Standard Specification as defined by Philips.

[I^2C Data Shift Register (S0)] $002B_{16}$

The I^2C data shift register (S0 : address $002B_{16}$) is an 8-bit shift register to store receive data and write transmit data.
When transmit data is written into this register, it is transferred to the outside from bit 7 in synchronization with the SCL clock, and each time one-bit data is output, the data of this register are shifted by one bit to the left. When data is received, it is input to this register from bit 0 in synchronization with the SCL clock, and each time one-bit data is input, the data of this register are shifted by one bit to the left. The minimum 2 machine cycles are required from the rising of the SCL clock until input to this register.
The I^2C data shift register is in a write enable status only when the I^2C-BUS interface enable bit (ES0 bit : bit 3 of address $002E_{16}$) of the I^2C control register is “1”. The bit counter is reset by a write instruction to the I^2C data shift register. When both the ES0 bit and the MST bit of the I^2C status register (address $002D_{16}$) are “1”, the SCL is output by a write instruction to the I^2C data shift register. Reading data from the I^2C data shift register is always enabled regardless of the ES0 bit value.

[I^2C Address Register (S0D)] $002C_{16}$

The I^2C address register (address $002C_{16}$) consists of a 7-bit slave address and a read/$\overline{\text{write}}$ bit. In the addressing mode, the slave address written in this register is compared with the address data to be received immediately after the START condition is detected.

•Bit 0: Read/$\overline{\text{write}}$ bit (RWB)

This is not used in the 7-bit addressing mode. In the 10-bit addressing mode, the first address data to be received is compared with the contents (SAD6 to SAD0 + RWB) of the I^2C address register.
The RWB bit is cleared to “0” automatically when the stop condition is detected.

•Bits 1 to 7: Slave address (SAD0–SAD6)

These bits store slave addresses. Regardless of the 7-bit addressing mode and the 10-bit addressing mode, the address data transmitted from the master is compared with the contents of these bits.

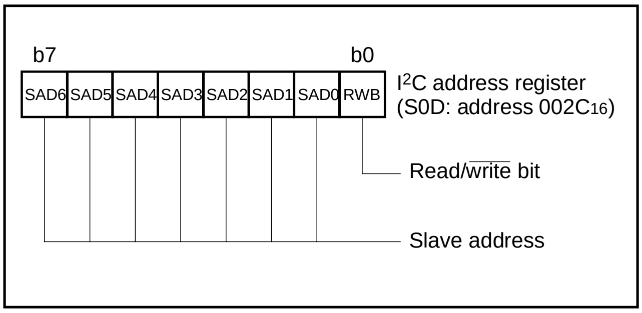


Fig. 28 Structure of I^2C address register

[I²C Clock Control Register (S2)] 002F16

The I²C clock control register (address 002F16) is used to set ACK control, SCL mode and SCL frequency.

•Bits 0 to 4: SCL frequency control bits (CCR0–CCR4)

These bits control the SCL frequency. Refer to Table 10.

•Bit 5: SCL mode specification bit (FAST MODE)

This bit specifies the SCL mode. When this bit is set to “0”, the standard clock mode is selected. When the bit is set to “1”, the high-speed clock mode is selected.

When connecting the bus of the high-speed mode I²C-BUS standard (maximum 400 kbits/s), use 8 MHz or more oscillation frequency f(XIN) and 2 division clock.

•Bit 6: ACK bit (ACK BIT)

This bit sets the SDA status when an ACK clock* is generated. When this bit is set to “0”, the ACK return mode is selected and SDA goes to “L” at the occurrence of an ACK clock. When the bit is set to “1”, the ACK non-return mode is selected. The SDA is held in the “H” status at the occurrence of an ACK clock.

However, when the slave address agree with the address data in the reception of address data at ACK BIT = “0”, the SDA is automatically made “L” (ACK is returned). If there is a disagreement between the slave address and the address data, the SDA is automatically made “H” (ACK is not returned).

*ACK clock: Clock for acknowledgment

•Bit 7: ACK clock bit (ACK)

This bit specifies the mode of acknowledgment which is an acknowledgment response of data transfer. When this bit is set to “0”, the no ACK clock mode is selected. In this case, no ACK clock occurs after data transmission. When the bit is set to “1”, the ACK clock mode is selected and the master generates an ACK clock each completion of each 1-byte data transfer. The device for transmitting address data and control data releases the SDA at the occurrence of an ACK clock (makes SDA “H”) and receives the ACK bit generated by the data receiving device.

Note: Do not write data into the I²C clock control register during transfer. If data is written during transfer, the I²C clock generator is reset, so that data cannot be transferred normally.

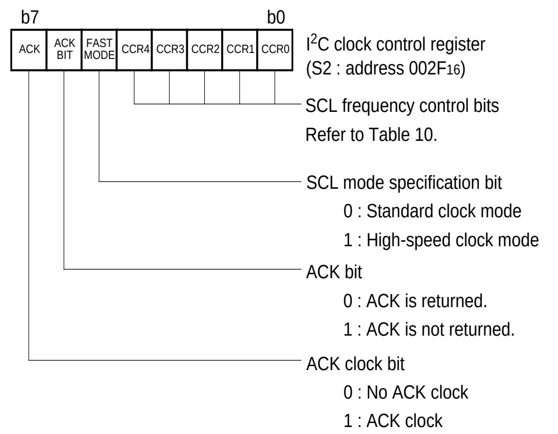


Fig. 29 Structure of I²C clock control register

Table 10 Set values of I²C clock control register and SCL frequency

Setting value of CCR4–CCR0					SCL frequency **(Note 1)** (at ϕ = 4 MHz, unit : kHz)	
CCR4	CCR3	CCR2	CCR1	CCR0	Standard clock mode	High-speed clock mode
0	0	0	0	0	Setting disabled	Setting disabled
0	0	0	0	1	Setting disabled	Setting disabled
0	0	0	1	0	Setting disabled	Setting disabled
0	0	0	1	1	– **(Note 2)**	333
0	0	1	0	0	– **(Note 2)**	250
0	0	1	0	1	100	400 **(Note 3)**
0	0	1	1	0	83.3	166
⋮	⋮	⋮	⋮	⋮	500/CCR value **(Note 3)**	1000/CCR value **(Note 3)**
1	1	1	0	1	17.2	34.5
1	1	1	1	0	16.6	33.3
1	1	1	1	1	16.1	32.3

Notes 1: Duty of SCL clock output is 50 %. The duty becomes 35 to 45 % only when the high-speed clock mode is selected and CCR value = 5 (400 kHz, at ϕ = 4 MHz). “H” duration of the clock fluctuates from –4 to +2 machine cycles in the standard clock mode, and fluctuates from –2 to +2 machine cycles in the high-speed clock mode. In the case of negative fluctuation, the frequency does not increase because “L” duration is extended instead of “H” duration reduction.
These are value when SCL clock synchronization by the synchronous function is not performed. CCR value is the decimal notation value of the SCL frequency control bits CCR4 to CCR0.

2: Each value of SCL frequency exceeds the limit at ϕ = 4 MHz or more. When using these setting value, use ϕ of 4 MHz or less.

3: The data formula of SCL frequency is described below:
$\phi/(8 \times \text{CCR value})$ Standard clock mode
$\phi/(4 \times \text{CCR value})$ High-speed clock mode (CCR value ≠ 5)
$\phi/(2 \times \text{CCR value})$ High-speed clock mode (CCR value = 5)
Do not set 0 to 2 as CCR value regardless of ϕ frequency.
Set 100 kHz (max.) in the standard clock mode and 400 kHz (max.) in the high-speed clock mode to the SCL frequency by setting the SCL frequency control bits CCR4 to CCR0.

[I^{2}C Control Register (S1D)] $002E_{16}$

The I^{2}C control register (address $002E_{16}$) controls data communication format.

•Bits 0 to 2: Bit counter (BC0–BC2)

These bits decide the number of bits for the next 1-byte data to be transmitted. The I^{2}C interrupt request signal occurs immediately after the number of count specified with these bits (ACK clock is added to the number of count when ACK clock is selected by ACK clock bit (bit 7 of address $002F_{16}$)) have been transferred, and BC0 to BC2 are returned to “000_2”.

Also when a START condition is received, these bits become “000_2” and the address data is always transmitted and received in 8 bits.

•Bit 3: I^{2}C interface enable bit (ES0)

This bit enables to use the multi-master I^{2}C-BUS interface. When this bit is set to “0”, the use disable status is provided, so that the SDA and the SCL become high-impedance. When the bit is set to “1”, use of the interface is enabled.

When ES0 = “0”, the following is performed.

- PIN = “1”, BB = “0” and AL = “0” are set (which are bits of the I^{2}C status register at address $002D_{16}$).
- Writing data to the I^{2}C data shift register (address $002B_{16}$) is disabled.

•Bit 4: Data format selection bit (ALS)

This bit decides whether or not to recognize slave addresses. When this bit is set to “0”, the addressing format is selected, so that address data is recognized. When a match is found between a slave address and address data as a result of comparison or when a general call (refer to “I^{2}C Status Register”, bit 1) is received, transfer processing can be performed. When this bit is set to “1”, the free data format is selected, so that slave addresses are not recognized.

•Bit 5: Addressing format selection bit (10BIT SAD)

This bit selects a slave address specification format. When this bit is set to “0”, the 7-bit addressing format is selected. In this case, only the high-order 7 bits (slave address) of the I^{2}C address register (address $002C_{16}$) are compared with address data. When this bit is set to “1”, the 10-bit addressing format is selected, and all the bits of the I^{2}C address register are compared with address data.

•Bit 6: SDA/SCL pin selection bit (TSEL)

This bit selects the input/output pins of SCL and SDA of the multi-master I^{2}C-BUS interface.

•Bit 7: I^{2}C-BUS interface pin input level selection bit (TISS)

This bit selects the input level of the SCL and SDA pins of the multi-master I^{2}C-BUS interface.

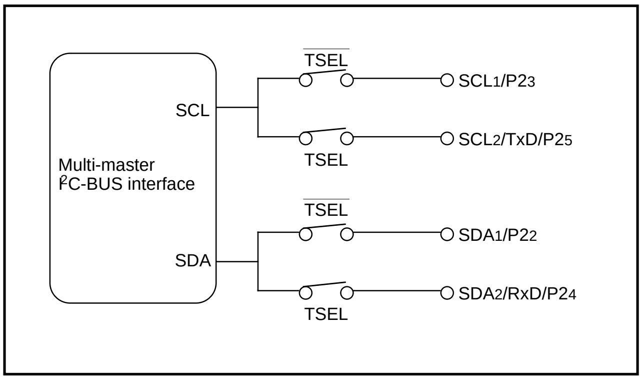


Fig. 30 SDA/SCL pin selection bit

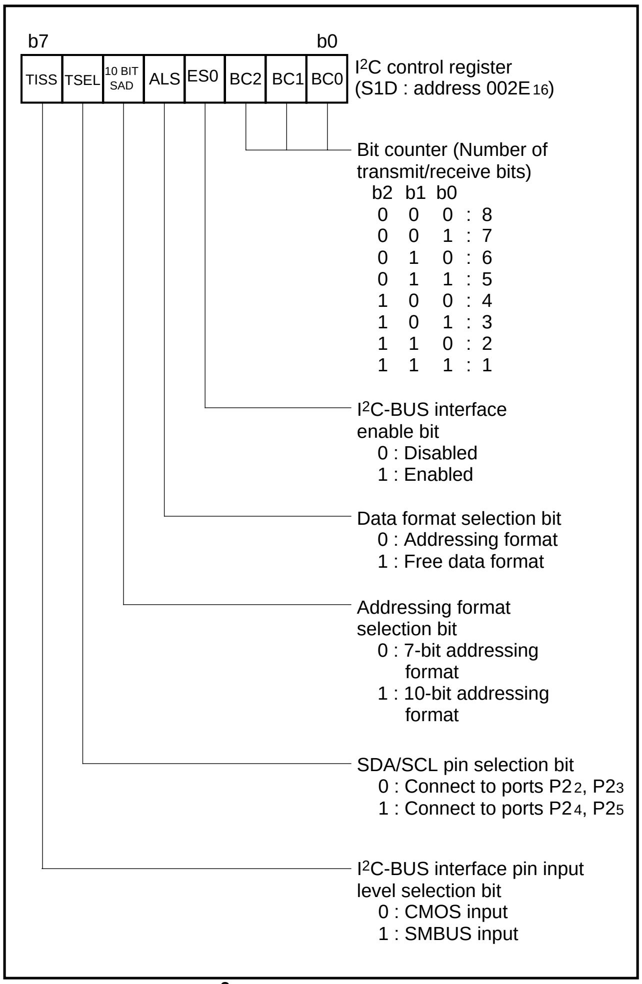


Fig. 31 Structure of I^{2}C control register

[I²C Status Register (S1)] 002D16

The I²C status register (address 002D16) controls the I²C-BUS interface status. The low-order 4 bits are read-only bits and the high-order 4 bits can be read out and written to.

Set "00002" to the low-order 4 bits, because these bits become the reserved bits at writing.

•Bit 0: Last receive bit (LRB)

This bit stores the last bit value of received data and can also be used for ACK receive confirmation. If ACK is returned when an ACK clock occurs, the LRB bit is set to "0". If ACK is not returned, this bit is set to "1". Except in the ACK mode, the last bit value of received data is input. The state of this bit is changed from "1" to "0" by executing a write instruction to the I²C data shift register (address 002B16).

•Bit 1: General call detecting flag (AD0)

When the ALS bit is "0", this bit is set to "1" when a general call✻ whose address data is all "0" is received in the slave mode. By a general call of the master device, every slave device receives control data after the general call. The AD0 bit is set to "0" by detecting the STOP condition or START condition, or reset.

✻General call: The master transmits the general call address "0016" to all slaves.

•Bit 2: Slave address comparison flag (AAS)

This flag indicates a comparison result of address data when the ALS bit is "0".

(1) In the slave receive mode, when the 7-bit addressing format is selected, this bit is set to "1" in one of the following conditions:
- The address data immediately after occurrence of a START condition agrees with the slave address stored in the high-order 7 bits of the I²C address register (address 002C16).
- A general call is received.

(2) In the slave receive mode, when the 10-bit addressing format is selected, this bit is set to "1" with the following condition:
- When the address data is compared with the I²C address register (8 bits consisting of slave address and RWB bit), the first bytes agree.

(3) This bit is set to "0" by executing a write instruction to the I²C data shift register (address 002B16) when ES0 is set to "1" or reset.

•Bit 3: Arbitration lost✻ detecting flag (AL)

In the master transmission mode, when the SDA is made "L" by any other device, arbitration is judged to have been lost, so that this bit is set to "1". At the same time, the TRX bit is set to "0", so that immediately after transmission of the byte whose arbitration was lost is completed, the MST bit is set to "0". The arbitration lost can be detected only in the master transmission mode. When arbitration is lost during slave address transmission, the TRX bit is set to "0" and the reception mode is set. Consequently, it becomes possible to detect the agreement of its own slave address and address data transmitted by another master device.

✻Arbitration lost :The status in which communication as a master is disabled.

•Bit 4: SCL pin low hold bit (PIN)

This bit generates an interrupt request signal. Each time 1-byte data is transmitted, the PIN bit changes from "1" to "0". At the same time, an interrupt request signal occurs to the CPU. The PIN bit is set to "0" in synchronization with a falling of the last clock (including the ACK clock) of an internal clock and an interrupt request signal occurs in synchronization with a falling of the PIN bit. When the PIN bit is "0", the SCL is kept in the "0" state and clock generation is disabled. Figure 33 shows an interrupt request signal generating timing chart.

The PIN bit is set to "1" in one of the following conditions:
- Executing a write instruction to the I²C data shift register (address 002B16). (This is the only condition which the prohibition of the internal clock is released and data can be communicated except for the start condition detection.)
- When the ES0 bit is "0"
- At reset
- When writing "1" to the PIN bit by software

The conditions in which the PIN bit is set to "0" are shown below:
- Immediately after completion of 1-byte data transmission (including when arbitration lost is detected)
- Immediately after completion of 1-byte data reception
- In the slave reception mode, with ALS = "0" and immediately after completion of slave address agreement or general call address reception
- In the slave reception mode, with ALS = "1" and immediately after completion of address data reception

•Bit 5: Bus busy flag (BB)

This bit indicates the status of use of the bus system. When this bit is set to "0", this bus system is not busy and a START condition can be generated. The BB flag is set/reset by the SCL, SDA pins input signal regardless of master/slave. This flag is set to "1" by detecting the start condition, and is set to "0" by detecting the stop condition. The condition of these detecting is set by the start/stop condition setting bits (SSC4–SSC0) of the I²C start/stop condition control register (address 003016). When the ES0 bit of the I²C control register (address 002E16) is "0" or reset, the BB flag is set to "0".

For the writing function to the BB flag, refer to the sections "START Condition Generating Method" and "STOP Condition Generating Method" described later.

•Bit 6: Communication mode specification bit (transfer direction specification bit: TRX)

This bit decides a direction of transfer for data communication. When this bit is “0”, the reception mode is selected and the data of a transmitting device is received. When the bit is “1”, the transmission mode is selected and address data and control data are output onto the SDA in synchronization with the clock generated on the SCL.

This bit is set/reset by software and hardware. About set/reset by hardware is described below. This bit is set to “1” by hardware when all the following conditions are satisfied:

• When ALS is “0”
• In the slave reception mode or the slave transmission mode
• When the $R/\overline{W}$ bit reception is “1”

This bit is set to “0” in one of the following conditions:

• When arbitration lost is detected.
• When a STOP condition is detected.
• When writing “1” to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
• With MST = “0” and when a START condition is detected.
• With MST = “0” and when ACK non-return is detected.
• At reset

•Bit 7: Communication mode specification bit (master/slave specification bit: MST)

This bit is used for master/slave specification for data communication. When this bit is “0”, the slave is specified, so that a START condition and a STOP condition generated by the master are received, and data communication is performed in synchronization with the clock generated by the master. When this bit is “1”, the master is specified and a START condition and a STOP condition are generated. Additionally, the clocks required for data communication are generated on the SCL.

This bit is set to “0” in one of the following conditions.

• Immediately after completion of 1-byte data transfer when arbitration lost is detected
• When a STOP condition is detected.
• Writing “1” to this bit by software is invalid by the START condition duplication preventing function **(Note)**.
• At reset

Note: START condition duplication preventing function
The MST, TRX, and BB bits is set to “1” at the same time after confirming that the BB flag is “0” in the procedure of a START condition occurrence. However, when a START condition by another master device occurs and the BB flag is set to “1” immediately after the contents of the BB flag is confirmed, the START condition duplication preventing function makes the writing to the MST and TRX bits invalid. The duplication preventing function becomes valid from the rising of the BB flag to reception completion of slave address.

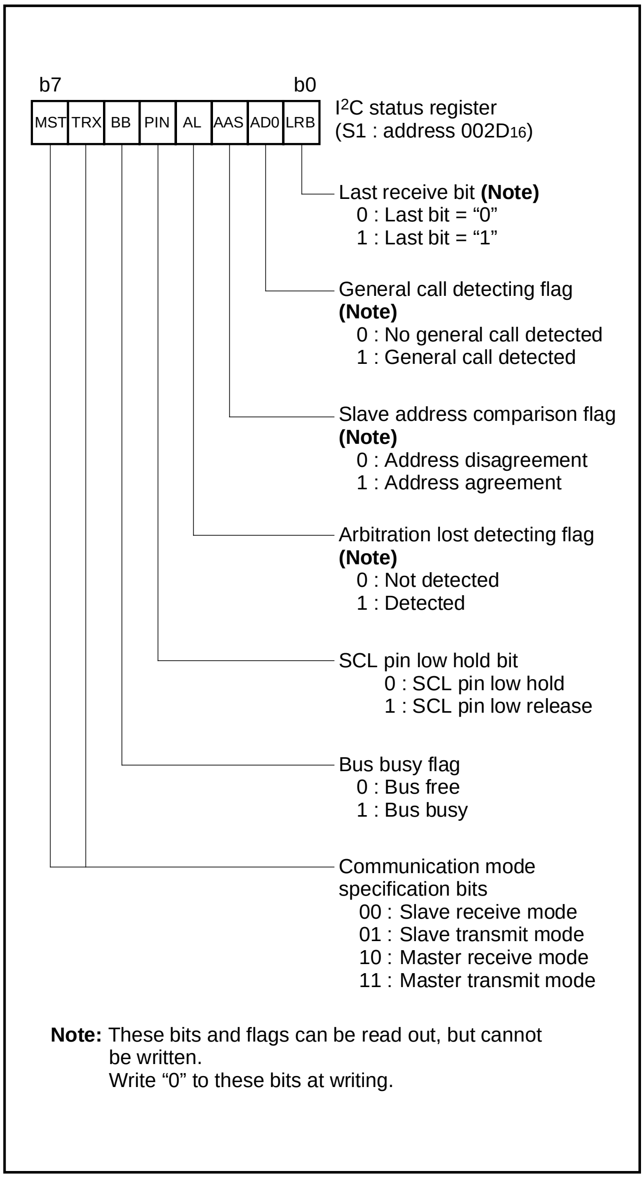


Fig. 32 Structure of I²C status register

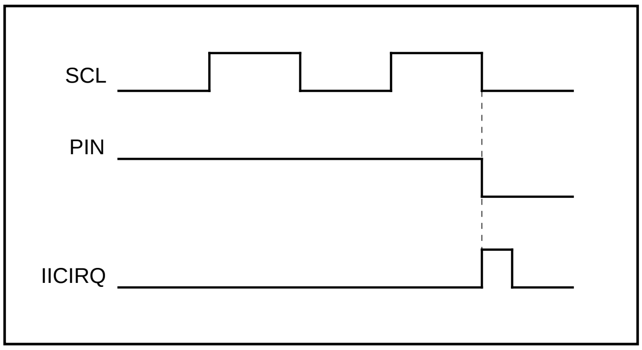


Fig. 33 Interrupt request signal generating timing

START Condition Generating Method

When writing “1” to the MST, TRX, and BB bits of the I²C status register (address $002D_{16}$) at the same time after writing the slave address to the I²C data shift register (address $002B_{16}$) with the condition in which the ES0 bit of the I²C control register (address $002E_{16}$) and the BB flag are “0”, a START condition occurs. After that, the bit counter becomes “000_2” and an SCL for 1 byte is output. The START condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 34, the START condition generating timing diagram, and Table 11, the START condition generating timing table.

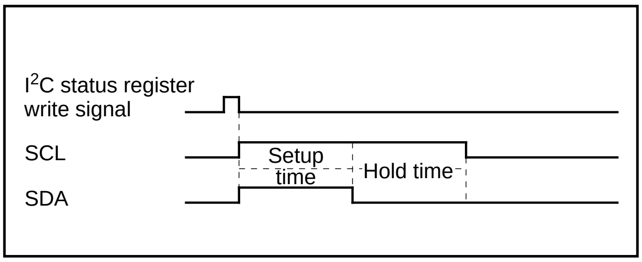


Fig. 34 START condition generating timing diagram

Table 11 START condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 µs (20 cycles)	2.5 µs (10 cycles)
Hold time	5.0 µs (20 cycles)	2.5 µs (10 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

STOP Condition Generating Method

When the ES0 bit of the I²C control register (address $002E_{16}$) is “1”, write “1” to the MST and TRX bits, and write “0” to the BB bit of the I²C status register (address $002D_{16}$) simultaneously. Then a STOP condition occurs. The STOP condition generating timing is different in the standard clock mode and the high-speed clock mode. Refer to Figure 35, the STOP condition generating timing diagram, and Table 12, the STOP condition generating timing table.

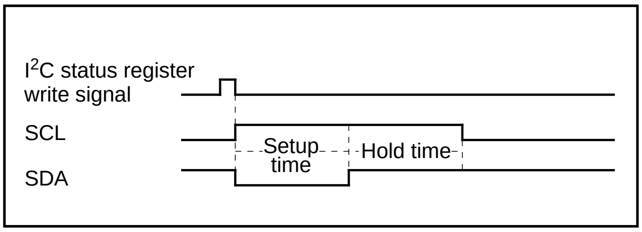


Fig. 35 STOP condition generating timing diagram

Table 12 STOP condition generating timing table

Item	Standard clock mode	High-speed clock mode
Setup time	5.0 µs (20 cycles)	3.0 µs (12 cycles)
Hold time	4.5 µs (18 cycles)	2.5 µs (10 cycles)

Note: Absolute time at ϕ = 4 MHz. The value in parentheses denotes the number of ϕ cycles.

START/STOP Condition Detecting Operation

The START/STOP condition detection operations are shown in Figures 36, 37, and Table 13. The START/STOP condition is set by the START/STOP condition set bit.

The START/STOP condition can be detected only when the input signal of the SCL and SDA pins satisfy three conditions: SCL release time, setup time, and hold time (see Table 13).

The BB flag is set to “1” by detecting the START condition and is reset to “0” by detecting the STOP condition.

The BB flag set/reset timing is different in the standard clock mode and the high-speed clock mode. Refer to Table 13, the BB flag set/reset time.

Note: When a STOP condition is detected in the slave mode (MST = 0), an interrupt request signal “IICIRQ” occurs to the CPU.

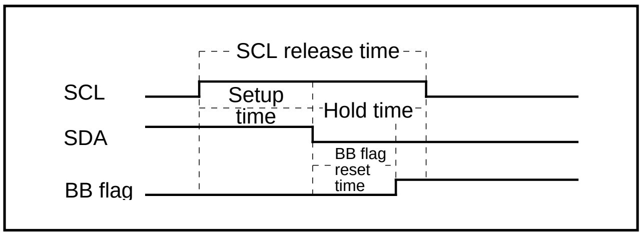


Fig. 36 START condition detecting timing diagram

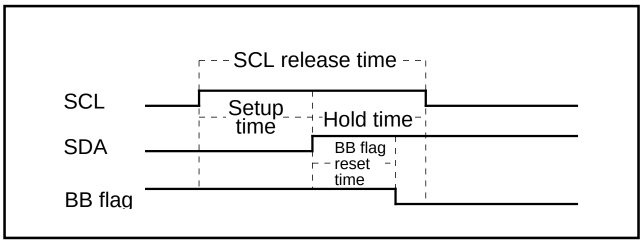


Fig. 37 STOP condition detecting timing diagram

Table 13 START condition/STOP condition detecting conditions

	Standard clock mode	High-speed clock mode
SCL release time	SSC value + 1 cycle (6.25 µs)	4 cycles (1.0 µs)
Setup time	$\frac{\text{SSC value} + 1}{2}$ cycle < 4.0 µs (3.125 µs)	2 cycles (1.0 µs)
Hold time	$\frac{\text{SSC value} + 1}{2}$ cycle < 4.0 µs (3.125 µs)	2 cycles (0.5 µs)
BB flag set/ reset time	$\frac{\text{SSC value} - 1}{2}$ + 2 cycles (3.375 µs)	3.5 cycles (0.875 µs)

Note: Unit : Cycle number of system clock ϕ
SSC value is the decimal notation value of the START/STOP condition set bits SSC4 to SSC0. Do not set “0” or an odd number to SSC value. The value in parentheses is an example when the I²C START/STOP condition control register is set to “18_{16}” at ϕ = 4 MHz.

[I^{2}C START/STOP Condition Control Register (S2D)] 0030_{16}

The I^{2}C START/STOP condition control register (address 0030_{16}) controls START/STOP condition detection.

•Bits 0 to 4: START/STOP condition set bit (SSC4–SSC0)

SCL release time, setup time, and hold time change the detection condition by value of the main clock divide ratio selection bit and the oscillation frequency f(X_{IN}) because these time are measured by the internal system clock. Accordingly, set the proper value to the START/STOP condition set bits (SSC4 to SSC0) in considered of the system clock frequency. Refer to Table 13.

Do not set "00000_2" or an odd number to the START/STOP condition set bit (SSC4 to SSC0).

Refer to Table 14, the recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency.

•Bit 5: SCL/SDA interrupt pin polarity selection bit (SIP)

An interrupt can occur when detecting the falling or rising edge of the SCL or SDA pin. This bit selects the polarity of the SCL or SDA pin interrupt pin.

•Bit 6: SCL/SDA interrupt pin selection bit (SIS)

This bit selects the pin of which interrupt becomes valid between the SCL pin and the SDA pin.

Note: When changing the setting of the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I^{2}C-BUS interface enable bit ES0, the SCL/SDA interrupt request bit may be set. When selecting the SCL/SDA interrupt source, disable the interrupt before the SCL/SDA interrupt pin polarity selection bit, the SCL/SDA interrupt pin selection bit, or the I^{2}C-BUS interface enable bit ES0 is set. Reset the request bit to "0" after setting these bits, and enable the interrupt.

Address Data Communication

There are two address data communication formats, namely, 7-bit addressing format and 10-bit addressing format. The respective address communication formats are described below.

(1) 7-bit addressing format

To adapt the 7-bit addressing format, set the 10BIT SAD bit of the I^{2}C control register (address $002E_{16}$) to "0". The first 7-bit address data transmitted from the master is compared with the high-order 7-bit slave address stored in the I^{2}C address register (address $002C_{16}$). At the time of this comparison, address comparison of the RWB bit of the I^{2}C address register (address $002C_{16}$) is not performed. For the data transmission format when the 7-bit addressing format is selected, refer to Figure 39, (1) and (2).

(2) 10-bit addressing format

To adapt the 10-bit addressing format, set the 10BIT SAD bit of the I^{2}C control register (address $002E_{16}$) to "1". An address comparison is performed between the first-byte address data transmitted from the master and the 8-bit slave address stored in the I^{2}C address register (address $002C_{16}$). At the time of this comparison, an address comparison between the RWB bit of the I^{2}C address register (address $002C_{16}$) and the R/$\overline{W}$ bit which is the last bit of the address data transmitted from the master is made. In the 10-bit addressing mode, the RWB bit which is the last bit of the address data not only specifies the direction of communication for control data, but also is processed as an address data bit.

When the first-byte address data agree with the slave address, the AAS bit of the I^{2}C status register (address $002D_{16}$) is set to "1". After the second-byte address data is stored into the I^{2}C data shift register (address $002B_{16}$), perform an address comparison between the second-byte data and the slave address by software. When the address data of the 2 bytes agree with the slave address, set the RWB bit of the I^{2}C address register (address $002C_{16}$) to "1" by software. This processing can make the 7-bit slave address and R/$\overline{W}$ data agree, which are received after a RESTART condition is detected, with the value of the I^{2}C address register (address $002C_{16}$). For the data transmission format when the 10-bit addressing format is selected, refer to Figure 39, (3) and (4).

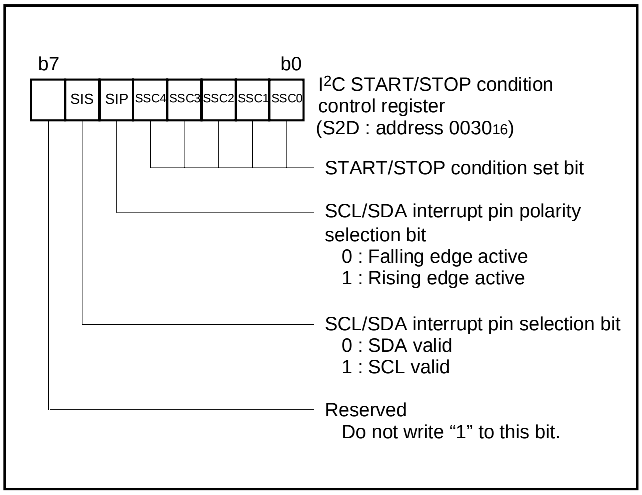


Fig. 38 Structure of I²C START/STOP condition control register

Table 14 Recommended set value to START/STOP condition set bits (SSC4–SSC0) for each oscillation frequency

Oscillation frequency f(XIN) (MHz)	Main clock divide ratio	System clock ϕ (MHz)	START/STOP condition control register	SCL release time (µs)	Setup time (µs)	Hold time (µs)
8	2	4	XXX11010	6.75 µs (27 cycles)	3.375 µs (13.5 cycles)	3.375 µs (13.5 cycles)
			XXX11000	6.25 µs (25 cycles)	3.125 µs (12.5 cycles)	3.125 µs (12.5 cycles)
8	8	1	XXX00100	5.0 µs (5 cycles)	2.5 µs (2.5 cycles)	2.5 µs (2.5 cycles)
4	2	2	XXX01100	6.5 µs (13 cycles)	3.25 µs (6.5 cycles)	3.25 µs (6.5 cycles)
			XXX01010	5.5 µs (11 cycles)	2.75 µs (5.5 cycles)	2.75 µs (5.5 cycles)
2	2	1	XXX00100	5.0 µs (5 cycles)	2.5 µs (2.5 cycles)	2.5 µs (2.5 cycles)

Note: Do not set an odd number to the START/STOP condition set bit (SSC4 to SSC0).

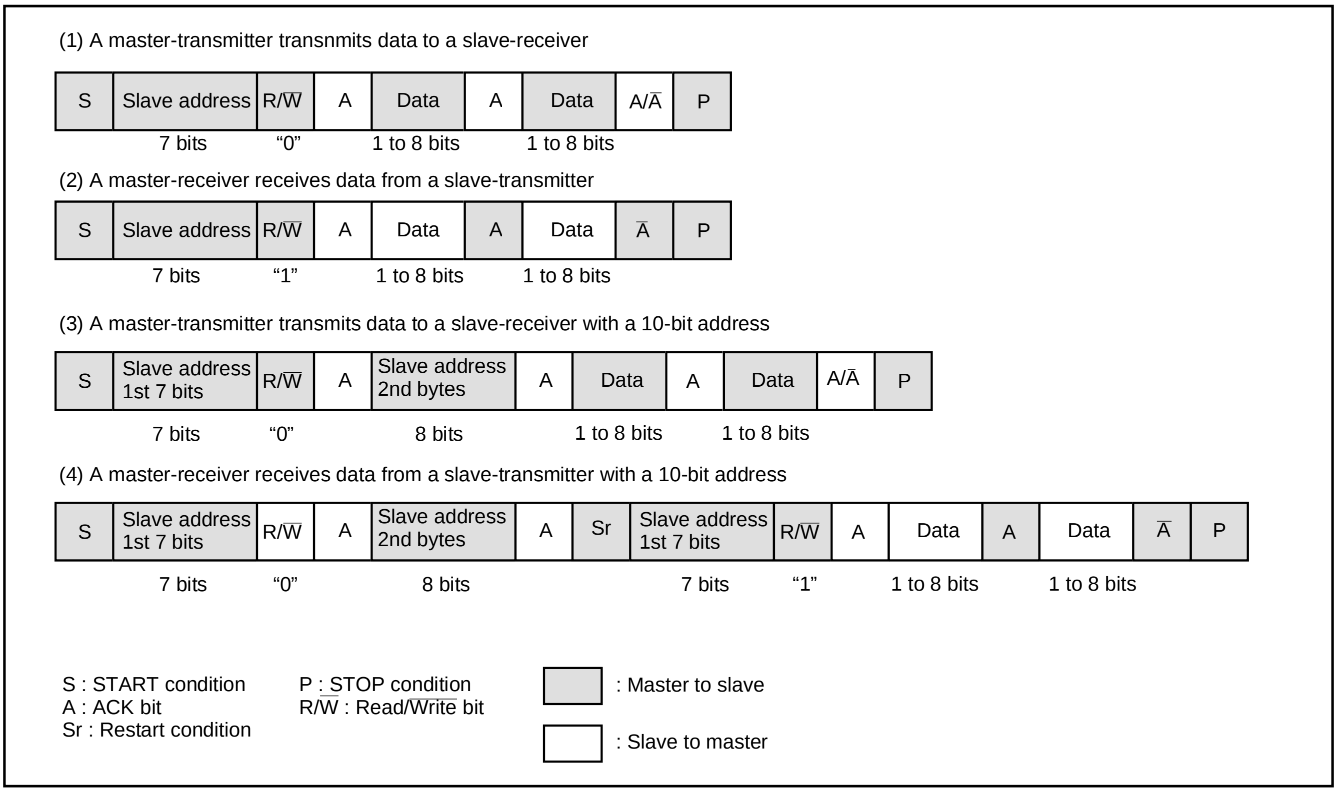


Fig. 39 Address data communication format

Example of Master Transmission

An example of master transmission in the standard clock mode, at the SCL frequency of 100 kHz and in the ACK return mode is shown below.

(1) Set a slave address in the high-order 7 bits of the I^2C address register (address $002C_{16}$) and “0” into the RWB bit.
(2) Set the ACK return mode and SCL = 100 kHz by setting “85_{16}” in the I^2C clock control register (address $002F_{16}$).
(3) Set “00_{16}” in the I^2C status register (address $002D_{16}$) so that transmission/reception mode can become initializing condition.
(4) Set a communication enable status by setting “08_{16}” in the I^2C control register (address $002E_{16}$).
(5) Confirm the bus free condition by the BB flag of the I^2C status register (address $002D_{16}$).
(6) Set the address data of the destination of transmission in the high-order 7 bits of the I^2C data shift register (address $002B_{16}$) and set “0” in the least significant bit.
(7) Set “$F0_{16}$” in the I^2C status register (address $002D_{16}$) to generate a START condition. At this time, an SCL for 1 byte and an ACK clock automatically occur.
(8) Set transmit data in the I^2C data shift register (address $002B_{16}$). At this time, an SCL and an ACK clock automatically occur.
(9) When transmitting control data of more than 1 byte, repeat step (8).
(10) Set “$D0_{16}$” in the I^2C status register (address $002D_{16}$) to generate a STOP condition if ACK is not returned from slave reception side or transmission ends.

Example of Slave Reception

An example of slave reception in the high-speed clock mode, at the SCL frequency of 400 kHz, in the ACK non-return mode and using the addressing format is shown below.

(1) Set a slave address in the high-order 7 bits of the I^2C address register (address $002C_{16}$) and “0” in the RWB bit.
(2) Set the no ACK clock mode and SCL = 400 kHz by setting “25_{16}” in the I^2C clock control register (address $002F_{16}$).
(3) Set “00_{16}” in the I^2C status register (address $002D_{16}$) so that transmission/reception mode can become initializing condition.
(4) Set a communication enable status by setting “08_{16}” in the I^2C control register (address $002E_{16}$).
(5) When a START condition is received, an address comparison is performed.
(6) • When all transmitted addresses are “0” (general call):
AD0 of the I^2C status register (address $002D_{16}$) is set to “1” and an interrupt request signal occurs.
• When the transmitted addresses agree with the address set in (1):
ASS of the I^2C status register (address $002D_{16}$) is set to “1” and an interrupt request signal occurs.
• In the cases other than the above AD0 and AAS of the I^2C status register (address $002D_{16}$) are set to “0” and no interrupt request signal occurs.
(7) Set dummy data in the I^2C data shift register (address $002B_{16}$).
(8) When receiving control data of more than 1 byte, repeat step (7).
(9) When a STOP condition is detected, the communication ends.

■Precautions when using multi-master I^{2}C-BUS interface

(1) Read-modify-write instruction

The precautions when the read-modify-write instruction such as SEB, CLB etc. is executed for each register of the multi-master I^{2}C-BUS interface are described below.

- I^{2}C data shift register (S0: address $002B_{16}$)
  When executing the read-modify-write instruction for this register during transfer, data may become a value not intended.
- I^{2}C address register (S0D: address $002C_{16}$)
  When the read-modify-write instruction is executed for this register at detecting the STOP condition, data may become a value not intended. It is because H/W changes the read/write bit (RWB) at the above timing.
- I^{2}C status register (S1: address $002D_{16}$)
  Do not execute the read-modify-write instruction for this register because all bits of this register are changed by H/W.
- I^{2}C control register (S1D: address $002E_{16}$)
  When the read-modify-write instruction is executed for this register at detecting the START condition or at completing the byte transfer, data may become a value not intended. Because H/W changes the bit counter (BC0-BC2) at the above timing.
- I^{2}C clock control register (S2: address $002F_{16}$)
  The read-modify-write instruction can be executed for this register.
- I^{2}C START/STOP condition control register (S2D: address 0030_{16})
  The read-modify-write instruction can be executed for this register.

(2) START condition generating procedure using multi-master

1. Procedure example (The necessary conditions of the generating procedure are described in Items 2 to 5 below.

```
        :
  LDA —                (Taking out of slave address value)
  SEI                  (Interrupt disabled)
  BBS 5, S1, BUSBUSY   (BB flag confirming and branch process)
BUSFREE:
  STA S0               (Writing of slave address value)
  LDM #$F0, S1         (Trigger of START condition generating)
  CLI                  (Interrupt enabled)
        :
BUSBUSY:
  CLI                  (Interrupt enabled)
        :
```

2. Use “Branch on Bit Set” of “BBS 5, $002D, –” for the BB flag confirming and branch process.
3. Use “STA $2B, STX $2B” or “STY $2B” of the zero page addressing instruction for writing the slave address value to the I^{2}C data shift register.
4. Execute the branch instruction of Item 2 and the store instruction of Item 3 continuously, as shown in the procedure example above.
5. Disable interrupts during the following three process steps:
   - BB flag confirming
   - Writing of slave address value
   - Trigger of START condition generating

   When the condition of the BB flag is bus busy, enable interrupts immediately.

(3) RESTART condition generating procedure

1. Procedure example (The necessary conditions for the procedure are described in items 2 to 4 below.)
   Execute the following procedure when the PIN bit is “0”.

```
        :
  LDM #$00, S1    (Select slave receive mode)
  LDA —           (Take out of slave address value)
  SEI             (Disable interrupt)
  STA S0          (Write slave address value)
  LDM #$F0, S1    (Trigger  RESTART condition generation)
  CLI             (Enable interrupt)
        :
```

2. Select the slave receive mode when the PIN bit is “0”. Do not write “1” to the PIN bit. Neither “0” nor “1” is specified as input to the BB bit.
   The TRX bit becomes “0” and the SDA pin is released.
3. The SCL pin is released by writing the slave address value to the I^{2}C data shift register.
4. Disable interrupts during the following two process steps:
   - Write slave address value
   - Trigger RESTART condition generation

(4) Writing to I^{2}C status register

Do not execute an instruction to set the PIN bit to “1” from “0” and an instruction to set the MST and TRX bits to “0” from “1” simultaneously. Because it may enter the state that the SCL pin is released and the SDA pin is released after about one machine cycle. Do not execute an instruction to set the MST and TRX bits to “0” from “1” simultaneously when the PIN bit is “1”. Because it may become the same as above.

(5) Process of after STOP condition generating

Do not write data in the I^{2}C data shift register S0 and the I^{2}C status register S1 until the bus busy flag BB becomes “0” after generating the STOP condition in the master mode. Because the STOP condition waveform might not be normally generated. Reading to the above registers do not have the problem.

PULSE WIDTH MODULATION (PWM)

The 3851 group (built-in 24 KB or more ROM) has a PWM function with an 8-bit resolution, based on a signal that is the clock input XIN or that clock input divided by 2.

Data Setting

The PWM output pin also functions as port P44. Set the PWM period by the PWM prescaler, and set the “H” term of output pulse by the PWM register.

If the value in the PWM prescaler is n and the value in the PWM register is m (where n = 0 to 255 and m = 0 to 255) :

PWM period = 255 X (n+1) / f(XIN)

= 31.875 X (n+1) µs

(when f(XIN) = 8 MHz,count source selection bit = “0”)

Output pulse “H” term = PWM period X m / 255

= 0.125 X (n+1) X m µs

(when f(XIN) = 8 MHz,count source selection bit = “0”)

PWM Operation

When bit 0 (PWM enable bit) of the PWM control register is set to “1”, operation starts by initializing the PWM output circuit, and pulses are output starting at an “H”.

If the PWM register or PWM prescaler is updated during PWM output, the pulses will change in the cycle after the one in which the change was made.

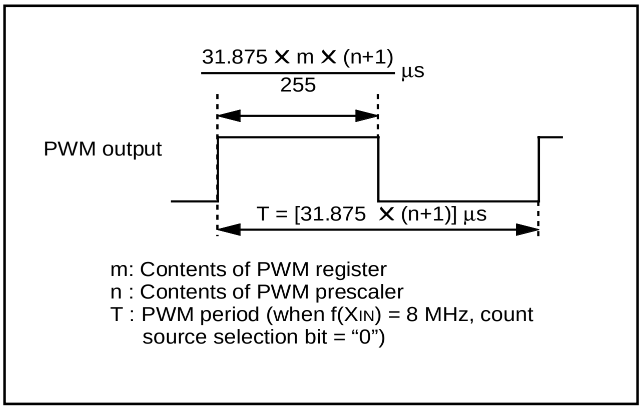


Fig. 40 Timing of PWM period

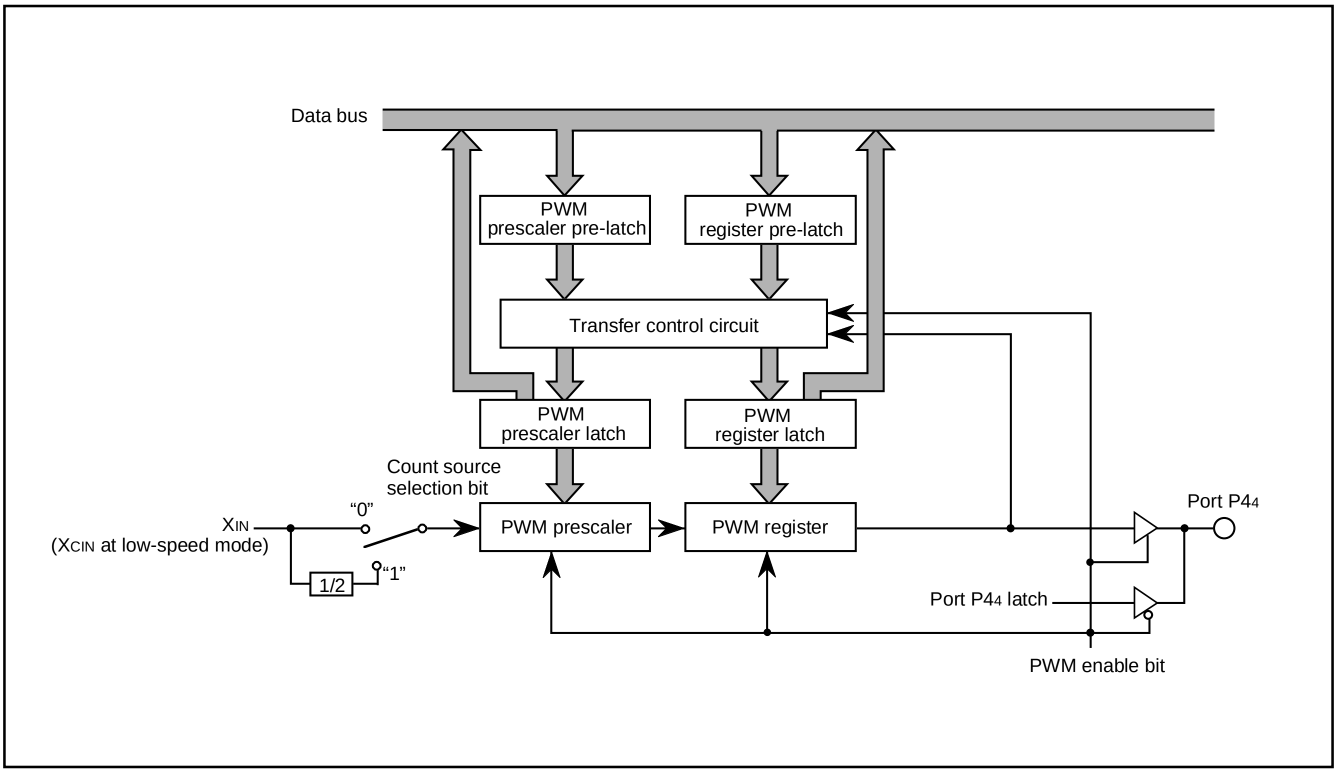


Fig. 41 Block diagram of PWM function

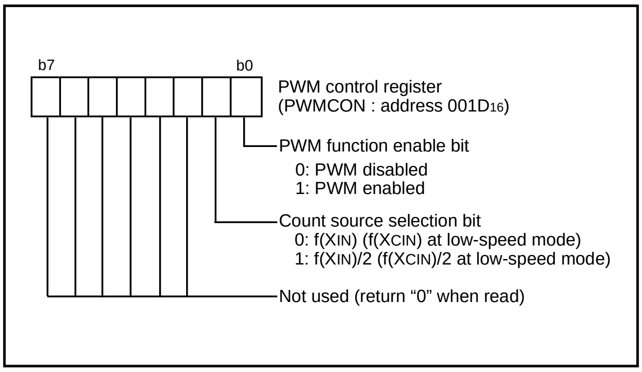


Fig. 42 Structure of PWM control register

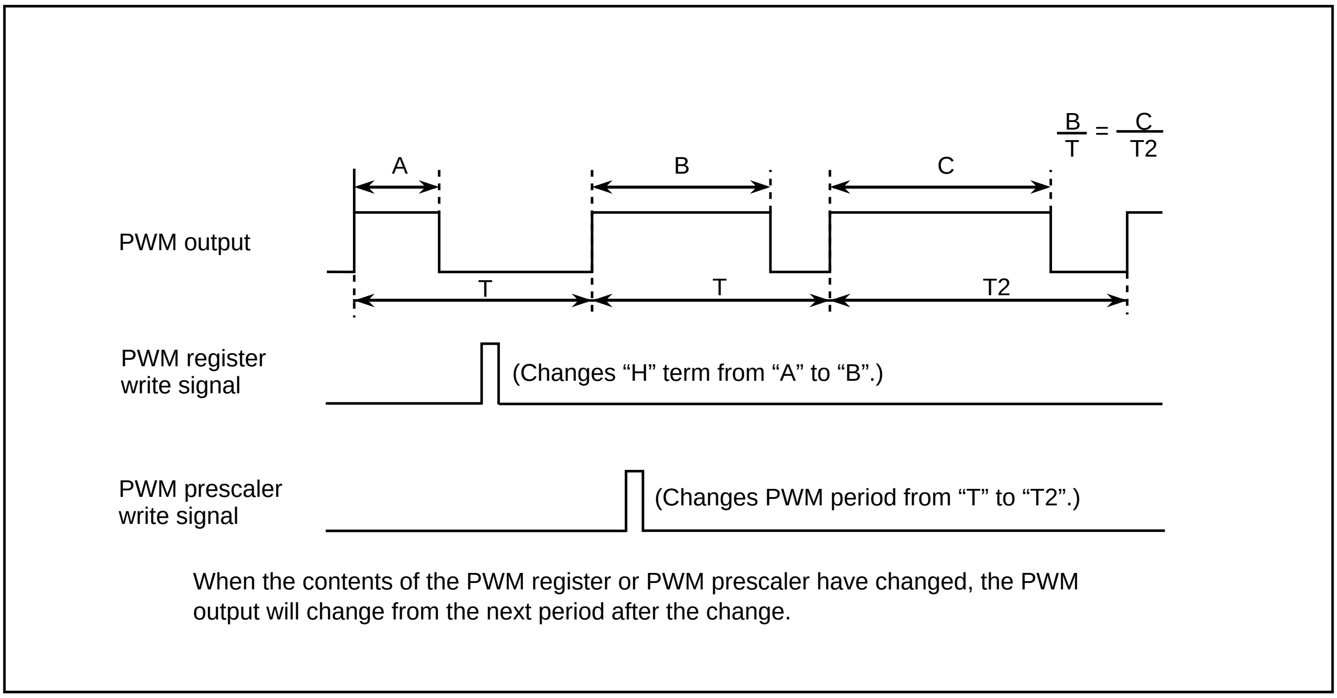


Fig. 43 PWM output timing when PWM register or PWM prescaler is changed

■Note

The PWM starts after the PWM function enable bit is set to enable and “L” level is output from the PWM pin.
The length of this “L” level output is as follows:

$$\frac{n+1}{2 \cdot f(X_{IN})} \text{ sec}$$ (Count source selection bit = 0, where n is the value set in the prescaler)

$$\frac{n+1}{f(X_{IN})} \text{ sec}$$ (Count source selection bit = 1, where n is the value set in the prescaler)

A-D CONVERTER
[A-D Conversion Registers (ADL, ADH)] 0035_{16}, 0036_{16}

The A-D conversion registers are read-only registers that store the result of an A-D conversion. Do not read these registers during an A-D conversion.

[A-D Control Register (ADCON)] 0034_{16}

The AD control register controls the A-D conversion process. Bits 0 to 2 select a specific analog input pin. Bit 4 indicates the completion of an A-D conversion. The value of this bit remains at "0" during an A-D conversion and changes to "1" when an A-D conversion ends. Writing "0" to this bit starts the A-D conversion.

Comparison Voltage Generator

The comparison voltage generator divides the voltage between AVSS and VREF into 1024 and outputs the divided voltages.

Channel Selector

The channel selector selects one of ports $P3_0/AN_0$ to $P3_4/AN_4$ and inputs the voltage to the comparator.

Comparator and Control Circuit

The comparator and control circuit compare an analog input voltage with the comparison voltage, and the result is stored in the A-D conversion registers. When an A-D conversion is completed, the control circuit sets the A-D conversion completion bit and the A-D interrupt request bit to "1".

Note that because the comparator consists of a capacitor coupling, set f(XIN) to 500 kHz or more during an A-D conversion.

When the A-D converter is operated at low-speed mode, f(XIN) and f(XCIN) do not have the lower limit of frequency, because of the A-D converter has a built-in self-oscillation circuit.

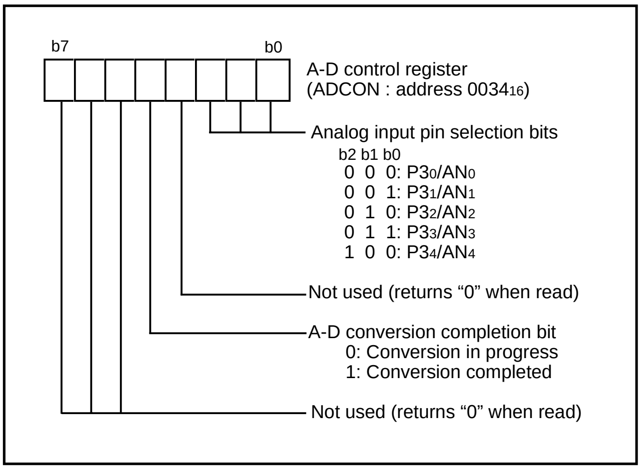


Fig. 44 Structure of A-D control register

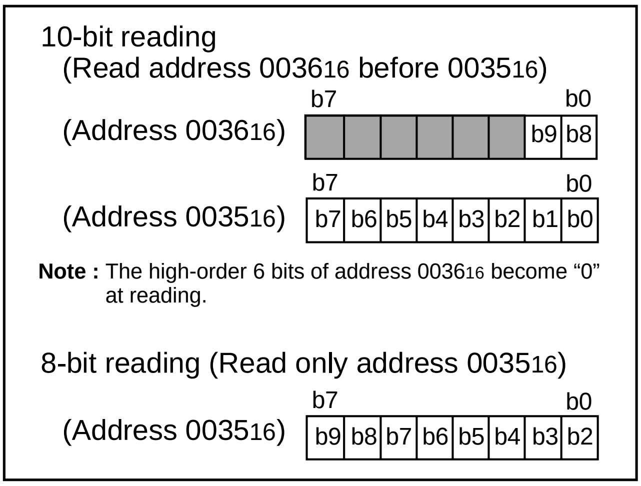


Fig. 45 Structure of A-D conversion registers

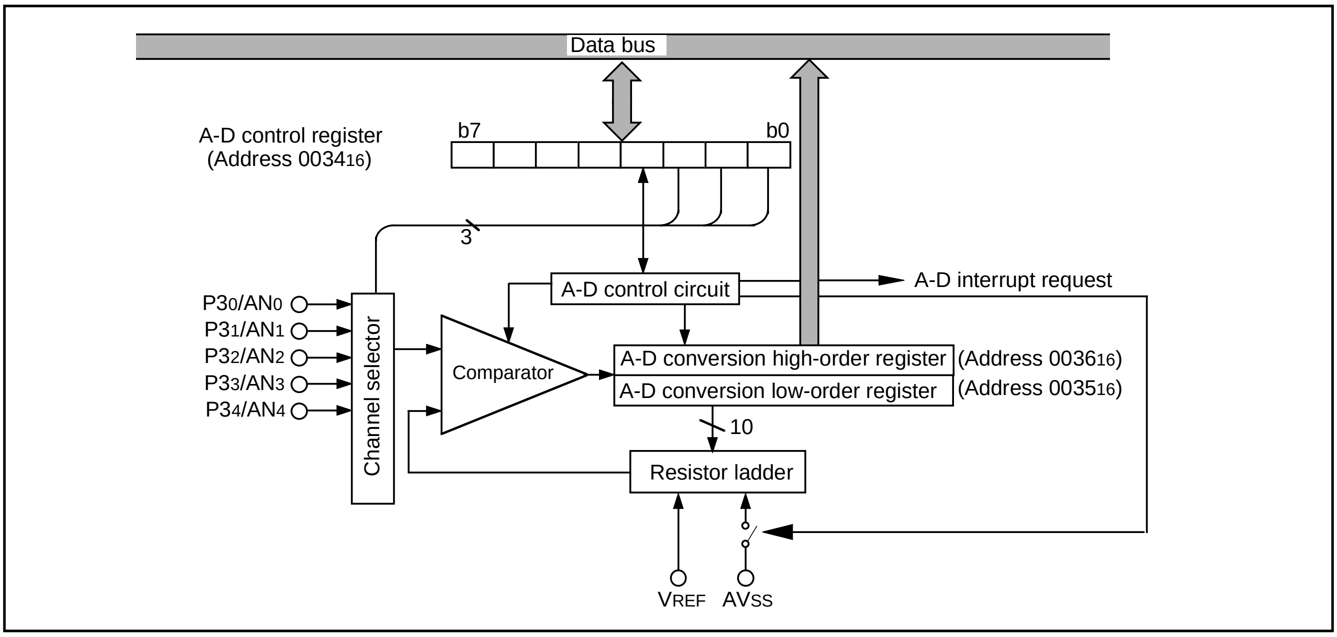


Fig. 46 Block diagram of A-D converter

WATCHDOG TIMER

The watchdog timer gives a mean of returning to the reset status when a program cannot run on a normal loop (for example, because of a software run-away). The watchdog timer consists of an 8-bit watchdog timer L and an 8-bit watchdog timer H.

Standard Operation of Watchdog Timer

When any data is not written into the watchdog timer control register (address 0039_{16}) after reset, the watchdog timer is in the stop state. The watchdog timer starts to count down by writing an optional value into the watchdog timer control register (address 0039_{16}) and an internal reset occurs at an underflow of the watchdog timer H.

Accordingly, programming is usually performed so that writing to the watchdog timer control register (address 0039_{16}) may be started before an underflow. When the watchdog timer control register (address 0039_{16}) is read, the values of the high-order 6 bits of the watchdog timer H, STP instruction disable bit, and watchdog timer H count source selection bit are read.

●Initial value of watchdog timer

At reset or writing to the watchdog timer control register (address 0039_{16}), each watchdog timer H and L are set to “FF_{16}”.

●Watchdog timer H count source selection bit operation

Bit 7 of the watchdog timer control register (address 0039_{16}) permits selecting a watchdog timer H count source. When this bit is set to “0”, the count source becomes the underflow signal of watchdog timer L. The detection time is set to 131.072 ms at f(XIN) = 8 MHz frequency and 32.768 s at f(XCIN) = 32 kHz frequency.

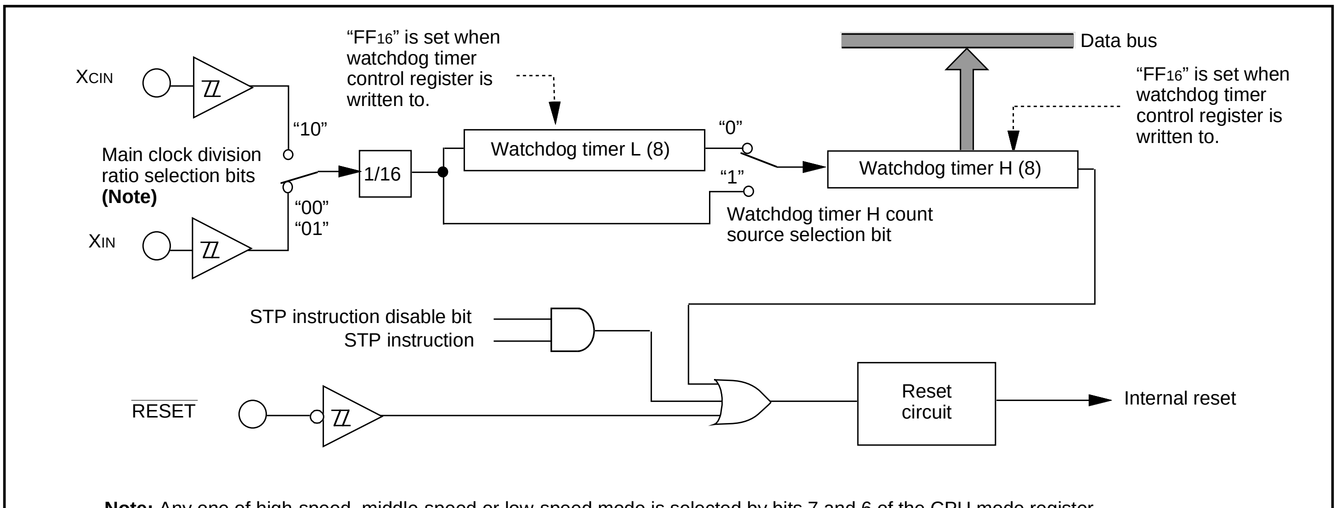
When this bit is set to “1”, the count source becomes the signal divided by 16 for f(XIN) (or f(XCIN)). The detection time in this case is set to 512 µs at f(XIN) = 8 MHz frequency and 128 ms at f(XCIN) = 32 kHz frequency. This bit is cleared to “0” after reset.

●Operation of STP instruction disable bit

Bit 6 of the watchdog timer control register (address 0039_{16}) permits disabling the STP instruction when the watchdog timer is in operation.

When this bit is “0”, the STP instruction is enabled.

When this bit is “1”, the STP instruction is disabled, once the STP instruction is executed, an internal reset occurs. When this bit is set to “1”, it cannot be rewritten to “0” by program. This bit is cleared to “0” after reset.



Note: Any one of high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register.

Fig. 47 Block diagram of Watchdog timer

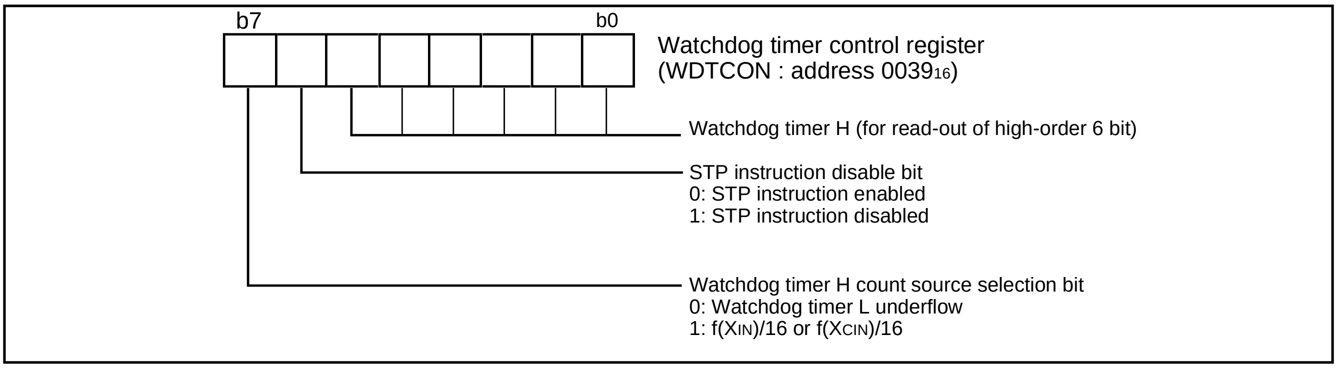


Fig. 48 Structure of Watchdog timer control register

RESET CIRCUIT

To reset the microcomputer, $\overline{\text{RESET}}$ pin must be held at an "L" level for 20 cycles or more of XIN. Then the $\overline{\text{RESET}}$ pin is returned to an "H" level (the power source voltage must be between 2.7 V and 5.5 V, and the oscillation must be stable), reset is released. After the reset is completed, the program starts from the address contained in address $FFFD_{16}$ (high-order byte) and address $FFFC_{16}$ (low-order byte). Make sure that the reset input voltage is less than 0.54 V for VCC of 2.7 V.

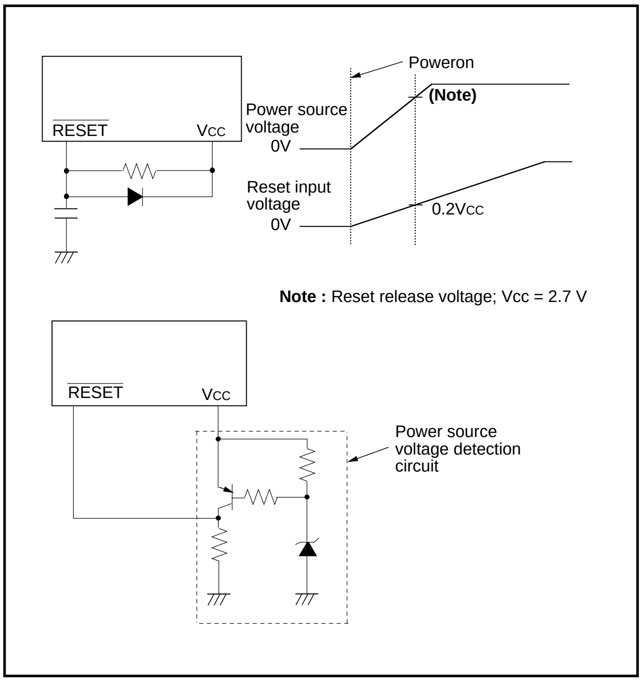


Fig. 49 Reset circuit example

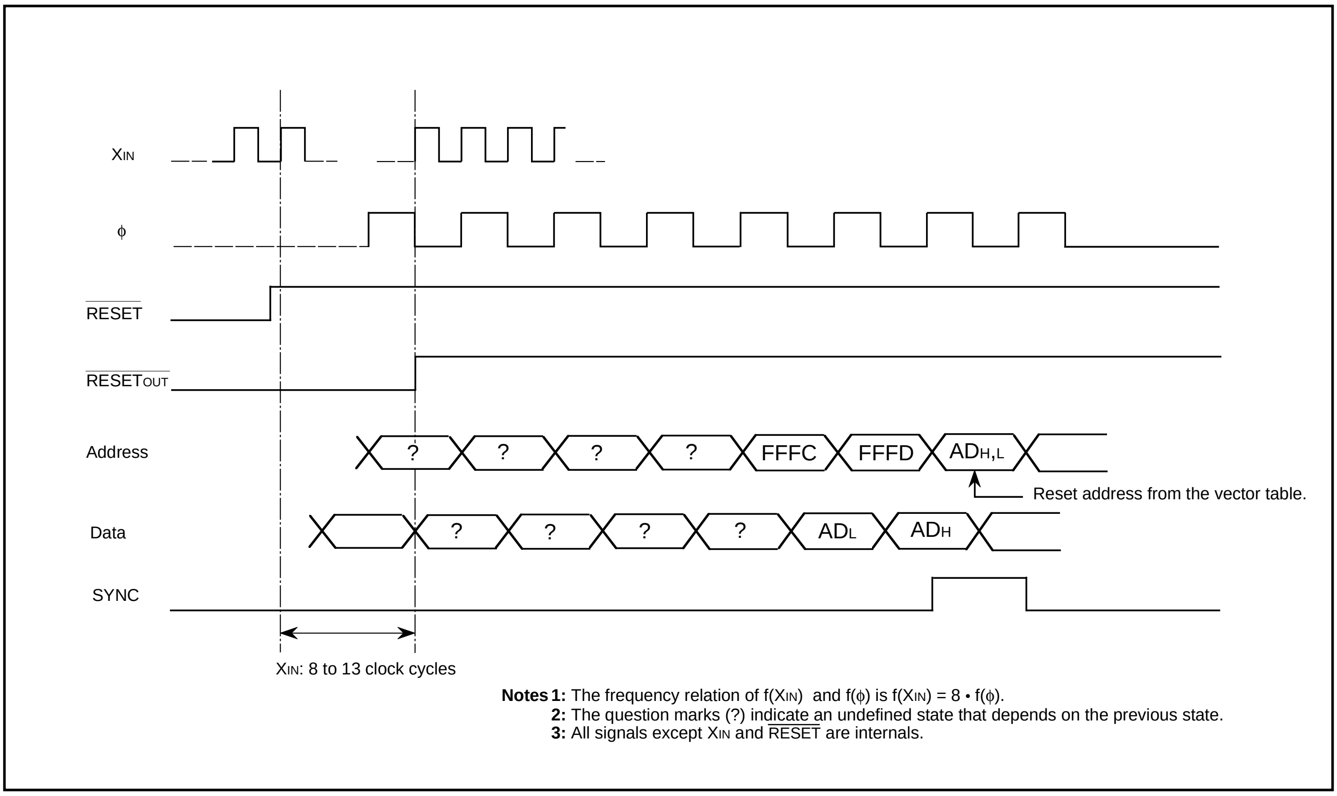


Fig. 50 Reset sequence

		Address	Register contents
(1)	Port P0 (P0)	0000_{16}	00_{16}
(2)	Port P0 direction register (P0D)	0001_{16}	00_{16}
(3)	Port P1 (P1)	0002_{16}	00_{16}
(4)	Port P1 direction register (P1D)	0003_{16}	00_{16}
(5)	Port P2 (P2)	0004_{16}	00_{16}
(6)	Port P2 direction register (P2D)	0005_{16}	00_{16}
(7)	Port P3 (P3)	0006_{16}	00_{16}
(8)	Port P3 direction register (P3D)	0007_{16}	00_{16}
(9)	Port P4 (P4)	0008_{16}	00_{16}
(10)	Port P4 direction register (P4D)	0009_{16}	00_{16}
(11)	Serial I/O2 control register 1 (SIO2CON1)	0015_{16}	00_{16}
(12)	Serial I/O2 control register 2 (SIO2CON2)	0016_{16}	0 0 0 0 0 1 1 1
(13)	Serial I/O2 register (SIO2)	0017_{16}	X X X X X X X X
(14)	Transmit/Receive buffer register (TB/RB)	0018_{16}	X X X X X X X X
(15)	Serial I/O1 status register (SIOSTS)	0019_{16}	1 0 0 0 0 0 0 0
(16)	Serial I/O1 control register (SIOCON)	$001A_{16}$	00_{16}
(17)	UART control register (UARTCON)	$001B_{16}$	1 1 1 0 0 0 0 0
(18)	Baud rate generator (BRG)	$001C_{16}$	X X X X X X X X
(19)	PWM control register (PWMCON)	$001D_{16}$	00_{16}
(20)	PWM prescaler (PREPWM)	$001E_{16}$	X X X X X X X X
(21)	PWM register (PWM)	$001F_{16}$	X X X X X X X X
(22)	Prescaler 12 (PRE12)	0020_{16}	FF_{16}
(23)	Timer 1 (T1)	0021_{16}	01_{16}
(24)	Timer 2 (T2)	0022_{16}	00_{16}
(25)	Timer XY mode register (TM)	0023_{16}	00_{16}
(26)	Prescaler X (PREX)	0024_{16}	FF_{16}
(27)	Timer X (TX)	0025_{16}	FF_{16}
(28)	Prescaler Y (PREY)	0026_{16}	FF_{16}
(29)	Timer Y (TY)	0027_{16}	FF_{16}
(30)	Timer count source selection register (TCSS)	0028_{16}	00_{16}
(31)	I²C address regiter (S0D)	$002C_{16}$	00_{16}
(32)	I²C status register (S1)	$002D_{16}$	0 0 0 1 0 0 0 X
(33)	I²C control register (S1D)	$002E_{16}$	00_{16}
(34)	I²C clock control register (S2)	$002F_{16}$	00_{16}
(35)	I²C start/stop condition control register (S2D)	0030_{16}	0 0 0 X X X X X

		Address	Register contents
(36)	A-D control register (ADCON)	0034_{16}	0 0 0 1 0 0 0 0
(37)	A-D conversion low-order register (ADL)	0035_{16}	X X X X X X X X
(38)	A-D conversion high-order register (ADH)	0036_{16}	0 0 0 0 0 0 X X
(39)	MISRG	0038_{16}	00_{16}
(40)	Watchdog timer control register (WDTCON)	0039_{16}	0 0 1 1 1 1 1 1
(41)	Interrupt edge selection register (INTEDGE)	$003A_{16}$	00_{16}
(42)	CPU mode register (CPUM)	$003B_{16}$	0 1 0 0 1 0 0 0
(43)	Interrupt request register 1 (IREQ1)	$003C_{16}$	00_{16}
(44)	Interrupt request register 2 (IREQ2)	$003D_{16}$	00_{16}
(45)	Interrupt control register 1 (ICON1)	$003E_{16}$	00_{16}
(46)	Interrupt control register 2 (ICON2)	$003F_{16}$	00_{16}
(47)	Processor status register	(PS)	X X X X X 1 X X
(48)	Program counter	(PC_H)	$FFFD_{16}$ contents
		(PC_L)	$FFFC_{16}$ contents

Note : X : Not fixed
Since the initial values for other than above mentioned registers and RAM contents are indefinite at reset, they must be set.

Fig. 51 Internal status at reset

CLOCK GENERATING CIRCUIT

The 3851 group (built-in 24 KB or more ROM) has two built-in oscillation circuits: main clock XIN-XOUT oscillation circuit and sub clock XCIN-XCOUT oscillation circuit. An oscillation circuit can be formed by connecting a resonator between XIN and XOUT (XCIN and XCOUT). Use the circuit constants in accordance with the resonator manufacturer's recommended values. No external resistor is needed between XIN and XOUT since a feed-back resistor exists on-chip. However, an external feed-back resistor is needed between XCIN and XCOUT.
Immediately after power on, only the XIN oscillation circuit starts oscillating, and XCIN and XCOUT pins function as I/O ports.

Frequency Control
(1) Middle-speed mode

The internal clock φ is the frequency of XIN divided by 8. After reset is released, this mode is selected.

(2) High-speed mode

The internal clock φ is half the frequency of XIN.

(3) Low-speed mode

The internal clock φ is half the frequency of XCIN.

■Note

If you switch the mode between middle/high-speed and low-speed, stabilize both XIN and XCIN oscillations. The sufficient time is required for the sub-clock to stabilize, especially immediately after power on and at returning from the stop mode. When switching the mode between middle/high-speed and low-speed, set the frequency on condition that f(XIN) > 3•f(XCIN).

(4) Low power dissipation mode

The low power consumption operation can be realized by stopping the main clock XIN in low-speed mode. To stop the main clock, set bit 5 of the CPU mode register to "1". When the main clock XIN is restarted (by setting the main clock stop bit to "0"), set sufficient time for oscillation to stabilize.
The sub-clock XCIN-XCOUT oscillation circuit can not directly input clocks that are generated externally. Accordingly, make sure to cause an external resonator to oscillate.

Oscillation Control
(1) Stop mode

If the STP instruction is executed, the internal clock φ stops at an "H" level, and XIN and XCIN oscillation stops. When the oscillation stabilizing time set after STP instruction released bit is "0", the prescaler 12 is set to "FF$_{16}$" and timer 1 is set to "01$_{16}$". When the oscillation stabilizing time set after STP instruction released bit is "1", set the sufficient time for oscillation of used oscillator to stabilize since nothing is set to the prescaler 12 and timer 1.
Either XIN or XCIN divided by 16 is input to the prescaler 12 as count source. Oscillator restarts when an external interrupt is received, but the internal clock φ is not supplied to the CPU (remains at "H") until timer 1 underflows. The internal clock φ is supplied for the first time, when timer 1 underflows. This ensures time for the clock oscillation using the ceramic resonators to be stabilized.
When the oscillator is restarted by reset, apply "L" level to the $\overline{\text{RESET}}$ pin until the oscillation is stable since a wait time will not be generated.

(2) Wait mode

If the WIT instruction is executed, the internal clock φ stops at an "H" level, but the oscillator does not stop. The internal clock φ restarts at reset or when an interrupt is received. Since the oscillator does not stop, normal operation can be started immediately after the clock is restarted.
To ensure that the interrupts will be received to release the STP or WIT state, their interrupt enable bits must be set to "1" before executing of the STP or WIT instruction.
When releasing the STP state, the prescaler 12 and timer 1 will start counting the clock XIN divided by 16. Accordingly, set the timer 1 interrupt enable bit to "0" before executing the STP instruction.

■Note

When using the oscillation stabilizing time set after STP instruction released bit set to "1", evaluate time to stabilize oscillation of the used oscillator and set the value to the timer 1 and prescaler 12.

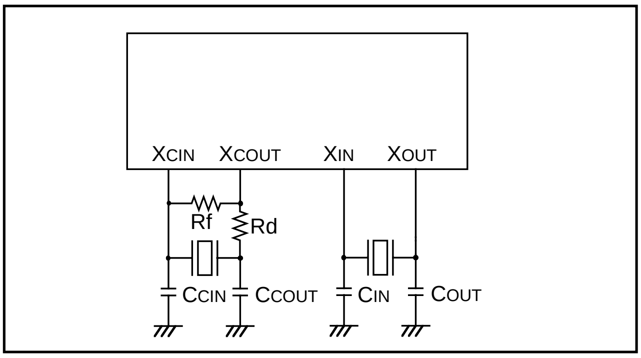


Fig. 52 Ceramic resonator circuit

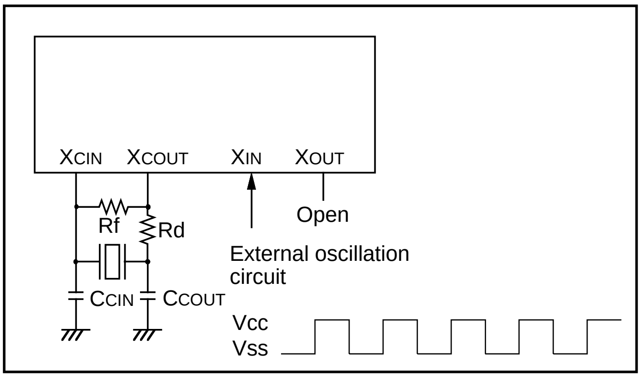
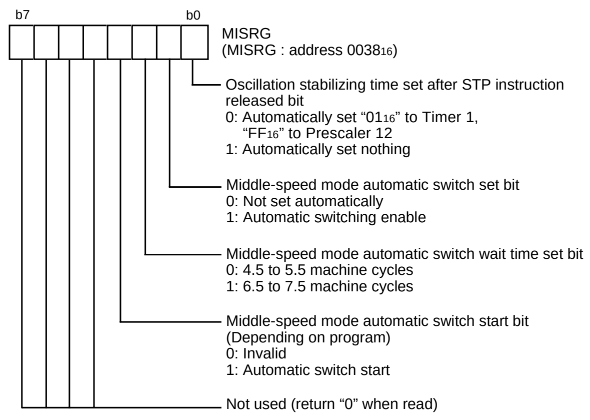


Fig. 53 External clock input circuit

RENESAS

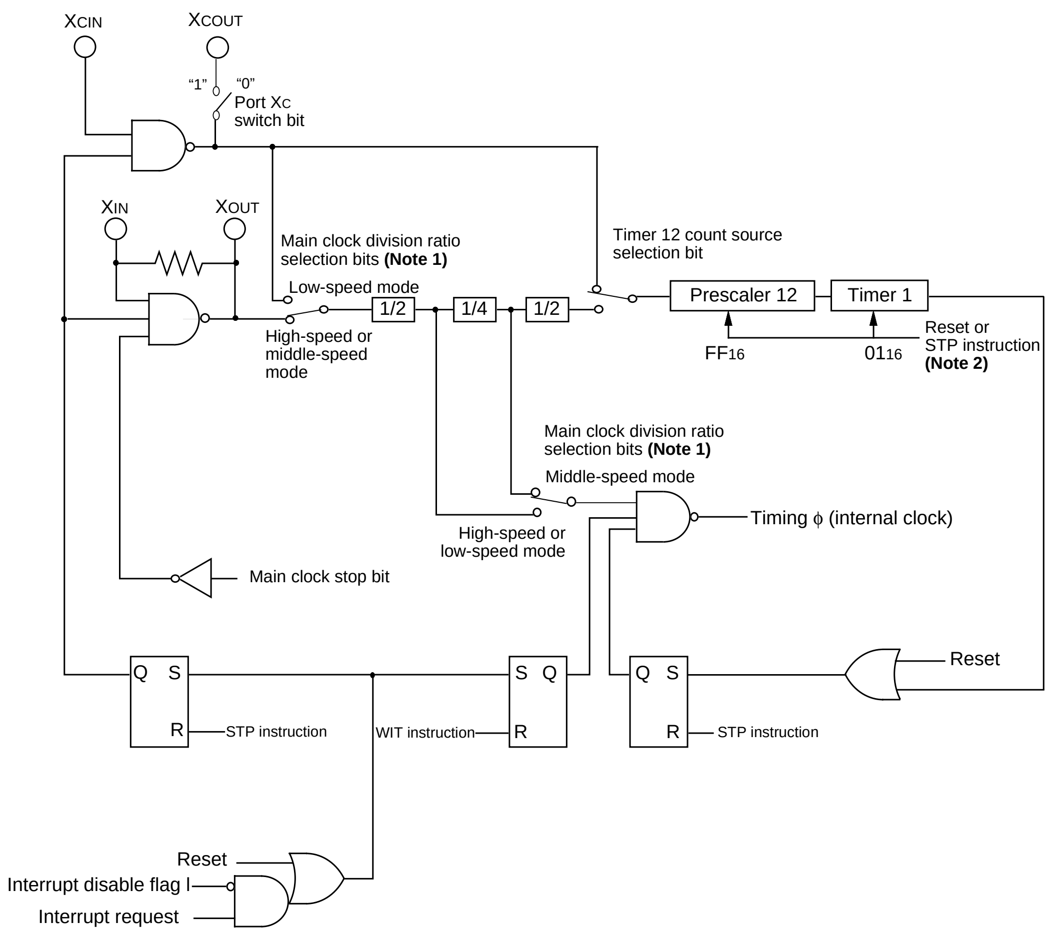
■Notes on middle-speed mode automatic switch set bit

When the middle-speed mode automatic switch set bit is set to “1” while operating in the low-speed mode, by detecting the rising/falling edge of the SCL or SDA pin, XIN oscillation automatically starts and the mode is automatically switched to the middle-speed mode. The timing which changes from the low-speed mode to the middle-speed mode can be set as 4.5 to 5.5 cycle, or 6.5 to 7.5 cycle in the low-speed mode by the middle-speed mode automatic switch waiting time set bit. Select according to the oscillation start characteristic of the XIN oscillator to be used.



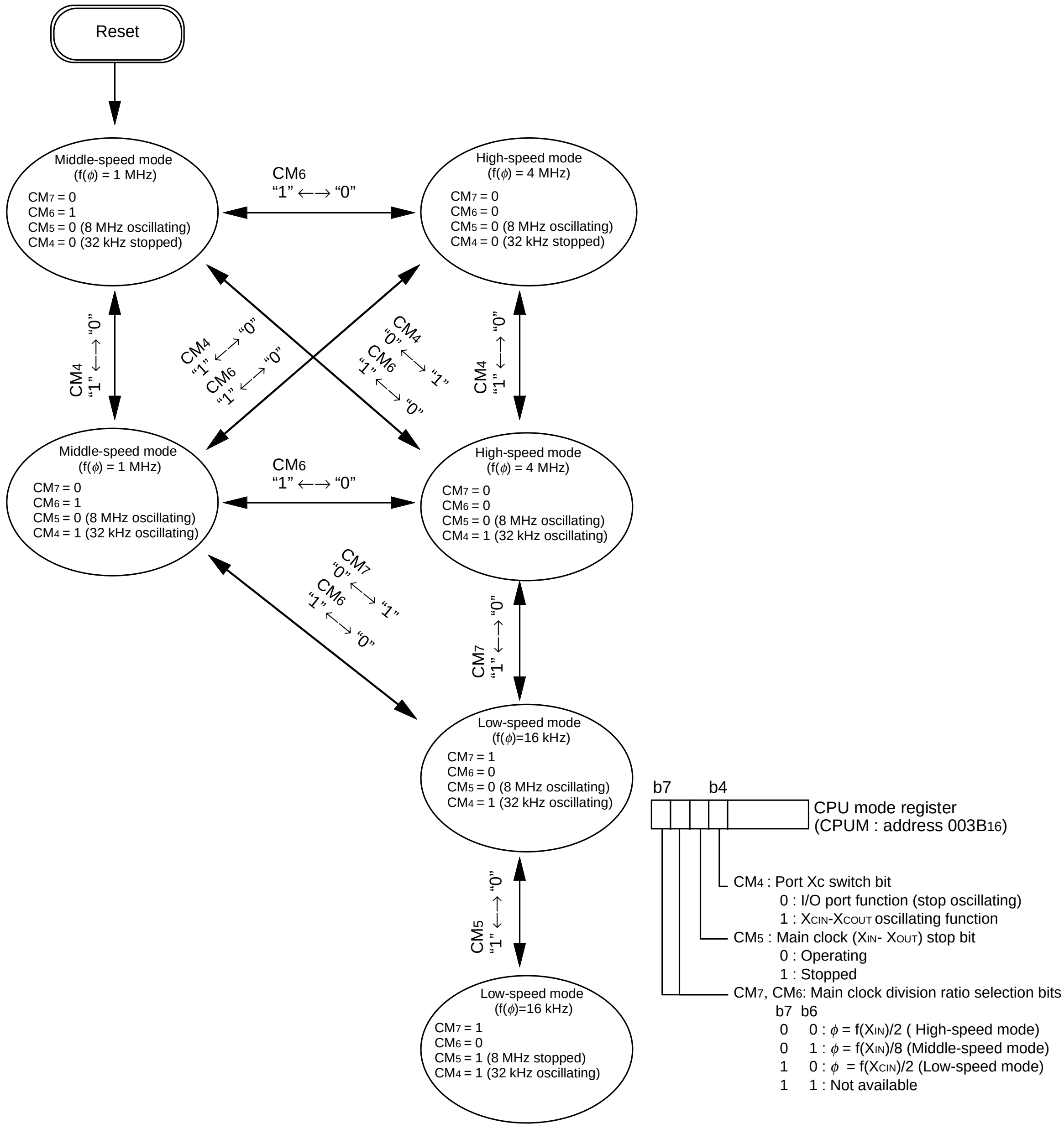
Note: When the mode is automatically switched from the low-speed mode to the middle-speed mode, the value of CPU mode register (address $003B_{16}$) changes.

Fig. 54 Structure of MISRG



Notes 1: Any one of high-speed, middle-speed or low-speed mode is selected by bits 7 and 6 of the CPU mode register.
When low-speed mode is selected, set port Xc switch bit (b4) to “1”.
2: When bit 0 of MISRG = “0”

Fig. 55 System clock generating circuit block diagram (Single-chip mode)



Notes 1 : Switch the mode by the allows shown between the mode blocks. (Do not switch between the modes directly without an allow.)

2 : The all modes can be switched to the stop mode or the wait mode and return to the source mode when the stop mode or the wait mode is ended.

3 : Timer operates in the wait mode.

4 : When bit 0 of MISRG is "0" and the stop mode is ended, a delay of approximately 1 ms occurs by connecting timer 1 in middle/high-speed mode.

5 : When bit 0 of MISRG is "0" and the stop mode is ended, the following is performed.
(1) After the clock is restarted, a delay of approximately 256 ms occurs in low-speed mode if Timer 12 count source selection bit is "0".
(2) After the clock is restarted, a delay of approximately 16 ms occurs in low-speed mode if Timer 12 count source selection bit is "1".

6 : Wait until oscillation stabilizes after oscillating the main clock X_{IN} before the switching from the low-speed mode to middle/high-speed mode.

7 : The example assumes that 8 MHz is being applied to the X_{IN} pin and 32 kHz to the X_{CIN} pin. ϕ indicates the internal clock.

Fig. 56 State transitions of system clock

FLASH MEMORY MODE

The M38517F8 (flash memory version) has an internal new DINOR (DIvided bit line NOR) flash memory that can be rewritten with a single power source when VCC is 5 V, and 2 power sources when VPP is 5 V and VCC is 3.0-5.5 V in the CPU rewrite and standard serial I/O modes.

For this flash memory, three flash memory modes are available in which to read, program, and erase: the parallel I/O and standard serial I/O modes in which the flash memory can be manipulated using a programmer and the CPU rewrite mode in which the flash memory can be manipulated by the Central Processing Unit (CPU).

Summary

Table 15 lists the summary of the M38517F8 (flash memory version).

The flash memory of the M38517F8 is divided into User ROM area and Boot ROM area as shown in Figure 57.

In addition to the ordinary User ROM area to store the MCU operation control program, the flash memory has a Boot ROM area that is used to store a program to control rewriting in CPU rewrite and standard serial I/O modes. This Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. However, the user can write a rewrite control program in this area that suits the user's application system. This Boot ROM area can be rewritten in only parallel I/O mode.

Table 15 Summary of M38517F8 (flash memory version)

Item		Specifications
Power source voltage		Vcc = 2.7– 5.5 V **(Note 1)** Vcc = 2.7–3.6 V **(Note 2)**
VPP voltage (For Program/Erase)		4.5-5.5 V
Flash memory mode		3 modes (Parallel I/O mode, Standard serial I/O mode, CPU rewrite mode)
Erase block division	User ROM area	1 block (32 Kbytes)
	Boot ROM area	1 block (4 Kbytes) (**Note 3**)
Program method		Byte program
Erase method		Batch erasing
Program/Erase control method		Program/Erase control by software command
Number of commands		6 commands
Number of program/Erase times		100 times
ROM code protection		Available in parallel I/O mode and standard serial I/O mode

Notes 1: The power source voltage must be Vcc = 4.5–5.5 V at program and erase operation.
2: The power source voltage can be Vcc = 3.0–3.6 V also at program and erase operation.
3: The Boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the factory. This Boot ROM area can be rewritten in only parallel I/O mode.

(1) CPU Rewrite Mode

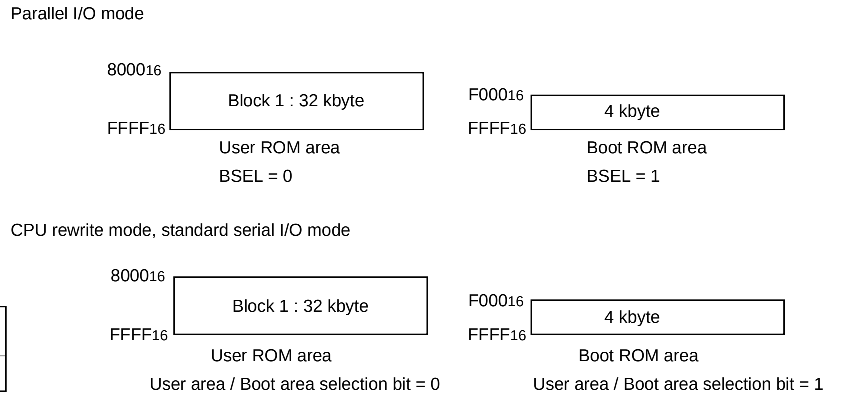
In CPU rewrite mode, the internal flash memory can be operated on (read, program, or erase) under control of the Central Processing Unit (CPU).
In CPU rewrite mode, only the User ROM area shown in Figure 57 can be rewritten; the Boot ROM area cannot be rewritten. Make sure the program and block erase commands are issued for only the User ROM area and each block area.
The control program for CPU rewrite mode can be stored in either User ROM or Boot ROM area. In the CPU rewrite mode, because the flash memory cannot be read from the CPU, the rewrite control program must be transferred to internal RAM area to be executed before it can be executed.

Microcomputer Mode and Boot Mode

The control program for CPU rewrite mode must be written into the User ROM or Boot ROM area in parallel I/O mode beforehand. (If the control program is written into the Boot ROM area, the standard serial I/O mode becomes unusable.)
See Figure 57 for details about the Boot ROM area.
Normal microcomputer mode is entered when the microcomputer is reset with pulling CNV_{SS} pin low. In this case, the CPU starts operating using the control program in the User ROM area.
When the microcomputer is reset by pulling the $P4_1/INT_0$ pin high, the CNVss pin high, the CPU starts operating using the control program in the Boot ROM area (program start address is $FFFC_{16}$, $FFFD_{16}$ fixation). This mode is called the “Boot” mode.

Block Address

Block addresses refer to the maximum address of each block. These addresses are used in the block erase command. In case of the M38517F8, it has only one block.



Product name	Flash memory start address
M38517F8	8000_{16}

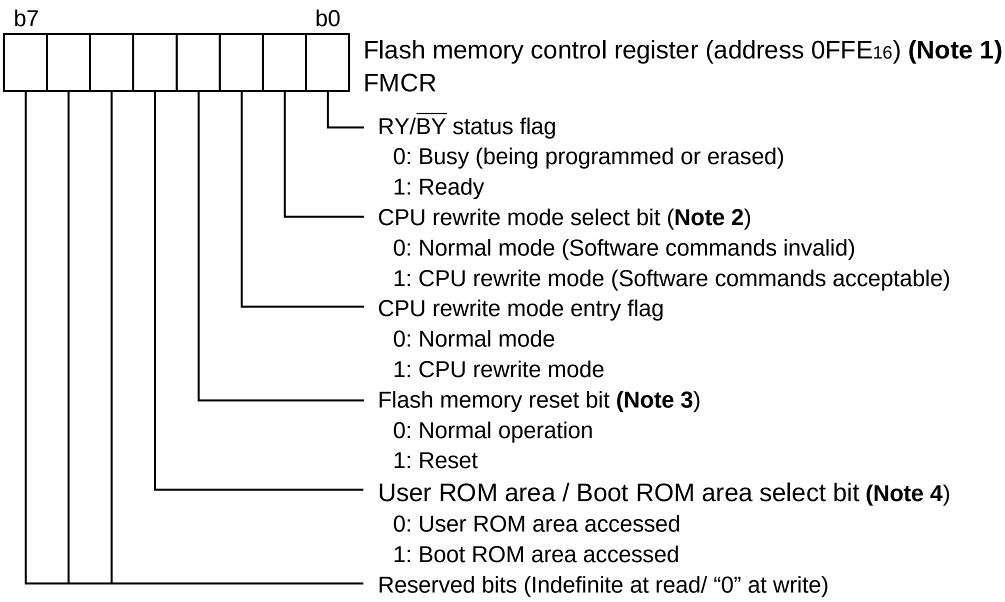
Notes 1: The Boot ROM area can be rewritten in only parallel input/output mode. (Access to any other areas is inhibited.)
2: To specify a block, use the maximum address in the block.

Fig. 57 Block diagram of built-in flash memory

Outline Performance (CPU Rewrite Mode)

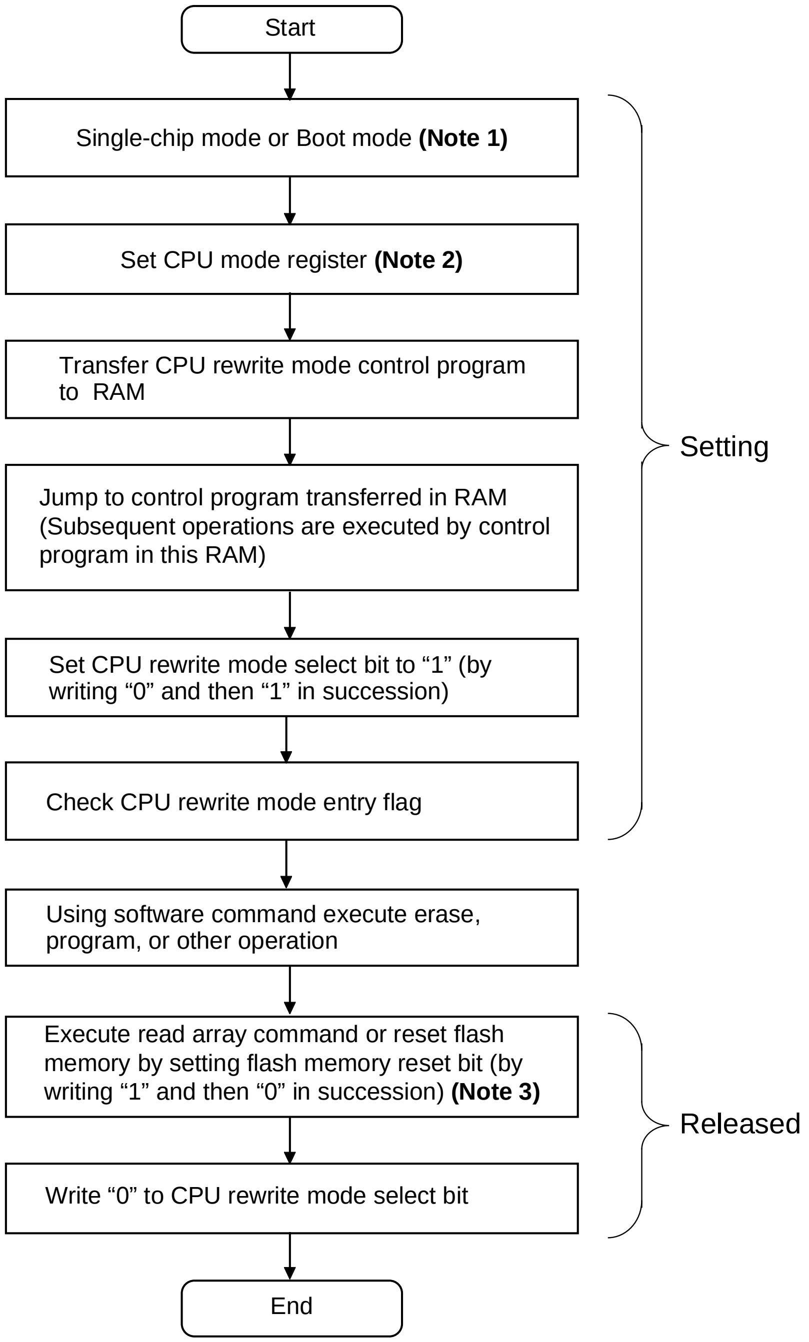
CPU rewrite mode is usable in the single-chip or Boot mode. The only User ROM area can be rewritten in CPU rewrite mode.
In CPU rewrite mode, the CPU erases, programs and reads the internal flash memory by executing software commands. This rewrite control program must be transferred to the RAM before it can be executed.
The MCU enters CPU rewrite mode by applying 5 V ± 0.5 V to the CNV$_{SS}$ pin and setting “1” to the CPU Rewrite Mode Select Bit (bit 1 of address 0FFE$_{16}$). Software commands are accepted once the mode is entered.
Use software commands to control program and erase operations. Whether a program or erase operation has terminated normally or in error can be verified by reading the status register.

Figure 58 shows the flash memory control register.
Bit 0 is the RY/$\overline{\text{BY}}$ status flag used exclusively to read the operating status of the flash memory. During programming and erase operations, it is “0” (busy). Otherwise, it is “1” (ready).
Bit 1 is the CPU Rewrite Mode Select Bit. When this bit is set to “1”, the MCU enters CPU rewrite mode. Software commands are accepted once the mode is entered. In CPU rewrite mode, the CPU becomes unable to access the internal flash memory directly. Therefore, use the control program in the RAM for write to bit 1. To set this bit to “1”, it is necessary to write “0” and then write “1” in succession. The bit can be set to “0” by only writing “0”.
Bit 2 is the CPU Rewrite Mode Entry Flag. This flag indicates “1” in CPU rewrite mode, so that reading this flag can check whether CPU rewrite mode has been entered or not.
Bit 3 is the flash memory reset bit used to reset the control circuit of internal flash memory. This bit is used when exiting CPU rewrite mode and when flash memory access has failed. When the CPU Rewrite Mode Select Bit is “1”, setting “1” for this bit resets the control circuit. To set this bit to “1”, it is necessary to write “0” and then write “1” in succession. To release the reset, it is necessary to set this bit to “0”.
Bit 4 is the User Area/Boot Area Select Bit. When this bit is set to “1”, Boot ROM area is accessed, and CPU rewrite mode in Boot ROM area is available. In Boot mode, this bit is set to “1” automatically. Reprogramming of this bit must be in the RAM.
Figure 59 shows a flowchart for setting/releasing CPU rewrite mode.



Notes **1**: The contents of flash memory control register are “XXX00001” just after reset release. In the mask ROM version, this address is reserved area.
2: For this bit to be set to “1”, the user needs to write “0” and then “1” to it in succession. If it is not this procedure, this bit will not be set to “1”. Additionally, it is required to ensure that no interrupt will be generated during that interval.
Use the control program in the area except the built-in flash memory for write to this bit.
3: This bit is valid when the CPU rewrite mode select bit is “1”. Set this bit 3 to “0” subsequently after setting bit 3 to “1”.
4: Use the control program in the area except the built-in flash memory for write to this bit.

Fig. 58 Structure of flash memory control register



Notes 1: When starting the MCU in the single-chip mode, supply 4.5 V to 5.5 V to the CNVss pin until checking the CPU rewrite mode entry flag.
2: Set bits 6, 7 (main clock division ratio selection bits) at CPU mode register ($003B_{16}$).
3: Before exiting the CPU rewrite mode after completing erase or program operation, always be sure to execute the read array command or reset the flash memory.

Fig. 59 CPU rewrite mode set/release flowchart

Precautions on CPU Rewrite Mode

Described below are the precautions to be observed when rewriting the flash memory in CPU rewrite mode.

(1) Operation speed

During CPU rewrite mode, set the internal clock frequency 4.0 MHz or less using the main clock division ratio selection bits (bit 6, 7 at 003B16).

(2) Instructions inhibited against use

The instructions which refer to the internal data of the flash memory cannot be used during CPU rewrite mode .

(3) Interrupts inhibited against use

The interrupts cannot be used during CPU rewrite mode because they refer to the internal data of the flash memory.

(4) Watchdog timer

In case of the watchdog timer has been running already, the internal reset generated by watchdog timer underflow does not happen, because of watchdog timer is always clearing during program or erase operation.

(5) Reset

Reset is always valid. In case of CNV_{SS} = H when reset is released, boot mode is active. So the program starts from the address contained in address $FFFC_{16}$ and $FFFD_{16}$ in boot ROM area.

Software Commands (CPU Rewrite Mode)

Table 16 lists the software commands.
After setting the CPU Rewrite Mode Select Bit of the flash memory control register to "1", execute a software command to specify an erase or program operation.
Each software command is explained below.

●Read Array Command (FF_{16})

The read array mode is entered by writing the command code "FF_{16}" in the first bus cycle. When an address to be read is input in one of the bus cycles that follow, the contents of the specified address are read out at the data bus (D_0 to D_7).
The read array mode is retained intact until another command is written.

●Read Status Register Command (70_{16})

The read status register mode is entered by writing the command code "70_{16}" in the first bus cycle. The contents of the status register are read out at the data bus (D_0 to D_7) by a read in the second bus cycle.
The status register is explained in the next section.

●Clear Status Register Command (50_{16})

This command is used to clear the bits SR1, SR4, and SR5 of the status register after they have been set. These bits indicate that operation has ended in an error. To use this command, write the command code "50_{16}" in the first bus cycle.

●Program Command (40_{16})

Program operation starts when the command code "40_{16}" is written in the first bus cycle. Then, if the address and data to program are written in the 2nd bus cycle, program operation (data programming and verification) will start.
Whether the write operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ Status Flag of the flash memory control register. When the program starts, the read status register mode is entered automatically and the contents of the status register is read at the data bus (D_0 to D_7). The status register bit 7 (SR7) is set to "0" at the same time the write operation starts and is returned to "1" upon completion of the write operation. In this case, the read status register mode remains active until the next command is written.
The RY/$\overline{BY}$ Status Flag is "0" (busy) during write operation and "1" (ready) when the write operation is completed as is the status register bit 7.
At program end, program results can be checked by reading bit 4 (SR4) of the status register.

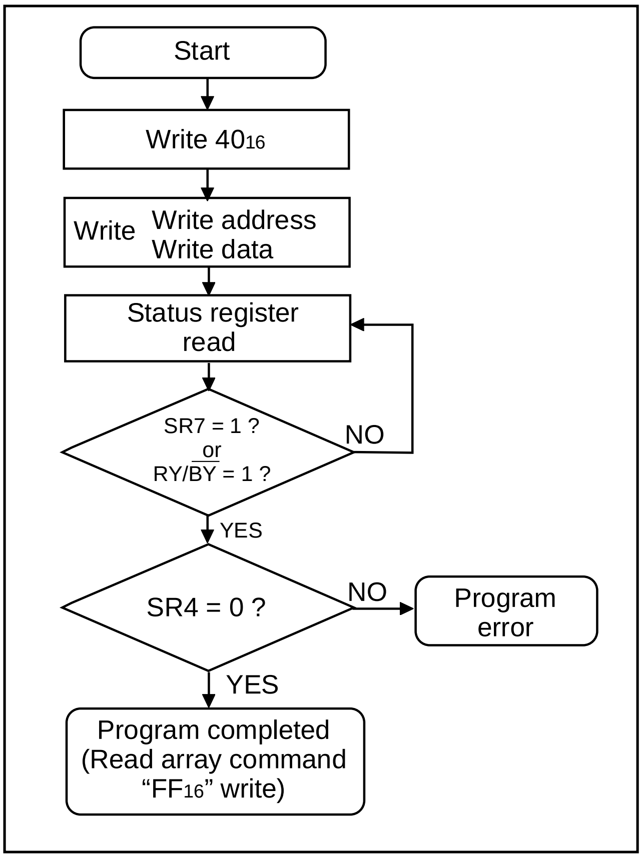


Fig. 60 Program flowchart

Table 16 List of software commands (CPU rewrite mode)

Command	Cycle number	First bus cycle			Second bus cycle		
		Mode	Address	Data (D_0 to D_7)	Mode	Address	Data (D_0 to D_7)
Read array	1	Write	X **(Note 1)**	FF_{16}			
Read status register	2	Write	X	70_{16}	Read	X	SRD **(Note 2)**
Clear status register	1	Write	X	50_{16}			
Program	2	Write	X	40_{16}	Write	WA **(Note 3)**	WD **(Note 3)**
Erase all blocks	2	Write	X	20_{16}	Write	X	20_{16}
Block erase	2	Write	X	20_{16}	Write	BA **(Note 4)**	$D0_{16}$

Notes 1: X denotes a given address in the User ROM area .
2: SRD = Status Register Data
3: WA = Write Address, WD = Write Data
4: BA = Block Address to be erased (Input the maximum address of each block.)

●Erase All Blocks Command (20_{16}/20_{16})

By writing the command code “20_{16}” in the first bus cycle and the confirmation command code “20_{16}” in the second bus cycle that follows, the operation of erase all blocks (erase and erase verify) starts.
Whether the erase all blocks command is terminated can be confirmed by reading the status register or the RY/$\overline{BY}$ Status Flag of flash memory control register. When the erase all blocks operation starts, the read status register mode is entered automatically and the contents of the status register can be read out at the data bus (D_0 to D_7). The status register bit 7 (SR7) is set to “0” at the same time the erase operation starts and is returned to “1” upon completion of the erase operation. In this case, the read status register mode remains active until another command is written.
The RY/$\overline{BY}$ Status Flag is “0” during erase operation and “1” when the erase operation is completed as is the status register bit 7 (SR7).
After the erase all blocks end, erase results can be checked by reading bit 5 (SRS) of the status register. For details, refer to the section where the status register is detailed.

●Block Erase Command (20_{16}/$D0_{16}$)

By writing the command code “20_{16}” in the first bus cycle and the confirmation command code “$D0_{16}$” and the block address in the second bus cycle that follows, the block erase (erase and erase verify) operation starts for the block address of the flash memory to be specified.
Whether the block erase operation is completed can be confirmed by reading the status register or the RY/$\overline{BY}$ Status Flag of flash memory control register. At the same time the block erase operation starts, the read status register mode is automatically entered, so that the contents of the status register can be read out. The status register bit 7 (SR7) is set to “0” at the same time the block erase operation starts and is returned to “1” upon completion of the block erase operation. In this case, the read status register mode remains active until the read array command (FF_{16}) is written.
The RY/$\overline{BY}$ Status Flag is “0” during block erase operation and “1” when the block erase operation is completed as is the status register bit 7.
After the block erase ends, erase results can be checked by reading bit 5 (SRS) of the status register. For details, refer to the section where the status register is detailed.

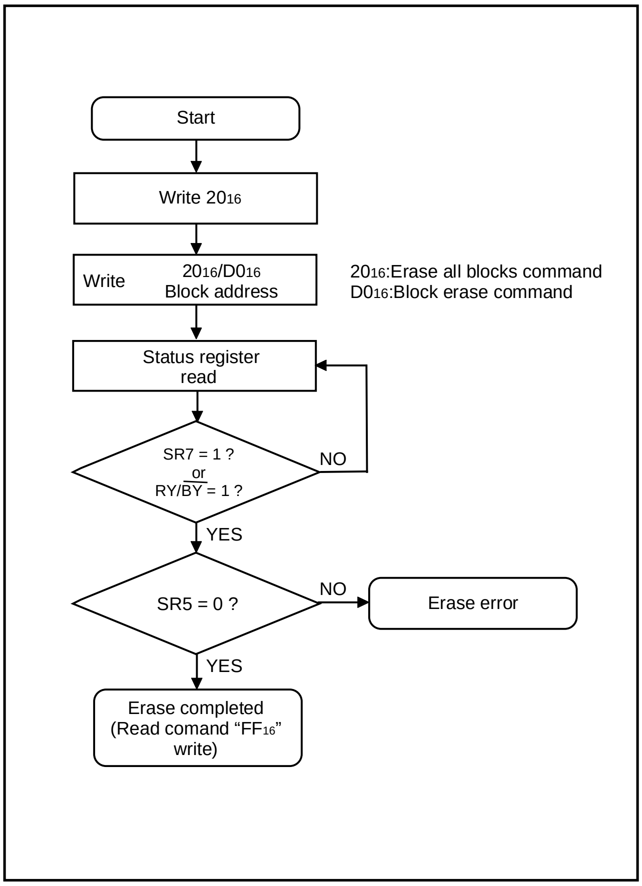


Fig. 61 Erase flowchart

Status Register (SRD)

The status register shows the operating status of the flash memory and whether erase operations and programs ended successfully or in error. It can be read in the following ways:

(1) By reading an arbitrary address from the User ROM area after writing the read status register command (70_{16})

(2) By reading an arbitrary address from the User ROM area in the period from when the program starts or erase operation starts to when the read array command (FF_{16}) is input.

Also, the status register can be cleared by writing the clear status register command (50_{16}).
After reset, the status register is set to “80_{16}”.
Table 17 shows the status register. Each bit in this register is explained below.

•Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory. This bit is set to “0” (busy) during write or erase operation and is set to “1” when these operations ends.
After power-on, the sequencer status is set to “1” (ready).

•Erase status (SR5)

The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to “1”. When the erase status is cleared, it is set to “0”.

•Program status (SR4)

The program status indicates the operating status of write operation. When a write error occurs, it is set to “1”.
The program status is set to “0” when it is cleared.

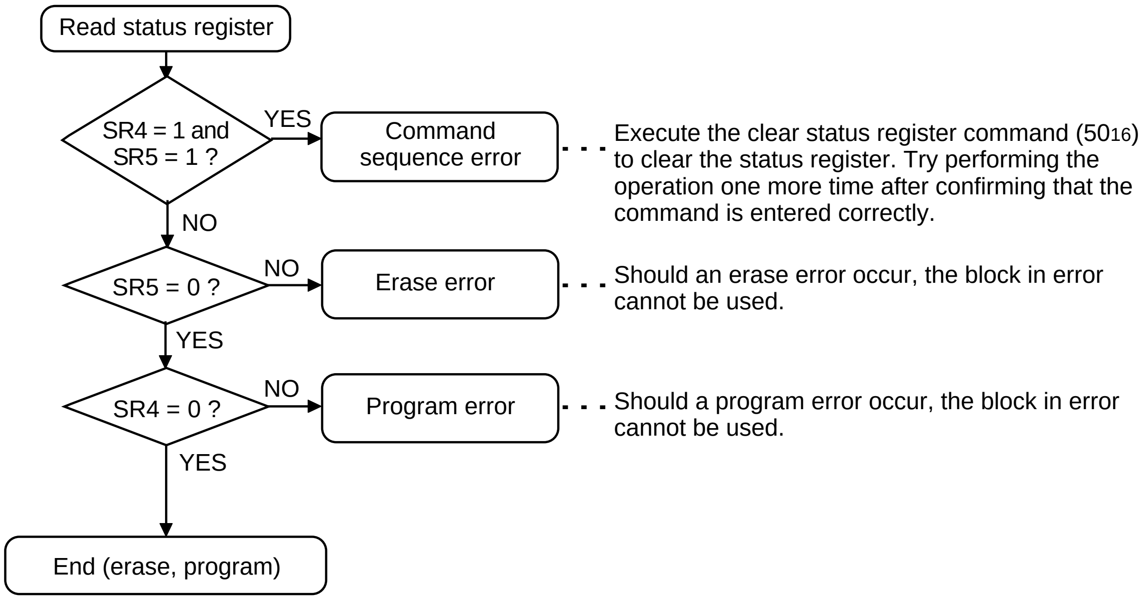
If “1” is written for any of the SR5 and SR4 bits, the program, erase all blocks, and block erase commands are not accepted. Before executing these commands, execute the clear status register command (50_{16}) and clear the status register.
Also, if any commands are not correct, both SR5 and SR4 are set to “1”.

Table 17 Definition of each bit in status register (SRD)

Symbol	Status name	Definition	
		“1”	“0”
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

Full Status Check

By performing full status check, it is possible to know the execution results of erase and program operations. Figure 62 shows a full status check flowchart and the action to be taken when each error occurs.



Note: When one of SR5 and SR4 is set to "1", none of the read array, the program, erase all blocks, and block erase commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 62 Full status check flowchart and remedial procedure for errors

Functions To Inhibit Rewriting Flash Memory Version

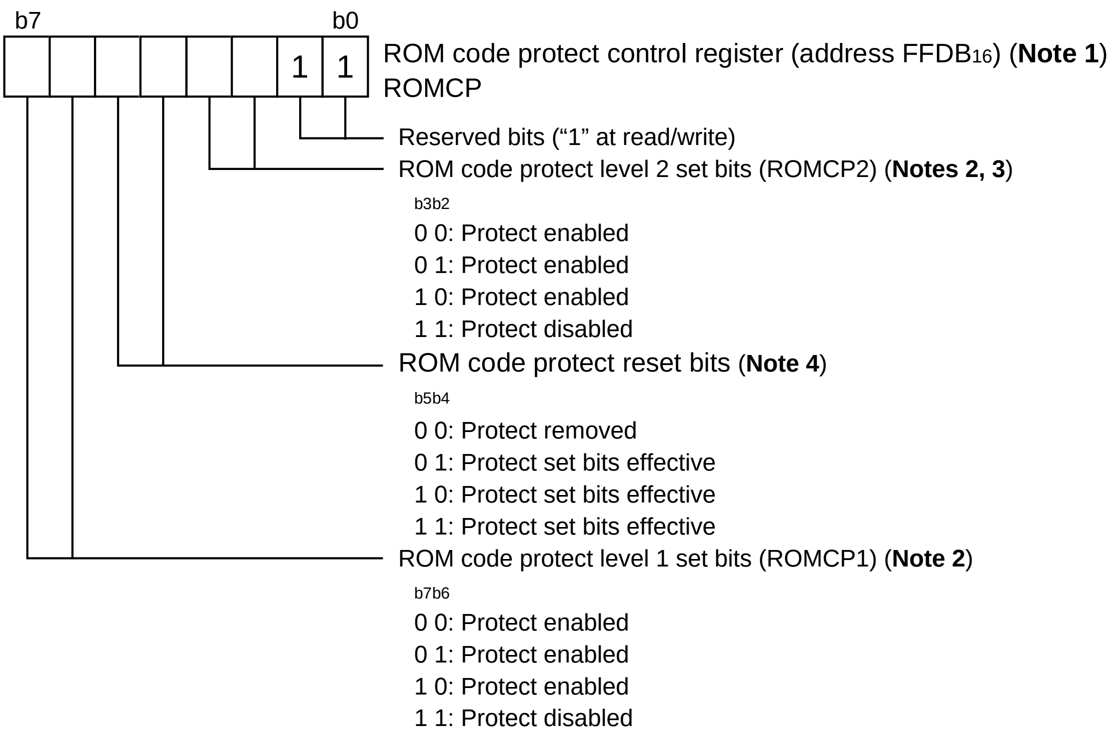
To prevent the contents of internal flash memory from being read out or rewritten easily, this MCU incorporates a ROM code protect function for use in parallel I/O mode and an ID code check function for use in standard serial I/O mode.

●ROM Code Protect Function (in Parallel I/O Mode)

The ROM code protect function is the function to inhibit reading out or modifying the contents of internal flash memory by using the ROM code protect control (address $FFDB_{16}$) in parallel I/O mode. Figure 63 shows the ROM code protect control (address $FFDB_{16}$). (This address exists in the User ROM area.)

If one or both of the pair of ROM Code Protect Bits is set to “0”, the ROM code protect is turned on, so that the contents of internal flash memory are protected against readout and modification. The ROM code protect is implemented in two levels. If level 2 is selected, the flash memory is protected even against readout by a shipment inspection LSI tester, etc. When an attempt is made to select both level 1 and level 2, level 2 is selected by default.

If both of the two ROM Code Protect Reset Bits are set to “00”, the ROM code protect is turned off, so that the contents of internal flash memory can be read out or modified. Once the ROM code protect is turned on, the contents of the ROM Code Protect Reset Bits cannot be modified in parallel I/O mode. Use the serial I/O or CPU rewrite mode to rewrite the contents of the ROM Code Protect Reset Bits.



Notes 1: This area is on the ROM in the mask ROM version.
2: When ROM code protect is turned on, the internal flash memory is protected against readout or modification in parallel I/O mode.
3: When ROM code protect level 2 is turned on, ROM code readout by a shipment inspection LSI tester, etc. also is inhibited.
4: The ROM code protect reset bits can be used to turn off ROM code protect level 1 and ROM code protect level 2. However, since these bits cannot be modified in parallel I/O mode, they need to be rewritten in standard serial I/O mode or CPU rewrite mode.

Fig. 63 Structure of ROM code protect control

ID Code Check Function (in Standard serial I/O mode)

Use this function in standard serial I/O mode. When the contents of the flash memory are not blank, the ID code sent from the programmer is compared with the ID code written in the flash memory to see if they match. If the ID codes do not match, the commands sent from the programmer are not accepted. The ID code consists of 8-bit data, and its areas are $FFD4_{16}$ to $FFDA_{16}$. Write a program which has had the ID code preset at these addresses to the flash memory.

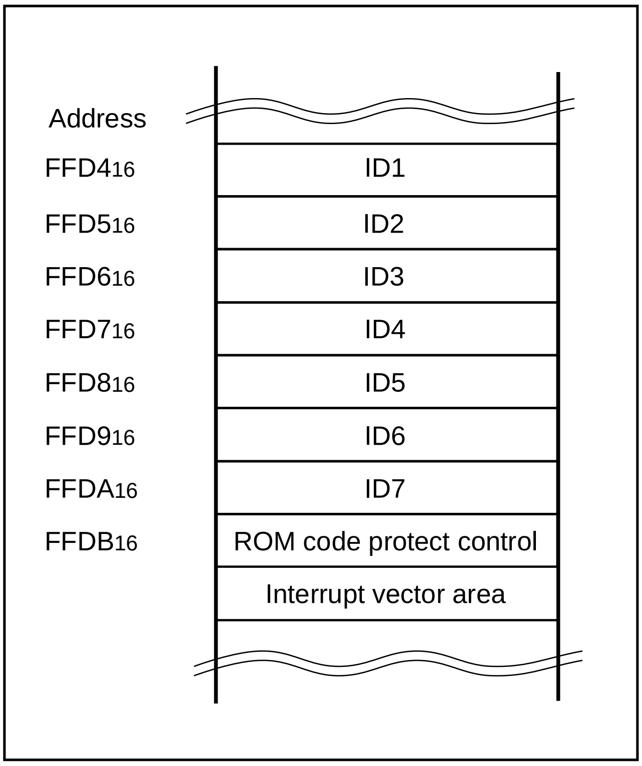


Fig. 64 ID code store addresses

(2) Parallel I/O Mode

Parallel I/O mode is the mode which parallel output and input software command, address, and data required for the operations (read, program, erase, etc.) to a built-in flash memory. Use the exclusive external equipment flash programmer which supports the 3851 Group (flash memory version). Refer to each programmer maker's handling manual for the details of the usage.

User ROM and Boot ROM Areas

In parallel I/O mode, the user ROM and boot ROM areas shown in Figure 57 can be rewritten. Both areas of flash memory can be operated on in the same way.
Program and block erase operations can be performed in the user ROM area. The user ROM area and its block is shown in Figure 57.
The boot ROM area is 4 Kbytes in size. It is located at addresses $F000_{16}$ through $FFFF_{16}$. Make sure program and block erase operations are always performed within this address range. (Access to any location outside this address range is prohibited.)
In the Boot ROM area, an erase block operation is applied to only one 4 Kbyte block. The boot ROM area has had a standard serial I/O mode control program stored in it when shipped from the Renesas factory. Therefore, using the device in standard serial I/O mode, you do not need to write to the boot ROM area.

(3) Standard serial I/O Mode

The standard serial I/O mode inputs and outputs the software commands, addresses and data needed to operate (read, program, erase, etc.) the internal flash memory. This I/O is clock synchronized serial. This mode requires the exclusive external equipment (serial programmer).

The standard serial I/O mode is different from the parallel I/O mode in that the CPU controls flash memory rewrite (uses the CPU rewrite mode), rewrite data input and so forth. The standard serial I/O mode is started by connecting "H" to the $P2_6$ (S_{CLK1}) pin and "H" to the $P4_1$ (INT_0) pin and "H" to the CNV_{SS} pin (apply 4.5 V to 5.5 V to Vpp from an external source), and releasing the reset operation. (In the ordinary microcomputer mode, set CNVss pin to "L" level.)

This control program is written in the Boot ROM area when the product is shipped from Renesas Technology Corporation. Accordingly, make note of the fact that the standard serial I/O mode cannot be used if the Boot ROM area is rewritten in parallel I/O mode. Figure 65 shows the pin connection for the standard serial I/O mode.

In standard serial I/O mode, serial data I/O uses the four serial I/O pins S_{CLK1}, RxD, TxD and $\overline{S_{RDY1}}$ (BUSY). The S_{CLK1} pin is the transfer clock input pin through which an external transfer clock is input. The TxD pin is for CMOS output. The $\overline{S_{RDY1}}$ (BUSY) pin outputs "L" level when ready for reception and "H" level when reception starts.

Serial data I/O is transferred serially in 8-bit units.

In standard serial I/O mode, only the User ROM area shown in Figure 57 can be rewritten. The Boot ROM area cannot.

In standard serial I/O mode, a 7-byte ID code is used. When there is data in the flash memory, commands sent from the peripheral unit (programmer) are not accepted unless the ID code matches.

Outline Performance (Standard Serial I/O Mode)

In standard serial I/O mode, software commands, addresses and data are input and output between the MCU and peripheral units (serial programmer, etc.) using 4-wire clock-synchronized serial I/O (serial I/O1).

In reception, software commands, addresses and program data are synchronized with the rise of the transfer clock that is input to the S_{CLK1} pin, and are then input to the MCU via the RxD pin. In transmission, the read data and status are synchronized with the fall of the transfer clock, and output from the TxD pin.

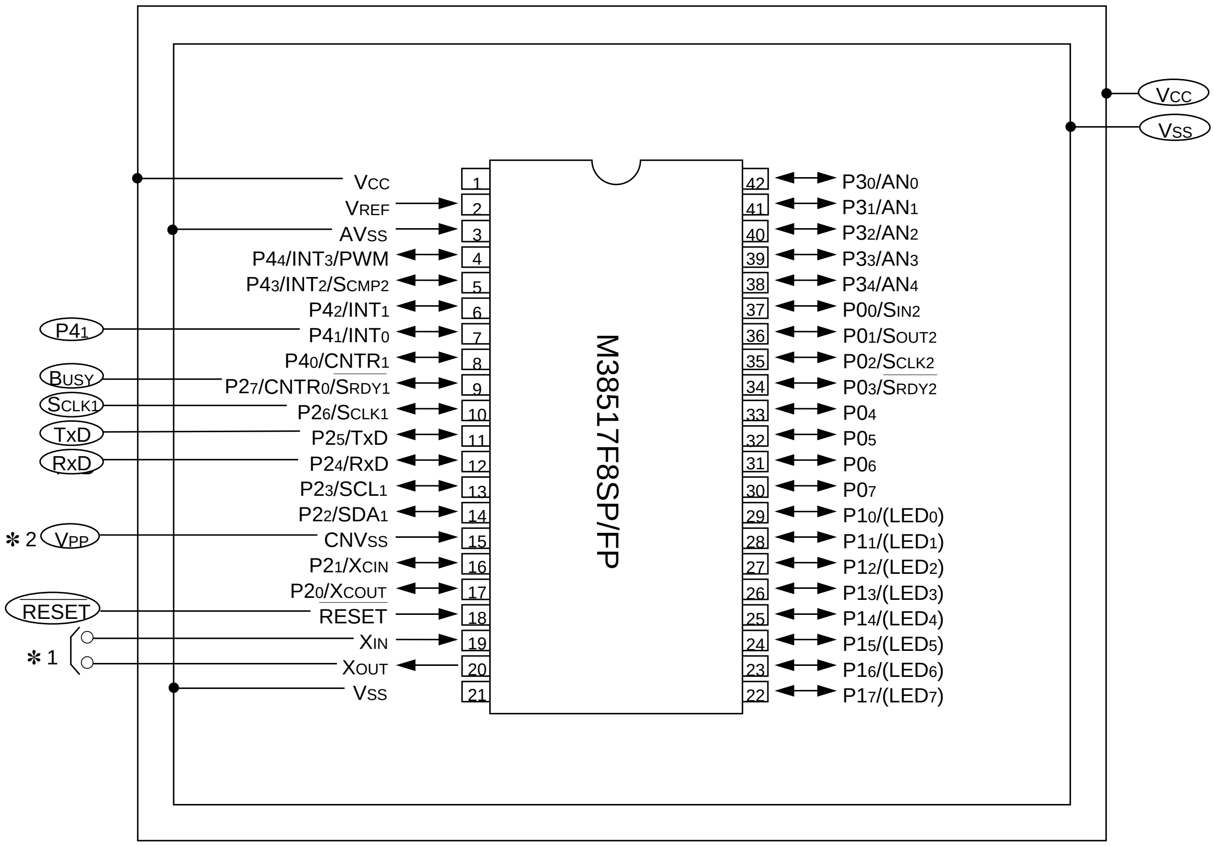
The TxD pin is for CMOS output. Transfer is in 8-bit units with LSB first.

When busy, such as during transmission, reception, erasing or program execution, the $\overline{S_{RDY1}}$ (BUSY) pin is "H" level. Accordingly, always start the next transfer after the $\overline{S_{RDY1}}$ (BUSY) pin is "L" level.

Also, data and status registers in a memory can be read after inputting software commands. Status, such as the operating state of the flash memory or whether a program or erase operation ended successfully or not, can be checked by reading the status register. Here following explains software commands, status registers, etc.

Table 18 Description of pin function (Standard Serial I/O Mode)

Pin	Name	I/O	Description
V_{CC},V_{SS}	Power input		Apply program/erase protection voltage to Vcc pin and 0 V to Vss pin.
CNV_{SS}	CNVss	I	Connect to V_{CC} when V_{CC} = 4.5 V to 5.5 V. Connect to Vpp (=4.5 V to 5.5 V) when V_{CC} = 2.7 V to 4.5 V.
$\overline{RESET}$	Reset input	I	Reset input pin. While reset is "L" level, a 20 cycle or longer clock must be input to X_{IN} pin.
X_{IN}	Clock input	I	Connect a ceramic resonator or crystal oscillator between X_{IN} and X_{OUT} pins. To input an externally generated clock, input it to X_{IN} pin and open X_{OUT} pin.
X_{OUT}	Clock output	O	
AV_{SS}	Analog power supply input		Connect AV_{SS} to V_{SS} .
V_{REF}	Reference voltage input	I	Enter the reference voltage for AD from this pin, or open.
$P0_0$ to $P0_7$	Input port P0	I	Input "H" or "L", or open.
$P1_0$ to $P1_7$	Input port P1	I	Input "H" or "L", or open.
$P2_0$ to $P2_3$	Input port P2	I	Input "H" or "L", or open.
$P2_4$	RxD input	I	This pin is for serial data input.
$P2_5$	TxD output	O	This pin is for serial data output.
$P2_6$	S_{CLK1} input	I	This pin is for serial clock input.
$P2_7$	BUSY output	O	This pin is for BUSY signal output.
$P3_0$ to $P3_4$	Input port P3	I	Input "H" or "L", or open.
$P4_0$, $P4_2$ to $P4_4$	Input port P4	I	Input "H" or "L", or open.
$P4_1$	Input port P4	I	Input "H" when RESET is released only.



Mode setup method

Signal	Value
CNVSS	4.5 to 5.5 V
P41	VCC ✻3
SCLK1	VCC ✻3
RESET	VSS → VCC

Notes 1: Connect oscillator circuit
2: Connect to Vcc when Vcc = 4.5 V to 5.5 V.
Connect to VPP (=4.5 V to 5.5 V) when Vcc = 2.7 V to 4.5 V.
3: It is necessary to apply Vcc only when reset is released.

Fig. 65 Pin connection diagram in standard serial I/O mode

Software Commands (Standard Serial I/O Mode)

Table 19 lists software commands. In standard serial I/O mode, erase, program and read are controlled by transferring software commands via the RxD pin. Software commands are explained here below.

Table 19 Software commands (Standard serial I/O mode)

	Control command	1st byte transfer	2nd byte	3rd byte	4th byte	5th byte	6th byte	.....	When ID is not verified
1	Page read	FF_{16}	Address (middle)	Address (high)	Data output	Data output	Data output	Data output to 259th byte	Not acceptable
2	Page program	41_{16}	Address (middle)	Address (high)	Data input	Data input	Data input	Data input to 259th byte	Not acceptable
3	Erase all blocks	$A7_{16}$	$D0_{16}$						Not acceptable
4	Read status register	70_{16}	SRD output	SRD1 output					Acceptable
5	Clear status register	50_{16}							Not acceptable
6	ID code check	$F5_{16}$	Address (low)	Address (middle)	Address (high)	ID size	ID1	To ID7	Acceptable
7	Download function	FA_{16}	Size (low)	Size (high)	Check-sum	Data input	To required number of times		Not acceptable
8	Version data output function	FB_{16}	Version data output	Version data output	Version data output	Version data output	Version data output	Version data output to 9th byte	Acceptable

Notes1: Shading indicates transfer from the internal flash memory microcomputer to a programmer. All other data is transferred from an external equipment (programmer) to the internal flash memory microcomputer.
2: SRD refers to status register data. SRD1 refers to status register 1 data.
3: All commands can be accepted when the flash memory is totally blank.
4: Address high must be “00_{16}”.

●Page Read Command

This command reads the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page read command as explained here following.

(1) Transfer the "FF_{16}" command code with the 1st byte.

(2) Transfer addresses A_8 to A_{15} and A_{16} to A_{23} with the 2nd and 3rd bytes respectively.

(3) From the 4th byte onward, data (D_0 to D_7) for the page (256 bytes) specified with addresses A_8 to A_{23} will be output sequentially from the smallest address first synchronized with the fall of the clock.

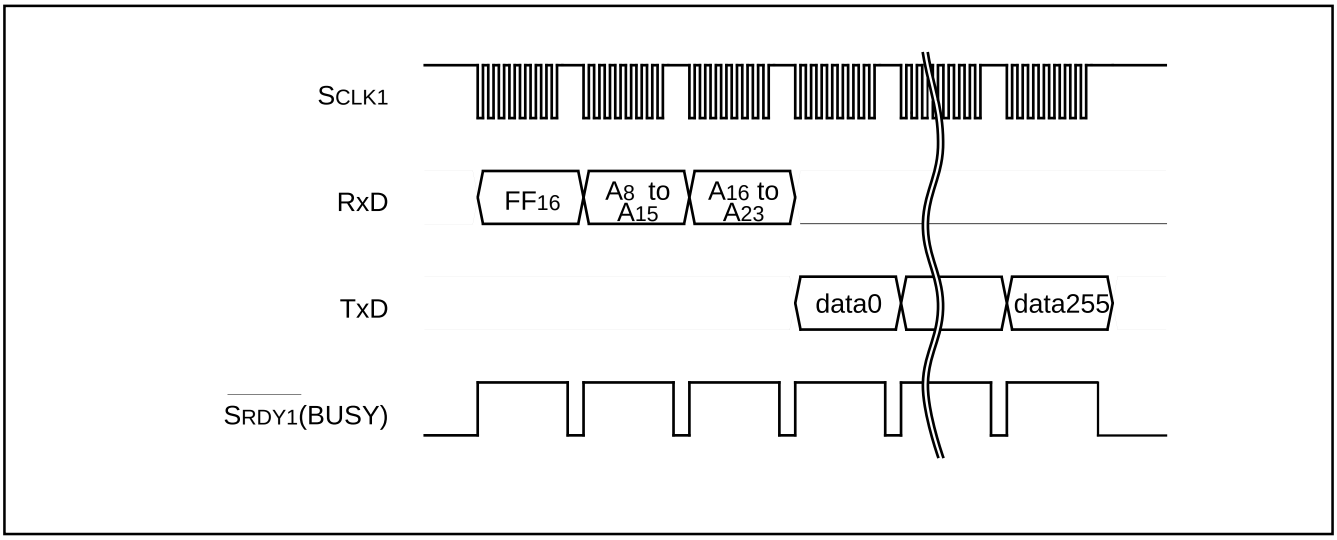


Fig. 66 Timing for page read

●Read Status Register Command

This command reads status information. When the "70_{16}" command code is transferred with the 1st byte, the contents of the status register (SRD) with the 2nd byte and the contents of status register 1 (SRD1) with the 3rd byte are read.

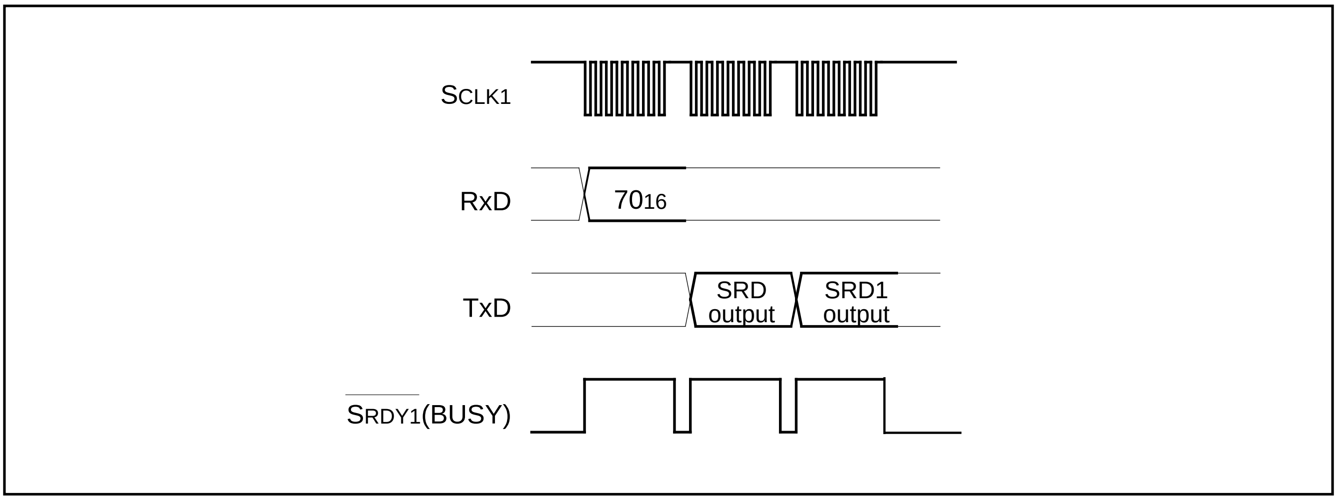


Fig. 67 Timing for reading status register

●Clear Status Register Command

This command clears the bits (SR4, SR5) which are set when the status register operation ends in error. When the “50_{16}” command code is sent with the 1st byte, the aforementioned bits are cleared. When the clear status register operation ends, the $\overline{\text{SRDY1}}$ (BUSY) signal changes from “H” to “L” level.

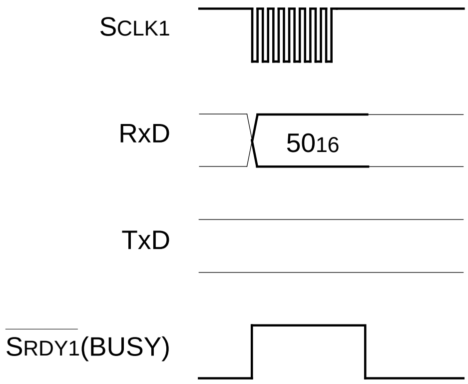


Fig. 68 Timing for clear status register

●Page Program Command

This command writes the specified page (256 bytes) in the flash memory sequentially one byte at a time. Execute the page program command as explained here following.

(1) Transfer the “41_{16}” command code with the 1st byte.

(2) Transfer addresses A_8 to A_{15} and A_{16} to A_{23} (“00_{16}”) with the 2nd and 3rd bytes respectively.

(3) From the 4th byte onward, as write data (D_0 to D_7) for the page (256 bytes) specified with addresses A_8 to A_{23} is input sequentially from the smallest address first, that page is automatically written.

When reception setup for the next 256 bytes ends, the $\overline{\text{SRDY1}}$ (BUSY) signal changes from “H” to “L” level. The result of the page program can be known by reading the status register. For more information, see the section on the status register.

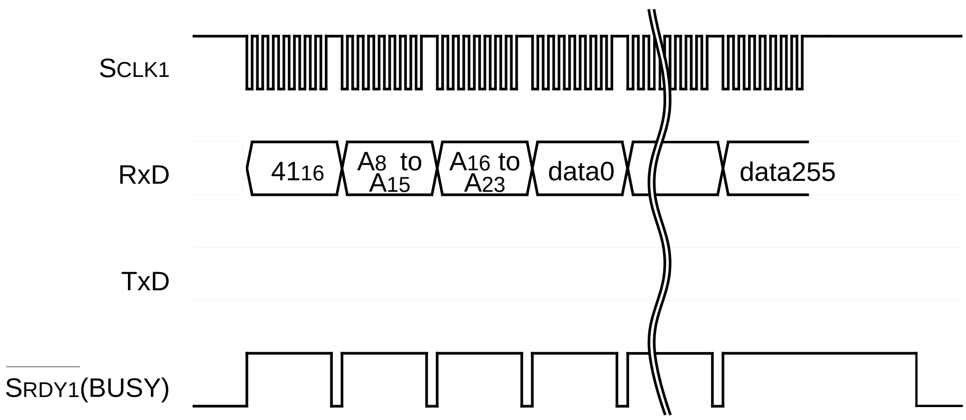


Fig. 69 Timing for page program

●**Erase All Blocks Command**

This command erases the contents of all blocks. Execute the erase all blocks command as explained here following.

(1) Transfer the "A7$_{16}$" command code with the 1st byte.

(2) Transfer the verify command code "D0$_{16}$" with the 2nd byte. With the verify command code, the erase operation will start and continue for all blocks in the flash memory.

When erase all blocks end, the $\overline{\text{SRDY1}}$ (BUSY) signal changes from "H" to "L" level. The result of the erase operation can be known by reading the status register.

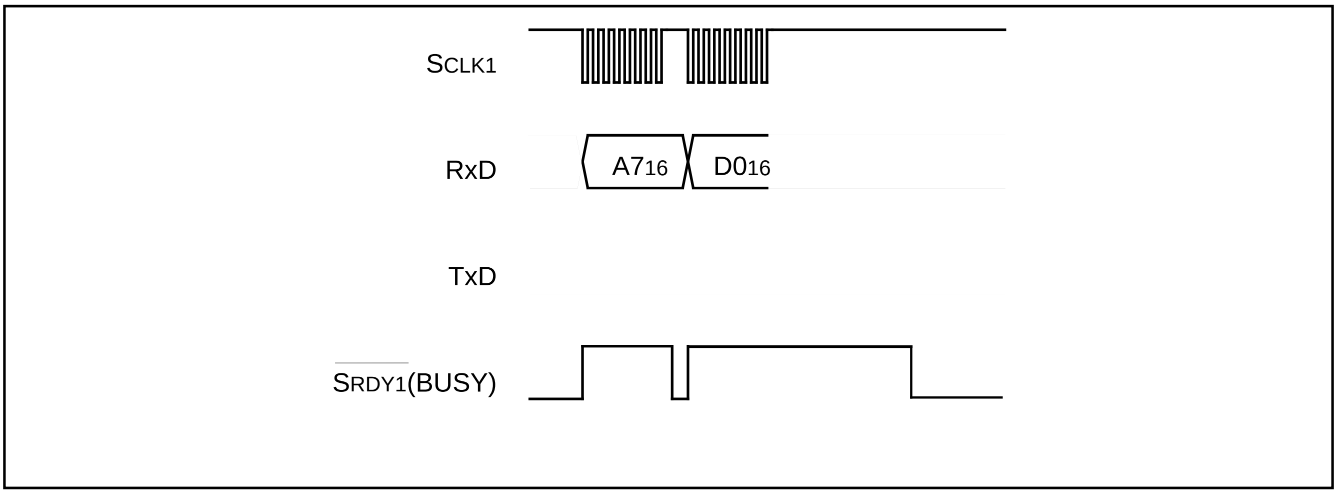


Fig. 70 Timing for erase all blocks

●Download Command

This command downloads a program to the RAM for execution.
Execute the download command as explained here following.

(1) Transfer the "FA16" command code with the 1st byte.
(2) Transfer the program size with the 2nd and 3rd bytes.
(3) Transfer the check sum with the 4th byte. The check sum is added to all data sent with the 5th byte onward.
(4) The program to execute is sent with the 5th byte onward.

When all data has been transmitted, if the check sum matches, the downloaded program is executed. The size of the program will vary according to the internal RAM.

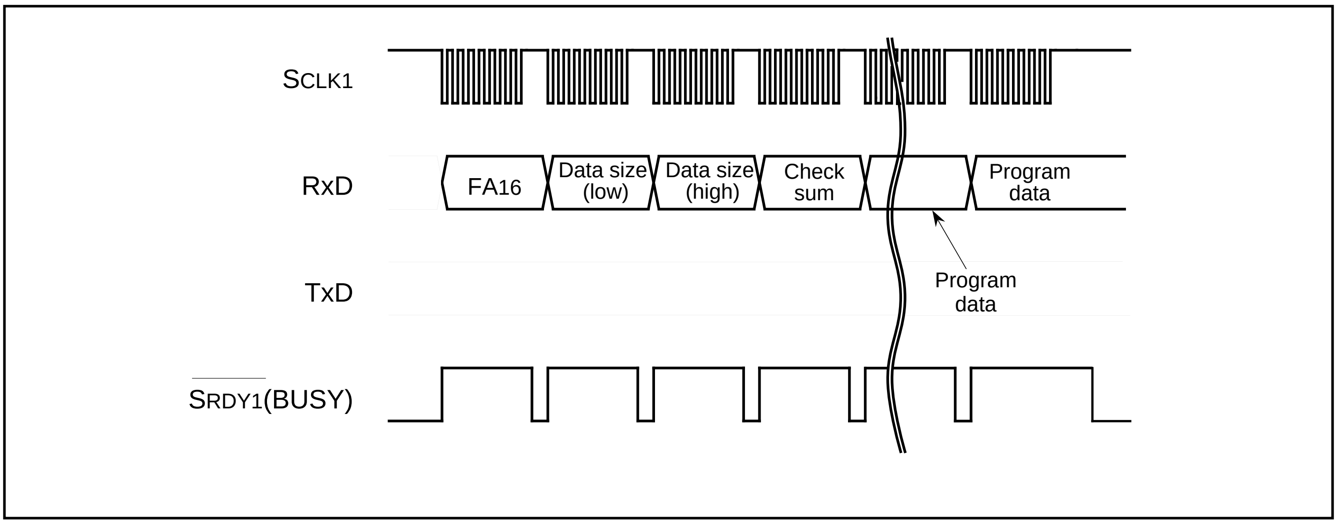


Fig. 71 Timing for download

●Version Information Output Command

This command outputs the version information of the control program stored in the Boot ROM area. Execute the version information output command as explained here following.

(1) Transfer the “FB_{16}” command code with the 1st byte.

(2) The version information will be output from the 2nd byte onward. This data is composed of 8 ASCII code characters.

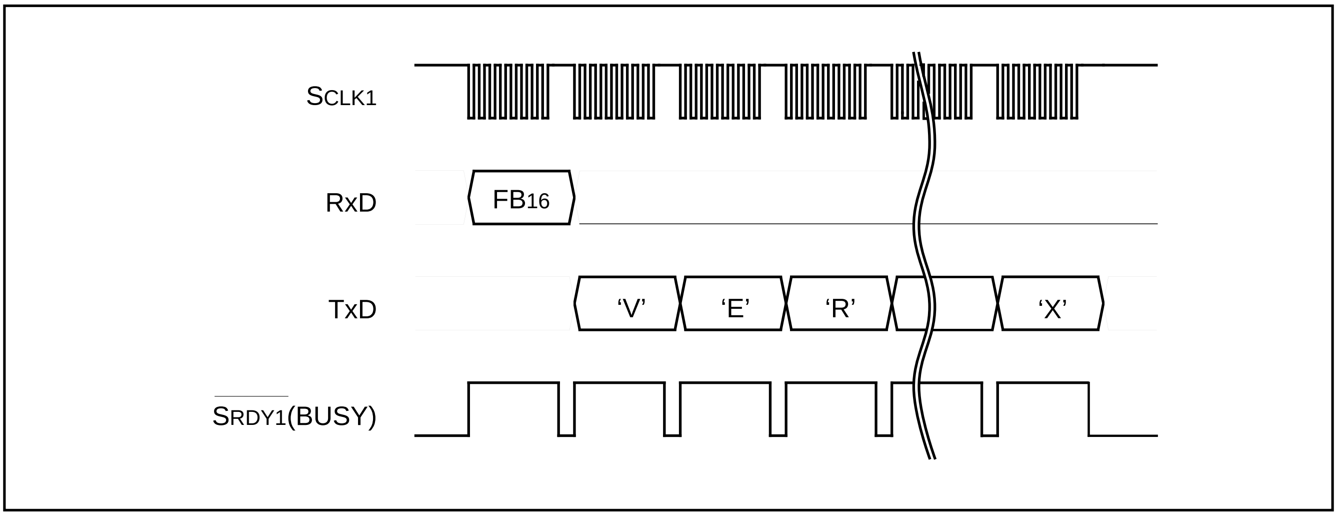


Fig. 72 Timing for version information output

●ID Check

This command checks the ID code. Execute the boot ID check command as explained here following.

(1) Transfer the “$F5_{16}$” command code with the 1st byte.
(2) Transfer addresses A_0 to A_7, A_8 to A_{15} and A_{16} to A_{23} (“00_{16}”) of the 1st byte of the ID code with the 2nd, 3rd, and 4th bytes respectively.
(3) Transfer the number of data sets of the ID code with the 5th byte.
(4) Transfer the ID code with the 6th byte onward, starting with the 1st byte of the code.

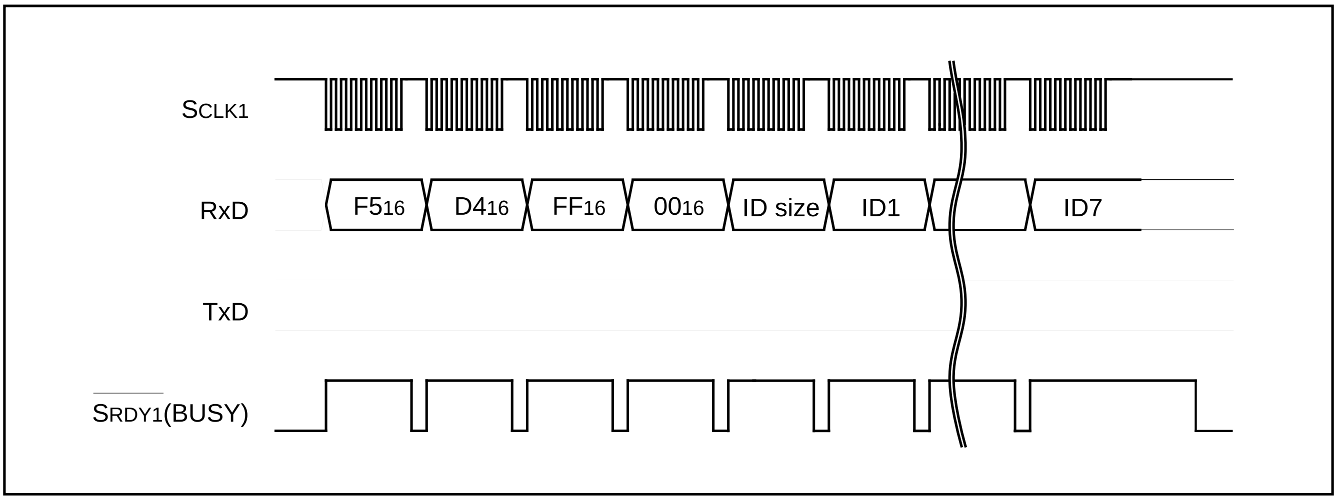


Fig. 73 Timing for ID check

●ID Code

When the flash memory is not blank, the ID code sent from the serial programmer and the ID code written in the flash memory are compared to see if they match. If the codes do not match, the command sent from the serial programmer is not accepted. An ID code contains 8 bits of data. Area is, from the 1st byte, addresses $FFD4_{16}$ to $FFDA_{16}$. Write a program into the flash memory, which already has the ID code set for these addresses.

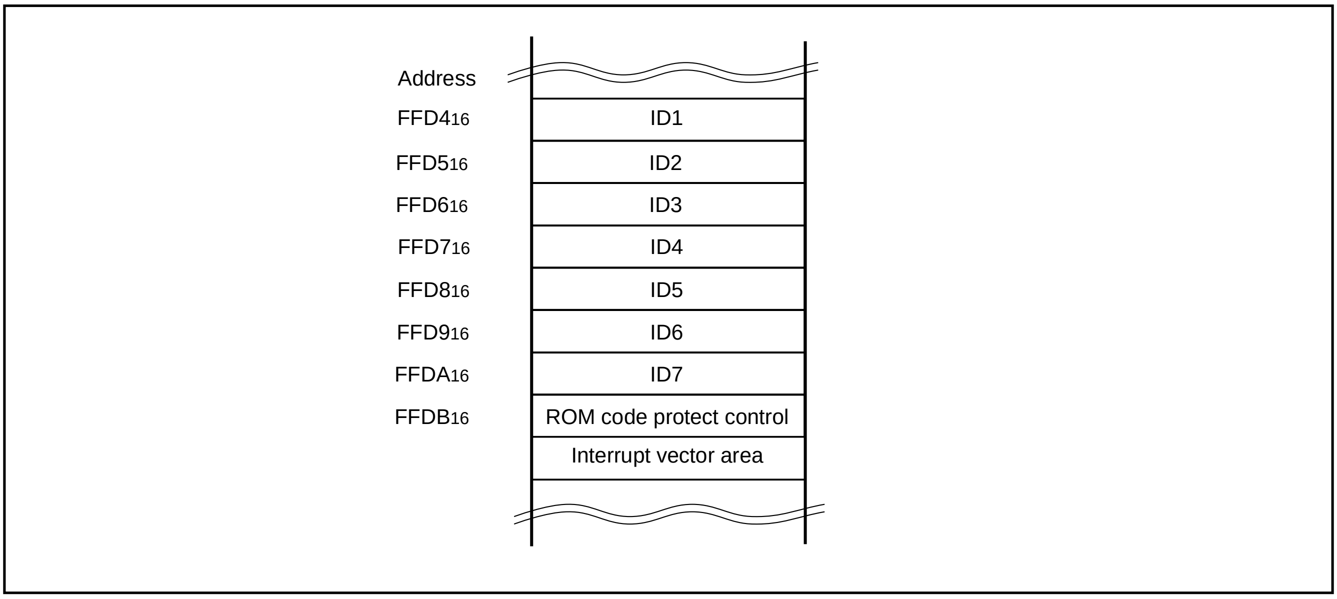


Fig. 74 ID code storage addresses

●Status Register (SRD)

The status register indicates operating status of the flash memory and status such as whether an erase operation or a program ended successfully or in error. It can be read by writing the read status register command (70_{16}). Also, the status register is cleared by writing the clear status register command (50_{16}).

Table 20 lists the definition of each status register bit. After releasing the reset, the status register becomes "80_{16}".

•Sequencer status (SR7)

The sequencer status indicates the operating status of the flash memory.

After power-on and recover from deep power down mode, the sequencer status is set to "1" (ready).

This status bit is set to "0" (busy) during write or erase operation and is set to "1" upon completion of these operations.

•Erase status (SR5)

The erase status indicates the operating status of erase operation. If an erase error occurs, it is set to "1". When the erase status is cleared, it is set to "0".

•Program status (SR4)

The program status indicates the operating status of write operation. If a program error occurs, it is set to "1". When the program status is cleared, it is set to "0".

Table 20 Definition of each bit of status register (SRD)

SRD0 bits	Status name	Definition	
		"1"	"0"
SR7 (bit7)	Sequencer status	Ready	Busy
SR6 (bit6)	Reserved	-	-
SR5 (bit5)	Erase status	Terminated in error	Terminated normally
SR4 (bit4)	Program status	Terminated in error	Terminated normally
SR3 (bit3)	Reserved	-	-
SR2 (bit2)	Reserved	-	-
SR1 (bit1)	Reserved	-	-
SR0 (bit0)	Reserved	-	-

●Status Register 1 (SRD1)

The status register 1 indicates the status of serial communications, results from ID checks and results from check sum comparisons. It can be read after the status register (SRD) by writing the read status register command (70_{16}). Also, status register 1 is cleared by writing the clear status register command (50_{16}).
Table 21 lists the definition of each status register 1 bit. This register becomes "00_{16}" when power is turned on and the flag status is maintained even after the reset.

•Boot update completed bit (SR15)
This flag indicates whether the control program was downloaded to the RAM or not, using the download function.

•Check sum consistency bit (SR12)
This flag indicates whether the check sum matches or not when a program, is downloaded for execution using the download function.

•ID check completed bits (SR11 and SR10)
These flags indicate the result of ID checks. Some commands cannot be accepted without an ID code check.

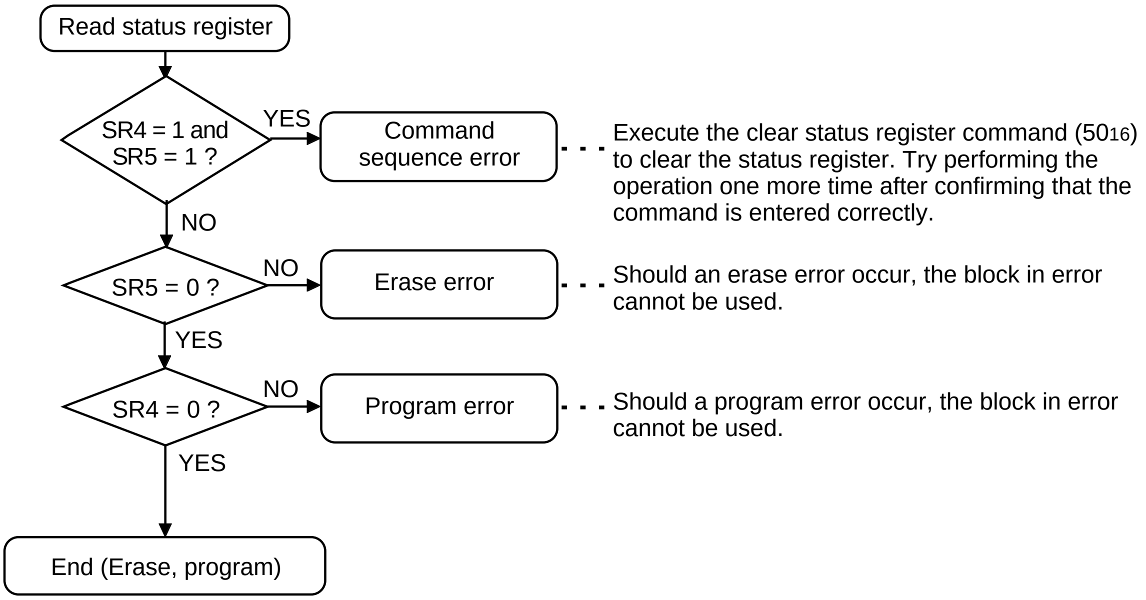
•Data reception time out (SR9)
This flag indicates when a time out error is generated during data reception. If this flag is attached during data reception, the received data is discarded and the MCU returns to the command wait state.

Table 21 Definition of each bit of status register 1 (SRD1)

SRD1 bits	Status name	Definition	
		"1"	"0"
SR15 (bit7)	Boot update completed bit	Update completed	Not Update
SR14 (bit6)	Reserved	-	-
SR13 (bit5)	Reserved	-	-
SR12 (bit4)	Checksum match bit	Match	Mismatch
SR11 (bit3) SR10 (bit2)	ID check completed bits	00 Not verified 01 Verification mismatch 10 Reserved 11 Verified	
SR9 (bit1)	Data reception time out	Time out	Normal operation
SR8 (bit0)	Reserved	-	-

Full Status Check

Results from executed erase and program operations can be known by running a full status check. Figure 75 shows a flowchart of the full status check and explains how to remedy errors which occur.

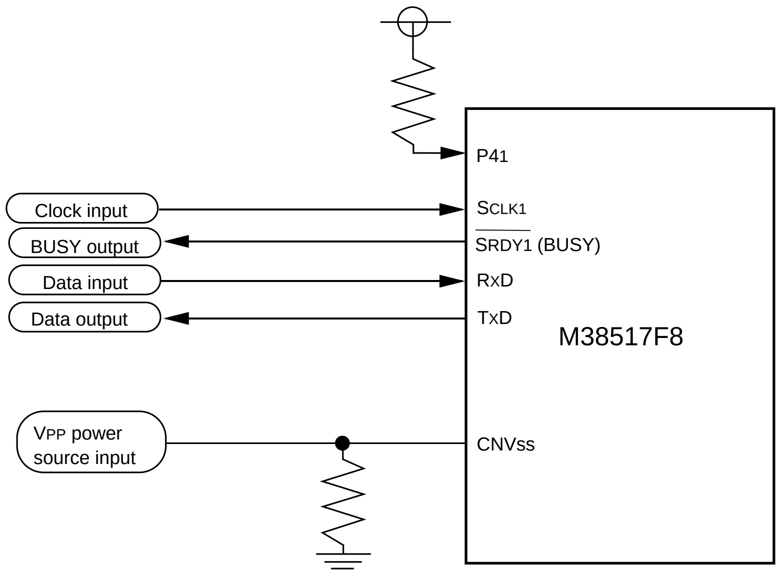


Note: When one of SR5 to SR4 is set to "1" , none of the program, erase all blocks commands is accepted. Execute the clear status register command (50_{16}) before executing these commands.

Fig. 75 Full status check flowchart and remedial procedure for errors

Example Circuit Application for Standard Serial I/O Mode

Figure 76 shows a circuit application for the standard serial I/O mode. Control pins will vary according to a programmer, therefore see a programmer manual for more information.



Notes 1: Control pins and external circuitry will vary according to peripheral unit. For more information, see the peripheral unit manual.
2: In this example, the Vpp power supply is supplied from an external source (writer). To use the user's power source, connect to 4.5 V to 5.5 V.
3: It is necessary to apply Vcc to SCLK1 pin only when reset is released.

Fig. 76 Example circuit application for standard serial I/O mode

Flash memory Electrical characteristics

Table 22 Absolute maximum ratings

Symbol	Parameter		Conditions	Ratings	Unit
V_{CC}	Power source voltage		All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage	P0₀–P0₇, P1₀–P1₇, P2₀, P2₁, P2₄–P2₇, P3₀–P3₄, P4₀–P4₄, V_{REF}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage	P2₂, P2₃		–0.3 to 5.8	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}		–0.3 to V_{CC} +0.3	V
V_I	Input voltage	CNV_{SS}		–0.3 to 6.5	V
V_O	Output voltage	P0₀–P0₇, P1₀–P1₇, P2₀, P2₁, P2₄–P2₇, P3₀–P3₄, P4₀–P4₄, X_{OUT}		–0.3 to V_{CC} +0.3	V
V_O	Output voltage	P2₂, P2₃		–0.3 to 5.8	V
P_d	Power dissipation		T_a = 25 °C	1000 (Note)	mW
T_{opr}	Operating temperature			25±5	°C
T_{stg}	Storage temperature			–40 to 125	°C

Note: The rating becomes 300 mW at the 42P2R-A/E package.

Table 23 Flash memory mode Electrical characteristics
(Ta = 25°C, Vcc = 4.5 to 5.5V unless otherwise noted)

Symbol	Parameter	Conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{PP1}	V_{PP} power source current (read)	V_{PP} = V_{CC}			100	µA
I_{PP2}	V_{PP} power source current (program)	V_{PP} = V_{CC}			60	mA
I_{PP3}	V_{PP} power source current (erase)	V_{PP} = V_{CC}			30	mA
V_{PP}	V_{PP} power source voltage		4.5		5.5	V
V_{CC}	V_{CC} power source voltage	Microcomputer mode operation at V_{CC} = 2.7 to 5.5V	4.5		5.5	V
		Microcomputer mode operation at V_{CC} = 2.7 to 3.6V	3.0		3.6	V

NOTES ON PROGRAMMING

Processor Status Register

The contents of the processor status register (PS) after a reset are undefined, except for the interrupt disable flag (I) which is “1”. After a reset, initialize flags which affect program execution. In particular, it is essential to initialize the index X mode (T) and the decimal mode (D) flags because of their effect on calculations.

Interrupts

The contents of the interrupt request bits do not change immediately after they have been written. After writing to an interrupt request register, execute at least one instruction before performing a BBC or BBS instruction.

Decimal Calculations

- To calculate in decimal notation, set the decimal mode flag (D) to “1”, then execute an ADC or SBC instruction. After executing an ADC or SBC instruction, execute at least one instruction before executing a SEC, CLC, or CLD instruction.
- In decimal mode, the values of the negative (N), overflow (V), and zero (Z) flags are invalid.

Timers

If a value n (between 0 and 255) is written to a timer latch, the frequency division ratio is 1/(n+1).

Multiplication and Division Instructions

- The index X mode (T) and the decimal mode (D) flags do not affect the MUL and DIV instruction.
- The execution of these instructions does not change the contents of the processor status register.

Ports

The contents of the port direction registers cannot be read. The following cannot be used:

- The data transfer instruction (LDA, etc.)
- The operation instruction when the index X mode flag (T) is “1”
- The addressing mode which uses the value of a direction register as an index
- The bit-test instruction (BBC or BBS, etc.) to a direction register
- The read-modify-write instructions (ROR, CLB, or SEB, etc.) to a direction register.

Use instructions such as LDM and STA, etc., to set the port direction registers.

Serial I/O

In serial I/O1 (clock synchronous mode), if the receive side is using an external clock and it is to output the $\overline{\text{SRDY1}}$ signal, set the transmit enable bit, the receive enable bit, and the $\overline{\text{SRDY1}}$ output enable bit to “1”.

Serial I/O1 continues to output the final bit from the TxD pin after transmission is completed.

SOUT2 pin for serial I/O2 goes to high impedance after transmission is completed.

When an external clock is used as synchronous clock in serial I/O1 or serial I/O2, write transmission data to the transmit buffer register or serial I/O2 register while the transfer clock is “H”.

A-D Converter

The comparator uses capacitive coupling amplifier whose charge will be lost if the clock frequency is too low.

Therefore, make sure that f(XIN) in the middle/high-speed mode is at least on 500 kHz during an A-D conversion.

Do not execute the STP instruction during an A-D conversion.

Instruction Execution Time

The instruction execution time is obtained by multiplying the frequency of the internal clock ϕ by the number of cycles needed to execute an instruction.

The number of cycles required to execute an instruction is shown in the list of machine instructions.

The frequency of the internal clock ϕ is half of the XIN frequency in high-speed mode.

NOTES ON USAGE

Differences between 3851 group (built-in 16 KB ROM) and 3851 group (built-in 24 KB or more ROM)

(1) The absolute maximum ratings of 3851 group (built-in 24 KB or more ROM) is smaller than that of 3851 group (built-in 16 KB ROM).

•Power source voltage Vcc = –0.3 to 6.5 V

•CNVss input voltage

VI = –0.3 to Vcc +0.3 V (M38514M6, M38517M8)

VI = –0.3 to 6.5 V (M38517F8)

(2) The oscillation circuit constants of XIN-XOUT, XCIN-XCOUT may be some differences between 3851 group (built-in 16 KB ROM) and 3851 group (built-in 24 KB or more ROM).

(3) Do not write any data to the reserved area and the reserved bit. (Do not change the contents after rest.)

(4) Fix bit 3 of the CPU mode register to “1”.

(5) Be sure to perform the termination of unused pins.

Handling of Source Pins

In order to avoid a latch-up occurrence, connect a capacitor suitable for high frequencies as bypass capacitor between power source pin (VCC pin) and GND pin (VSS pin) and between power source pin (VCC pin) and analog power source input pin (AVSS pin). Besides, connect the capacitor to as close as possible. For bypass capacitor which should not be located too far from the pins to be connected, a ceramic capacitor of 0.01 µF–0.1µF is recommended.

EPROM Version/One Time PROM Version/ Flash Memory Version

The CNVss pin is connected to the internal memory circuit block by a low-ohmic resistance, since it has the multiplexed function to be a programmable power source pin (VPP pin) as well.

To improve the noise reduction, connect a track between CNVss pin and Vss pin or Vcc pin with 1 to 10 kΩ resistance.

The mask ROM version track of CNVss pin has no operational interference even if it is connected to Vss pin or Vcc pin via a resistor.

Electric Characteristic Differences Among Mask ROM, Flash Memory, and One Time PROM Version MCUs

There are differences in electric characteristics, operation margin, noise immunity, and noise radiation among mask ROM, flash memory, and One Time PROM version MCUs due to the differences in the manufacturing processes.
When manufacturing an application system with the flash memory, One Time PROM version and then switching to use of the mask ROM version, perform sufficient evaluations for the commercial samples of the mask ROM version.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:
1. Mask ROM Order Confirmation Form*
2. Mark Specification Form*
3. Data to be written to ROM, in EPROM form (three identical copies) or one floppy disk.

DATA REQUIRED FOR One Time PROM PROGRAMMING ORDERS

The following are necessary when ordering a PROM programming service:
1. ROM Programming Confirmation Form*
2. Mark Specification Form* (only special mark with customer's trade mark logo)
3. Data to be programmed to PROM, in EPROM form (three identical copies) or one floppy disk.

✻For the mask ROM confirmation and the mark specifications, refer to the "Renesas Technology " Homepage ROM ordering (http://www.renesas.com/eng/rom).

ROM PROGRAMMING METHOD

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter. Set the address of PROM programmer in the user ROM area.

Table 20 Programming adapter

Package	Name of Programming Adapter
42P4B, 42S1B	PCA4738S-42A
42P2R-A/E	PCA4738F-42A

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 77 is recommended to verify programming.

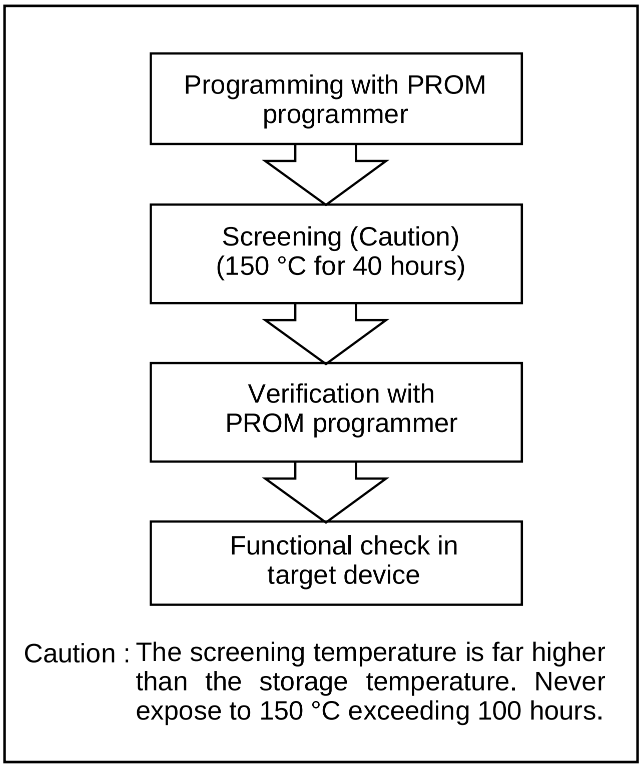


Fig. 77 Programming and testing of One Time PROM version

Electrical characteristics

Absolute maximum ratings

Table 25 Absolute maximum ratings

Symbol	Parameter			Conditions	Ratings	Unit
V_{CC}	Power source voltage			All voltages are based on V_{SS}. Output transistors are cut off.	–0.3 to 6.5	V
V_I	Input voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$, V_{REF}			–0.3 to V_{CC} +0.3	V
V_I	Input voltage	$P2_2$, $P2_3$			–0.3 to 5.8	V
V_I	Input voltage	$\overline{RESET}$, X_{IN}			–0.3 to V_{CC} +0.3	V
V_I	Input voltage	CNV_{SS}	M38514M6, M38514M8		–0.3 to V_{CC} +0.3	V
			M38514E6		–0.3 to 13	V
			M38517F8		–0.3 to 6.5	V
V_O	Output voltage	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$, X_{OUT}			–0.3 to V_{CC} +0.3	V
V_O	Output voltage	$P2_2$, $P2_3$			–0.3 to 5.8	V
P_d	Power dissipation			T_a = 25 °C	1000 **(Note)**	mW
T_{opr}	Operating temperature				–20 to 85	°C
T_{stg}	Storage temperature				–40 to 125	°C

Note : The rating becomes 300mW at the 42P2R-A/E package.

Recommended operating conditions

Table 26 Recommended operating conditions (1)
(V_{CC} = 2.7 to 5.5 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits Min.	Limits Typ.	Limits Max.	Unit
V_{CC}	Power source voltage	8 MHz (high-speed mode)	4.0	5.0	5.5	V
		8 MHz (middle-speed mode), 4 MHz(high-speed mode)	2.7	5.0	5.5	V
V_{SS}	Power source voltage			0		V
V_{REF}	A-D convert reference voltage		2.0		V_{CC}	V
AV_{SS}	Analog power source voltage		0	0		V
V_{IA}	Analog input voltage	AN_0–AN_4	AV_{SS}		V_{CC}	V
V_{IH}	“H” input voltage	P00–P07, P10–P17, P20–P27, P30–P34, P40–P44	0.8V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (when I^2C-BUS input level is selected)	SDA_1, SCL_1	0.7V_{CC}		5.8	V
		SDA_2, SCL_2	0.7V_{CC}		V_{CC}	V
V_{IH}	“H” input voltage (when SMBUS input level is selected)	SDA_1, SCL_1	1.4		5.8	V
		SDA_2, SCL_2	1.4		V_{CC}	V
V_{IH}	“H” input voltage	$\overline{RESET}$, X_{IN}, CNV_{SS}	0.8V_{CC}		V_{CC}	V
V_{IL}	“L” input voltage	P00–P07, P10–P17, P20–P27, P30–P34, P40–P44	0		0.2V_{CC}	V
V_{IL}	“L” input voltage (when I^2C-BUS input level is selected)	SDA_1, SDA_2, SCL_1, SCL_2	0		0.3V_{CC}	V
V_{IL}	“L” input voltage (when SMBUS input level is selected)	SDA_1, SDA_2, SCL_1, SCL_2	0		0.6	V
V_{IL}	“L” input voltage	$\overline{RESET}$, CNV_{SS}	0		0.2V_{CC}	V
V_{IL}	“L” input voltage	X_{IN}	0		0.16V_{CC}	V
$\Sigma I_{OH(peak)}$	“H” total peak output current **(Note)**	P00–P07, P10–P17, P30–P34			–80	mA
$\Sigma I_{OH(peak)}$	“H” total peak output current **(Note)**	P20, P21, P24–P27, P40–P44			–80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current **(Note)**	P00–P07, P30–P34			80	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current **(Note)**	P10–P17			120	mA
$\Sigma I_{OL(peak)}$	“L” total peak output current **(Note)**	P20–P27,P40–P44			80	mA
$\Sigma I_{OH(avg)}$	“H” total average output current **(Note)**	P00–P07, P10–P17, P30–P34			–40	mA
$\Sigma I_{OH(avg)}$	“H” total average output current **(Note)**	P20, P21, P24–P27, P40–P44			–40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current **(Note)**	P00–P07, P30–P34			40	mA
$\Sigma I_{OL(avg)}$	“L” total average output current **(Note)**	P10–P17			60	mA
$\Sigma I_{OL(avg)}$	“L” total average output current **(Note)**	P20–P27,P40–P44			40	mA

Note : The total output current is the sum of all the currents flowing through all the applicable ports. The total average current is an average value measured over 100 ms. The total peak current is the peak value of all the currents.

Table 27 Recommended operating conditions (2)
(V_{CC} = 2.7 to 5.5 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min.	Typ.	Max.	
$I_{OH(peak)}$	“H” peak output current **(Note 1)**	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$			–10	mA
$I_{OL(peak)}$	“L” peak output current **(Note 1)**	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$,			10	mA
		$P1_0$–$P1_7$			20	mA
$I_{OH(avg)}$	“H” average output current **(Note 2)**	$P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$			–5	mA
$I_{OL(avg)}$	“L” average output current **(Note 2)**	$P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$,			5	mA
		$P1_0$–$P1_7$			15	mA
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC} = 4.0 to 5.5V) **(Note 3)**				8	MHz
$f(X_{IN})$	Internal clock oscillation frequency (V_{CC} = 2.7 to 5.5V) **(Note 3)**				4	MHz

Notes 1: The peak output current is the peak current flowing in each port.
2: The average output current I_{OL}(avg), I_{OH}(avg) are average value measured over 100 ms.
3: When the oscillation frequency has a duty cycle of 50%.

Electrical characteristics

Table 28 Electrical characteristics (1)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
V_{OH}	“H” output voltage $P0_0$–$P0_7$, $P1_0$–$P1_7$, $P2_0$, $P2_1$, $P2_4$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$ **(Note)**	I_{OH} = –10 mA, V_{CC} = 4.0–5.5 V	V_{CC}–2.0			V
		I_{OH} = –1.0 mA, V_{CC} = 2.7–5.5 V	V_{CC}–1.0			V
V_{OL}	“L” output voltage $P0_0$–$P0_7$, $P2_0$–$P2_7$, $P3_0$–$P3_4$, $P4_0$–$P4_4$	I_{OL} = 10 mA, V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 1.0 mA, V_{CC} = 2.7–5.5 V			1.0	V
V_{OL}	“L” output voltage $P1_0$–$P1_7$	I_{OL} = 20 mA, V_{CC} = 4.0–5.5 V			2.0	V
		I_{OL} = 10 mA, V_{CC} = 2.7–5.5 V			1.0	V

Note: $P2_5$ is measured when the $P2_5$/SCL_2/T_XD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.

RENESAS

Table 29 Electrical characteristics (2)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits Min.	Limits Typ.	Limits Max.	Unit
$V_{T+}–V_{T-}$	Hysteresis CNTR0, CNTR1, INT0–INT3			0.4		V
$V_{T+}–V_{T-}$	Hysteresis RxD, SCLK1, SIN2, SCLK2			0.5		V
$V_{T+}–V_{T-}$	Hysteresis $\overline{\text{RESET}}$			0.5		V
I_{IH}	"H" input current P00–P07, P10–P17, P20, P21, P24–P27, P30–P34, P40–P44	$V_I = V_{CC}$			5.0	µA
I_{IH}	"H" input current $\overline{\text{RESET}}$, CNVSS	$V_I = V_{CC}$			5.0	µA
I_{IH}	"H" input current XIN	$V_I = V_{CC}$		4		µA
I_{IL}	"L" input current P00–P07, P10–P17, P20–P27, P30–P34, P40–P44	$V_I = V_{SS}$			–5.0	µA
I_{IL}	"L" input current $\overline{\text{RESET}}$,CNVSS	$V_I = V_{SS}$			–5.0	µA
I_{IL}	"L" input current XIN	$V_I = V_{SS}$		–4		µA
V_{RAM}	RAM hold voltage	When clock stopped	2.0		5.5	V

Table 30 Electrical characteristics (3)
(VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits Min.	Limits Typ.	Limits Max.	Unit
ICC	Power source current	High-speed mode f(XIN) = 8 MHz f(XCIN) = 32.768 kHz Output transistors “off”			6.8	13	mA
		High-speed mode f(XIN) = 8 MHz (in WIT state) f(XCIN) = 32.768 kHz Output transistors “off”			1.6		mA
		Low-speed mode f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors “off”	Except M38517F8FP/SP		60	200	µA
			M38517F8FP/SP		250		µA
		Low-speed mode f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors “off”	Except M38517F8FP/SP		20	40	µA
			M38517F8FP/SP		70		µA
		Low-speed mode (VCC = 3 V) f(XIN) = stopped f(XCIN) = 32.768 kHz Output transistors “off”	Except M38517F8FP/SP		20	55	µA
			M38517F8FP/SP		150		µA
		Low-speed mode (VCC = 3 V) f(XIN) = stopped f(XCIN) = 32.768 kHz (in WIT state) Output transistors “off”	Except M38517F8FP/SP		5.0	10.0	µA
			M38517F8FP/SP		20		µA
		Middle-speed mode f(XIN) = 8 MHz f(XCIN) = stopped Output transistors “off”			4.0	7.0	mA
		Middle-speed mode f(XIN) = 8 MHz (in WIT state) f(XCIN) = stopped Output transistors “off”			1.5		mA
		Increment when A-D conversion is executed f(XIN) = 8 MHz			800		µA
		All oscillation stopped (in STP state) Output transistors “off”	Ta = 25 °C		0.1	1.0	µA
			Ta = 85 °C			10	µA

A-D converter characteristics

Table 31 A-D converter characteristics
(V_{CC} = 2.7 to 5.5 V, V_{SS} = AV_{SS} = 0 V, T_a = –20 to 85 °C, f(X_{IN}) = 8 MHz, unless otherwise noted)

<table>
<tr><th rowspan="2">Symbol</th><th rowspan="2" colspan="2">Parameter</th><th rowspan="2">Test conditions</th><th colspan="3">Limits</th><th rowspan="2">Unit</th></tr>
<tr><th>Min.</th><th>Typ.</th><th>Max.</th></tr>
<tr><td>–</td><td colspan="2">Resolution</td><td></td><td></td><td></td><td>10</td><td>bit</td></tr>
<tr><td>–</td><td colspan="2">Absolute accuracy (excluding quantization error)</td><td></td><td></td><td></td><td>±4</td><td>LSB</td></tr>
<tr><td rowspan="2">t_{CONV}</td><td rowspan="2" colspan="2">Conversion time</td><td>High-speed mode,
Middle-speed mode</td><td></td><td></td><td>61</td><td>tc(φ)</td></tr>
<tr><td>Low-speed mode</td><td></td><td>40</td><td></td><td>µs</td></tr>
<tr><td>R_{LADDER}</td><td colspan="2">Ladder resistor</td><td></td><td></td><td>35</td><td></td><td>kΩ</td></tr>
<tr><td rowspan="2">I_{VREF}</td><td rowspan="2">Reference power source input current</td><td>V_{REF} “on”</td><td rowspan="2">V_{REF} = 5.0 V</td><td>50</td><td>150</td><td>200</td><td rowspan="2">µA</td></tr>
<tr><td>V_{REF} “off”</td><td></td><td></td><td>5.0</td></tr>
<tr><td>$I_{I(AD)}$</td><td colspan="2">A-D port input current</td><td></td><td></td><td>0.5</td><td>5.0</td><td>µA</td></tr>
</table>

Timing requirements

Table 32 Timing requirements (1)
(V_{CC} = 4.0 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\overline{RESET})$	Reset input “L” pulse width	20			X_{IN} cycle
$t_c(X_{IN})$	External clock input cycle time	125			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	50			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	50			ns
$t_c(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	200			ns
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	80			ns
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	80			ns
$t_{WH}(INT)$	INT_0 to INT_3 input “H” pulse width	80			ns
$t_{WL}(INT)$	INT_0 to INT_3 input “L” pulse width	80			ns
$t_c(S_{CLK1})$	Serial I/O1 clock input cycle time **(Note)**	800			ns
$t_{WH}(S_{CLK1})$	Serial I/O1 clock input “H” pulse width **(Note)**	370			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock input “L” pulse width **(Note)**	370			ns
$t_{su}(R_xD\text{-}S_{CLK1})$	Serial I/O1 input setup time	220			ns
$t_h(S_{CLK1}\text{-}R_xD)$	Serial I/O1 input hold time	100			ns
$t_c(S_{CLK2})$	Serial I/O2 clock input cycle time	1000			ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock input “H” pulse width	400			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock input “L” pulse width	400			ns
$t_{su}(S_{IN2}\text{-}S_{CLK2})$	Serial I/O2 clock input setup time	200			ns
$t_h(S_{CLK2}\text{-}S_{IN2})$	Serial I/O2 clock input hold time	200			ns

Note : When $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when $f(X_{IN})$ = 8 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

Table 33 Timing requirements (2)
(V_{CC} = 2.7 to 5.5 V, V_{SS} = 0 V, T_a = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
$t_w(\overline{RESET})$	Reset input “L” pulse width	20			X_{IN} cycle
$t_c(X_{IN})$	External clock input cycle time	250			ns
$t_{WH}(X_{IN})$	External clock input “H” pulse width	100			ns
$t_{WL}(X_{IN})$	External clock input “L” pulse width	100			ns
$t_c(CNTR)$	$CNTR_0$, $CNTR_1$ input cycle time	500			ns
$t_{WH}(CNTR)$	$CNTR_0$, $CNTR_1$ input “H” pulse width	230			ns
$t_{WL}(CNTR)$	$CNTR_0$, $CNTR_1$ input “L” pulse width	230			ns
$t_{WH}(INT)$	INT_0 to INT_3 input “H” pulse width	230			ns
$t_{WL}(INT)$	INT_0 to INT_3 input “L” pulse width	230			ns
$t_c(S_{CLK1})$	Serial I/O1 clock input cycle time **(Note)**	2000			ns
$t_{WH}(S_{CLK1})$	Serial I/O1 clock input “H” pulse width **(Note)**	950			ns
$t_{WL}(S_{CLK1})$	Serial I/O1 clock input “L” pulse width **(Note)**	950			ns
$t_{su}(R_xD\text{-}S_{CLK1})$	Serial I/O1 input setup time	400			ns
$t_h(S_{CLK1}\text{-}R_xD)$	Serial I/O1 input hold time	200			ns
$t_c(S_{CLK2})$	Serial I/O2 clock input cycle time	2000			ns
$t_{WH}(S_{CLK2})$	Serial I/O2 clock input “H” pulse width	950			ns
$t_{WL}(S_{CLK2})$	Serial I/O2 clock input “L” pulse width	950			ns
$t_{su}(S_{IN2}\text{-}S_{CLK2})$	Serial I/O2 clock input setup time	400			ns
$t_h(S_{CLK2}\text{-}S_{IN2})$	Serial I/O2 clock input hold time	300			ns

Note : When $f(X_{IN})$ = 4 MHz and bit 6 of address $001A_{16}$ is “1” (clock synchronous).
Divide this value by four when $f(X_{IN})$ = 4 MHz and bit 6 of address $001A_{16}$ is “0” (UART).

Switching characteristics

Table 34 Switching characteristics (1)
(VCC = 4.0 to 5.5 V, VSS = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (SCLK1)	Serial I/O1 clock output “H” pulse width	Fig. 79	t_C(SCLK1)/2–30			ns
t_{WL} (SCLK1)	Serial I/O1 clock output “L” pulse width		t_C(SCLK1)/2–30			ns
t_d (SCLK1-TXD)	Serial I/O1 output delay time **(Note 1)**				140	ns
t_v (SCLK1-TXD)	Serial I/O1 output valid time **(Note 1)**		–30			ns
t_r (SCLK1)	Serial I/O1 clock output rising time				30	ns
t_f (SCLK1)	Serial I/O1 clock output falling time				30	ns
t_{WH} (SCLK2)	Serial I/O2 clock output “H” pulse width		t_C(SCLK2)/2–160			ns
t_{WL} (SCLK2)	Serial I/O2 clock output “L” pulse width		t_C(SCLK2)/2–160			ns
t_d (SCLK2-SOUT2)	Serial I/O2 output delay time **(Note 2)**				200	ns
t_v (SCLK2-SOUT2)	Serial I/O2 output valid time **(Note 2)**		0			ns
t_f (SCLK2)	Serial I/O2 clock output falling time				30	ns
t_r (CMOS)	CMOS output rising time **(Note 3)**			10	30	ns
t_f (CMOS)	CMOS output falling time **(Note 3)**			10	30	ns

Notes **1:** When the P25/TXD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: When the P01/SOUT2 and P02/SCLK2 P-channel output disable bit of the Serial I/O2 control register 1 (bit 7 of address 0015_{16}) is “0”.
3: The XOUT pin is excluded.

Table 35 Switching characteristics (2)
(VCC = 2.7 to 5.5 V, VSS = 0 V, Ta = –20 to 85 °C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
t_{WH} (SCLK1)	Serial I/O1 clock output “H” pulse width	Fig. 79	t_C(SCLK1)/2–50			ns
t_{WL} (SCLK1)	Serial I/O1 clock output “L” pulse width		t_C(SCLK1)/2–50			ns
t_d (SCLK1-TXD)	Serial I/O1 output delay time **(Note 1)**				350	ns
t_v (SCLK1-TXD)	Serial I/O1 output valid time **(Note 1)**		–30			ns
t_r (SCLK1)	Serial I/O1 clock output rising time				50	ns
t_f (SCLK1)	Serial I/O1 clock output falling time				50	ns
t_{WH} (SCLK2)	Serial I/O2 clock output “H” pulse width		t_C(SCLK2)/2–240			ns
t_{WL} (SCLK2)	Serial I/O2 clock output “L” pulse width		t_C(SCLK2)/2–240			ns
t_d (SCLK2-SOUT2)	Serial I/O2 output delay time **(Note 2)**				400	ns
t_v (SCLK2-SOUT2)	Serial I/O2 output valid time **(Note 2)**		0			ns
t_f (SCLK2)	Serial I/O2 clock output falling time				50	ns
t_r (CMOS)	CMOS output rising time **(Note 3)**			20	50	ns
t_f (CMOS)	CMOS output falling time **(Note 3)**			20	50	ns

Notes **1:** When the P25/TXD P-channel output disable bit of the UART control register (bit 4 of address $001B_{16}$) is “0”.
2: When the P01/SOUT2 and P02/SCLK2 P-channel output disable bit of the Serial I/O2 control register 1 (bit 7 of address 0015_{16}) is “0”.
3: The XOUT pin is excluded.

MULTI-MASTER I^2C-BUS BUS LINE CHARACTERISTICS

Table 36 Multi-master I^2C-BUS bus line characteristics

Symbol	Parameter	Test conditions	Standard clock mode		High-speed clock mode		Unit
			Min.	Max.	Min.	Max.	
t_{BUF}	Bus free time	Fig. 80	4.7		1.3		µs
$t_{HD;STA}$	Hold time for START condition		4.0		0.6		µs
t_{LOW}	Hold time for SCL clock = “0”		4.7		1.3		µs
t_R	Rising time of both SCL and SDA signals			1000	20+0.1Cb	300	ns
$t_{HD;DAT}$	Data hold time		0		0	0.9	µs
t_{HIGH}	Hold time for SCL clock = “1”		4.0		0.6		µs
t_F	Falling time of both SCL and SDA signals			300	20+0.1Cb	300	ns
$t_{SU;DAT}$	Data setup time		250		100		ns
$t_{SU;STA}$	Setup time for repeated START condition		4.7		0.6		µs
$t_{SU;STO}$	Setup time for STOP condition		4.0		0.6		µs

Note: C_b = total capacitance of 1 bus line

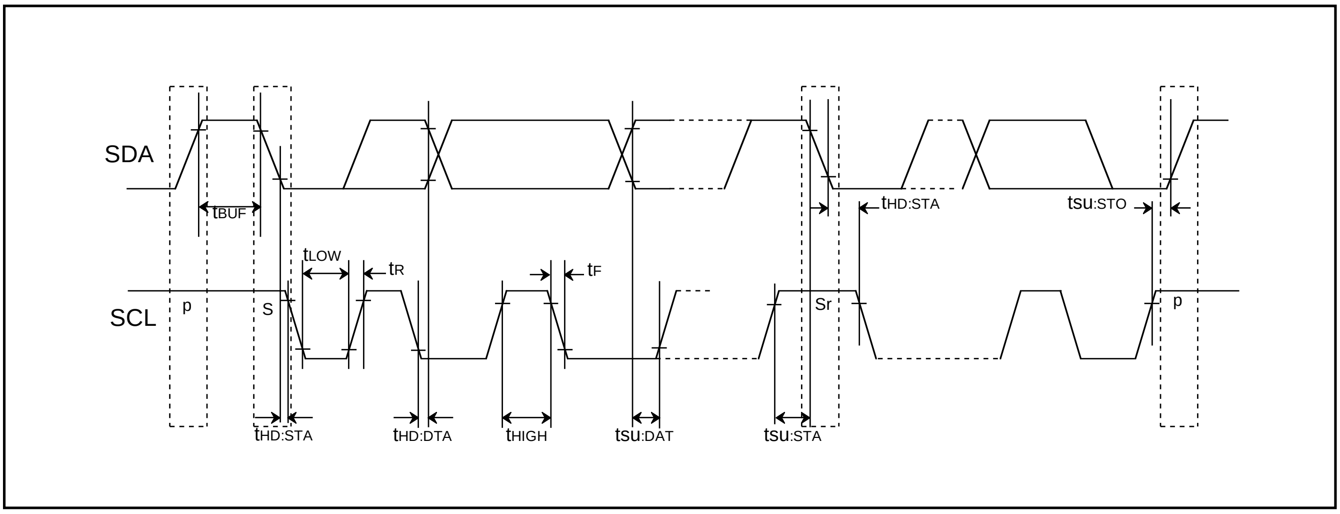


Fig. 78 Timing diagram of multi-master I^2C-BUS

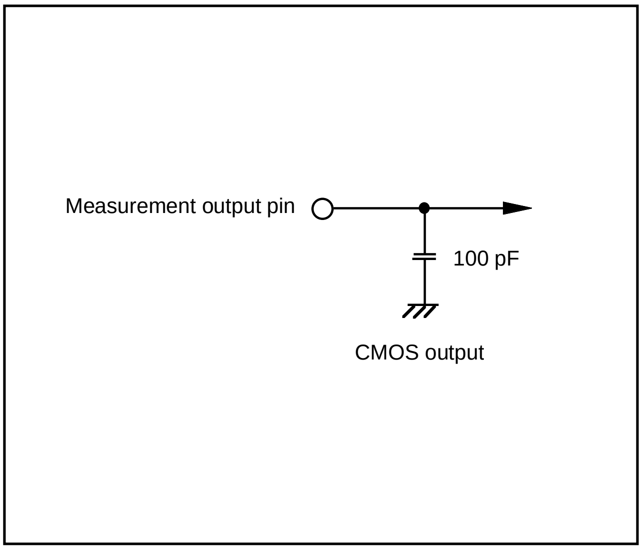


Fig. 79 Circuit for measuring output switching characteristics (1)

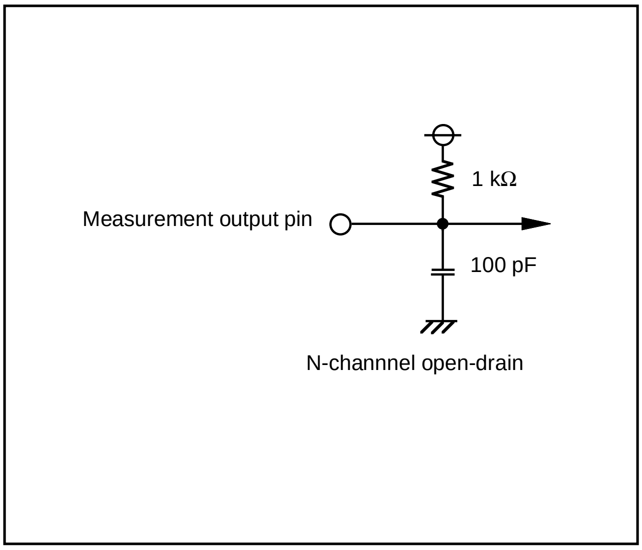


Fig. 80 Circuit for measuring output switching characteristics (2)

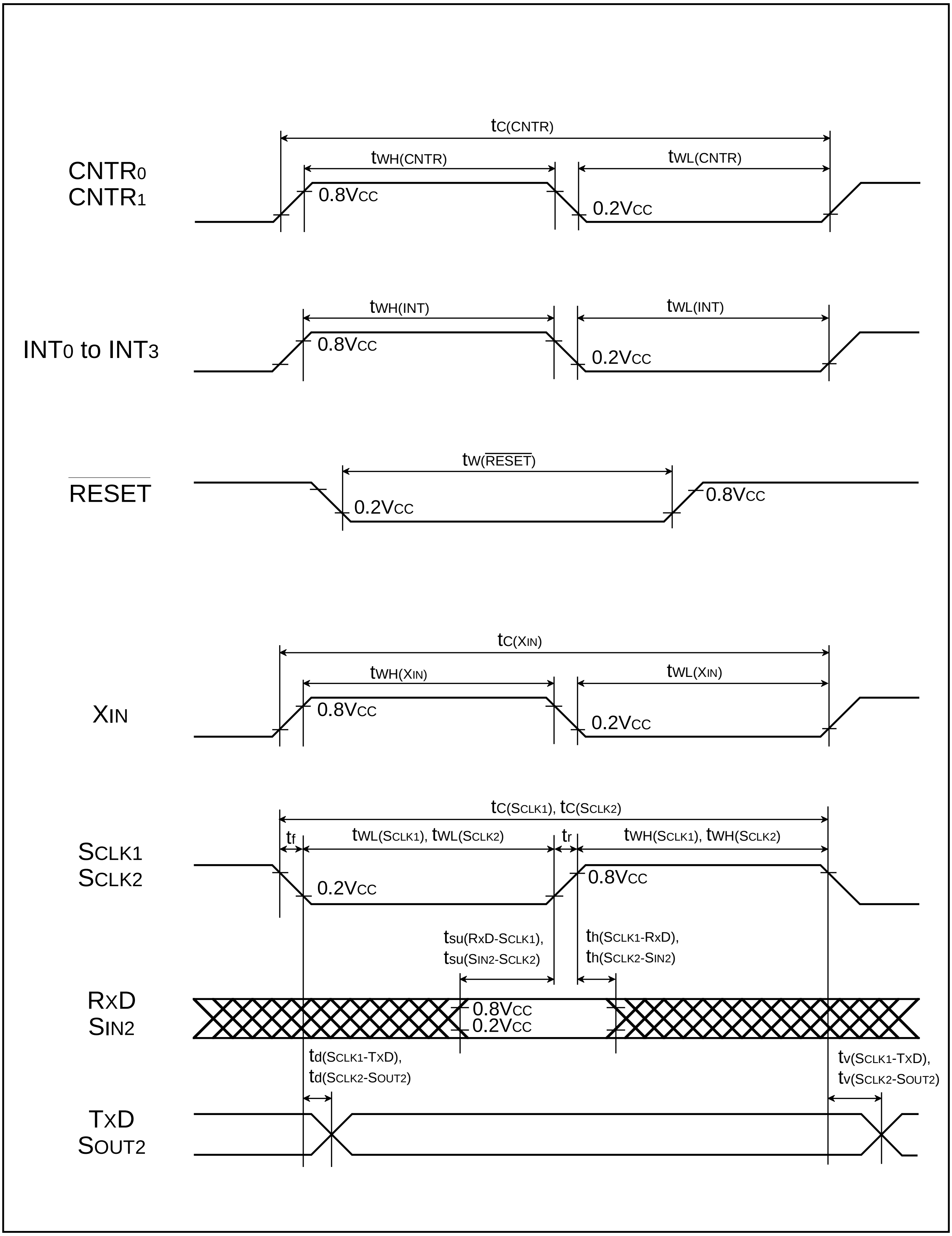


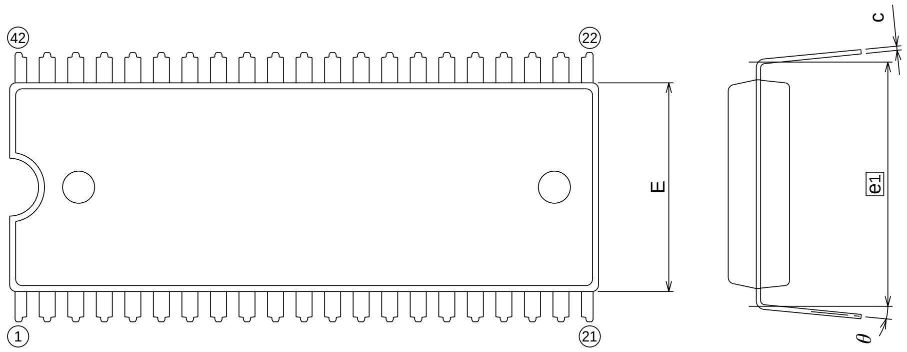
Fig. 81 Timing diagram

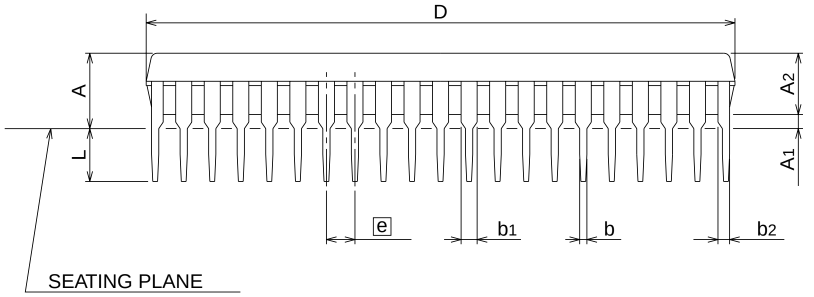
PACKAGE OUTLINE

42P4B (MMP)

Plastic 42pin 600mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP42-P-600-1.78	–	4.1	Alloy 42/Cu Alloy



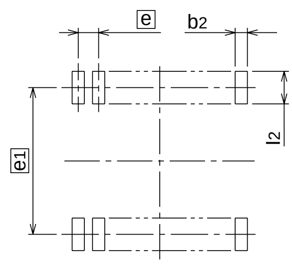


Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.5
A_1	0.51	–	–
A_2	–	3.8	–
b	0.35	0.45	0.55
b_1	0.9	1.0	1.3
b_2	0.63	0.73	1.03
c	0.22	0.27	0.34
D	36.5	36.7	36.9
E	12.85	13.0	13.15
$\boxed{e}$	–	1.778	–
$\boxed{e_1}$	–	15.24	–
L	3.0	–	–
θ	0°	–	15°

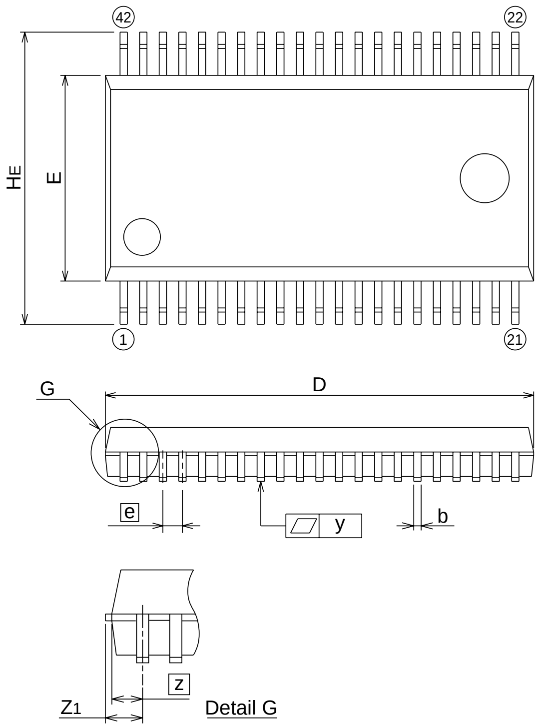
42P2R-A/E

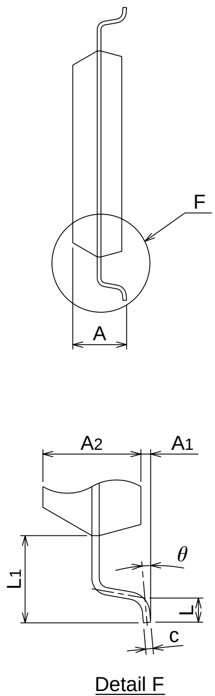
Plastic 42pin 450mil SSOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SSOP42-P-450-0.80	–	0.63	Alloy 42



Recommended Mount Pad





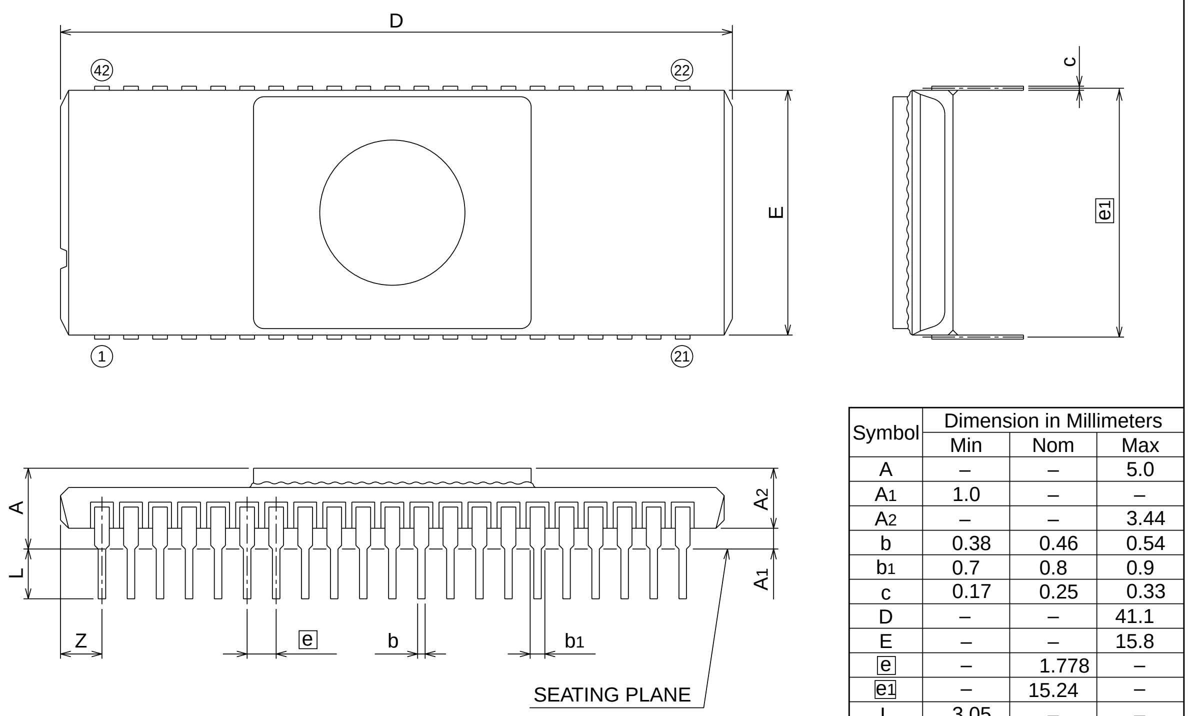
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	2.4
A_1	0.05	–	–
A_2	–	2.0	–
b	0.25	0.3	0.4
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
$\boxed{e}$	–	0.8	–
H_E	11.63	11.93	12.23
L	0.3	0.5	0.7
L_1	–	1.765	–
$\boxed{z}$	–	0.75	–
Z_1	–	–	0.9
y	–	–	0.15
θ	0°	–	10°
b_2	–	0.5	–
$\boxed{e_1}$	–	11.43	–
l_2	1.27	–	–

RENESAS

42S1B-A

Metal seal 42pin 600mil DIP

EIAJ Package Code	JEDEC Code	Weight(g)
WDIP42-C-600-1.78	–	



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	–	–	5.0
A_1	1.0	–	–
A_2	–	–	3.44
b	0.38	0.46	0.54
b_1	0.7	0.8	0.9
c	0.17	0.25	0.33
D	–	–	41.1
E	–	–	15.8
$\boxed{e}$	–	1.778	–
$\boxed{e_1}$	–	15.24	–
L	3.05	–	–
Z	–	–	3.05

REVISION HISTORY	3851 Group (built-in 24 KB or more ROM) Data Sheet

Rev.	Date	Description: Page	Description: Summary
1.00	Jul. 26, 2002	–	First edition issued
1.01	Oct. 15, 2003		•Mitsubishi, Mitsubishi Electric Corporation → Renesas Technology Corporation
			•SCLK → $SCLK_1$
		1	●Multi-master I^2C-BUS interface (option) → ●Multi-master I^2C-BUS interface
		5	Fig.4 Memory expansion plan
			Under development M38517M8/F8 → Mass production M38517M8/F8
		14-15	“SDA input”, “SCL input”
			“Serial I/O1 input”
		15	(12)Port $P2_6$ External clock input → Serial I/O1 external clock input
			(13)Port $P2_7$ Serial ready output → Serial I/O1 ready output
		17	•Interrupt occur by 17 sources among 17 sources seven external
			→ Interrupt occur by 17 sources : seven external
			•address $3A_{16}$, address 23_{16} → address $003A_{16}$, address 0023_{16}
		18	Table 8 Interrupt vector addresses and priority
			Serial I/O1 reception, Serial I/O transmission : Remarks
			Valid when serial I/O1 is selected → Valid when serial I/O is selected
		22	Fig.18 Block diagram of clock synchronous serial I/O
			$P2_7/\overline{SRDY_1}$ → $P2_7/CNTR_0/\overline{SRDY_1}$
		29	MITSUBISHI ELECTRIC CORPORATION’S → Renesas Technology Corporation’s
		32	•Bit 6: SDA/SCL pin selection bit → Bit 6: SDA/SCL pin selection bit (TSEL)
			•Bit 7: I^2C-BUS interface pin input level selection bit
			→ Bit 7: I^2C-BUS interface pin input level selection bit (TISS)
		77	“Mitsubishi MCU Technical Information” Homepage (http:// www. infomicom.maec.co.jp/indexe.htm)
			→ “Renesas Technology” Homepage Rom ordering (http:// www. renesas.com/eng/rom)
		79	Table 26 Recommended operating conditions (1)

Symbol	Parameter		Limits: Min.	Limits: Typ.	Limits: Max.	Unit
V_{IH}	“H” input voltage (when I^2C-BUS input level is selected)		$0.7V_{CC}$		V_{CC}	V
	SDA2, SCL2	SDA1, SCL1	$0.7V_{CC}$		5.8	V
V_{IH}	“H” input voltage (when SMBUS input level is selected)		1.4		V_{CC}	V
	SDA2, SCL2	SDA1, SCL1	1.4		5.8	V

↓

Symbol	Parameter		Limits: Min.	Limits: Typ.	Limits: Max.	Unit
V_{IH}	“H” input voltage (when I^2C-BUS input level is selected)	SDA1, SCL1	$0.7V_{CC}$		5.8	V
		SDA2, SCL2	$0.7V_{CC}$		V_{CC}	V
V_{IH}	“H” input voltage (when SMBUS input level is selected)	SDA1, SCL1	1.4		5.8	V
		SDA2, SCL2	1.4		V_{CC}	V

Rev.	Date	Page	Summary
		81	Table 29 Electrical characteristics (2)
			$V_{T+}-V_{T-}$ Hysterisis RxD, SCLK → RxD, $SCLK_1$, SIN_2, $SCLK_2$

Sales Strategic Planning Div. Nippon Bldg., 2-6-2, Ohte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

http://www.renesas.com