

M62420SP/ FP/ AFP

2ch Electronic Volume with Tone by I²C Bus System

REJ03F0051-0100Z

Rev.1.0

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Description

M62420SP/FP/AFP is the tone and volume controller which is controlled by I²C bus. This IC can apply the broad application because of low noise and distortion.

M62420AFP changes the slave address from M62420FP.

Features

- TONE(Bass/Treble) control and 1 dB step volume control are enabled.
- Low noise and low distortion .
 $V_{NO} = 4.5 \mu V_{rms}$, CTHD=0.1% max
- Controlling by serial data in conformity to the I²C bus format .

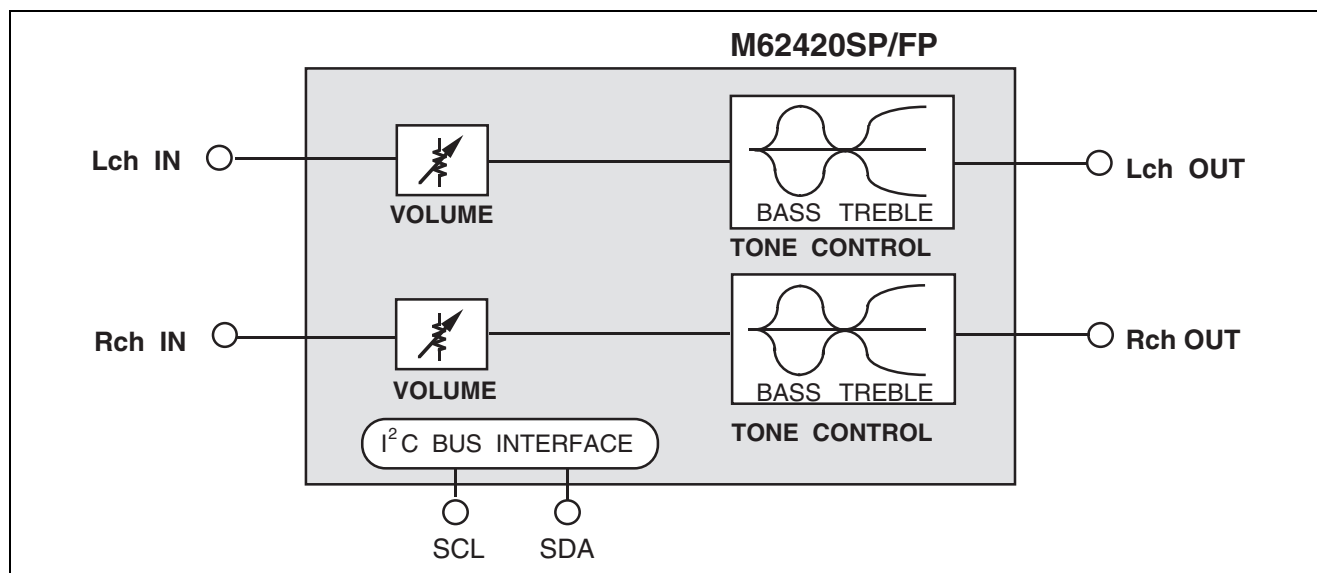
Applications

- TV, Mini-Stereo, etc

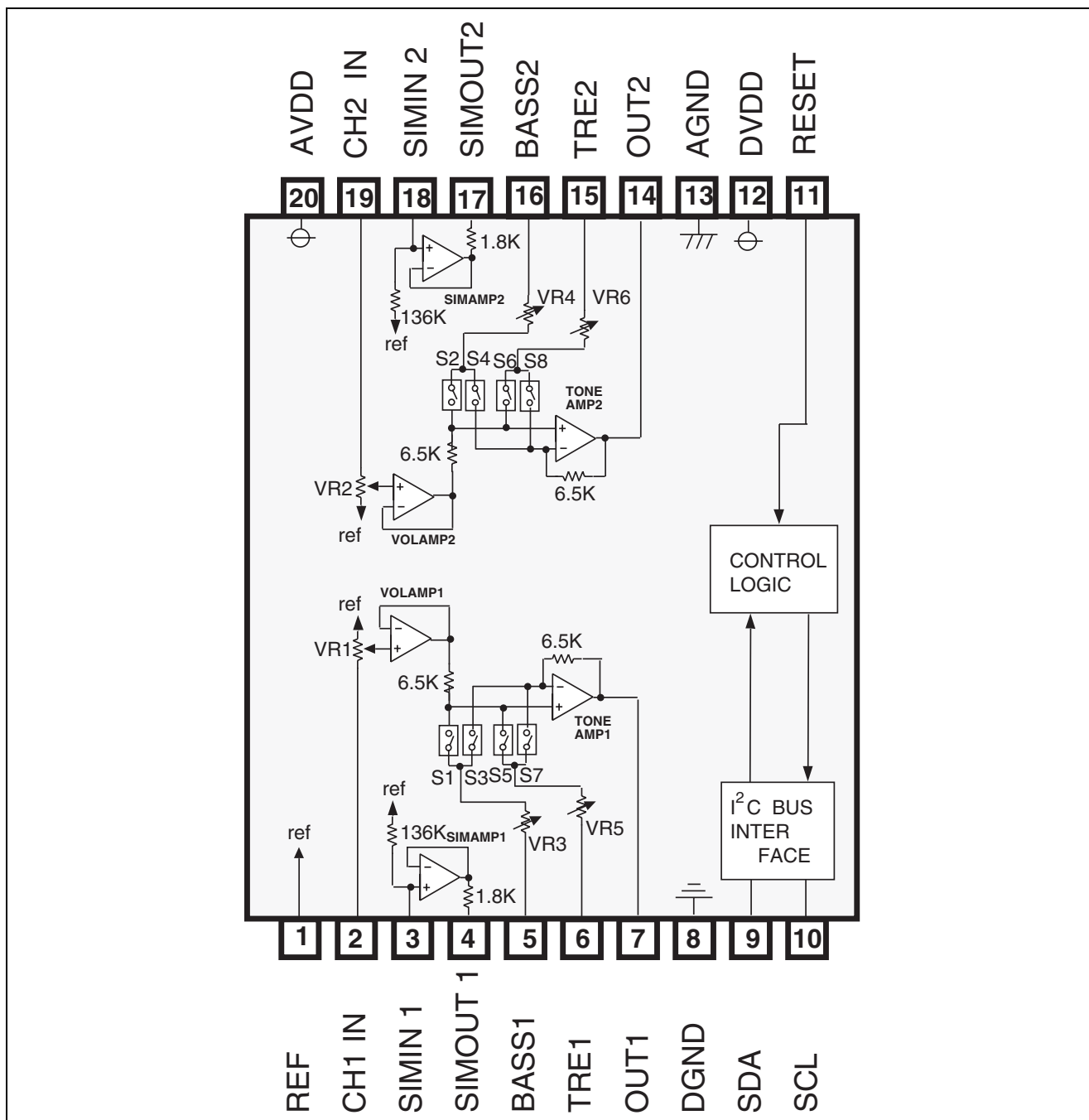
Recommended Operating Condition

- Supply voltage range: 8.5 to 9.5 V (analog) 4.5 to 5.5 V (digital)
- Rated supply voltage: 9 V (analog) 5 V (digital)

System Block Diagram



Block diagram and Pin Configuration



Pin Description

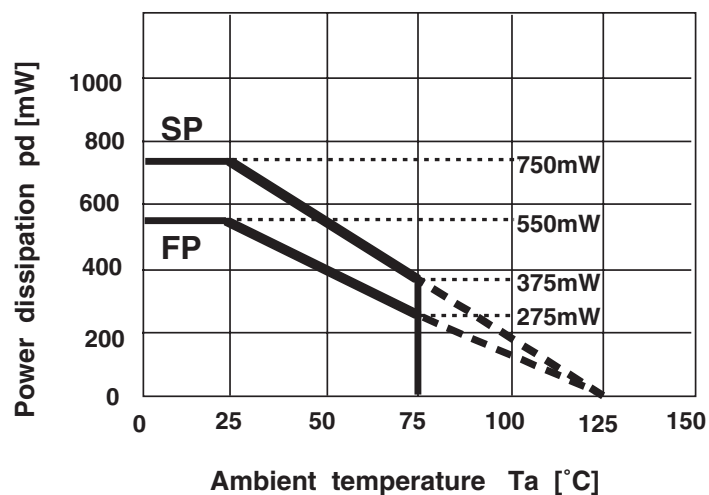
Pin No.	Pin Name	I/O	Description
1	REF	I	Reference voltage terminal for analog
2	CH1 IN	I	Input terminal (ch1)
3	SIMIN1	I	Pin for capacitor of simulated inductor 1
4	SIMOUT 1	O	Pin for capacitor of simulated inductor 1
5	BASS1	I	Pin for capacitor of ch1-side bass setting
6	TRE1	I	Pin for capacitor of ch1-side treble setting
7	VOL OUT1	O	Output terminal (ch1)
8	DGND	I	Digital GND
9	SDA	I/O	I/O terminal of DATA I ² C bus format
10	SCL	I	Input terminal of CLOCK I ² C bus format
11	RESET	I	RESET terminal of built-in logic circuit
12	DVDD	I	VDD for digital circuit
13	AGND	I	GND for analog circuit
14	VOL OUT2	O	Output terminal (ch2)
15	TRE2	I	Pin for capacitor of ch2-side treble setting
16	BASS2	I	Pin for capacitor of ch2-side bass setting
17	SIMOUT2	O	Pin for capacitor of simulated inductor 2
18	SIMIN 2	I	Pin for capacitor of simulated inductor 2
19	CH2 IN	I	Input terminal (ch2)
20	AVDD	I	VCC for analog circuit

Absolute Maximum Ratings

(Ta = 25°C)

Symbol	Parameter	Condition	Limits	Unit
AVdd	Analog supply voltage		10.0	V
DVdd	Digital supply voltage		7.0	V
Pd	Power dissipation	Ta ≤ 25°C	750	mW
Kθ	Thermal Derating ratio	Ta > 25°C	7.5	mW / °C
Topr	Operating temperature		−20 to +75	°C
Tstg	Storage temperature		−40 to +125	°C

Thermal Derating Curves



Recommended Operating Condition

($T_a = 25^\circ\text{C}$ unless otherwise noted)

Item	Symbol	Condition	MIN	TYP	MAX	Unit
Analog supply voltage	AVDD		8.5	9.0	9.5	V
Digital supply voltage	DVDD		4.5	5.0	5.5	V
H level input voltage (logic circuit)	VIH		0.7DVDD	—	VDD	V
H level input voltage (logic circuit)	VIL		0	—	0.3DVDD	V

Electrical Characteristics (DC)

(Ta = 25°C, AVDD = 9 V, DVDD = 5 V and tone, bassboost = 0 dB unless otherwise noted)

(1) Supply voltage

Item	Symbol	Conditions	Limit			Unit
			Min.	Typ.	Max.	
Analog supply current	Icc	AVdd = 9.0 V Measure terminal = 20 pin No signal input	—	10	20	mA
Digital supply current	Idd	DVdd = 5 V Measure terminal = 12 pin No signal input	—	0	2	μA

(2) I/O CHARACTERISTICS

Item	Symbol	Conditions	Limit			Unit
			Min.	Typ.	Max.	
Maximum input voltage	VIM	2,19 pin input, 7,14 pin output RL = 10 K, THD = 1%, f = 1 kHz ATT = -6dB	2.0	3.2	—	Vrms
Output voltage	Vodc	7 pin, 14 pin, no signal	4.35	4.5	4.65	V
Gain	Gv	Vin = 0dBm, FLAT, f = 1 kHz 2-7PIN 19-14PIN gain	-2	0	2	dB
Output noise voltage	Vono	JIS-A filter, no signal, Rg = 10 KΩ 7,14 pin	—	4.5	30	μVrms
Total harmonic distortion	THD	7 pin, 14 pin f=1kHz Vo = 0.5 Vrms, RL = 10KΩ LPF = 30 kHz	—	0.05	0.1	%
Channel separation	CT	RL = 10 K S:Vin = 1 Vrms,f=1kHz M:Rg = 10 kΩ, JIS-A filter	—	-100	-70	dB

(3) Tone Characteristics

Item	Symbol	Conditions	Limit			Unit
			Min.	Typ.	Max.	
Tone control gain (bass)	Gbassb	f = 100 Hz	9	12	15	dB
	Gbassc		-15	-12	-9	dB
Tone control gain (treble)	Gtrebb	f = 10 Hz	9	12	15	dB
	Gtrebc		-15	-12	-9	dB

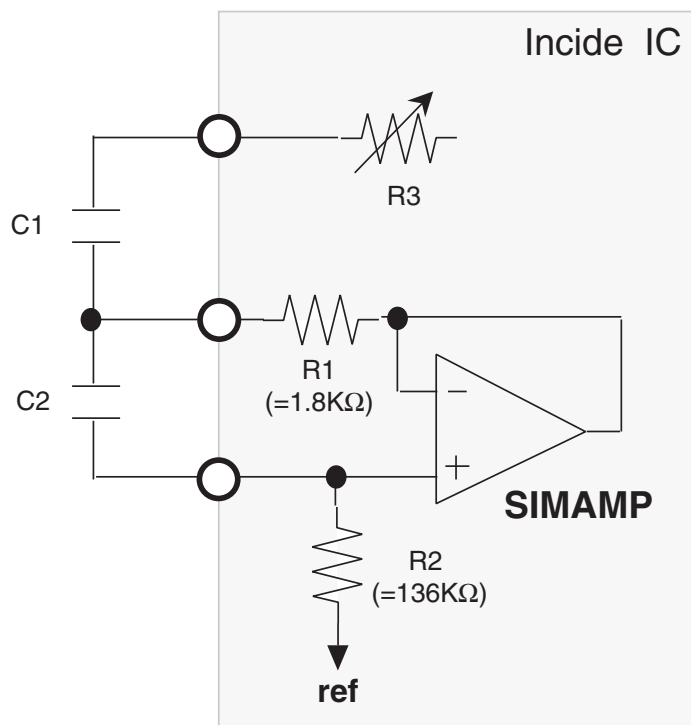
(4) Volume Characteristics

Item	Symbol	Conditions	Limit			Unit
			Min.	Typ.	Max.	
Maximum attenuation	ATTmax	f = 1KHz, Vin = 0dBm	-108	-100	-80	dB
Minimum attenuation	ATTmin	2 pin to 7 pin 19 pin to 14pin gain JIS-A filter	-1.5	0	1.5	dB

Function Explanation

(1) Equivaration Circuit of Tone Control

The resonance circuit is able to construct by using built-in amplifier for simulated inductor. (Shows the constant as follow)



Center frequency

$$f_0 = 1 / 2\pi \sqrt{C1 \cdot C2 \cdot R1 \cdot R2} \text{ [Hz]}$$

$$Q = \sqrt{(C2 \cdot R2) / (C1 \cdot R1)}$$

(EX) BASS band (f=100Hz)

R1=1.8KΩ , R2=136KΩ

C1=0.47μF , C2=0.022μF

FIG1. The circuit used simulated inductor.

FIG1 is equal to FIG2.

The following relation is concluded.

$$L = C2 \cdot ER1 \cdot ER2$$

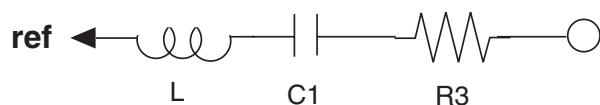
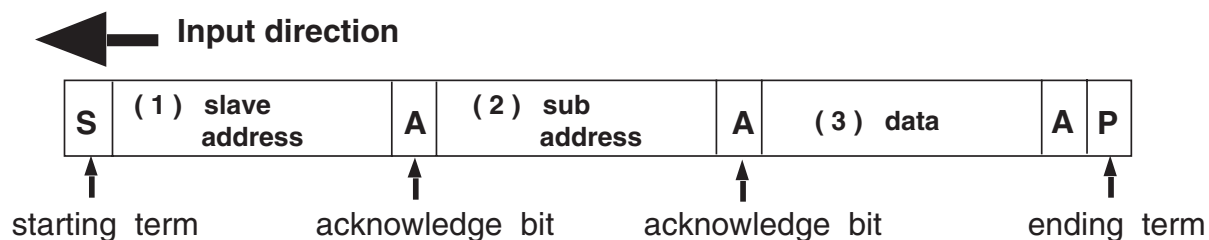


FIG2. The equivalent circuit used L.

I²C BUS Input Data Format

(1) Slave address

M62420SP / FP

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	0	0

M62420AFP

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	1	0

(2) sub address

The following sub address is defined at this IC.

subA7	subA6	subA5	subA4	subA3	subA2	subA1	subA0
← empty slot →			MUTE mode	TREBLE level mode	BASS level mode	channel2 volume mode	channel1 volume mode
			1: ON 0: OFF	1: ON 0: OFF	1: ON 0: OFF	1: ON 0: OFF	1: ON 0: OFF

(3) -1: volume control

The volume control is enabled at following condition.

subA0 :

0
1

 ,

1
0

 ,

1
1

 (either bit is 1)

subA2 :

0
0

 (both bits are 0)

volume code

ATT	D4	D3	D2	D1	D0
0dB	H	H	H	H	H
2dB	H	H	H	H	L
4dB	H	H	H	L	H
6dB	H	H	H	L	L
8dB	H	H	L	H	H
10dB	H	H	L	H	L
12dB	H	H	L	L	H
14dB	H	H	L	L	L
16dB	H	L	H	H	H
18dB	H	L	H	H	L
20dB	H	L	H	L	H
22dB	H	L	H	L	L
24dB	H	L	L	H	H
26dB	H	L	L	H	L
28dB	H	L	L	L	H
30dB	H	L	L	L	L
32dB	L	H	H	H	H
34dB	L	H	H	H	L
36dB	L	H	H	L	H
38dB	L	H	H	L	L
40dB	L	H	L	H	H
42dB	L	H	L	H	L
46dB	L	H	L	L	H
50dB	L	H	L	L	L
54dB	L	L	H	H	H
58dB	L	L	H	H	L
62dB	L	L	H	L	H
66dB	L	L	H	L	L
70dB	L	L	L	H	H
74dB	L	L	L	H	L
78dB	L	L	L	L	H
∞dB	L	L	L	L	L

ATT	D6	D5
0dB	H	H
1dB	H	L
* 2dB	L	H
* 3dB	L	L

* 2dB,3dB setting is enabled at less than 42dB step.

(3) -2 : tone level control

The tone level controlling is enabled at following condition.

subA0 : 0
subA1 : 0

(both bits are 0)

subA2 : 0 , 1 , 1
subA3 : 1 , 0 , 1

(either bit is 1)

tone code

	BASS				TREBLE			
	D7	D6	D5	D4	D3	D2	D1	D0
12dB	L	H	H	L	L	H	H	L
10dB	L	H	L	H	L	H	L	H
8dB	L	H	L	L	L	H	L	L
6dB	L	L	H	H	L	L	H	H
4dB	L	L	H	L	L	L	H	L
2dB	L	L	L	H	L	L	L	H
0dB	L	L	L	L	L	L	L	L
-2dB	H	L	L	H	H	L	L	H
-4dB	H	L	H	L	H	L	H	L
-6dB	H	L	H	H	H	L	H	H
-8dB	H	H	L	L	H	H	L	L
-10dB	H	H	L	H	H	H	L	H
-12dB	H	H	H	L	H	H	H	L

non-used code

HHHH
LHHH
HLLL

(3) -3 : Mute mode

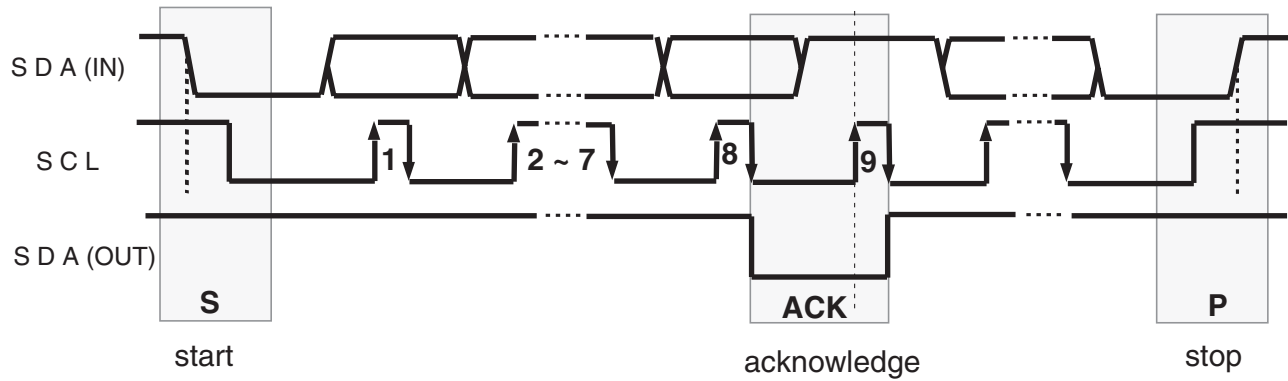
The mute mode is enabled at following condition.

subA0 : no definition
subA1 : no definition

subA2 : no definition
subA3 : no definition

subA4 : 1

DATA and CLOCK



start

This term is defined by SDA(in) falling edge at SCL H.

stop

This term is defined by SDA(in) rising edge at SCL H.

CAUTION

The SDA(IN) level never change at SCK=H except start and stop.

data transmission

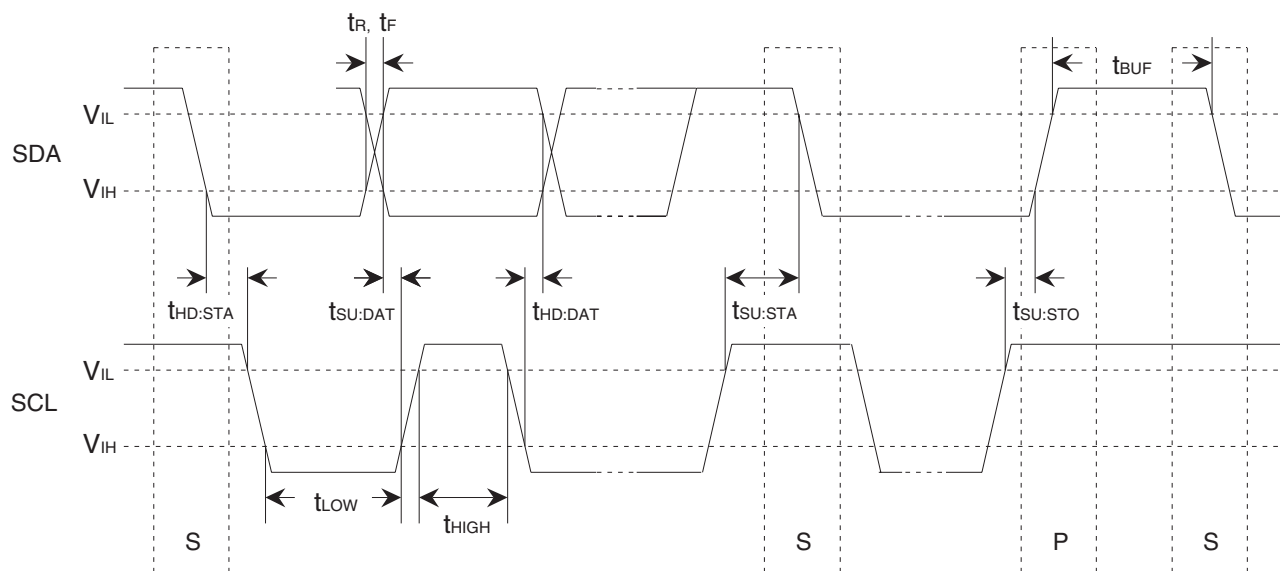
The SDA(IN) is enabled at SCL rising edge and H.

acknowledge

Transmitter must send H during ninth clock pulse of SCL.

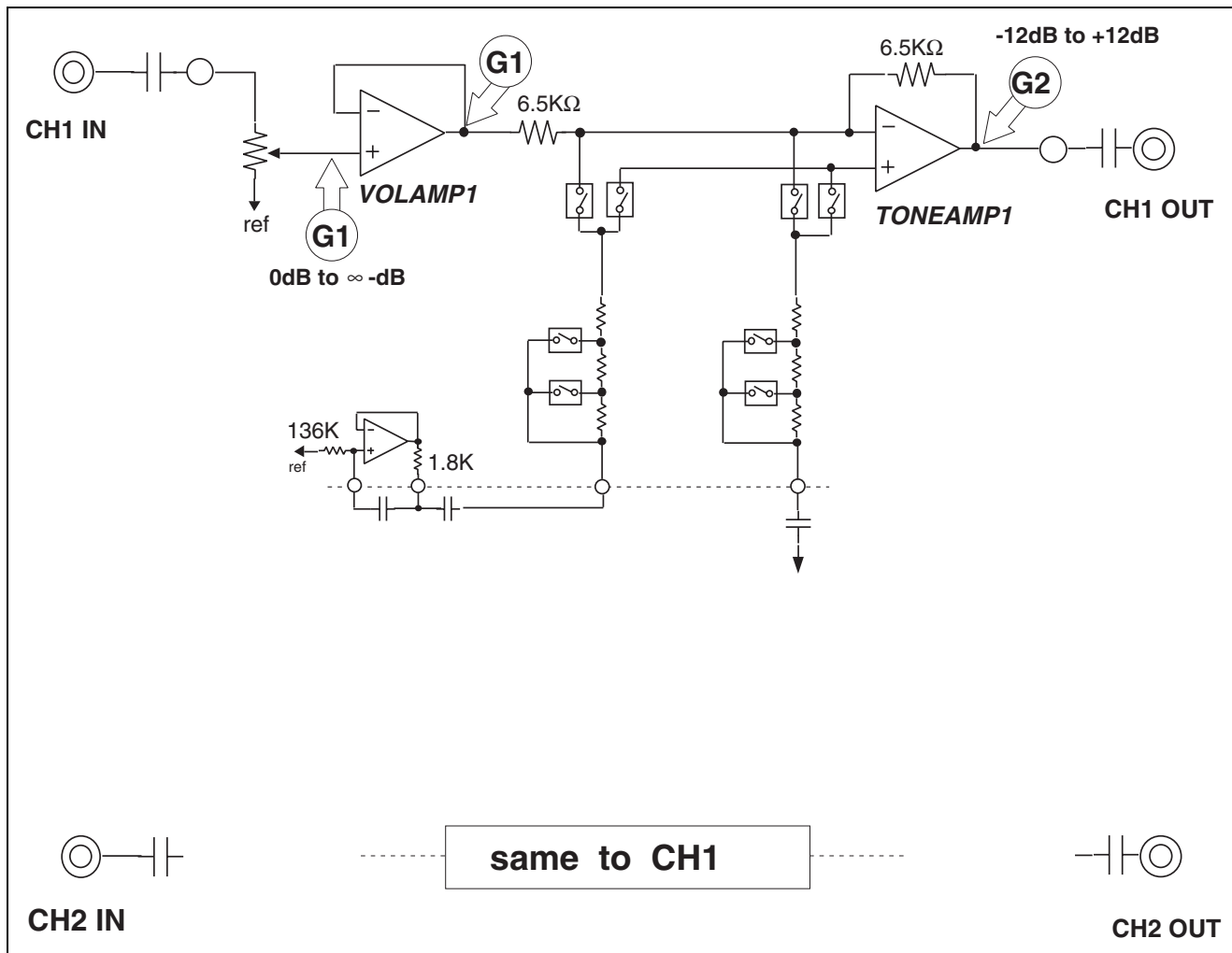
The case of finished receiving, the receiver replies L synchronized to falling edge of eighth pulse. And restart receiving the transmitted data synchronized to falling edge of ninth pulse.

BUS Line Timing Specification

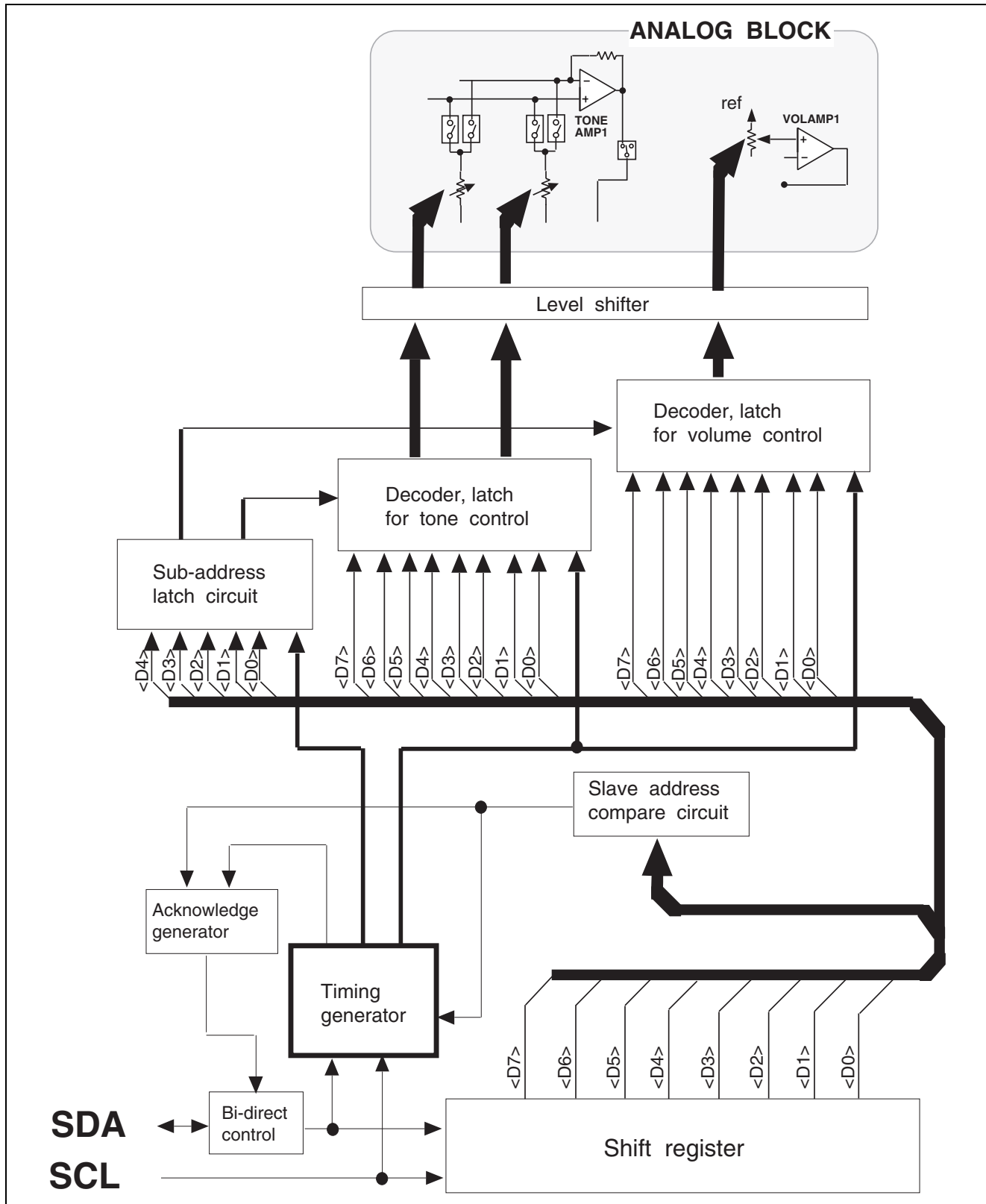


Parameter	Symbol	MIN	MAX	Units
Min. input low voltage	V_{IL}	-0.5	1.5	V
Max. input high voltage	V_{IH}	3.0	5.5	V
SCL clock frequency	f_{SCL}	0	100	kHz
Time the bus must be free before a new transmission can start	t_{BUF}	4.7		μs
Hold time start condition. After this period the first clock pulse is generated	$t_{HD:STA}$	4.0		μs
The LOW period of the clock	t_{LOW}	4.7		μs
The HIGH period of the clock	t_{HIGH}	4.0		μs
Set up time for start condition (Only relevant for a repeated start condition)	$t_{SU:STA}$	4.7		μs
Hold time DATA	$t_{HD:DAT}$	0		μs
Set-up time DATA	$t_{SU:DAT}$	250		ns
Rise time of both SDA and SCL lines	t_R		1000	ns
Fall time of both SDA and SCL lines	t_F		300	ns
Set-up time for stop condition	$t_{SU:STO}$	4.0		μs

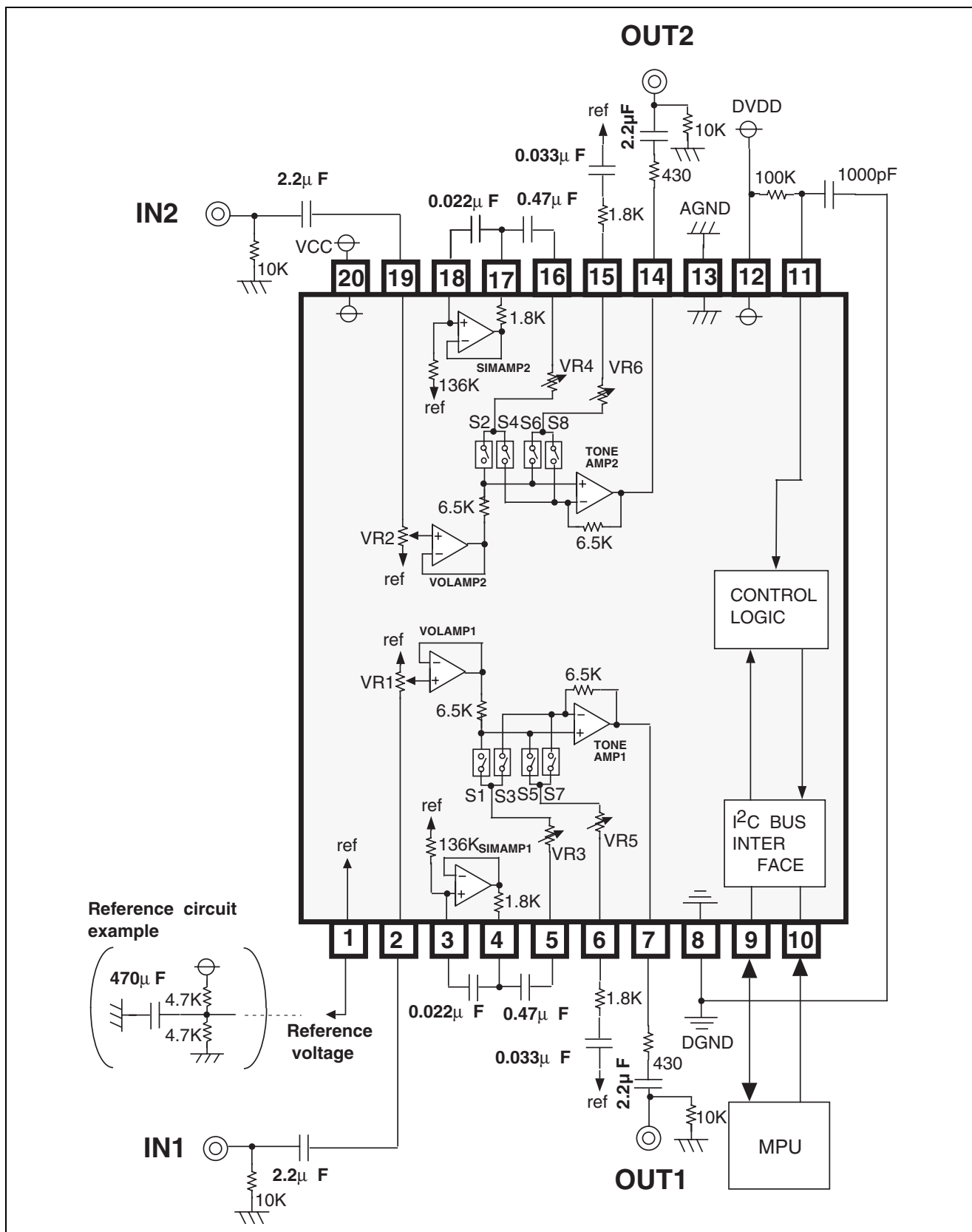
Level Diagram



Logic Circuit



Application Example



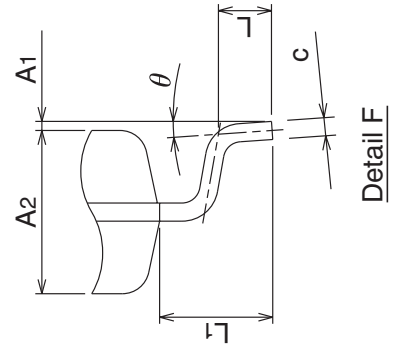
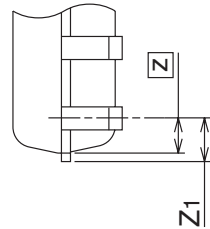
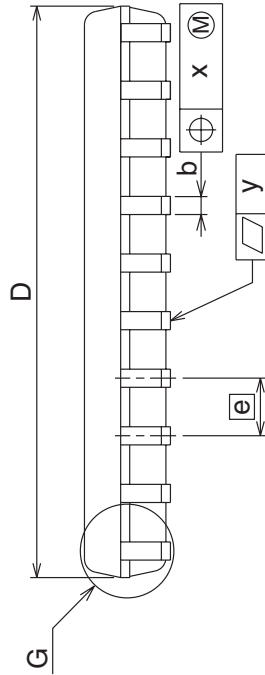
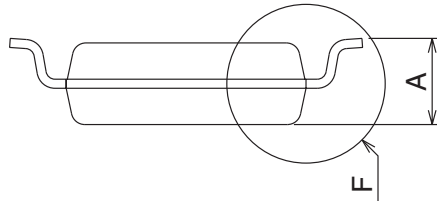
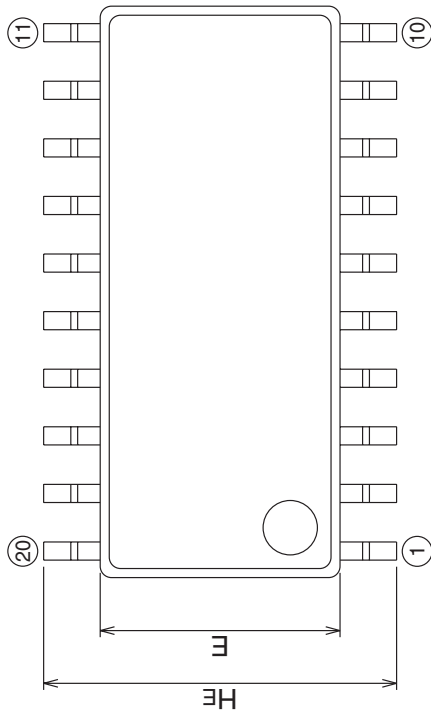
Package Dimensions

20P2N-A

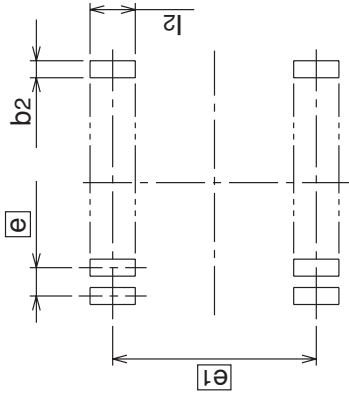
(MMP)

Plastic 20pin 300mil SOP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SOP20-P-300-1.27	—	0.26	Cu Alloy



Recommended Mount Pad



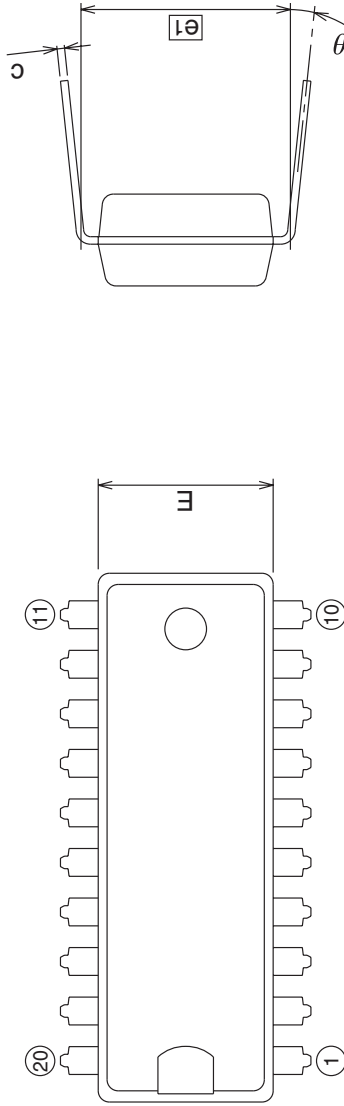
Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.1
A1	0	0.1	0.2
A2	—	1.8	—
b	0.35	0.4	0.5
c	0.18	0.2	0.25
D	12.5	12.6	12.7
E	5.2	5.3	5.4
e	—	1.27	—
HE	7.5	7.8	8.1
L	0.4	0.6	0.8
L1	—	1.25	—
L2	—	0.585	—
Z1	—	—	0.735
x	—	—	0.25
y	—	—	0.1
theta	0°	—	8°
b2	—	0.76	—
e1	—	7.62	—
l2	1.27	—	—

20P4B

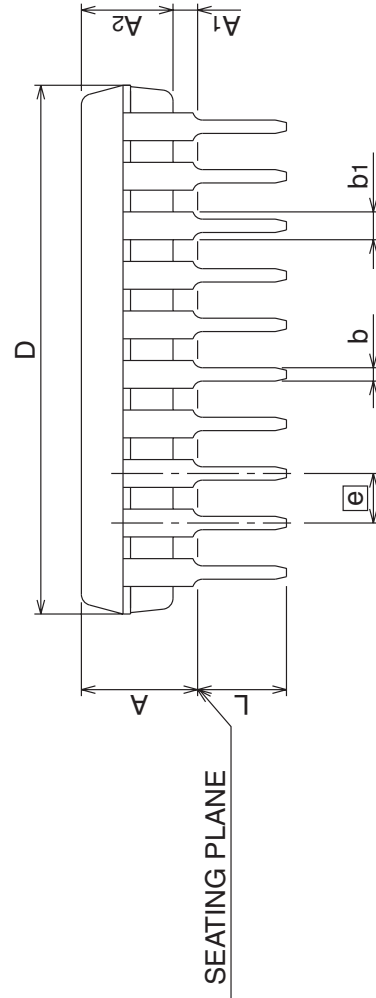
MMP

Plastic 20pin 300mil SDIP

EIAJ Package Code	JEDEC Code	Weight(g)	Lead Material
SDIP20-P-300-1.78	—	1.0	Alloy 42/Cu Alloy



Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	4.5
A1	0.51	—	—
A2	—	3.3	—
b	0.38	0.48	0.58
b1	0.9	1.0	1.3
c	0.22	0.27	0.34
D	18.8	19.0	19.2
E	6.15	6.3	6.45
e	—	1.778	—
e1	—	7.62	—
L	3.0	—	—
theta	0°	—	15°



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