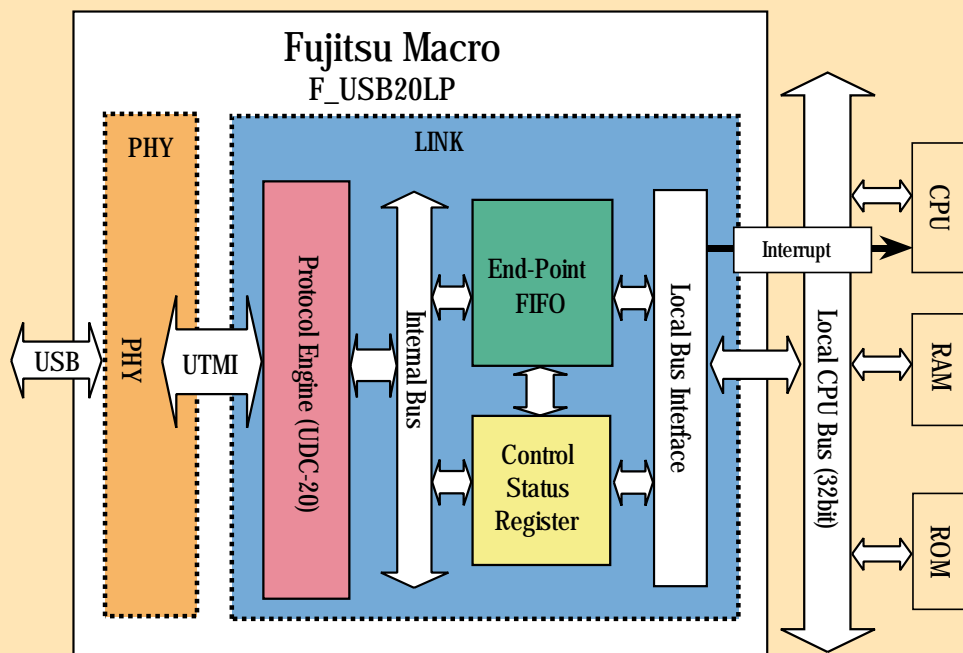


# Standard Bus IP: High Speed USB 2.0 Device Controller



## Features

- Full compliance with USB 2.0 Device Controller standard
- Integrated PHY macro for system cost reduction and space saving
- Supports high-speed (480Mbps) and full-speed (12Mbps)
- Customize endpoint numbers and configurations
- UTMI (USB2.0 Transceiver Macrocell Interface)

## Overview

Fujitsu USB 2.0 device controller is a synthesizable core suitable for different process. Corresponding physical interface in 0.18um and 0.11um technology (supporting high and full speed operation) also available for integration.

Generic CPU interface makes it easy to be integrated into overall ASIC. Different endpoints are available for application such as printer, scanner, digital still camera, bluetooth devices, digital set top box, cable modems and PC Access Point to high speed wireless connectivity.

Integrated SIE performs synchronization pattern recognition, bit stuffing/ stripping, CRC check/ generation, serial/ parallel conversion, PID verification, address recognition and handshake evaluation/ response.

The macro decodes and handles standard USB commands. Device class specific command is passed on to the ASIC for further processing.

## Description

### Link

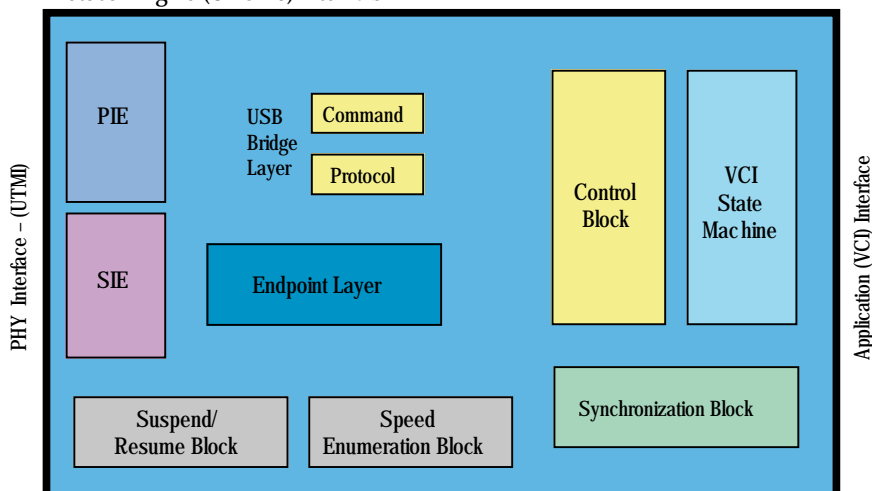
- Protocol Engine (UDC-20) is a fully synthesizable soft core that supports high-speed (480 Mbps), full-speed (12Mbps) signaling bit rates.
- Protocol engine reduces CPU burden by processing basic USB 2.0 protocols in hardware.
- Endpoint numbers, configurations, and its FIFO densities are flexible. Following is one of the configuration examples.

1) End Point 0	control out	64Byte
2) End Point 0	control in	64Byte
3) End Point 1	Bulk out	512Byte (Double buffer)
4) End Point 2	Bulk in	512Byte (Double buffer)
5) End Point 3	Interrupt in	64Byte

### PHY

- PHY block consists of a 0.18um hard macro and a soft macro (Receiving Block).
- PHY block supports high-speed (480Mbps) and full-speed (12Mbps).
- Contains high-speed Analog Blocks and high-speed SERDES (serializer and de-serializer Logic) and provides a parallel interface to UDC-20 protocol Engine.
- 16bit parallel connection to Link

Protocol Engine (UDC-20) Internals



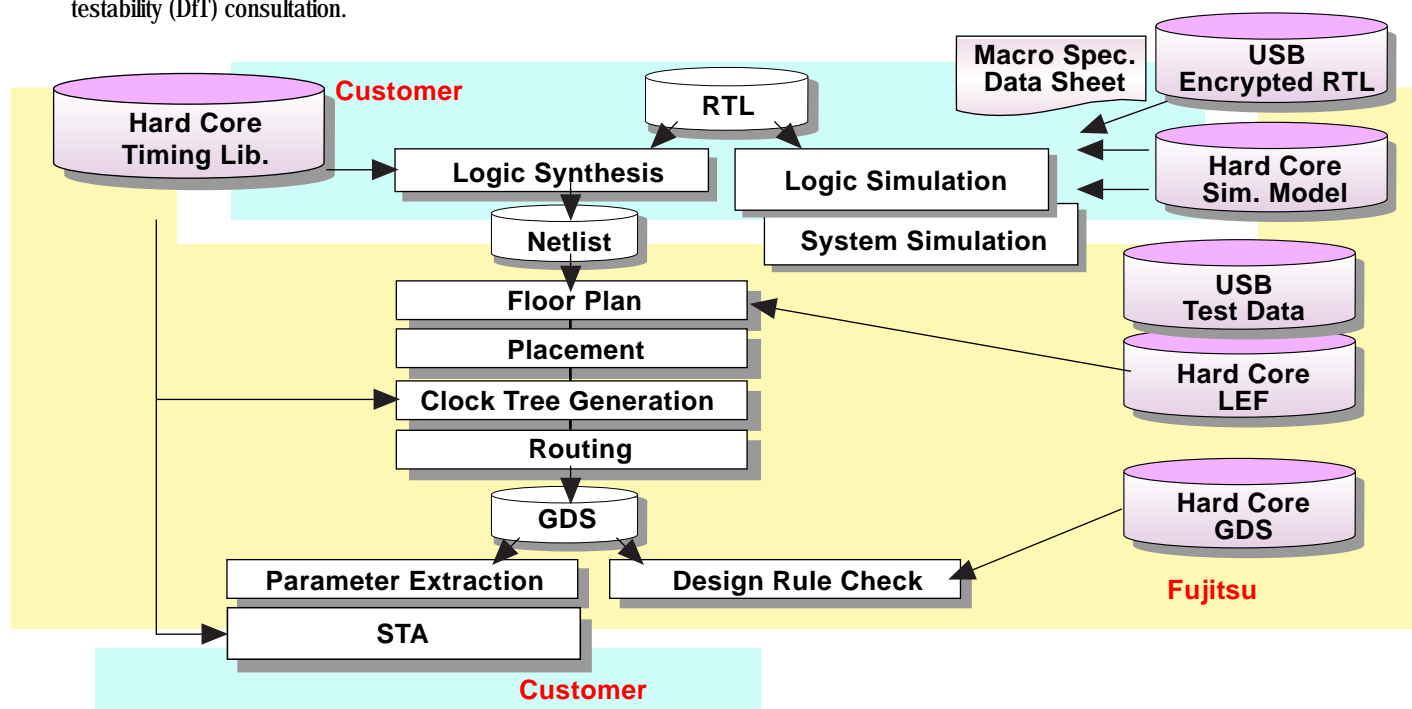
### ASIC Development Support

Fujitsu provide analog macro to supplement ASIC development, such as USB transceiver, and APLL (various speed combinations). Accurate timing model is provided for synthesis, simulation and Static Timing Analysis (STA).

Small gate count and soft coach approach makes it efficient to integrate into an ASIC. Fujitsu provides a set of functional vectors to customer for module hand-shake and full chip verification. Our application engineer works with you on full chip design for testability (DfT) consultation.

### Deliverables:

- USB test chip with selectable configurations,
- Test chip and macro specifications
- Encrypted RTL for top level simulation
- Application notes and testability guide
- Test benches for standalone IP verifications



[www.fmal.fujitsu.com](http://www.fmal.fujitsu.com)

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