

NDP04N50Z, NDD04N50Z

N-Channel Power MOSFET 500 V, 2.7 Ω

Features

- Low ON Resistance
- Low Gate Charge
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	NDP	NDD	Unit
Drain-to-Source Voltage	V_{DS}	500		V
Continuous Drain Current $R_{\theta JC}$	I_D	3.4	3.0	A
Continuous Drain Current $R_{\theta JC}$, $T_A = 100^\circ\text{C}$	I_D	2.1	1.9	A
Pulsed Drain Current, $V_{GS} @ 10\text{ V}$	I_{DM}	14	12	A
Power Dissipation $R_{\theta JC}$	P_D	75	61	W
Gate-to-Source Voltage	V_{GS}	± 30		V
Single Pulse Avalanche Energy, $I_D = 3.4\text{ A}$	E_{AS}	120		mJ
ESD (HBM) (JESD22-A114)	V_{esd}	2800		V
Peak Diode Recovery	dv/dt	4.5 (Note 1)		V/ns
Continuous Source Current (Body Diode)	I_S	3.4		A
Maximum Temperature for Soldering Leads	T_L	260		$^\circ\text{C}$
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

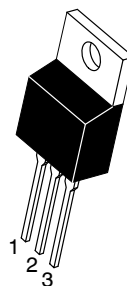
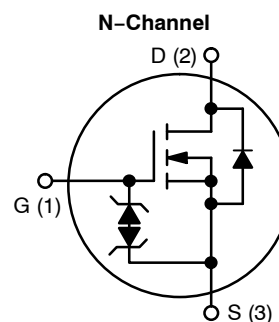
1. $I_D \leq 3.4\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DS}$, $T_J \leq 150^\circ\text{C}$.



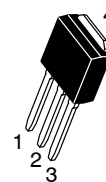
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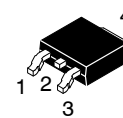
V_{DS}	$R_{DS(on)} (MAX) @ 1.5\text{ A}$
500 V	2.7 Ω



TO-220AB
CASE 221A
STYLE 5



IPAK
CASE 369D
STYLE 2



DPAK
CASE 369AA
STYLE 2

MARKING AND ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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THERMAL RESISTANCE

2. Insertion mounted

3. Surface mounted on FR4 board using 1" sq. pad size, (Cu area = 1.127 in sq [2 oz] including traces).

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Characteristic	Symbol	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	BV_{DSS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	500			V
Breakdown Voltage Temperature Coefficient	$\Delta BV_{DSS} / \Delta T_J$	Reference to 25°C , $I_D = 1\text{ mA}$		0.6		V/°C
Drain-to-Source Leakage Current	I_{DSS}	$V_{DS} = 500\text{ V}, V_{GS} = 0\text{ V}$	25°C		1	μA
			150°C		50	
Gate-to-Source Forward Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$			±10	μA

ON CHARACTERISTICS (Note 4)

Static Drain-to-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 1.5\text{ A}$		2.3	2.7	Ω
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 50\text{ μA}$	3.0		4.5	V
Forward Transconductance	g_{FS}	$V_{DS} = 15\text{ V}, I_D = 1.5\text{ A}$		2.1		S

DYNAMIC CHARACTERISTICS

Input Capacitance	C_{iss}	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V},$ $f = 1.0\text{ MHz}$		308		pF
Output Capacitance	C_{oss}			43		
Reverse Transfer Capacitance	C_{rss}			9		
Total Gate Charge	Q_g	$V_{DD} = 250\text{ V}, I_D = 3.4\text{ A},$ $V_{GS} = 10\text{ V}$		12		nC
Gate-to-Source Charge	Q_{gs}			2.6		
Gate-to-Drain ("Miller") Charge	Q_{gd}			6.1		
Plateau Voltage	V_{GP}			6.6		V
Gate Resistance	R_g			5.4		Ω

RESISTIVE SWITCHING CHARACTERISTICS

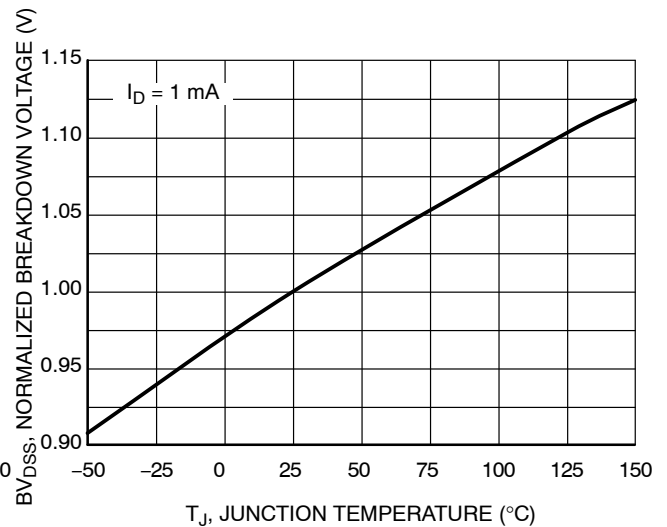
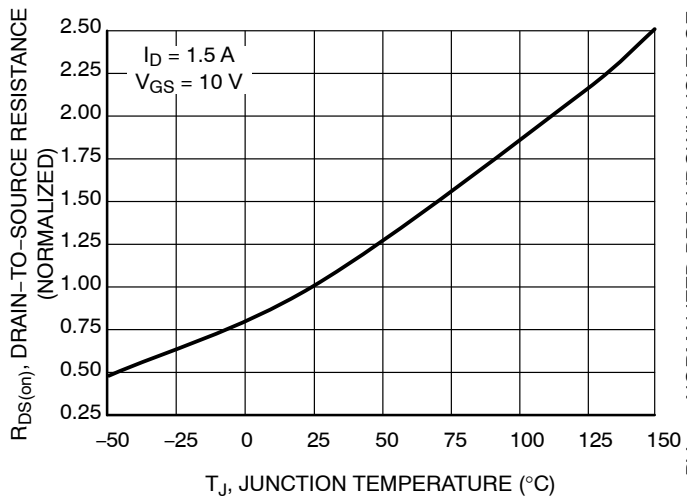
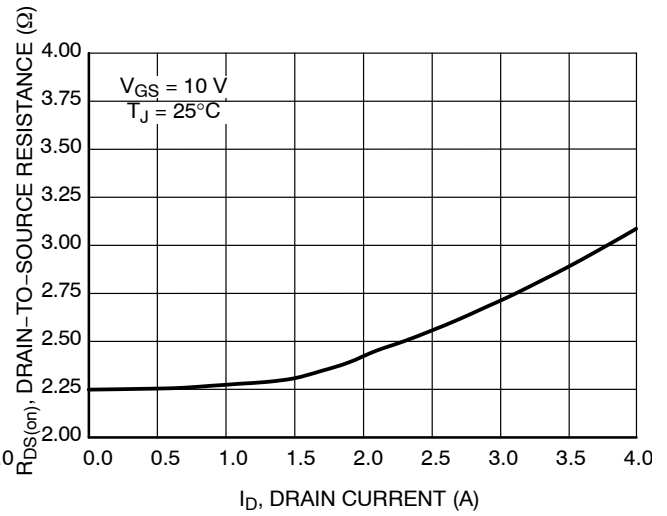
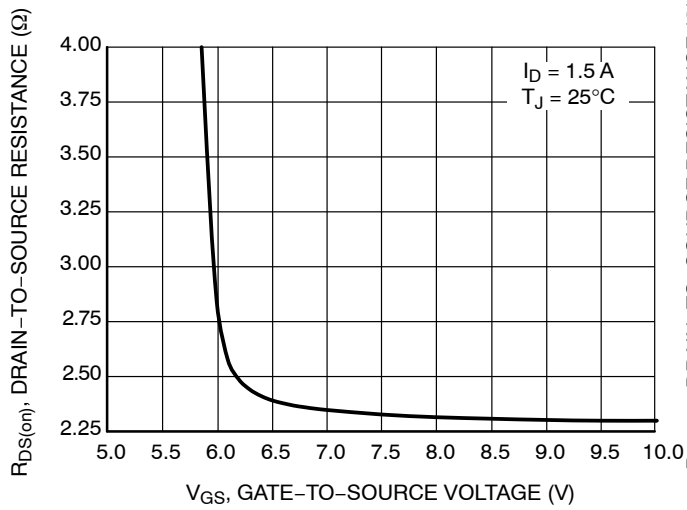
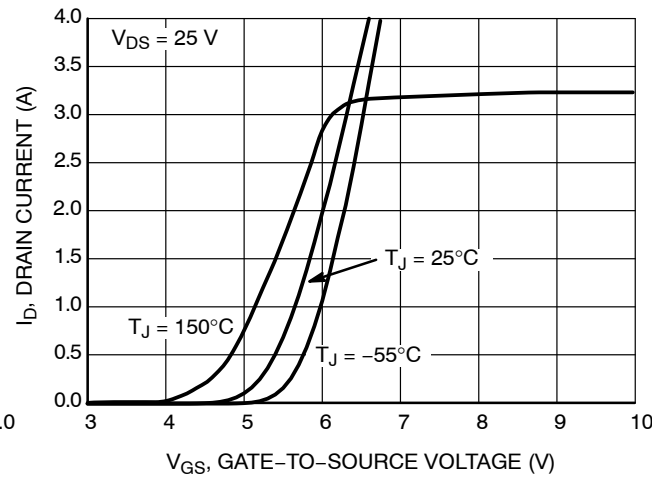
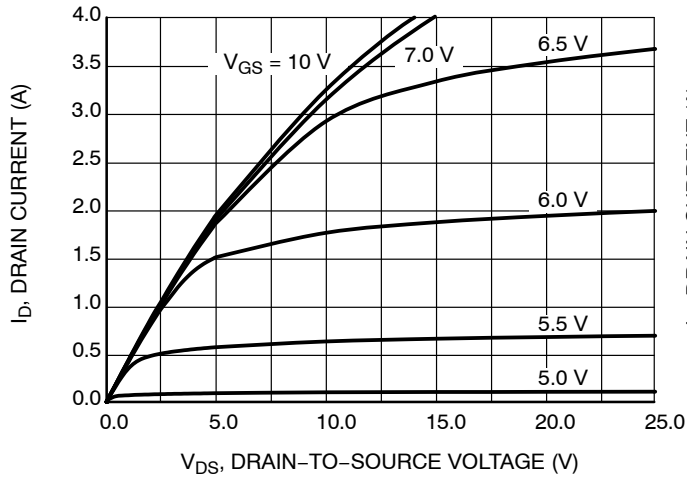
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 250\text{ V}, I_D = 3.4\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 5\text{ Ω}$		9		ns
Rise Time	t_r			9		
Turn-Off Delay Time	$t_{d(off)}$			16		
Fall Time	t_f			10		

SOURCE-DRAIN DIODE CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Diode Forward Voltage	V_{SD}	$I_S = 3.4\text{ A}, V_{GS} = 0\text{ V}$			1.6	V
Reverse Recovery Time	t_{rr}	$V_{GS} = 0\text{ V}, V_{DD} = 30\text{ V}$ $I_S = 3.4\text{ A}, di/dt = 100\text{ A/μs}$		240		ns
Reverse Recovery Charge	Q_{rr}			0.9		μC

4. Pulse Width ≤ 380 μs, Duty Cycle ≤ 2%.

NDP04N50Z, NDD04N50Z



NDP04N50Z, NDD04N50Z

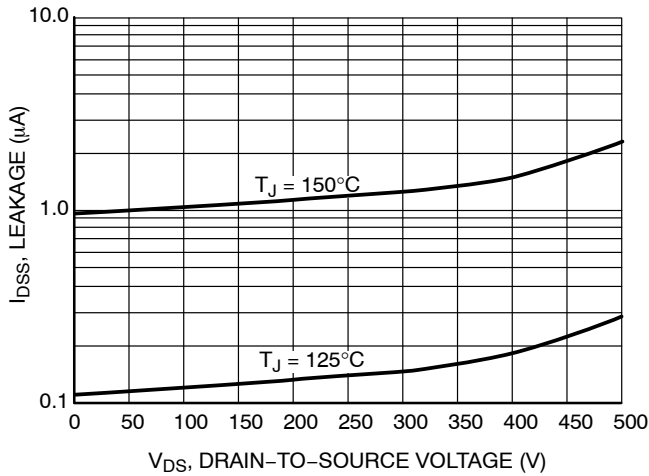


Figure 7. Drain-to-Source Leakage Current versus Voltage

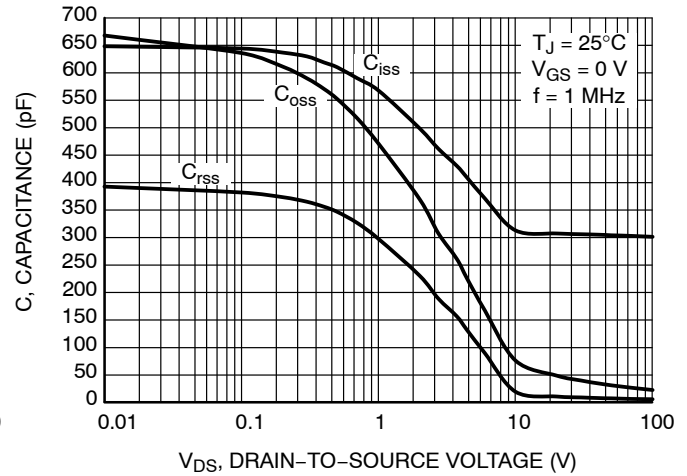


Figure 8. Capacitance Variation

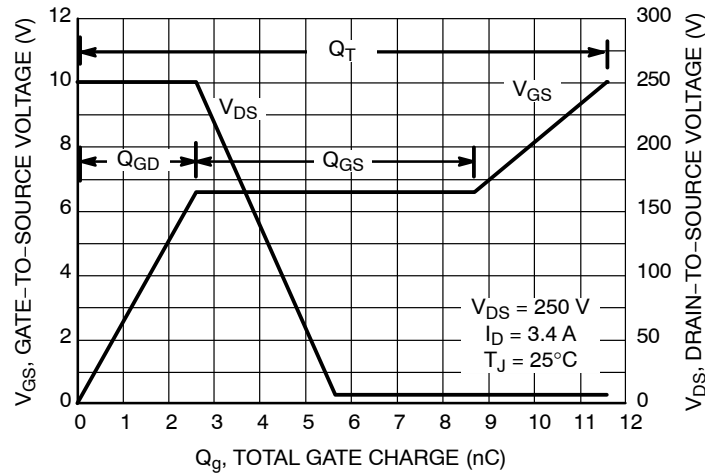


Figure 9. Gate-to-Source Voltage and Drain-to-Source Voltage versus Total Charge

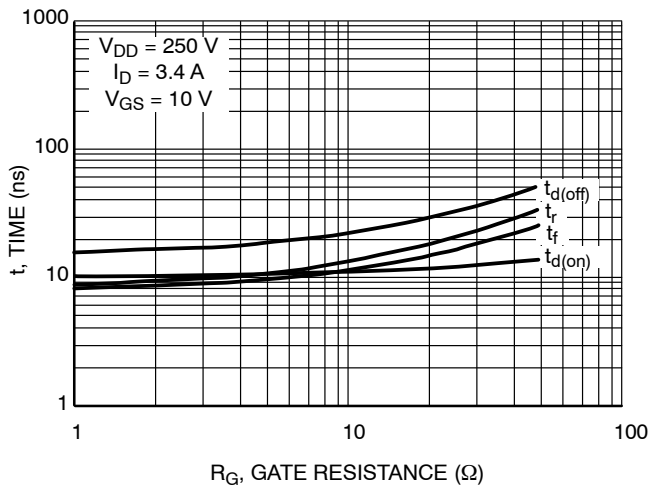


Figure 10. Resistive Switching Time Variation versus Gate Resistance

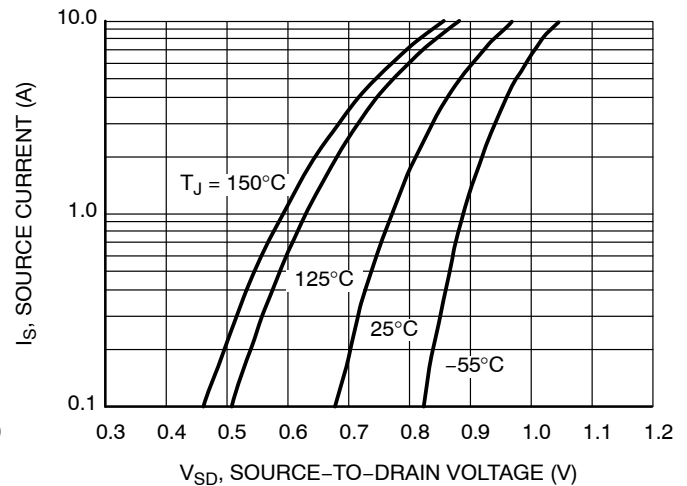


Figure 11. Diode Forward Voltage versus Current

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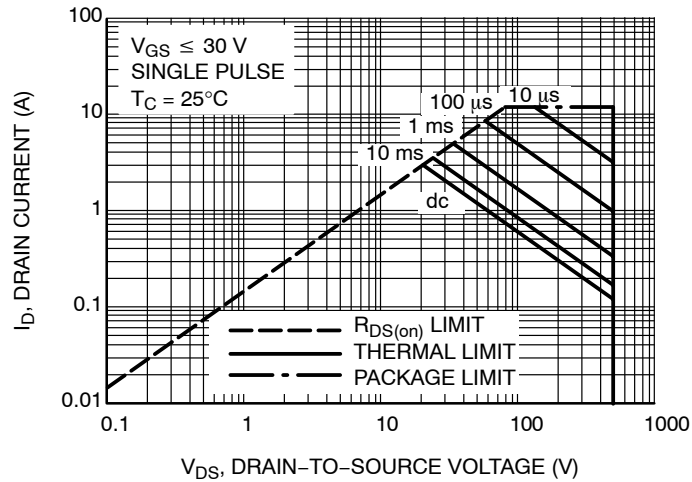


Figure 12. Maximum Rated Forward Biased Safe Operating Area NDD04N50Z

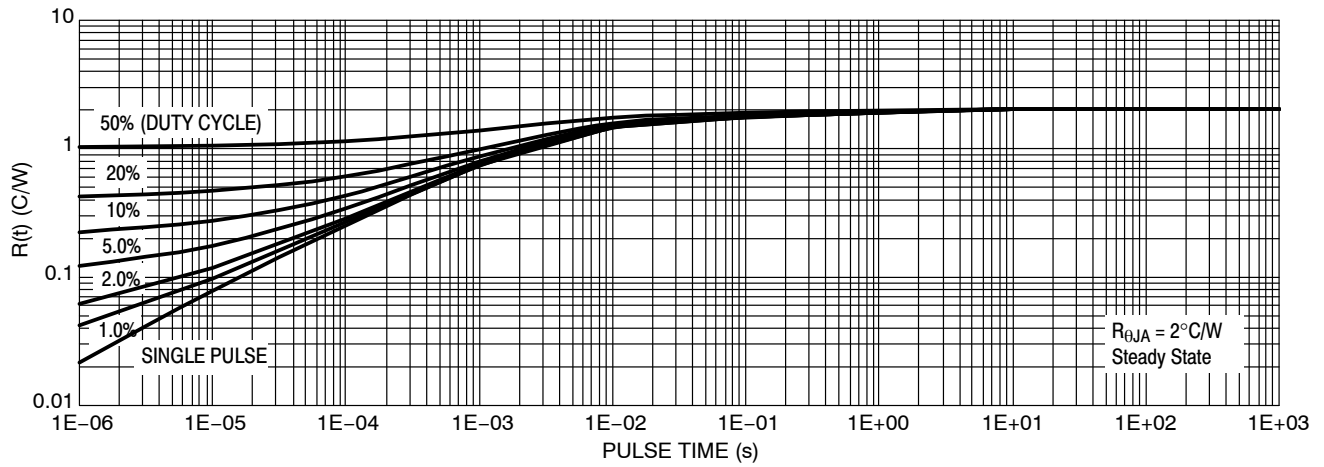


Figure 13. Thermal Impedance (Junction-to-Case) for NDD04N50Z

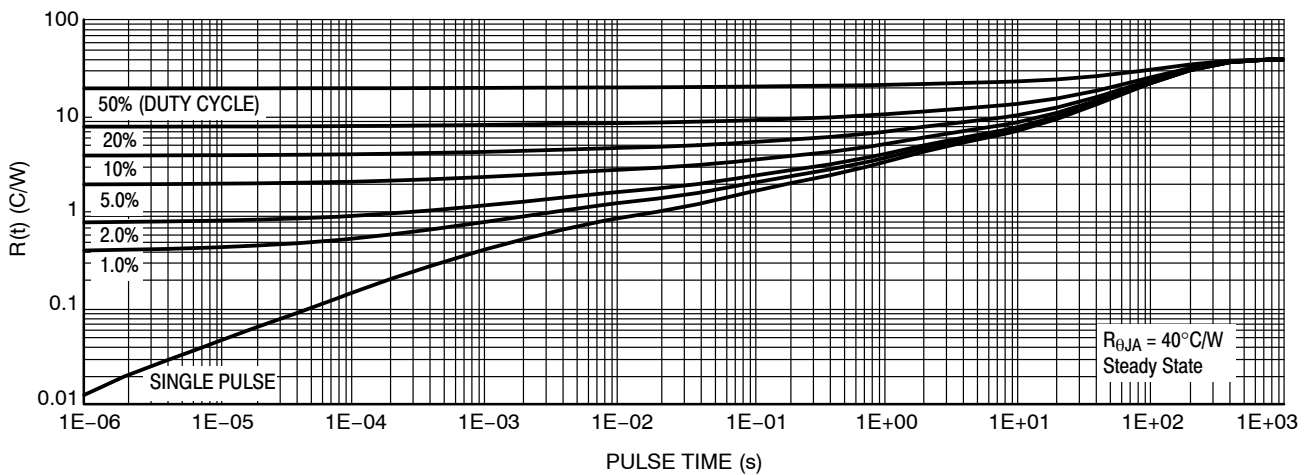


Figure 14. Thermal Impedance (Junction-to-Ambient) for NDD04N50Z

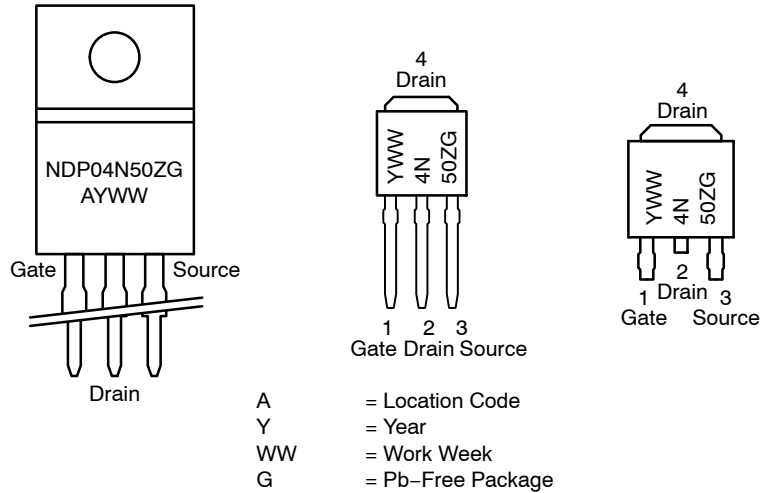
NDP04N50Z, NDD04N50Z

ORDERING INFORMATION

Order Number	Package	Shipping†
NDP04N50ZG	TO-220AB (Pb-Free)	50 Units / Rail (In Development)
NDD04N50Z-1G	IPAK (Pb-Free)	75 Units / Rail
NDD04N50ZT4G	DPAK (Pb-Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

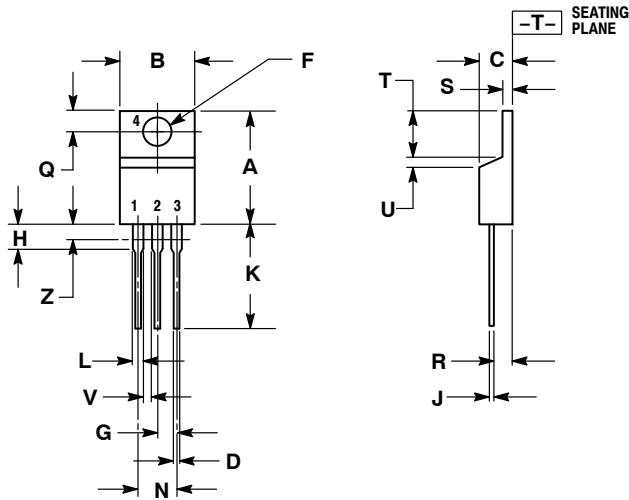
MARKING DIAGRAMS



NDP04N50Z, NDD04N50Z

PACKAGE DIMENSIONS

TO-220
CASE 221A-09
ISSUE AF



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.
 3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

- STYLE 5:
- PIN 1. GATE
 2. DRAIN
 3. SOURCE
 4. DRAIN

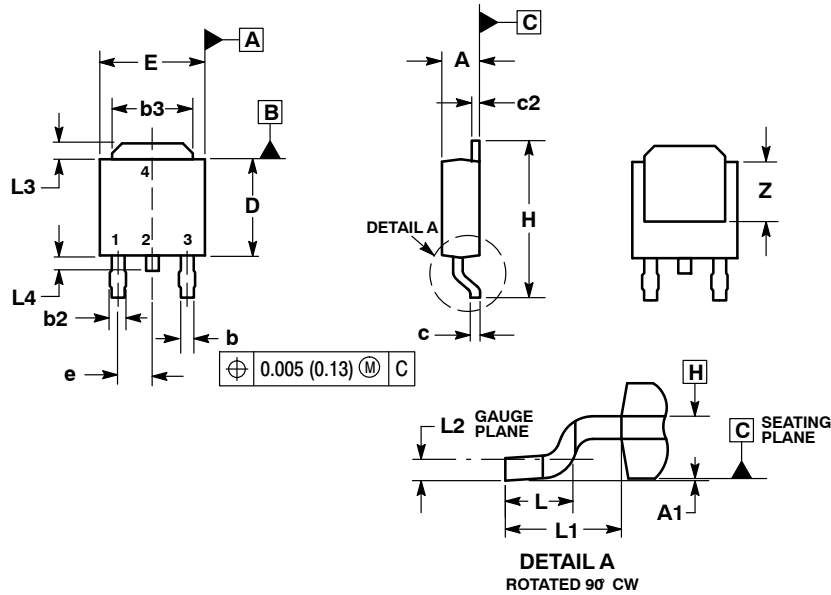
NDP04N50Z, NDD04N50Z

PACKAGE DIMENSIONS

DPAK (SINGLE GUAGE)

CASE 369AA-01

ISSUE B

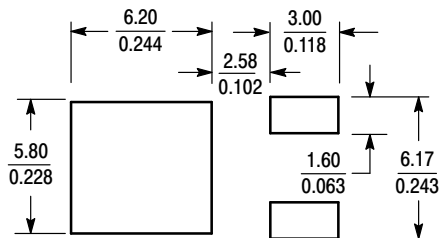


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

SOLDERING FOOTPRINT*



SCALE 3:1 ($\frac{\text{mm}}{\text{inches}}$)

STYLE 2:

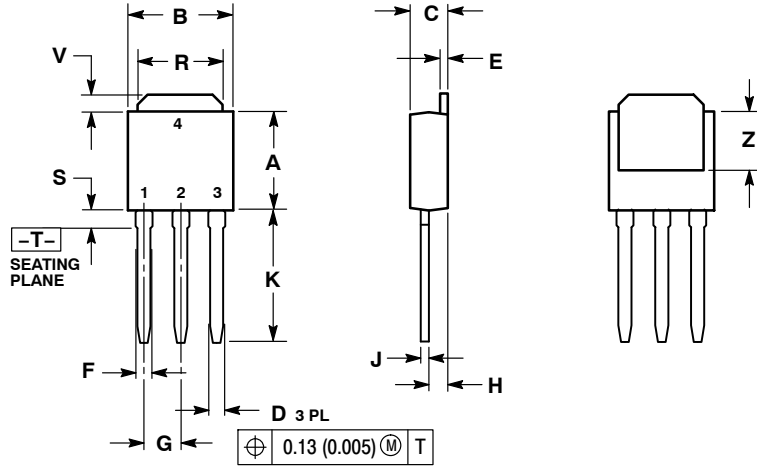
- PIN 1. GATE
- DRAIN
- SOURCE
- DRAIN

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NDP04N50Z, NDD04N50Z

PACKAGE DIMENSIONS

IPAK CASE 369D-01 ISSUE B



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.235	0.245	5.97	6.35
B	0.250	0.265	6.35	6.73
C	0.086	0.094	2.19	2.38
D	0.027	0.035	0.69	0.88
E	0.018	0.023	0.46	0.58
F	0.037	0.045	0.94	1.14
G	0.090	BSC	2.29	BSC
H	0.034	0.040	0.87	1.01
J	0.018	0.023	0.46	0.58
K	0.350	0.380	8.89	9.65
R	0.180	0.215	4.45	5.45
S	0.025	0.040	0.63	1.01
V	0.035	0.050	0.89	1.27
Z	0.155	---	3.93	---

- STYLE 2:
- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

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