SINGLE SYNCHRONOUS STEP-DOWN CONTROLLER FOR LOW VOLTAGE POWER RAILS

FEATURES

- **High Efficiency, Low-Power Consumption**
- **D-CAP2™ Mode Enables Fast Transient Response**
- **No external parts required for loop compensation**
- **Allows Ceramic Output Capacitor**
- **Integrated Enable Pin to Select POSCAP or Ceramic Capacitor (MLCC) Use**
- **High Initial Reference Accuracy**
- **Low Output Ripple**
- **Wide Input Voltage Range: 4.5V to 24V**
- **Output Voltage Range: 0.76V to 5.5V**
- **Low-Side $R_{DS(on)}$ Loss-less Current Sensing**
- **Adaptive Gate Drivers with Integrated Boost Diode**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **Selectable Switching frequency 350kHz/700kHz**
- **Built-In 5V Linear Regulator**

APPLICATIONS

- **Point-of-load regulation in low power systems for wide range of applications**
  - **Digital TV Power Supply**
  - **Networking Home Terminal**
  - **Digital Set Top Box (STB)**
  - **DVD player / recorder**
  - **Gaming consoles and other**

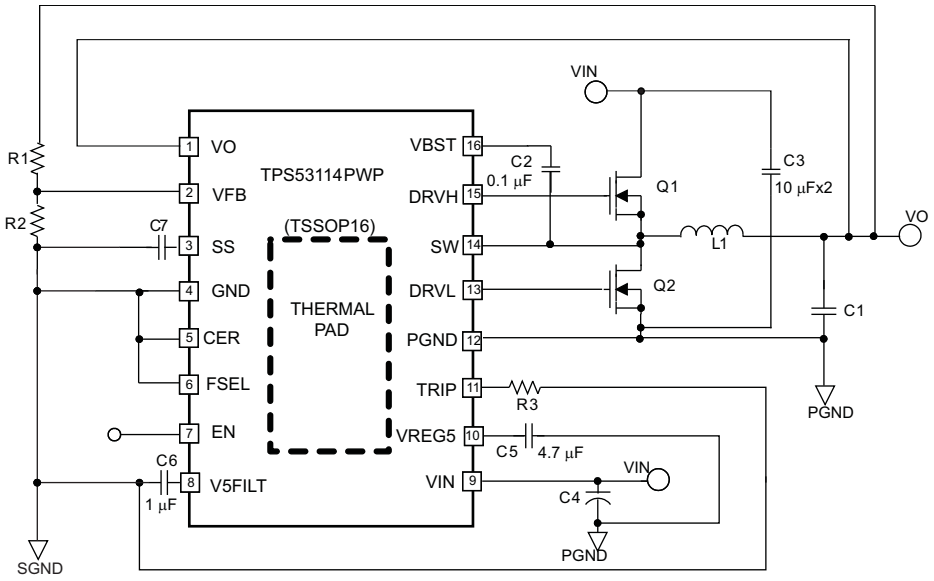
DESCRIPTION

The TPS53114 is a single, adaptive on-time D-CAP2™ mode synchronous buck controller. The part enables system designers to cost effectively complete the suite of various end equipment's power bus regulators with a low external component count and low standby consumption. The main control loop for the TPS53114 uses the D-CAP2™ mode topology which provides a very fast transient response with no external components. The TPS53114 also has a **PROPRIETARY** circuit that enables the device to adapt to not only low equivalent series resistance (ESR) output capacitors such as POSCAP/SP-CAP, but also ceramic using the CER pin. The part provides convenient and efficient operation with conversion voltages from 4.5V to 24V and output voltage from 0.76V to 5.5V.

The TPS53114 is available in the 16 pin TSSOP package, and is specified from –40°C to 85°C temperature range.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

TYPICAL APPLICATION CIRCUIT



ORDERING INFORMATION

T_A	PACKAGE	ORDERING PART NUMBER	PINS	OUTPUT SUPPLY	ECO PLAN
–40°C to 85°C	HTSSOP（Thermal Pad）	TPS53114PWPR	16	Tape-and-Reel	Green (RoHS & no Sb/Br)
		TPS53114PWP		Tube	

ABSOLUTE MAXIMUM RATINGS

Operating under free-air temperature range (unless otherwise noted) (1)

			VALUE	UNIT
	Input voltage range	VIN, EN	–0.3 to 26	V
		VBST	–0.3 to 32	
		VBST(wrt SW)	–0.3 to 6	
		V5FILT, VFB, TRIP, VO, FSEL, CER	–0.3 to 6	
		SW	–2 to 26	
	Output voltage range	DRVH	–1 to 32	V
		DRVH (wrt SW)	–0.3 to 6	
		DRVL, VREG5, SS	–0.3 to 6	
		PGND	–0.3 to 0.3	
T_A	Operating ambient temperature range		–40 to 85	°C
T_{STG}	Storage temperature range		–55 to 150	
T_J	Junction temperature range		–40 to 150	

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

DISSIPATION RATING TABLE (2 oz. trace and copper pad with solder)

PACKAGE	T_A < 25°C POWER RATING	DERATING FACTOR ABOVE T_A = 25°C	T_A = 85°C POWER RATING
16 pin HTSSOP(PWP)	2.73W	16.4mW/°C	1.09W

RECOMMENDED OPERATING CONDITIONS

		MIN	MAX	UNIT
Supply input voltage range	VIN	4.5	24	V
	V5FILT	4.5	5.5	
Input voltage range	VBST	–0.1	30	V
	VBST (wrt SW)	–0.1	5.5	
	VFB, VO, FSEL, CER	–0.1	5.5	
	TRIP	–0.1	0.3	
	EN	–0.1	24	
	SW	-1.8	24	
Output Voltage range	DRVH	–0.1	30	V
	VBST (wrt SW)	–0.1	5.5	
	DRVL, VREG5, SS	–0.1	5.5	
	PGND	–0.1	0.1	
T_A Operating free-air temperature		–40	85	°C
T_J Operating junction temperature		–40	125	

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	VIN supply current	VIN current, T_A = 25°C, VREG5 tied to V5FLT, EN = 5V, VFB = 0.8V, SW = 0.5V		350	600	µA
I_{VINSDN}	VIN shutdown current	VIN current, T_A = 25°C, No Load , EN = 0V, VREG5 = ON		28	60	µA
VFB VOLTAGE and DISCHARGE RESISTANCE						
V_{BG}	Bandgap Initial regulation accuracy	T_A = 25°C	–1.0		1.0	%
V_{VFBTHL}	VFB threshold voltage	T_A = 25°C , FSEL = 0 V, CER = V5FILT	755	765	775	mV
		T_A = –40°C to 85°C, FSEL = 0V, CER = V5FILT	752		778	
V_{VFBTHH}	VFB threshold voltage	T_A = 25°C , FSEL = CER = V5FILT	748	758	768	mV
		T_A = –40°C to 85°C, FSEL = CER = V5FILT	745		771	
I_{VFB}	VFB Input Current	VFB = 0.8V, T_A = 25°C		–0.01	±0.1	µA
R_{Dischg}	Vo Discharge Resistance	EN = 0V, VO = 0.5V, T_A = 25°C		40	80	Ω
VREG5 OUTPUT						
V_{VREG5}	VREG5 Output Voltage	T_A=25°C, 5.5V < VIN < 24V, 0 < I_{VREG5} < 10mA	4.8	5.0	5.2	V
V_{LN5}	Line regulation	5.5V < VIN < 24V, I_{VREG5} = 10mA			20	mV
V_{LD5}	Load regulation	1mA < I_{VREG5} < 10mA			40	mV
I_{VREG5}	Output current	VIN = 5.5V, V_{VREG5} = 4.0V, T_A = 25°C		170		mA
OUTPUT: N-CHANNEL MOSFET GATE DRIVERS						
R_{DRVH}	DRVH resistance	Source, I_{DRVH} = –100mA		5.5	11	Ω
		Sink, I_{DRVH} = 100mA		2.5	5	
R_{DRVL}	DRVL resistance	Source, I_{DRVL} = –100mA		4	8	Ω
		Sink, I_{DRVL} = 100mA		2	4	

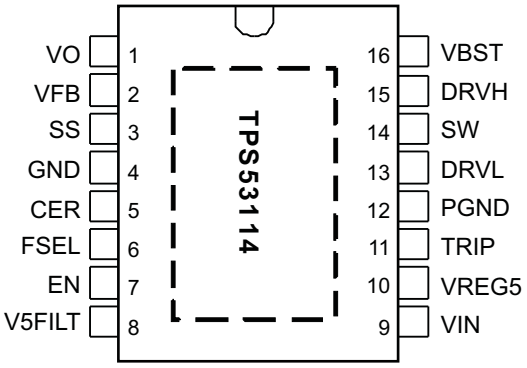
ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range, VIN = 12 V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
T_D	Dead time	DRVH-low to DRVL-on	20	50	80	ns
		DRVL-low to DRVH-on	20	40	80	
INTERNAL BST DIODE						
V_{FBST}	Forward Voltage	$V_{VREG5-VBST}$, IF = 10mA, T_A = 25°C	0.7	0.8	0.9	V
I_{VBSTLK}	VBST Leakage Current	VBST = 29V, SW = 24V, T_A = 25°C		0.1	1	µA
ON-TIME TIMER CONTROL						
T_{ONL}	On Time	SW = 12V, VO = 1.8V, FSEL = 0V		390		ns
T_{ONH}	On Time	SW = 12V, VO = 1.8V, FSEL = V5FILT		139		ns
T_{OFFL}	Min off time	SW = 0.7V, T_A = 25°C, VFB = 0.7V, FSEL = 0V		285		ns
T_{OFFH}	Min off time	SW = 0.7V, T_A = 25°C, VFB = 0.7V, FSEL = V5FILT		216		ns
SOFT START						
Issc	SS charge current	VSS = 0V , SOURCE CURRENT	1.4	2.0	2.6	µA
Issd	SS discharge current	VSS = 0.5V , SINK CURRRENT	0.1	0.15		mA
UVLO						
$V_{UV5VFILT}$	V5FILT UVLO threshold	Wake up	3.7	4.0	4.3	V
		Hysteresis	0.2	0.3	0.4	
LOGIC THRESHOLD						
V_{ENH}	EN H-level input voltage	EN	2.0			V
V_{ENL}	EN L-level input voltage	EN			0.3	V
CURRENT SENSE						
I_{TRIP}	TRIP source current	VTRIP = 0.1V, T_A = 25°C	8.5	10	11.5	µA
TC_{ITRIP}	I_{TRIP} temperature coefficient	on the basis of 25°C		4000		ppm/°C
V_{OCLoff}	OCP compensation offset	($V_{TRIP-GND}$-$V_{PGND-SW}$) voltage, $V_{TRIP-GND}$ = 60mV, T_A = 25°C	–10	0	10	mV
		($V_{TRIP-GND}$-$V_{PGND-SW}$) voltage, VTRIP-GND = 60mV	–15		15	mV
V_{Rtrip}	Current limit threshold setting range	$V_{TRIP-GND}$ voltage	30		200	mV
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
V_{OVP}	Output OVP trip threshold	OVP detect	110	115	120	%
T_{OVPDEL}	Output OVP prop delay			1.5		µs
V_{UVP}	Output UVP trip threshold	UVP detect	65	70	75	%
		Hysteresis (recovery <20µs)		10		%
T_{UVPDEL}	Output UVP delay		17	30	40	µs
T_{UVPEN}	Output UVP enable delay	UVP enable delay / softstart time	X1.4	X1.7	X2.0	
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature(1)		150		°C
		Hysteresis(1)		20		

(1) Ensured by design. Not production tested.

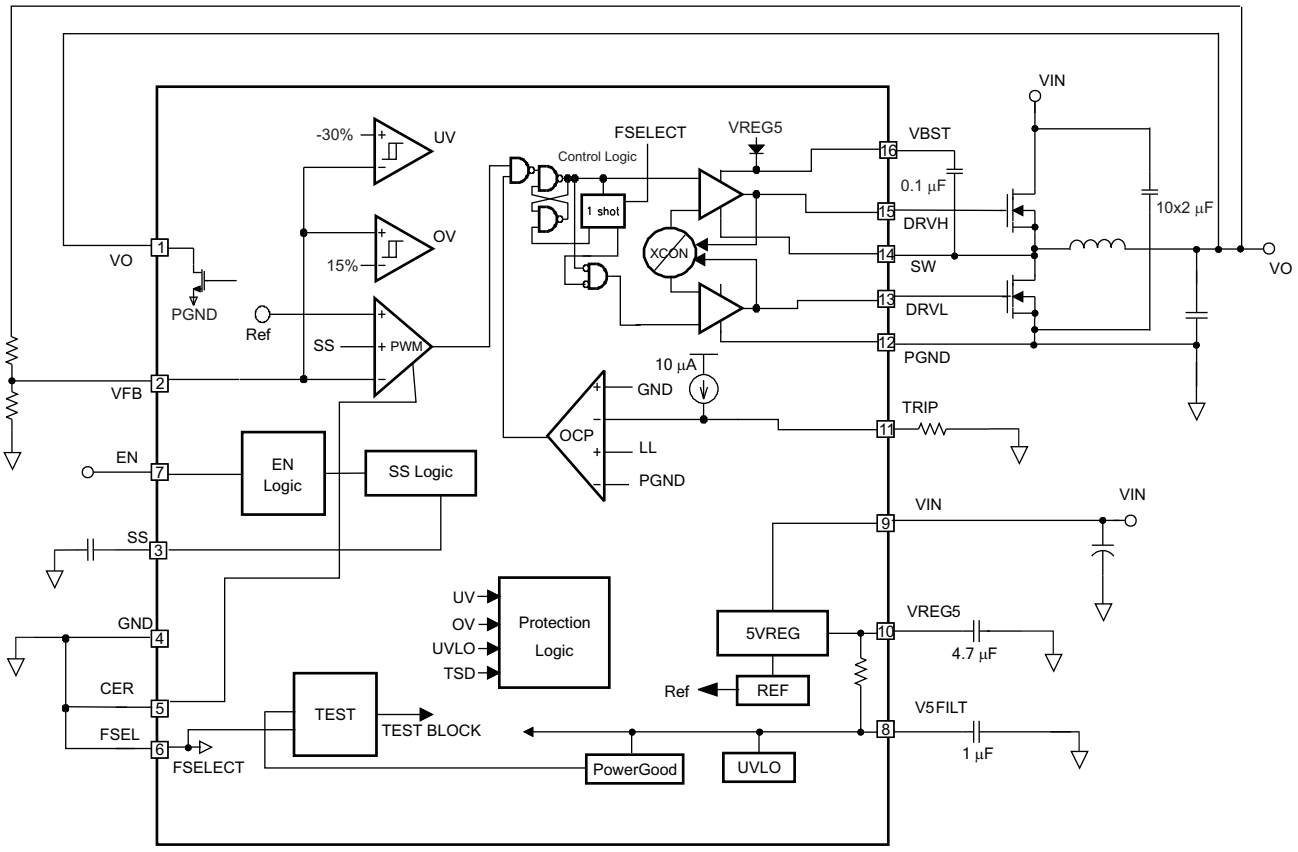
PIN ASSIGNMENT (TOP VIEW)



PIN FUNCTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
VBST	16	I	Supply input for high-side NFET driver (Boost Terminal). Connect capacitor from this pin to SW terminal. An internal PN diode is connected between VREG5 and VBST. User can add external schottky diode if forward drop is critical to drive the NFET.
EN	7	I	High level enable pin.
SS	3	O	Connect Capacitor from SS pin to GND.
VO	1	I	Connect to output of converter. This terminal is used for On-Time Adjustment and Output Discharge.
VFB	2	I	Converter feedback input. Connect with feedback resistor divider.
GND	4	I	Signal ground pin.
DRVH	15	O	High-side NFET driver output. SW referenced floating driver. The gate drive voltage is defined by the voltage across VBST to SW node capacitor.
SW	14	I/O	Switch node connections for high-side driver. Also serves as input to current comparator.
DRVL	13	O	Synchronous NFET driver output. PGND referenced driver. The gate drive voltage is defined by VREG5 voltage.
PGND	12	I/O	Ground return for DRVL. Also serves as input of current comparator. Connect PGND and GND together near the IC.
TRIP	11	I	Over current trip point set input. Connect resistor from this pin to GND to set threshold for synchronous FET $R_{DS(on)}$ sense. Voltage across this pin and GND is compared to voltage across PGND and SW by over current comparator.
VIN	9	I	Supply Input for 5V linear regulator.
V5FILT	8	I	5V supply input for the entire control circuit except the NFET driver. Connect Capacitor (typical 1uF) from GND to V5FILT. V5FILT is connected to VREG5 via internal resistor.
VREG5	10	O	5V power supply output. VREG5 is connected to V5FILT via internal resistor.
CER	5	I	Connect to GND for ceramic output capacitors. Connect to V5FILT for polymer electrolyte output capacitors (SP-CAP, POS-CAP, PXE).
FSEL	6	I	Switching frequency selection pin. Connect to GND for low switching frequency or connect to V5FILT for high switching frequency.

FUNCTIONAL BLOCK DIAGRAM



DETAILED DESCRIPTION

PWM OPERATION

The main control loop of the switching mode power supply (SMPS) is designed as an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ Mode. D-CAP2™ mode uses internal compensation circuit and it is suitable for low external component count configuration with appropriate amount of equivalent series resistance (ESR) at the output capacitor(s) and/or ceramic output capacitors. D-CAP2 mode topology integrates a ripple injection circuit to allow use of ceramic output capacitors without external components. It can be stable even if ripple voltage at the output, $VO_{(ripple)}$, is virtually zero. The output ripple valley voltage is monitored at a feedback point voltage.

At the beginning of each cycle, the synchronous high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. The one shot timer is determined by the converter's input voltage, VIN, and the output voltage, VO, to keep frequency fairly constant over the input voltage range, hence it is called adaptive on-time control. The high-side MOSFET is turned on again when the feedback information indicates insufficient output voltage. Repeating the MOSFET operation in this manner, the controller regulates the output voltage.

LOW-SIDE DRIVER

The low-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). The drive capability is represented by its internal resistance. To prevent shoot through, a dead time is internally generated between high-side MOSFET off to low-side MOSFET on, and low-side MOSFET off to high-side MOSFET on. 5V bias voltage is delivered from the internal regulator VREG5 output. The instantaneous drive current is supplied by a capacitor connected between VREG5 and GND. The average drive current is equal to the gate charge at Vgs=5V times switching frequency. This gate drive current as well as the high-side gate drive current times 5V approximates the driving power which is dissipated in the TPS53114 package.

HIGH-SIDE DRIVER

The high-side driver is designed to drive high current, low $R_{DS(on)}$ N-channel MOSFET(s). When configured as a floating driver, a 5V bias voltage is delivered from VREG5 supply. The average drive current is also calculated by the gate charge at Vgs=5V times switching frequency. The instantaneous drive current is supplied by the capacitor between VBST and SW pins. The drive capability is represented by its internal resistance.

PWM FREQUENCY AND ADAPTIVE ON-TIME CONTROL

The TPS53114 uses an adaptive on-time control scheme and does not have a dedicated on board oscillator; however, the device runs with pseudo-constant frequency by feed-forwarding the input and output voltage into the on-time one-shot timer. The on-time control is inversely proportional to the input voltage and proportional to the output voltage; therefore, the duty ratio is VO/VIN and has the same cycle time.

SOFT START AND PRE-BIASED SOFTSTART

The TPS53114 has an adjustable soft-start. When the EN pin becomes high, 2.0μA current begins charging the capacitor which is connected from SS pin to GND. Smooth control of the output voltage is maintained during start up.

The TPS53114 contains a unique circuit to prevent current from being pulled from the output during startup in the condition the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft-start becomes greater than feedback voltage [VFB]), the controller slowly activates synchronous rectification by starting the first DRVL pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensures that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

SWITCHING FREQUENCY SELECTION

Connect FSEL pin to GND for a switching frequency (f_{SW}) is 350kHz. Connect FSEL pin to V5FILT for a switching frequency (f_{SW}) is 700kHz.

OUTPUT DISCHARGE CONTROL

The TPS53114 discharges the outputs when EN is low, or the controller is turned off by the protection functions (OVP, UVP, UVLO, and thermal shutdown). The device discharges output using an internal 40-Ω MOSFET which is connected to VO and PGND. The external low-side MOSFET is not turned on during the output discharge operation to avoid the possibility of causing negative voltage at the output. This discharge ensures that, on start, the regulated voltage always initializes from zero volts.

CURRENT PROTECTION

The TPS53114 has cycle-by-cycle over current limiting control. The inductor current is monitored during the OFF state and the controller retains the OFF state when the inductor current is larger than the over current trip level. In order to provide both accuracy and cost effective solution, the device supports temperature compensated MOSFET $R_{DS(on)}$ sensing. The TRIP pin should be connected to GND through the trip voltage setting resistor, R_{trip}. The TRIP terminal provides 10μA (I_{trip}) of current at the ambient temperature and the trip level is set to the OCL trip voltage (V_{trip}) as follows.

$$V_{trip}(mV) = R_{trip}(k\Omega) \times 10(\mu A) \quad (1)$$

The trip level is in the range of 30mV to 200mV over all operational temperatures. The inductor current is monitored by the voltage between PGND pin and SW pin. I_{trip} has 4000ppm/°C temperature slope to compensate the temperature dependency of $R_{DS(on)}$. PGND is used as the positive current sensing node so that PGND is connected to the source terminal of the bottom MOSFET. As the comparison is done during the OFF state, V_{trip} sets the valley level of the inductor current; therefore, the load current at over current threshold, I_{ocp}, can be calculated as follows:

$$I_{ocp} = V_{trip}/R_{DS(on)} + I_{L1(ripple)}/2 = \frac{V_{trip}}{R_{DS(on)}} + \frac{1}{2 \times L1 \times f_{sw}} \times \frac{(V_{IN} - VO) \times VO}{V_{IN}} \quad (2)$$

In an over current condition, the current to the load exceeds the current to the output capacitor; thus, the output voltage tends to fall off. Eventually, it will cross the under voltage protection threshold and shutdown.

OVER/UNDER VOLTAGE PROTECTION

The TPS53114 monitors a resistor divided feedback voltage to detect over and under voltages. When the feedback voltage becomes higher than 115% of the target voltage, the OVP comparator output goes high and the circuit latches the high-side MOSFET driver turns off and the low-side MOSFET driver turns on.

When the feedback voltage becomes lower than 70% of the target voltage, the UVP comparator output goes high and an internal UVP delay counter begins. After 30us, the TPS53114 latches off both top and bottom MOSFET drivers. This function is enabled approximately 2.0ms after power-on. The latch off is reset when EN pin goes low.

UVLO PROTECTION

The TPS53114 has under voltage lock out protection (UVLO) that monitors the voltage of V5FILT pin. When the V5FILT voltage is lower than UVLO threshold voltage, the device is shut off. The UVLO protection is a non-latch protection.

THERMAL SHUTDOWN

If the temperature exceeds the threshold value (typically 150°C), the drivers will be shut off both DRVH and DRVL are set low, the output discharge function is enabled and the device is shut off. Thermal shutdown is a non-latch protection.

TYPICAL CHARACTERISTICS

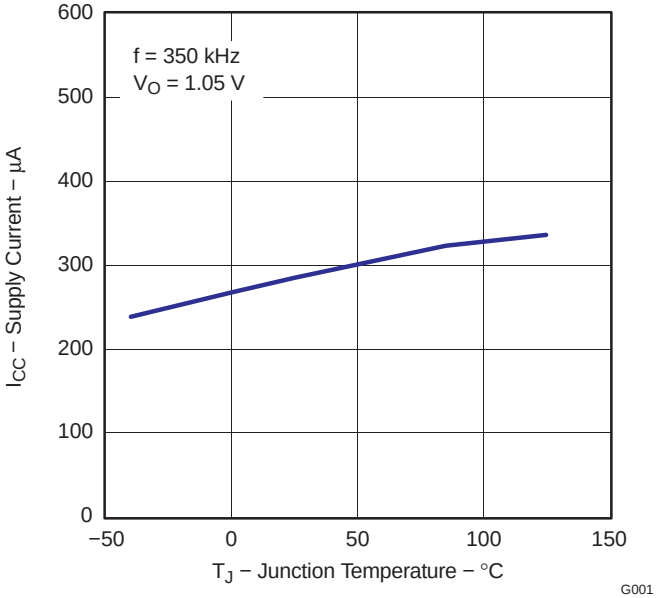


Figure 1. VIN SUPPLY CURRENT vs. JUNCTION TEMPERATURE

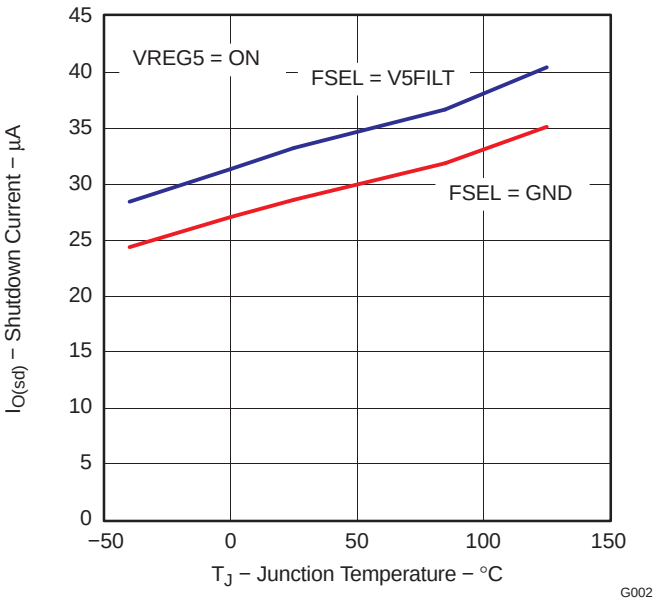


Figure 2. VIN SHUTDOWN CURRENT vs. JUNCTION TEMPERATURE

TYPICAL CHARACTERISTICS (continued)

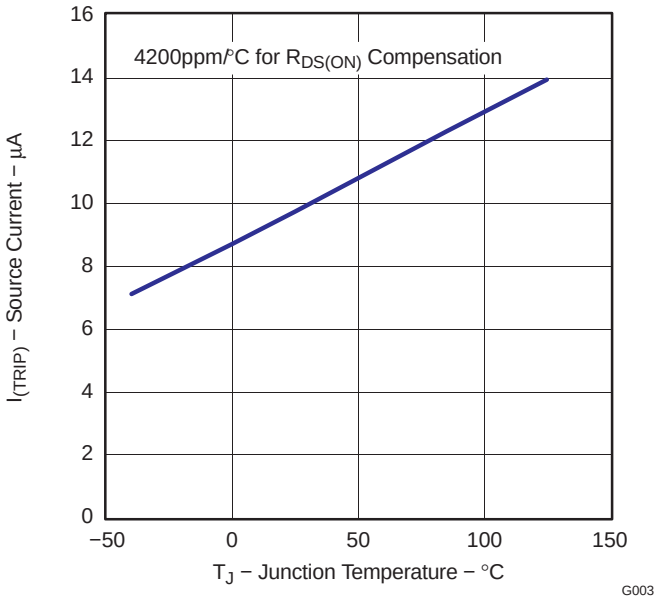


Figure 3. TRIP SOURCE CURRENT vs. JUNCTION TEMPERATURE

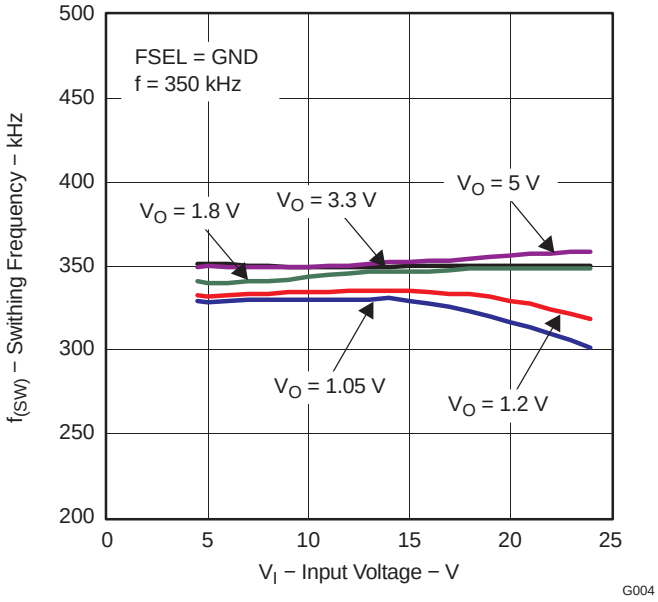


Figure 4. SWITCHING FREQUENCY (I_O = 1 A) vs. INPUT VOLTAGE

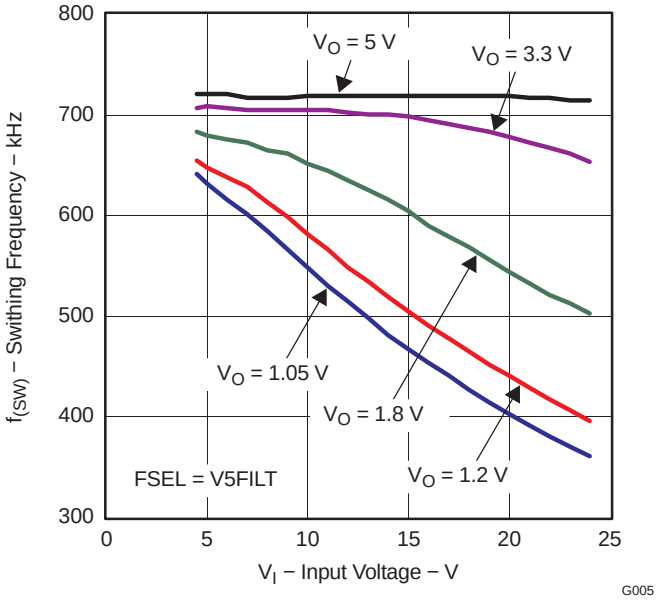


Figure 5. SWITCHING FREQUENCY vs. INPUT VOLTAGE

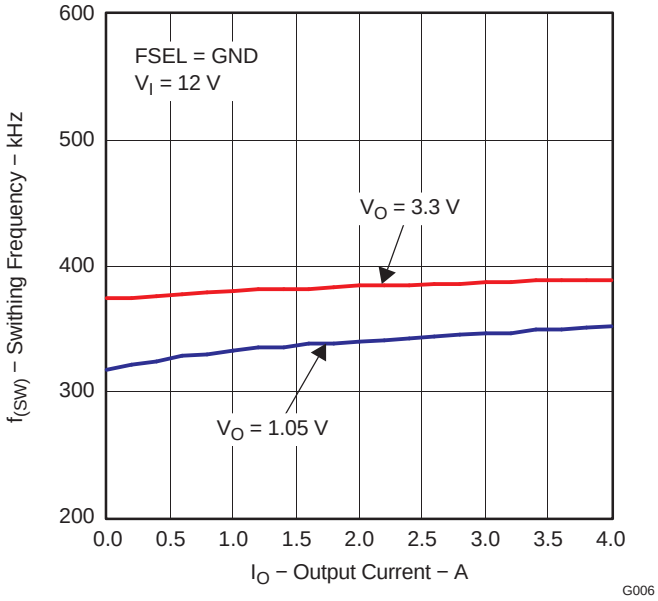


Figure 6. SWITCHING FREQUENCY vs. OUTPUT CURRENT

TYPICAL CHARACTERISTICS (continued)

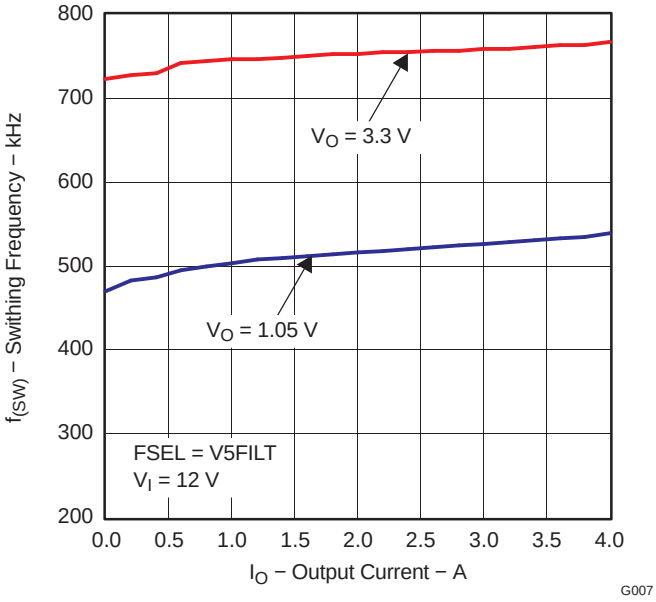


Figure 7. SWITCHING FREQUENCY vs. OUTPUT CURRENT

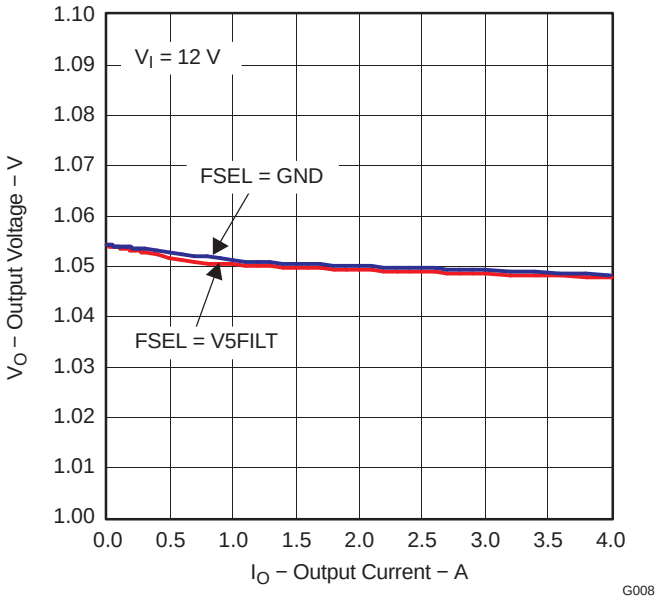


Figure 8. 1.05-V OUTPUT VOLTAGE vs. OUTPUT CURRENT

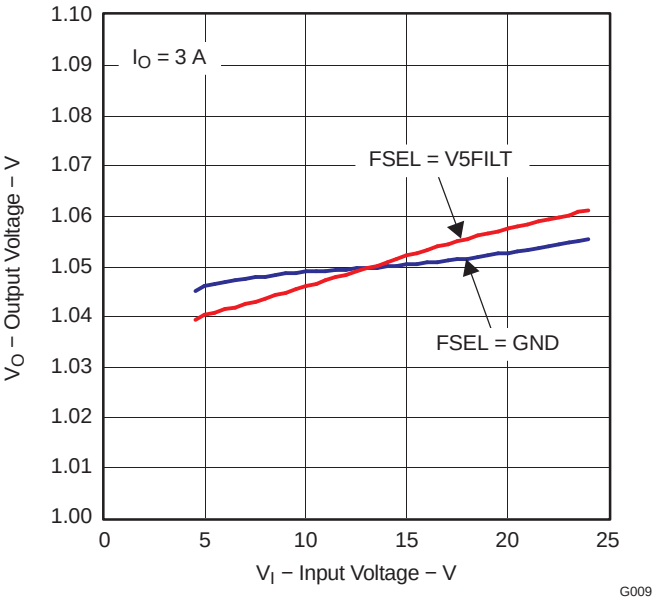


Figure 9. 1.05-V OUTPUT VOLTAGE vs. INPUT VOLTAGE

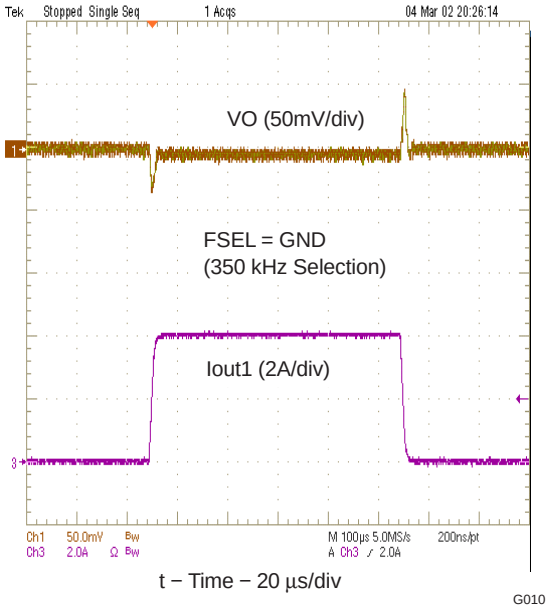


Figure 10. 1.05-V LOAD TRANSIENT RESPONSE

TYPICAL CHARACTERISTICS (continued)

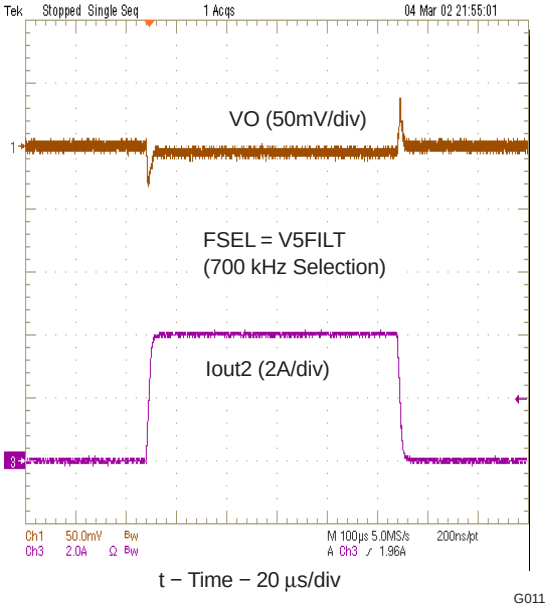


Figure 11. 1.05-V LOAD TRANSIENT RESPONSE

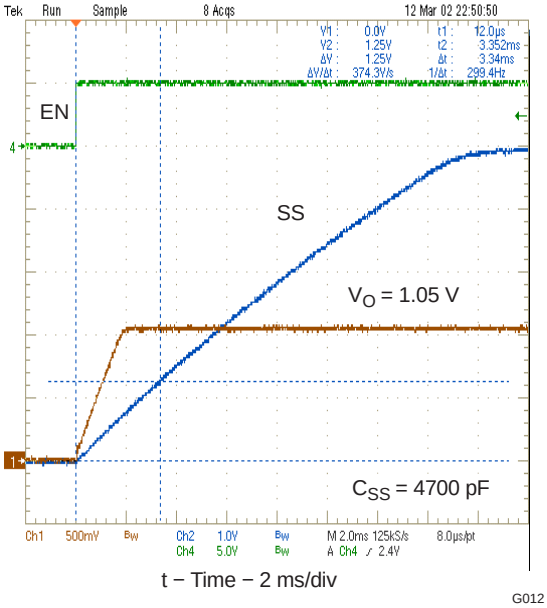


Figure 12. STARTUP WAVEFORM

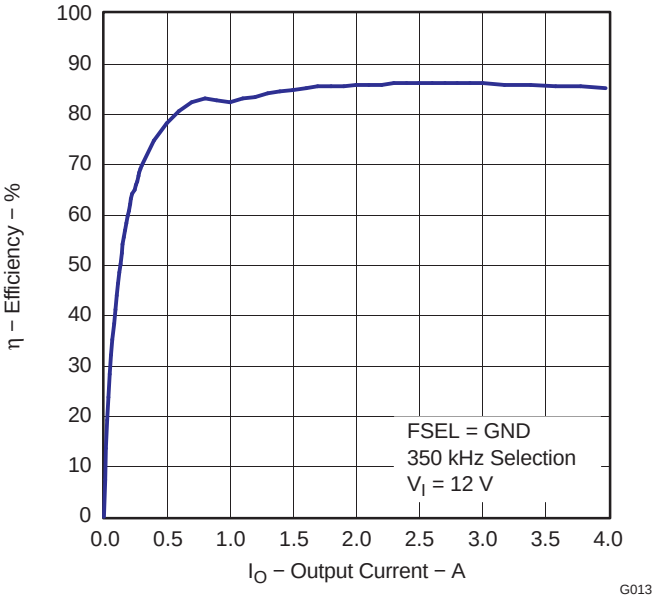


Figure 13. 1.05-V EFFICIENCY vs. OUTPUT CURRENT

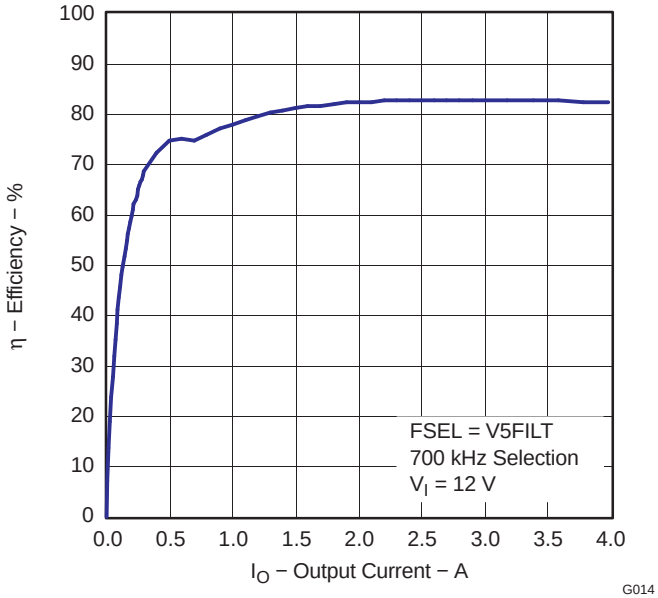


Figure 14. 1.05-V EFFICIENCY vs. OUTPUT CURRENT

APPLICATION INFORMATION

CHOOSE INDUCTOR

The inductance value should be determined, using Equation 3, to give the ripple current a value of approximately 1/4 to of the maximum output current. Large ripple current increases output ripple voltage, improves S/N ratio, and contributes to a stable operation.

$$L1 = \frac{1}{I_{L1(ripple)} \times f_{sw}} \times \frac{\left(V_{IN(max)} - VO\right) \times VO}{V_{IN(max)}} = \frac{3}{IO_{(max)} \times f_{sw}} \times \frac{\left(V_{IN(max)} - VO\right) \times VO}{V_{IN(max)}} \quad (3)$$

The inductor must have low DCR to achieve ideal efficiency, as well as enough room above peak inductor current before saturation. The peak inductor current can be estimated using the following (Equation 4).

$$I_{L1(peak)} = \frac{V_{trip}}{R_{DS(on)}} + \frac{1}{L1 \times f_{sw}} \times \frac{(V_{IN(max)} - VO) \times VO}{V_{IN(max)}} \quad (4)$$

CHOOSE OUTPUT CAPACITOR

The capacitor value and ESR determines the amount of output voltage ripple. A ceramic output capacitor is recommended.

$$C1 = \rangle \frac{1}{8 \times f_{sw}} \times \frac{(V_{IN(max)} - VO) \times VO}{\frac{VO_{(ripple)}}{I_{L1(ripple)}} - R_{ESR}} \quad (5)$$

$$R_{ESR} \langle \frac{VO_{(ripple)}}{I_{L1(ripple)}} \quad (6)$$

$$I_{C1(rms)} = \frac{VO \times (V_{IN} - VO)}{\sqrt{12} \times V_{IN} \times L1 \times f_{sw}} \quad (7)$$

CHOOSE INPUT CAPACITOR

The TPS53114 requires an input decoupling capacitor and may require a bulk capacitor depending on the application. A ceramic capacitor over 10µF is recommended for the decoupling capacitor. The capacitor voltage rating must be greater than the maximum input voltage.

CHOOSE BOOTSTRAP CAPACITOR

0.1µF ceramic capacitor must be connected between the VBST and SW pins for proper operation.

CHOOSE VREG5 AND V5FILT CAPACITOR

A 4.7µF ceramic capacitor must be connected between the VREG5 and GND for proper operation. A 1µF ceramic capacitor must be connected between the V5FILT and GND for proper operation.

CHOOSE OUTPUT VOLTAGE RESISTOR

The output voltage is set with a resistor divider from output node to the VFB pin. The use of 1% tolerance or better divider resistors are recommended. Start with a 10kΩ for the RI resistor and use the Equation 8 and Equation 9 to calculate output voltage.

$$V_{out} = 0.765 \times \left(1 + \frac{R1}{R2}\right) \quad \text{(FSEL=GND)} \quad (8)$$

$$V_{out} = 0.758 \times \left(1 + \frac{R1}{R2}\right) \quad \text{(FSEL=V5FILT)} \quad (9)$$

CHOOSE SOFTSTART CAPACITOR

Softstart timing equations are as follows:

$$Tss = \frac{Css \times 0.765}{2e-6} \text{ (s)} \quad \text{(FSEL=GND)} \tag{10}$$

$$Tss = \frac{Css \times 0.758}{2e-6} \text{ (s)} \quad \text{(FSEL=V5FILT)} \tag{11}$$

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
TPS53114PWP	ACTIVE	HTSSOP	PWP	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
TPS53114PWPR	ACTIVE	HTSSOP	PWP	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

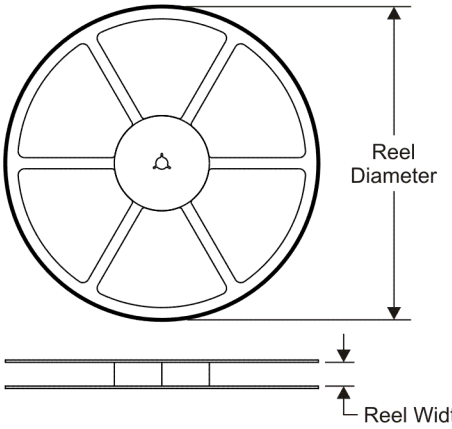
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

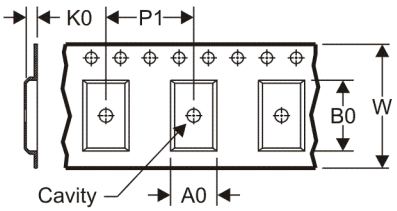
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

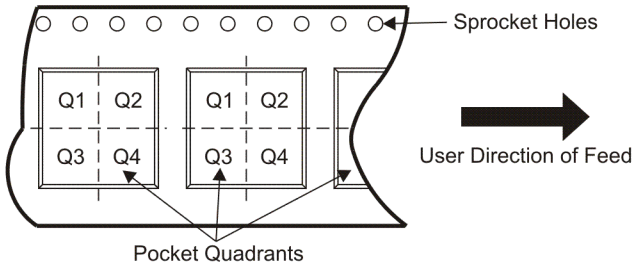


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

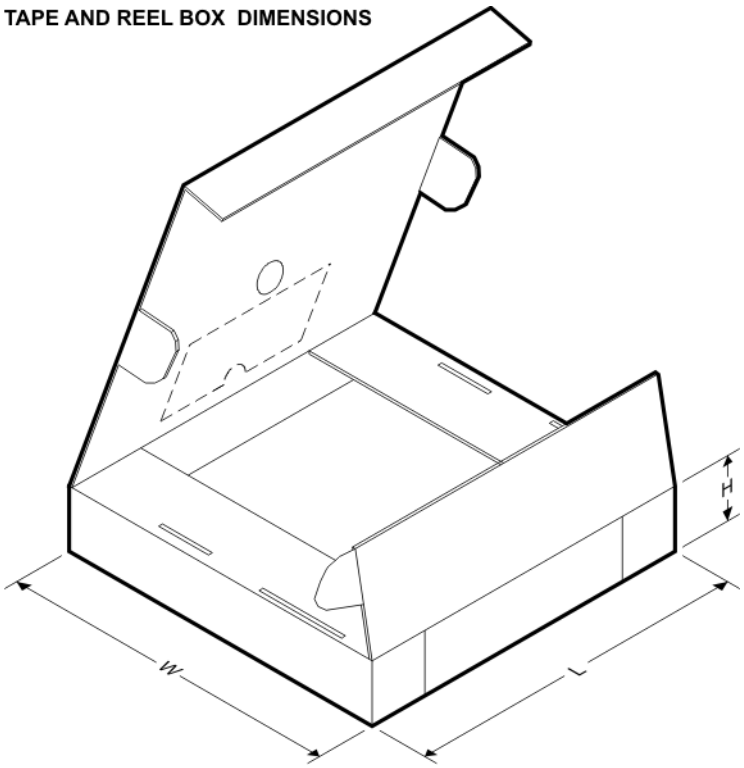
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS53114PWPR	HTSSOP	PWP	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

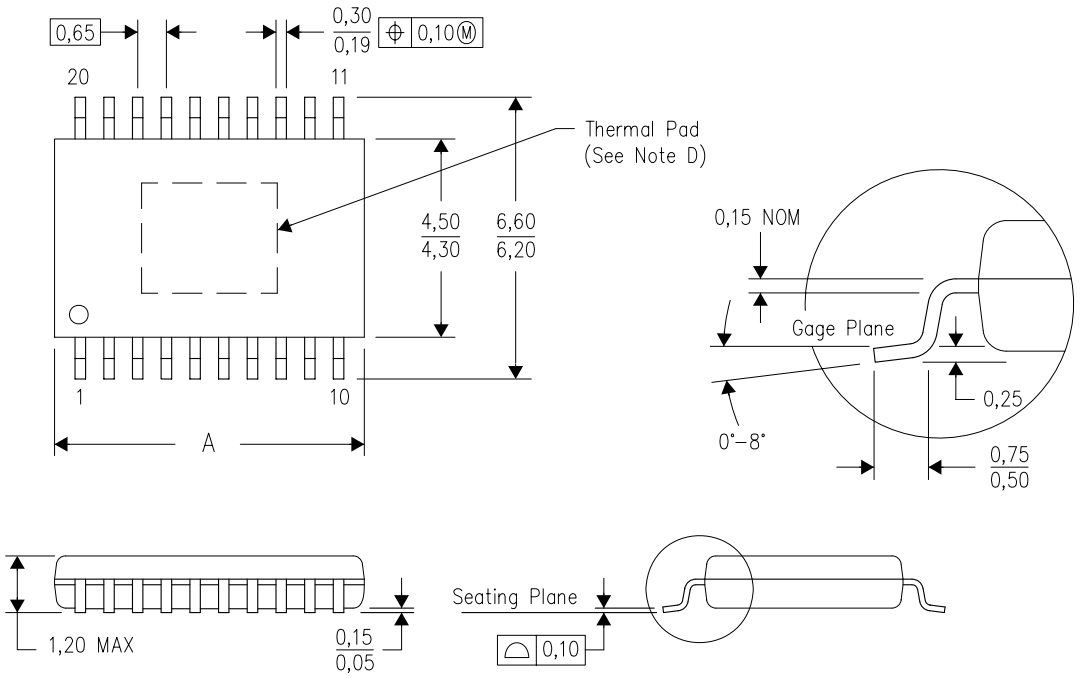


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS53114PWPR	HTSSOP	PWP	16	2000	346.0	346.0	29.0

PWP (R–PDSO–G**) PowerPAD™ PLASTIC SMALL–OUTLINE PACKAGE

20 PIN SHOWN



DIM \ PINS **	14	16	20	24	28
A MAX	5,10	5,10	6,60	7,90	9,80
A MIN	4,90	4,90	6,40	7,70	9,60

4073225/H 12/05

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http://www.ti.com>.
E. Falls within JEDEC MO–153

THERMAL PAD MECHANICAL DATA

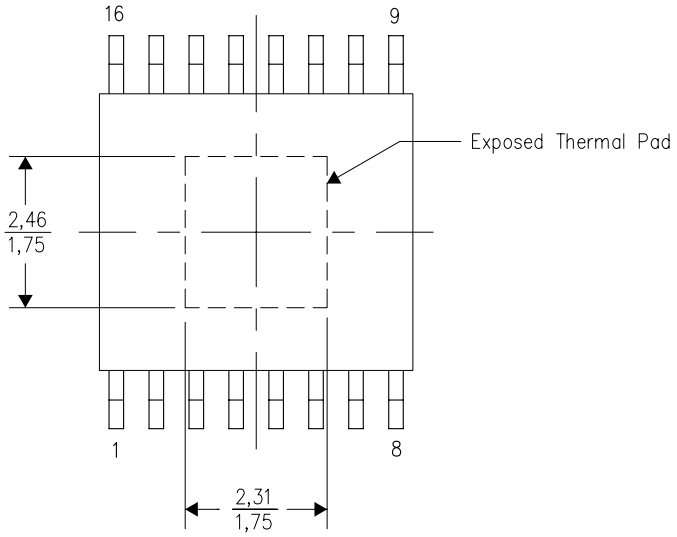
PWP (R–PDSO–G16)

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

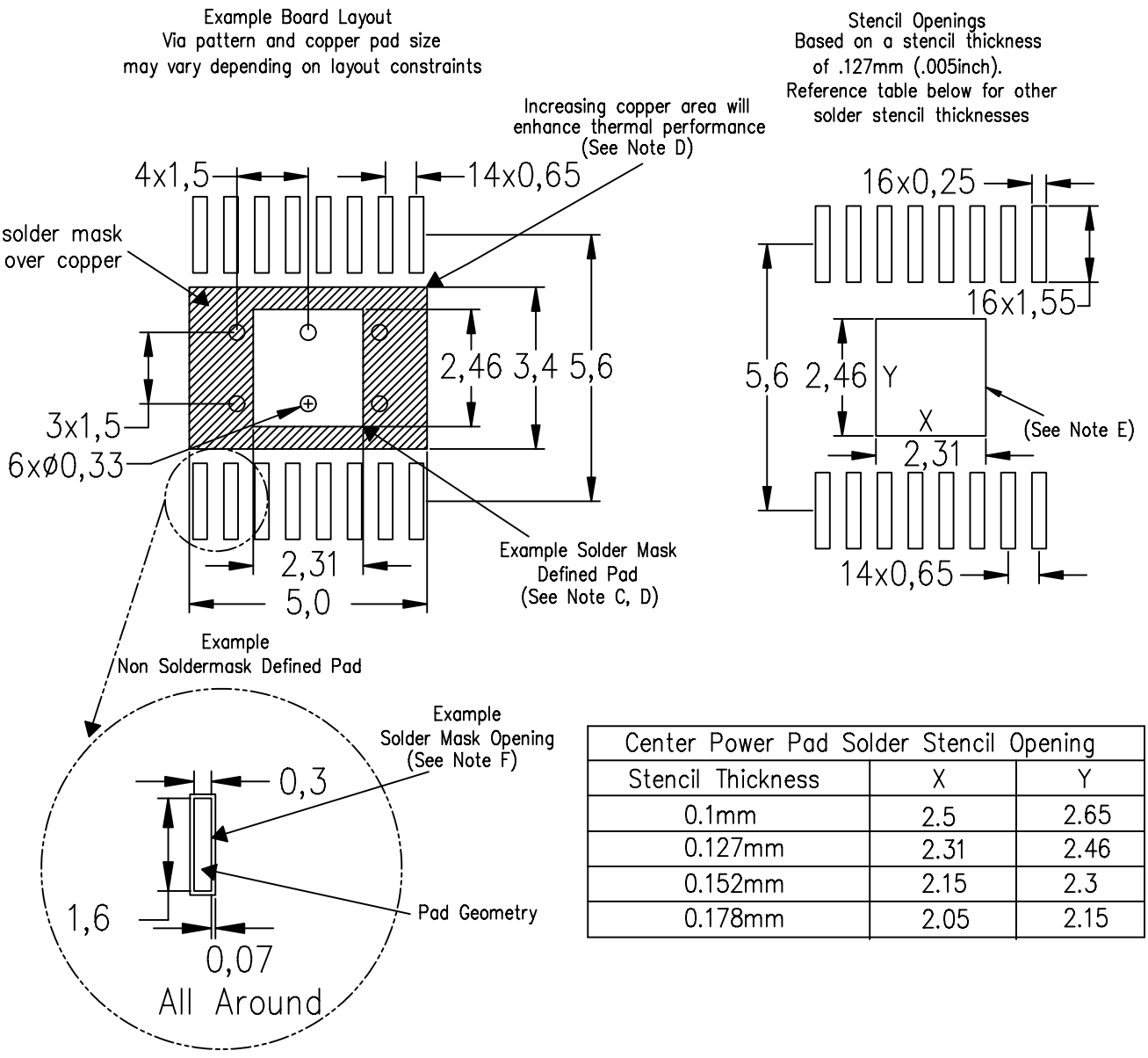


Top View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

PWP (R–PDSO–G16) PowerPAD™



Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.5	2.65
0.127mm	2.31	2.46
0.152mm	2.15	2.3
0.178mm	2.05	2.15

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.
F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

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