

Positive Voltage Intelligent Protection Device Hotswap Controller and I²C Current Monitor

Check for Samples: [TPS2480](#), [TPS2481](#)

FEATURES

- Programmable FET Power Limit
- External N-Channel FET Gate Drive
- Programmable Fault Timer
- Open Drain Power Good Output
- I²C monitoring of Current, Voltage and Power
- High Accuracy Current Monitoring (1% over temperature)
- Dynamic Calibration
- 9-V to 20-V Input Range

APPLICATIONS

- Servers
- Hard Drives
- Storage Networks
- Base Stations

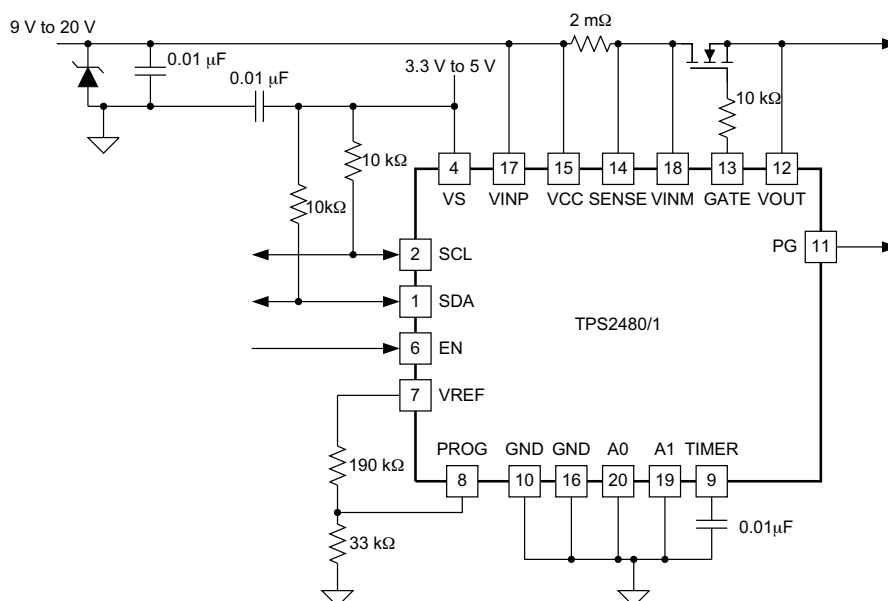
DESCRIPTION

The TPS2480/81 are designed to minimize inrush into applications and protect both the load and the FET from over-current or short circuit events. They control an external N-channel MOSFET switch and provide accurate voltage, current, and power monitoring using a configurable 12 bit A/D converter via an I²C interface. The independently adjustable power limit and current limit ensure that the external MOSFET operates within the FET's Safe Operating Area (SOA).

The flexible design includes a Power Good output which can be used for sequencing as well as load fault indication. An external timer capacitor can set the fault time to help immunize the system from nuisance shutdowns during brief transient events.

The monitoring circuitry incorporates a high accuracy A/D converter which can be configured from a 9 to 13 bit converter. The internal gain of the A/D can be configured to scale the current, voltage and power readings to the needs of the application. An additional multiplying register calculates power in Watts. The I²C interface uses multi-level addressing to allow up to 16 programmable addresses.

Functional Block Diagram



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

DESCRIPTION (CONT.)

The TPS2480 and TPS2481 monitors shunts on buses that can vary from 9 V to 26 V and with a few external components it is possible to monitor buses as high as 80 V.

The monitoring circuitry uses a single 3-V to 5.5-V supply, drawing a maximum of 1 mA of supply current.

ORDERING INFORMATION

DEVICE	JUNCTION TEMPERATURE	PACKAGE	ORDERING CODE	MARKING
TPS2480	-40°C to 125°C	PW20	TPS2480PW	TPS2480
TPS2481	-40°C to 125°C	PW20	TPS2481PW	TPS2481

DISSIPATION RATINGS^{(1) (2) (3)}

PACKAGE	θ_{JA} HIGH K, °C/W	θ_{JA} (Air Flow) HIGH-k ⁽⁴⁾ , °C/W
TPS2480	88.3	74.5
TPS2481	88.3	74.5

(1) Tested per JEDEC JESD51, natural convection. The definitions of high-k and low-k are per JESD 51-7 and JESD 51-3.

(2) Low-k (2 signal - no plane, 3 in. by 3 in. board, 0.062 in. thick, 1 oz. copper) test board with the pad soldered, and an additional 0.12 in. of top-side copper added to the pad.

(3) High-k is a (2 signal – 2 plane) test board with the pad soldered.

(4) The best case thermal resistance is obtained using the recommendations per SLMA002A (2 signal - 2 plane with the pad connected to the plane).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Input voltage range	9		80	V
PROG	Input voltage range	0.4		4	
V _{REF}	Sourcing current	0		1	mA
V _S	Input voltage range	3		5.5	V
V _{INP} , V _{INM}	Input voltage range	0		20	
T _{stg}	Operating free air temperature	-40		85	°C
T _J	Operating junction temperature	-40		125	

ABSOLUTE MAXIMUM RATINGS^{(1) (2) (3)}

over operating free-air temperature range (unless otherwise noted)

		UNIT
Input voltage range, VCC, Sense, Enable, OUT	-0.3 to 100	V
Supply voltage, V _S	GND - 0.3 to 6	
Input voltage, common mode, VINP, VINM	GND- 0.3 to + 26	
Input voltage, differential, VINP, VINM	-26 to + 26	
Input voltage range, PROG	-0.3 to 6	
Output voltage range, GATE, PG	-0.3 to 100	
Output voltage range, TIMER, VREF	-0.3 to 6	
Sink current, PG	10	mA
Source current, VREF	0 to 2	
Sink current, PROG	2	
SDA	GND- 0.3 to + 6.0	V
SCL	GND- 0.3 to VS + 0.3	
Current into SDA, SCL, VS, VINP, VINM, A0, A1, GNDB	5	mA
Open drain digital output current	10	
ESD rating, HBM	2 k	V
ESD rating, CDM	500	
Operating junction temperature range, T _J	- 40 to + 125	°C
Storage temperature range, T _{stg}	- 40 to 150	

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.
- (2) All voltage values are with respect to GND unless otherwise stated.
- (3) Do not apply voltage to these pins.

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Current (VCC)						
I _{VCC}	Enabled	V _{EN} = Hi V _{SENSE} = V _{OUT} = V _{VCC}		450	1000	μA
	Disabled	V _{EN} = Lo V _{SENSE} = V _{VCC} = V _{OUT} = 0		90	250	
I _{VS}	Quiescent current	operating		0.7	1.0	mA
	Quiescent current	Power down mode		6	15	μA
V _{POR}	Power On reset threshold			2		V
Current Sense Input (SENSE)						
I _{SENSE}	Input bias current	V _{SENSE} = V _{VCC} V _{OUT} = V _{VCC}		7.5	20	μA
Reference Voltage Output (VREF)						
V _{REF}	Reference voltage	0 < I _{VREF} < 1 mA	3.9	4	4.1	V
Power Limiting Input (PROG)						
I _{PROG}	Input bias current; device enabled; sourcing or sinking	0 < V _{PROG} < 4 V V _{EN} = 48 V			5	μA
R _{PROG}	Pulldown resistance; device disabled	I _{PROG} = 200 μA; V _{EN} = 0 V		375	600	Ω
Power Limiting and Current Limiting (SENSE)						
V _{CL}	Current sense threshold V(VCC-SENSE) with power limiting trip	V _{PROG} = 2.4 V; V _{OUT} = 0 V or V _{PROG} = 0.9 V; V _{OUT} = 30 V; V _{VCC} = 48 V	17	25	33	mV
V _{SENSE}	Current sense threshold V(VCC-sense) without power limiting trip	V _{PROG} = 4 V; V _{SENSE} = V _{OUT}	45	50	55	
t _{F_TRIP}	Large overload response time to GATE low	V _{PROG} = 4 V; V _{OUT} = V _{SENSE} ; V(VCC-SENSE): 0 rising to 200 mV; C(GATE-OUT) = 2 nF; V(GATE-OUT) = 1 V			1.2	μs
Timer Operation (TIMER)						
I _{SOURCE}	Charge current (sourcing)	V _{TIMER} = 0 V	15.0	25.0	34.0	μA
		V _{TIMER} = 0 V; T _J = 25°C	20.0	25.0	30.0	
I _{SINK}	Discharge current (sinking)	V _{TIMER} = 5 V	1.50	2.5	3.70	
		V _{TIMER} = 5 V; T _J = 25°C	2.10	2.5	3.10	
	TIMER upper threshold voltage		3.9	4.0	4.1	V
	TIMER lower reset threshold voltage	TPS2481 only	0.96	1.0	1.04	
D _{RETRY}	Fault retry duty cycle	TPS2481 only	0.5%	0.75%	1.0%	
Gate Drive Output (GATE)						
I _{GATE}	GATE sourcing current	V _{SENSE} = V _{VCC} ; V(GATE-OUT) = 7 V; V _{EN} = Hi	15	22	35	μA
	GATE sinking current	V _{EN} = Lo; V _{GATE} = V _{VCC}	1.8	2.4	2.8	mA
		V _{EN} = Hi; V _{GATE} = V _{VCC} ; V(VCC-SENSE) ³ 200 mV	75	125	250	
V _{GATE-OUT}	GATE output voltage		12		16	V
t _{D_ON}	Propagation delay: EN going true to GATE output high	V _{EN} = 0 → 2.5 V, 50% of V _{EN} to 50% of V _{GATE} , V _{OUT} = V _{VCC} , R(GATE-OUT) = 1 MOhm		25	40	μs
t _{D_OFF}	Propagation delay: EN going false (0 V) to GATE output low	V _{EN} = 2.5 V → 0 V, 50% of V _{EN} to 50% of V _{GATE} , V _{OUT} = V _{VCC} , R(GATE-OUT) = 1 MΩ, t _{FALL} < 0.1 μs		0.5	1	
	Propagation delay: TIMER expires to GATE output low	V _{TIMER} : 0 → 5 V, t _{RISE} < 0.1 μs. 50% of V _{TIMER} to 50% of V _{GATE} , V _{OUT} = V _{CC} , R(GATE-OUT) = 1 MΩ,		0.8	1	

ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Good Output (PG)						
V _{PG_L}	Low voltage (sinking)	I _{PG} = 2 mA		0.1	0.25	V
		I _{PG} = 4 mA		0.25	0.5	
V _{PGTL}	PG threshold voltage; V _{OUT} rising; PG goes open drain	V _{SENSE} = V _{VCC} ; measure V _(VCC-OUT)	0.8	1.25	1.7	
V _{PGTH}	PG threshold voltage; V _{OUT} falling; PG goes low	V _{SENSE} = V _{VCC} ; measure V _(VCC-OUT)	2.2	2.7	3.2	
V _{HYST_PG}	PG threshold hysteresis voltage; V(SENSE-OUT)	V _{SENSE} = V _{VCC}		1.4		
t _{DPG}	PG deglitch delay; detection to output; rising and falling edges	V _{SENSE} = V _{VCC}	5	9	15	
	Leakage current; PG false;	open drain			10	μA
Output Voltage Feedback Input (OUT)						
I _{OUT}	Bias current	V _{OUT} = V _{VCC} ; V _{EN} = Hi; sinking		8	20	μA
		V _{OUT} = GND; V _{EN} = Lo; sourcing		18	40	
Enable Input (EN)						
V _{EN_H}	Threshold VEN going high		1.32	1.35	1.38	V
V _{EN_L}	Threshold VEN going low		1.20	1.25	1.30	
	VEN hysteresis			100		mV
	Leakage current	V _{EN} = 30 V			1	μA
Input Supply UVLO (VCC)						
	V _{VCC} turn on	Rising		8.4	8.8	V
	V _{VCC} turn off	Falling	7.2	8.3		
	Hysteresis			75		mV
Digital Inputs (SDA in input mode, SCL, A0, A1)						
C _{IN}	Input capacitance			3		pF
I _{LEAKAGE}	Input leakage current	0 < V _{IN} < V _S		0.1	1	μA
V _{IN_HI}	Logic Hi input level			0.7(V _S)	6	V
V _{INLO}	Logic low input level		-0.3	0.3(V _S)		
V _{HYS}	Hysteresis			0.5		
Open Drain Digital Output (SDA)						
V _{LO}	SDA Low Output	Sinking 5 mA		0.15	0.4	V
I _{LEAKAGE}	High level leakage current	V _{OUT} = V _S		0.1	1.0	μA

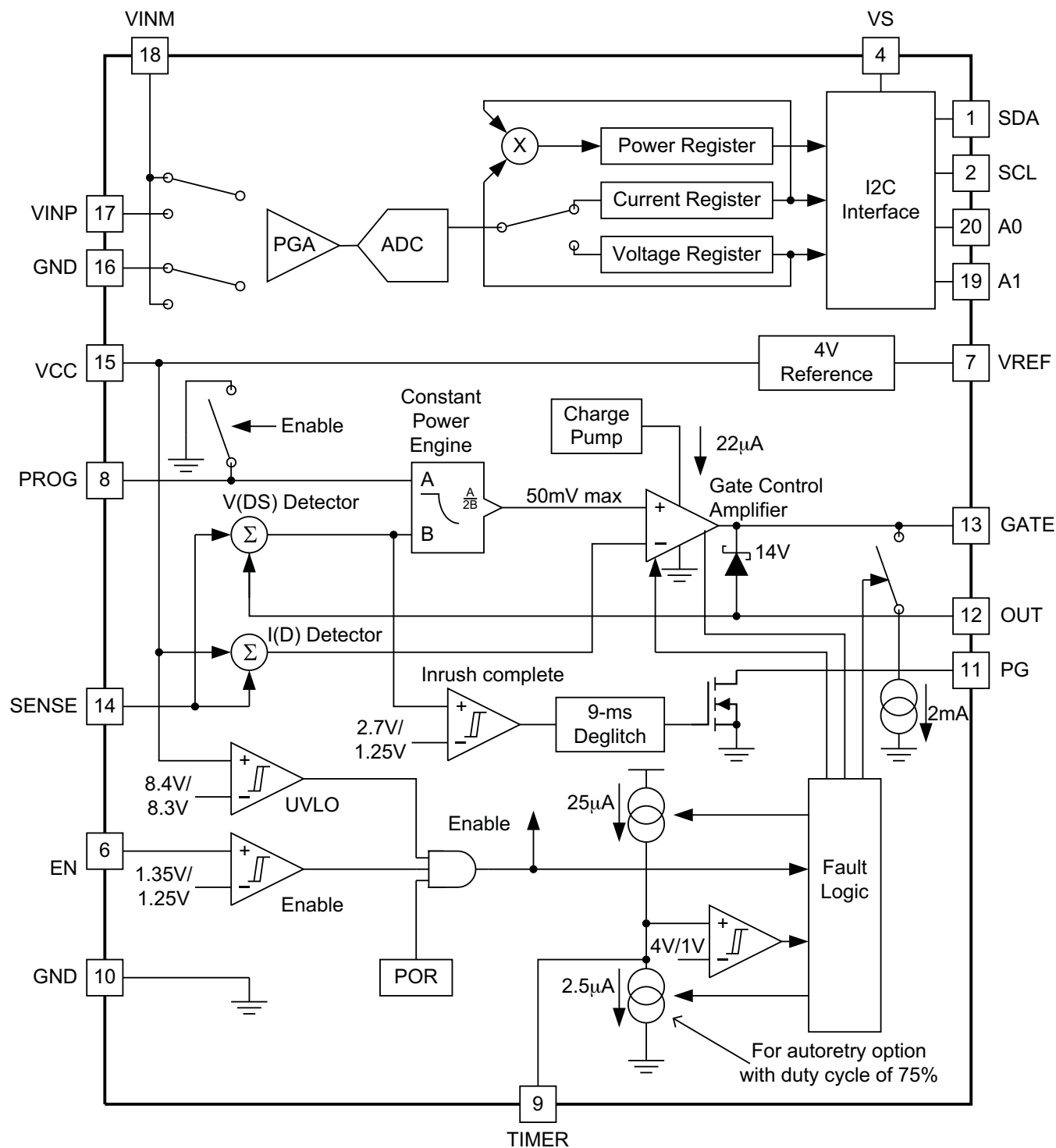
ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range (unless otherwise noted)

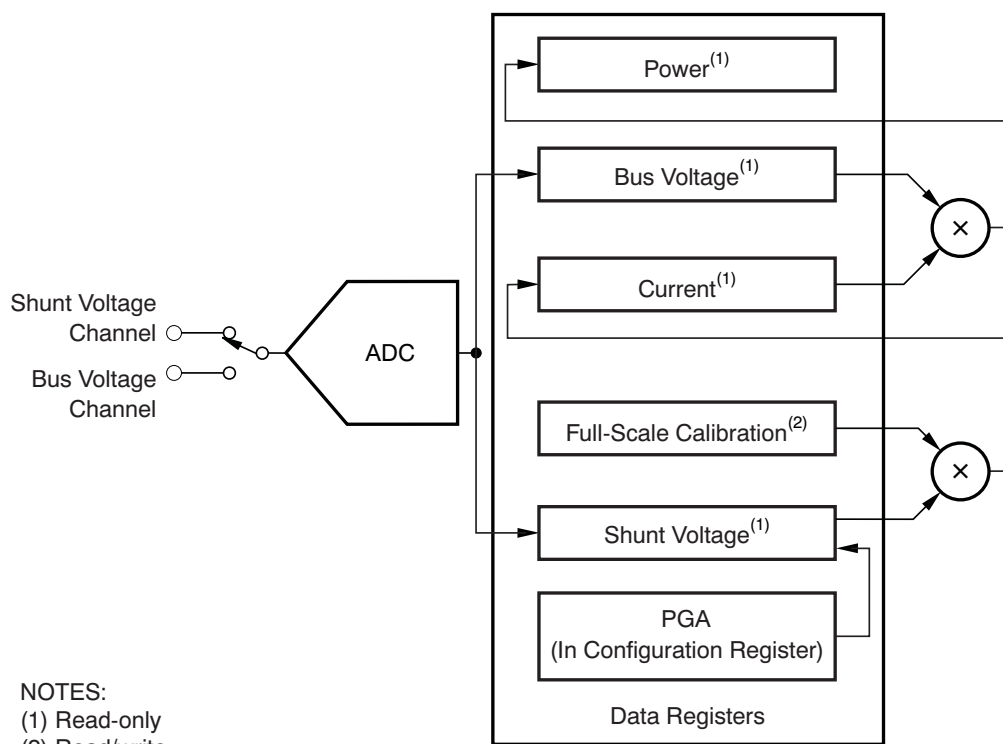
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input						
	Full-scale current sense (input) voltage range	PGA = x 1	0		±40	mV
		PGA = x 2	0		±80	
		PGA = x 4	0		±160	
		PGA = x 8	0		±320	
	Bus voltage (input voltage) range	BRNG = 1	0		32	V
		BRNG = 0	0		16	
	Common-mode rejection CMRR	VIN+ = 0 V to 26 V	100	120		dB
V _{OS}	Input offset	PGA = x 1		±10	±100	μV
		PGA = x 2		±20	±125	
		PGA = x 4		±30	±150	
		PGA = x 8		±40	±200	
	Temp stability			0.1		μV/°C
	PSRR	VS = 3 V to 5.5 V		10		μV/V
Gain _{CSA}	CSA gain error			±0.04%		
	Temp stability			10		ppm
I _{VNP} , I _{VINM}	Input bias current	Active mode		20		μA
I _{LEAKAGE}	I _{VNP} , I _{VINM}	Power down mode, leakage input current		0.1	±0.5	
A/D Converter						
Step Size	1 LSB	Shunt voltage		10		μV
		Bus voltage		4		mV
Current Accuracy	Current measurement	Error		±0.2%	±0.5%	
	Temp drift	Over full range			±1.0%	
Voltage Accuracy	Bus voltage measurement	Error		±0.2%	±0.5%	
	Temp drift (-25°C to 85°C)	Over full range			±1.0%	
T _{CONV}	Conversion time	12 Bit		532	586	μs
		11 Bit		276	304	
		10 Bit		148	163	
		9 Bit		84	92	
T _{LOWCONV}	Conversion time	Minimum A/D conversion time	4			

DEVICE INFORMATION

Functional Block Diagram



Register Block Diagram



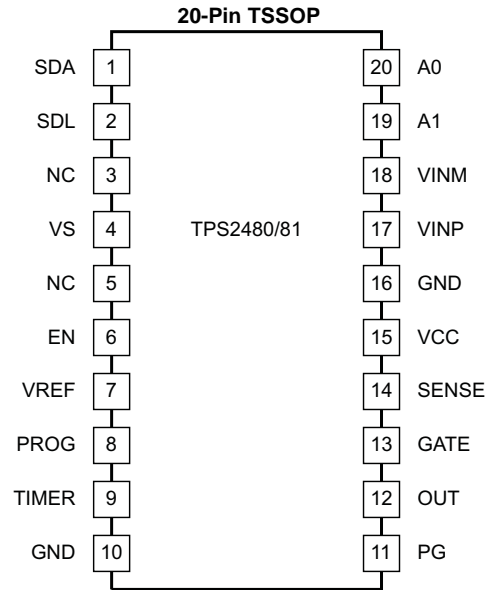


Table 1. TERMINAL FUNCTIONS

FUNCTION	TPS2480/81	DESCRIPTION
SDA	1	I ² C Data Line
SCL	2	I ² C Clock
NC	3	Tie to GND or float
VS	4	Power input to the I ² C block, 3.3 V to 5 V
NC	5	No connection, tie to GND or float
EN	6	Device enable
VREF	7	Reference voltage output, used to set power threshold on PROG pin
PROG	8	Power-limit setting input
TIMER	9	Fault timing capacitor
GND	10	GND
PG	11	Power good reporting output, open-drain
OUT	12	Output voltage feedback
GATE	13	Gate output
SENSE	14	Current-limit sense input
VCC	15	Main power supply input to device and FET
GND	16	GND
VINP	17	Positive differential shunt voltage. Connect to positive side of shunt resistor
VINM	18	Negative differential shunt voltage. Connect to negative side of shunt resistor. Bus voltage is measured from this pin to GND
A1	19	Address pin. Table 2 shows pin settings and corresponding addresses.
A0	20	Address pin. Table 2 shows pin settings and corresponding addresses.

Pin Description

A0, A1: Address pins for setting the TPS2480 I²C address. These bits can be tied to one of four pins (GND, SDA, SCL, VS) which gives a total of 16 different address as shown in [Table 2](#).

EN: The GATE driver is enabled if the positive threshold is exceeded and the internal POR and UVLO thresholds have been satisfied. EN can be used as a logic control input, an analog input voltage monitor as illustrated by R1/R2 in the Functional Block Diagram, or it can be tied to VCC to always enable the TPS2480/81. The hysteresis associated with the internal comparator makes this a stable method of detecting a low input condition and shutting the downstream circuits off. A TPS2480 that has latched off can be reset by cycling EN below its negative threshold and back high.

GATE: Provides the high side (above VCC) gate drive for the external FET. It is controlled by the internal gate drive amplifier, which provides a pull-up of 22 μ A from an internal charge pump and a strong pull-down to ground of 75 mA (min). The pull-down current is a non-linear function of the amplifier overdrive; it provides small drive for small overloads, but large overdrive for fast reaction to an output short. There is a separate pull-down of 2 mA to shut the external FET off when EN or UVLO causes this to happen. An internal clamp protects the gate of the external FET (to OUT) and generally eliminates the need for an external clamp in almost all cases for devices with 20-V $V_{GS(max)}$ ratings; an external Zener may be required to protect the gate of devices with $V_{GS(max)} < 16$ V. A small series resistance of 10 Ω should be inserted in the gate lead if the C_{ISS} of the external FET > 200 pF, otherwise use 33 Ω for small MOSFETs. A capacitor can be connected from GATE to ground to create a slower inrush with a constant current profile without affecting the amplifier stability. Add a series resistor of about 1 k Ω to the gate capacitor to maintain the gate clamping and current limit response time.

GND: This pin is connected to system ground.

OUT: This input pin is used by the constant power engine and the PG comparator to measure V_{DS} of the external FET as $V_{(SENSE-OUT)}$. Internal protection circuits leak a small current from this pin when it is low. If the load circuit can drive OUT below ground, connect a clamp (or freewheel) diode from OUT (cathode) to GND (anode).

PG: This open-drain output is intended to interface to downstream dc/dc converters or monitoring circuits. PG goes open-drain (high voltage with a pull-up) after V_{DS} of the external FET has fallen to about 1.25 V and a 9-ms deglitch time period has elapsed. PG is false (low or low resistance to ground) whenever EN is false, V_{DS} of the external FET is above 2.7 V, or UVLO is active. PG can also be viewed as having an input and output voltage monitor function. The 9-ms deglitch circuit operates to filter short events that could cause PG to go inactive (low) such as a momentary overload or input voltage step. V_{PG} voltage can be greater than V_{VCC} because its ESD protection is only with respect to ground.

PROG: The voltage applied to this pin (0.4 V to 4.0 V) programs the power limit used by the constant power engine. Normally, a resistor divider R3/R4 is connected from VREF to PROG to set the power limit according to the following equation:

$$V_{PROG} = \frac{P_{LIM}}{(10 \times I_{LIM})} \quad (1)$$

where P_{LIM} is the desired power limit of the external FET and I_{LIM} is the current limit setpoint (see SENSE). P_{LIM} is determined by the desired thermal stress on the external FET:

$$P_{LIM} < \frac{T_{J(max)} - T_{S(max)}}{R_{\theta JC(max)}} \quad (2)$$

where $T_{J(max)}$ is the maximum desired transient junction temperature of the external FET and $T_{S(max)}$ is the maximum case temperature prior to a start or restart.

V_{PROG} is used in conjunction with V_{DS} to compute the (scaled) current, $I_{D_ALLOWED}$, by the constant power engine. $I_{D_ALLOWED}$ is compared by the gate amplifier to the actual I_D , and used to generate a gate drive. If $I_D < I_{D_ALLOWED}$, the amplifier turns the gate of the external FET full on because there is no overload condition; otherwise GATE is regulated to maintain the $I_D = I_{D_ALLOWED}$ relationship. A capacitor may be tied from PROG to

ground to alter the natural constant power inrush current shape. If properly designed, the effect is to cause the leading step of current in [Figure 12](#) to look like a ramp. PROG is internally pulled to ground whenever EN, POR, or UVLO are not satisfied or the TPS2480 is latched off. This feature serves to discharge any capacitance connected to the pin. Do not apply voltages greater than 4 V to PROG. If the constant power limit is not used, PROG should be tied to VREF through a 47-kΩ resistor.

SCL: This pin is the clock input for the I²C interface.

SDA: This pin is the data input for the I²C interface.

SENSE: Monitors the voltage at the drain of the external FET, and the downstream side of R_S providing the constant power limit engine with feedback of both the external FET current (I_D) and voltage (V_{DS}). Voltage is determined by the difference between SENSE and OUT, while the current analog is the difference between VCC and SENSE. The constant power engine uses V_{DS} to compute the allowed I_D and is clamped to 50 mV, acting like a traditional current limit at low V_{DS}. The maximum current limit is set by the following equation:

$$I_{LIM} = \frac{50\text{mV}}{R_S} \quad (3)$$

Design the connections to SENSE to minimize R_S voltage sensing errors. Don't drive SENSE to a large voltage difference from VCC because it is internally clamped to VCC. The current limit function can be disabled by connecting SENSE to VCC.

TIMER: An integrating capacitor, C_T, connected to the TIMER pin provides a timing function that controls the fault-time for both versions and the restart interval for the TPS2481. The timer charges at 25 μA whenever the TPS2480/81 is in power limit or current limit and discharges at 2.5 μA otherwise. The charge-to-discharge current ratio is constant with temperature even though there is a positive temperature coefficient to both. If TIMER reaches 4 V, the TPS2480 pulls GATE to ground, latches off, and discharges C_T. The TPS2491 pulls GATE to ground and attempt a restart (re-enable GATE) after a timing sequence consisting of discharging C_T down to 1 V followed by 15 more charge and discharge cycles. The TPS2480 can be reset by either cycling the EN pin or the UVLO (e.g. power cycling). TIMER discharges when EN is low or UVLO or POR are active. The TIMER pin should be tied to ground if this feature is not used. The general equation for fault retry time as a function of C_T is:

$$T_F = C_T \times 1347 \times 10^6 \quad (4)$$

VCC: This pin is associated with three functions:

1. biasing power to the integrated circuit,
2. input to power on reset (POR) and under voltage lockout (UVLO) functions, and
3. voltage sense at one terminal of R_S for the external FET current measurement.

The voltage must exceed the POR (about 6 V for roughly 400 ms) and the internal UVLO (about 8 V) before normal operation (driving the GATE) may begin. Connections to VCC should be designed to minimize R_S voltage sensing errors and to maximize the effect of C1 and D1; place C1 at R_S rather than at the device pin to eliminate transient sensing errors. GATE, PROG, PG, and TIMER are held low when either UVLO or POR are active.

VINM: This pin is Kelvin connected to the negative (load) side of the current sensing resistor. It will appear to external circuitry as a 20-μA sink in parallel with a 320-kΩ resistor to GND.

VINP: This pin is Kelvin connected to the positive (source) side of the current sensing resistor. It will typically sink ~ 20 μA.

VS: Power source for the logic and I²C interface. Typically between 3 V and 5 V.

VREF: Provides a 4.0-V reference voltage for use in conjunction with the resistor divider of a typical application circuit to set the voltage on the PROG pin. The reference voltage is available once the internal POR and UVLO thresholds have been met. It is not designed as a supply voltage for other circuitry, therefore ensure that no more than 1 mA is drawn. Although not typically required, up to 1000 pF can be placed on this pin.

TYPICAL CHARACTERISTICS

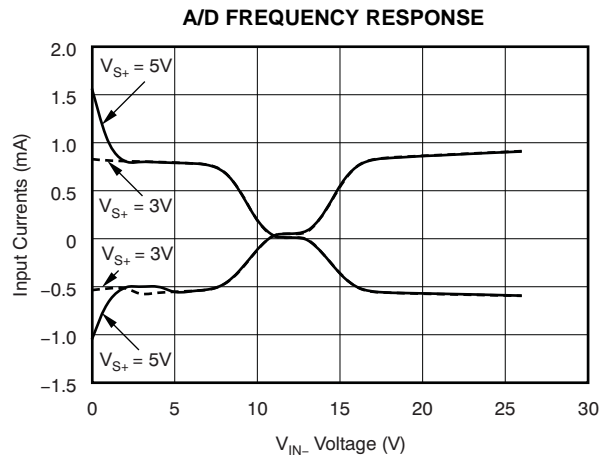


Figure 1.

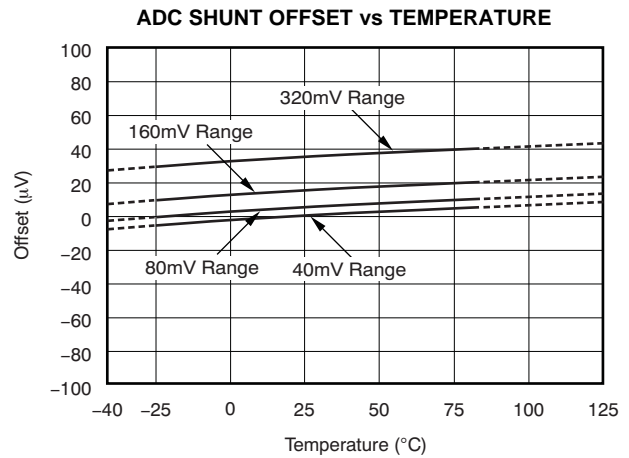


Figure 2.

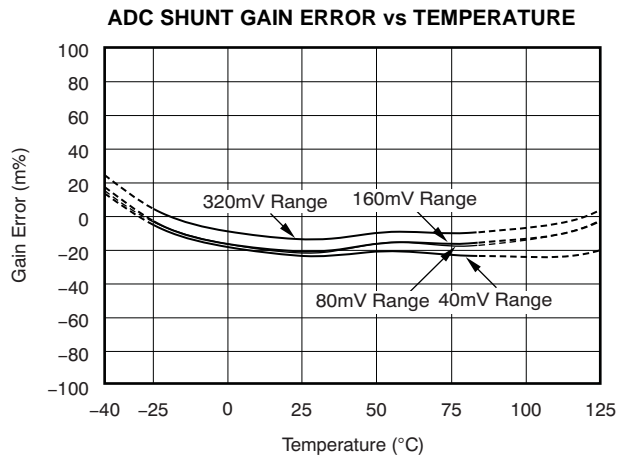


Figure 3.

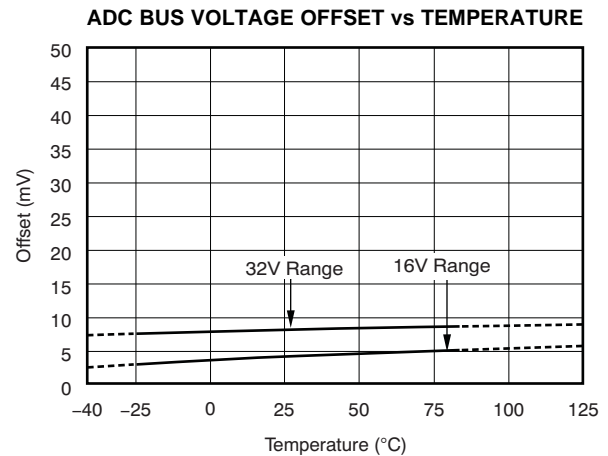


Figure 4.

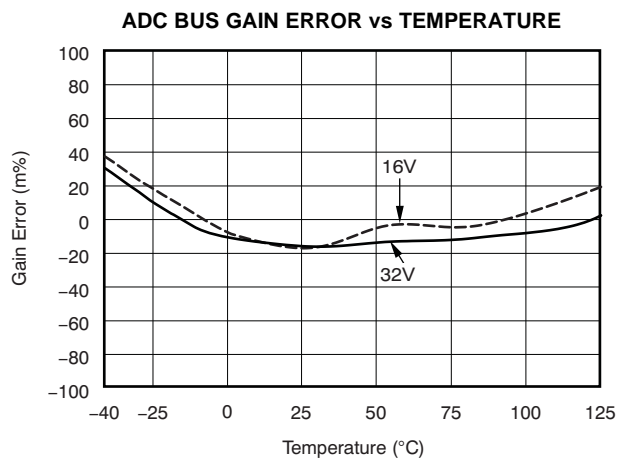


Figure 5.

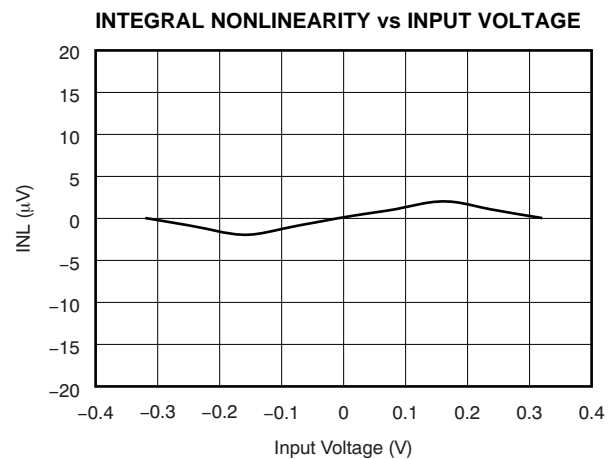


Figure 6.

TYPICAL CHARACTERISTICS (continued)

INPUT CURRENTS WITH LARGE DIFFERENTIAL VOLTAGES

(V_{IN+} at 12V, Sweep of V_{IN-})

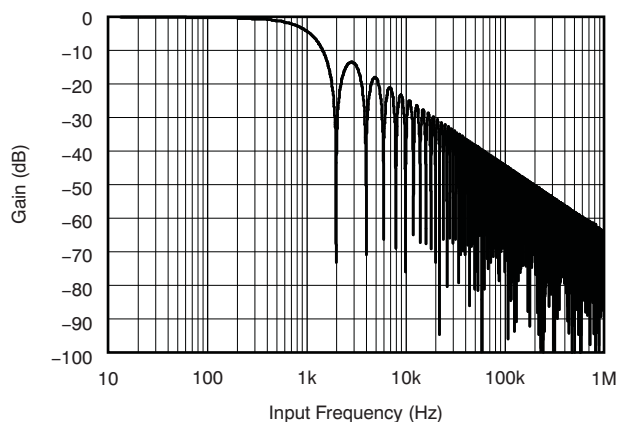


Figure 7.

ACTIVE I_Q vs TEMPERATURE

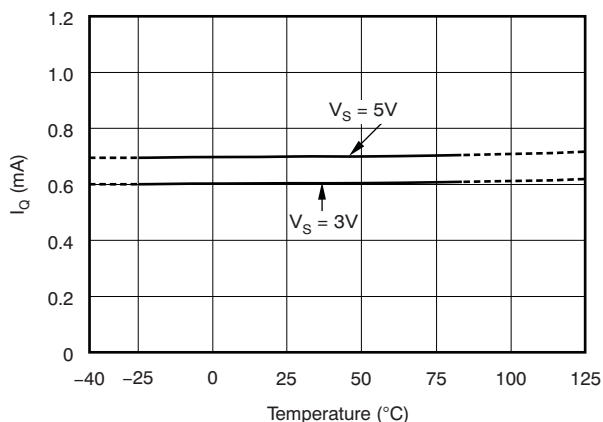


Figure 8.

SHUTDOWN I_Q vs TEMPERATURE

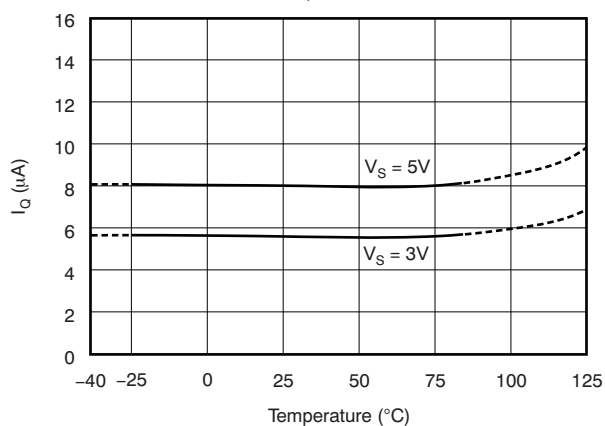


Figure 9.

ACTIVE I_Q vs I²C CLOCK FREQUENCY

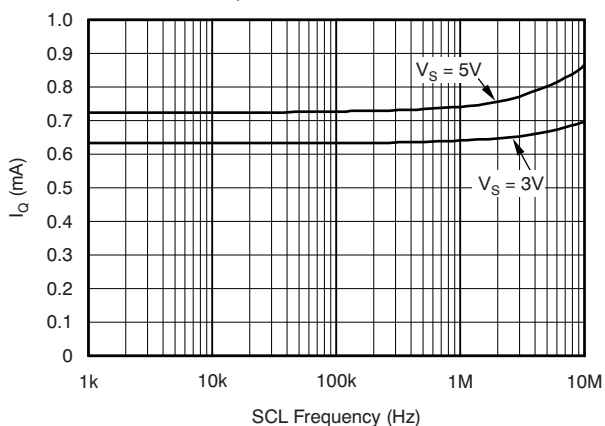


Figure 10.

SHUTDOWN I_Q vs I²C CLOCK FREQUENCY

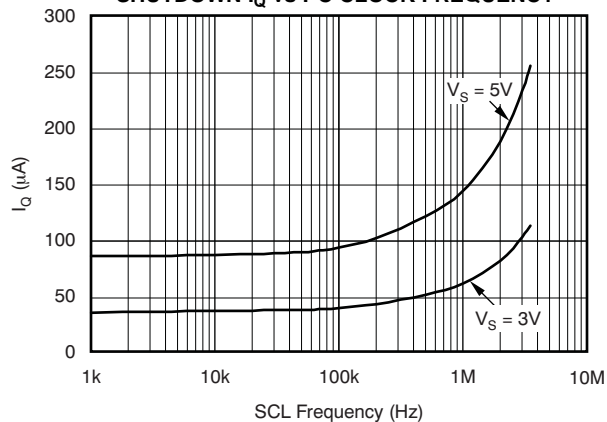


Figure 11.

APPLICATION INFORMATION

Basic Operation

The TPS2480/81 provides all the features needed for a positive hotswap controller.

These features include:

1. Under-voltage lockout;
2. Adjustable (system-level) enable;
3. Turn-on inrush limit;
4. High-side gate drive for an external N-channel MOSFET;
5. MOSFET protection (power limit and current limit);
6. Adjustable overload timeout (also called an electronic circuit breaker);
7. Charge-complete indicator for downstream converter sequencing; and
8. Optional automatic restart mode.

The TPS2480/81 features superior power-limiting, MOSFET protection that allows independent control of current limit (to set maximum full-load current), power limit and overload time (to keep FET in its SOA), and overload time (to control case temperature rise). The typical application circuit, and oscilloscope plots of [Figure 12](#) and [Figure 16](#) demonstrate many of the functions described above.

Board Plug-In ([Figure 12](#))

Only the bypass capacitor charge current and small bias currents are evident when a board is first plugged in. The TPS2480/81 is held inactive, and GATE, PROG, TIMER, and PG are held low for less than 1 ms while internal voltages stabilize, then GATE, PROG, TIMER, and PG are released and the part begins sourcing current to the GATE pin and the external FET begins to turn on while the voltage across it, $V_{(\text{SENSE-OUT})}$, and current through it, $V_{(\text{VCC-SENSE})}$, are monitored. Current initially rises to the value which satisfies the power limit engine ($P_{\text{LIM}} \div V_{\text{VCC}}$) since the output capacitor was discharged.

TIMER and PG Operation (Figure 12)

The TIMER pin charges C_T as long as limiting action continues, and discharges at a 1/10 charge rate when limiting stops. If the voltage on C_T reaches 4 V before the output is charged, the external FET is turned off and either a latch-off or restart cycle commences, depending on the part type. The open-drain PG output provides a deglitched end-of-charge indication which is based on the voltage across the external FET. PG is useful for preventing a downstream DC-to-DC converter from starting while C_O is still charging. PG goes active (open drain) about 9 ms after C_O is charged. This delay allows the external FET to fully turn on and any transients in the power circuits to end before the converter starts up. The resistor pull-up shown on pin PG in the typical application diagram only demonstrates operation; the actual connection to the converter depends on the application. Timing can appear to terminate early in some designs if operation transitions out of the power limit mode into a gate charge limited mode at low V_{DS} values.

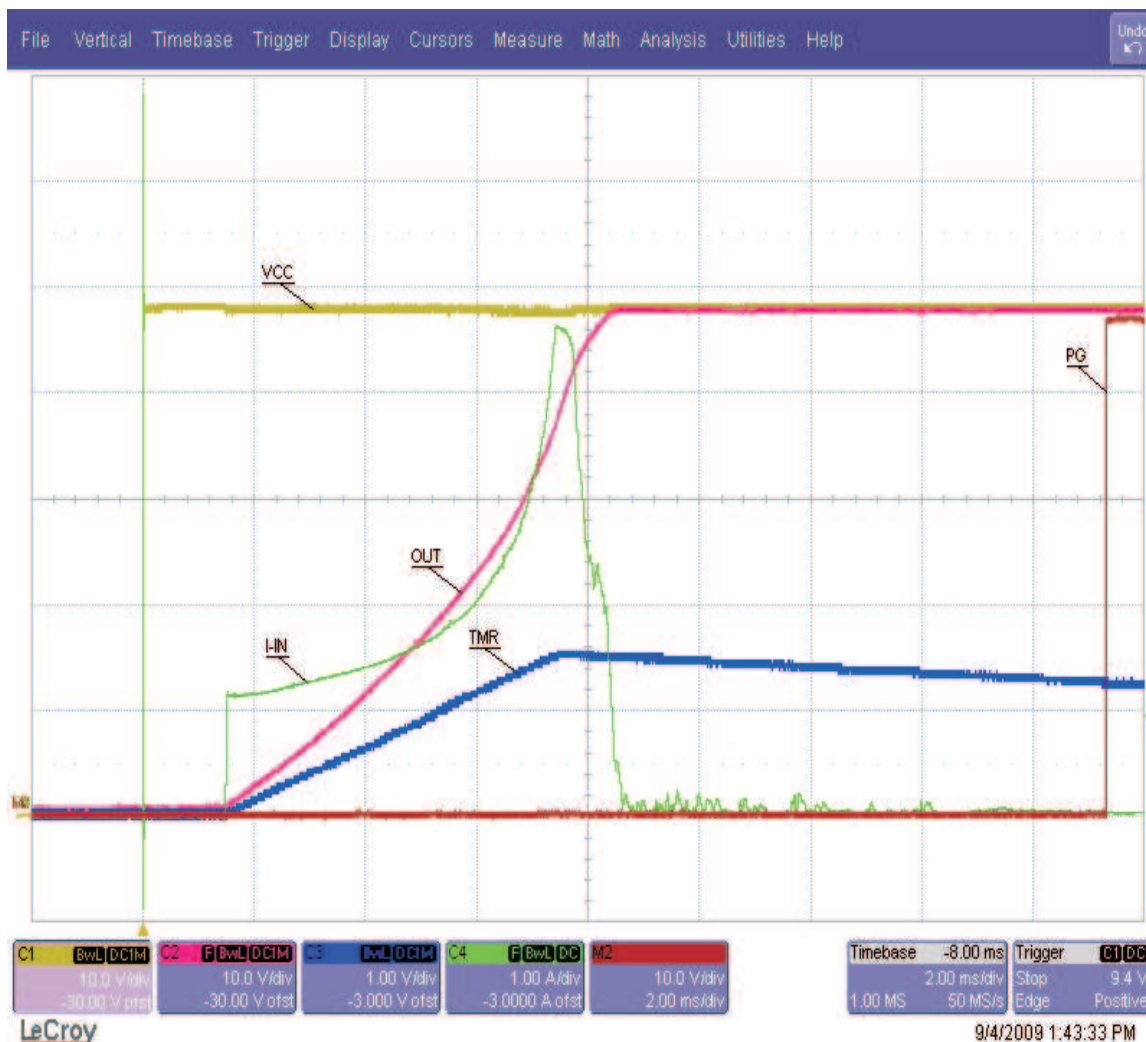


Figure 12. Basic Board Insertion

Action of the Constant Power Engine (Figure 13)

The calculated power dissipated in the external FET, $V_{DS} \times I_D$, is computed under the same startup conditions as Figure 12. The current of the external FET, labeled I_{IN} , initially rises to the value that satisfies the constant power engine; in this case it is $54\text{ W} / 48\text{ V} = 1.1\text{ A}$. The 54-W value is programmed into the engine by setting the PROG voltage using Equation 1. V_{DS} of the external FET, which is calculated as $V_{(SENSE-OUT)}$, falls as C_O charges, thus allowing the the external FET drain current to increase. This is the result of the internal constant power engine adjusting the current limit reference to the GATE amplifier as C_O charges and V_{DS} falls. The calculated device power in Figure 13, labeled MOSFET POWER, is seen to be flat-topped and constant within the limitations of circuit tolerance and acquisition noise. A fixed current limit is implemented by clamping the constant power engine output to 50 mV when V_{DS} is low. This protection technique can be viewed as a specialized form of foldback limiting; the benefit over linear foldback is that it yields the maximum output current from a device over the full range of V_{DS} and still protects the device.



Figure 13. Computation of the External FET Stress During Startup

Response to a Hard Output Short (Figure 14 and Figure 15)

Figure 14 shows the short circuit response over the full time-out period. This begins when the output voltage falls and ends when the external FET is turned off. The external FET current is actively controlled by the power limiting engine and gate amplifier circuit while the TIMER pin charges C_T to the 4-V threshold. Once this threshold is reached, the TPS2480/81 disable and latch off the external FET. The TPS2480 remains latched off until either the input voltage drops below the UVLO threshold or EN cycles through the false (low) state. The TPS2481 will attempt a restart after going through a timing cycle.

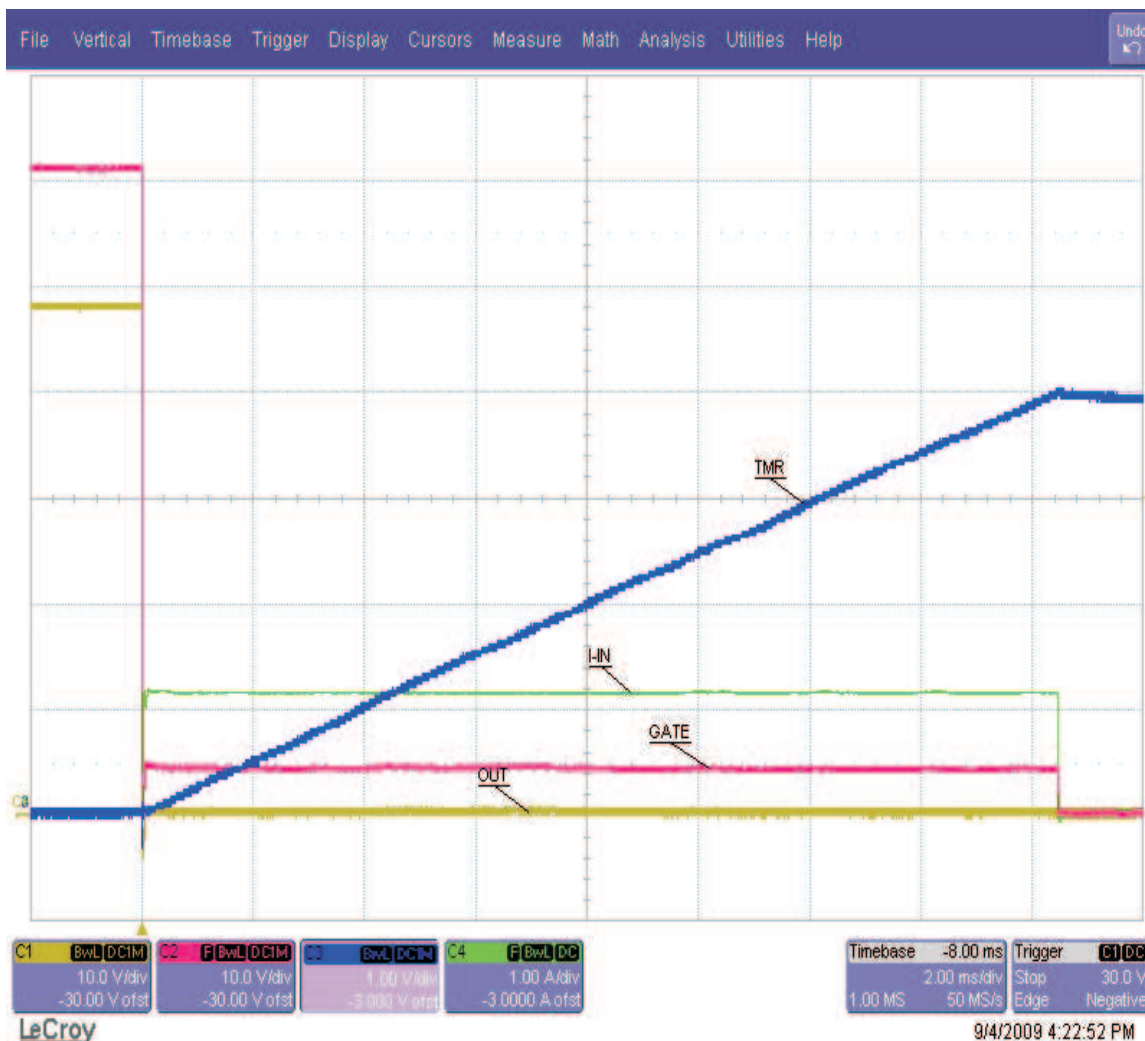


Figure 14. Current Limit Overview

The TPS2480/81 responds rapidly to the short circuit as seen in [Figure 15](#). The falling OUT voltage is the result of the external FET and C_O currents through the short circuit impedance. The internal GATE clamp causes the GATE voltage to follow the output voltage down and subsequently limits the negative V_{DS} to 1.2 V. The rapidly rising fault current overdrives the GATE amplifier causing it to overshoot and rapidly turn the external FET off by sinking current to ground. The external FET slowly turns back on as the GATE amplifier recovers; the external FET then settles to an equilibrium operating point determined by the power limiting circuit.



Figure 15. Current Limit Onset

Minimal input voltage overshoot appears in [Figure 15](#) because a local 100- μ F bypass capacitor and very short input leads were used. The input voltage would overshoot as the input current abruptly drops in a typical application due to the stored energy in the input distribution inductance. The exact waveforms seen in an application depend upon many factors including parasitics of the voltage distribution, circuit layout, and the short itself.

Automatic Restart (Figure 16)

The TPS2481 automatically initiates a restart after a fault has caused it to turn off the external FET. Internal control circuits use C_T to count 16 cycles before re-enabling the external FET. This sequence repeats if the fault persists. The TIMER has a 1:10 charge-to-discharge current ratio, and uses a 1-V lower threshold. The fault-retry duty cycle specification quantifies this behavior. This small duty cycle often reduces the average short-circuit power dissipation to levels associated with normal operation and reduces the need for additional protection devices.



Figure 16. TPS2480/81 Restart Cycle Timing

Low Voltage Application Design Example

The following example illustrates the design and component selection process for a 12-V, 40-A hotswap application. Figure 17 shows the application circuit for this design example.

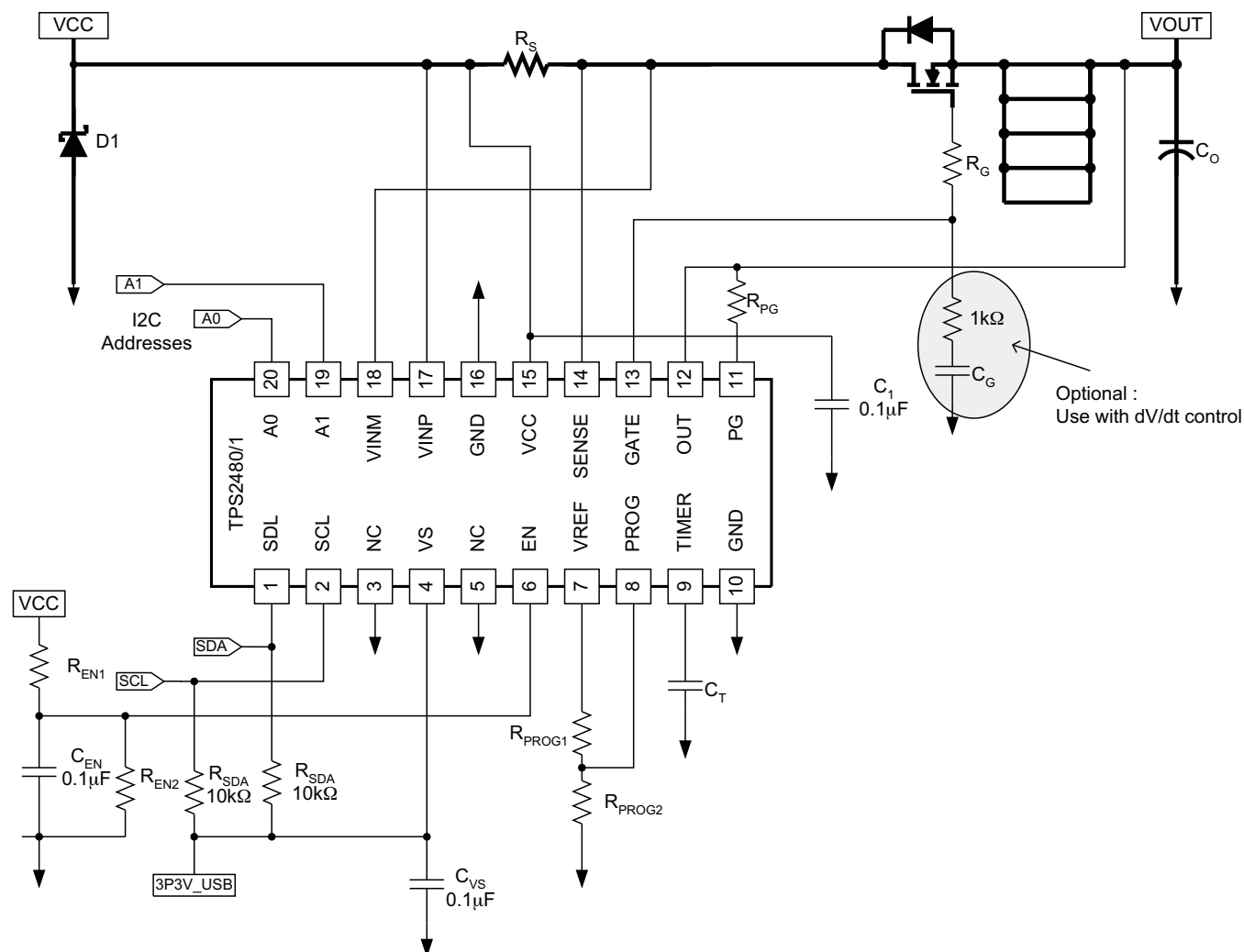


Figure 17. TPS2480/81 Low Voltage Design Example Schematic

1. Choose R_S

The following equation includes a factor of 1.2 (20%) for V_{SENSE} and R_S tolerance along with some additional margin.

$$R_S = \frac{V_{SENSE}}{1.2 \times I_{LIMIT}} = \frac{50mV}{1.2 \times 40A} = 1.042m\Omega \quad (5)$$

- Choose $R_S = 1\text{ m}\Omega$

$$I_{LIMIT(MAX)} = \frac{V_{SENSE(MAX)}}{R_S} = \frac{55mV}{1m\Omega} = 55A \quad (6)$$

$$R_S Power = I_{LIMIT(MAX)}^2 \times R_S = 55A^2 \times 1m\Omega = 3.025W \quad (7)$$

Multiple sense resistors in parallel should be considered.

2. Choose M1

Select the M1 V_{DS} rating allowing for maximum input voltage and transients. Then select an operating $R_{DS(on)}$, package, and cooling to control the operating temperature. Most manufacturers list $R_{DS(on)(MAX)}$ at 25°C and provide a derating curve from which values at other temperatures can be derived. The next equation can be used to estimate desired $R_{DS(on)(MAX)}$ at the maximum operating junction temperature of $T_{J(MAX)}$. ($T_{A(MAX)}$ is the maximum expected ambient temperature).

$$T_{J(MAX)} = 125C, T_{A(MAX)} = 50C, R_{\theta JA} = 10 \frac{C}{W}, I_{LIMIT(NOM)} = 50A \quad (8)$$

$$R_{DS(on)(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{R_{\theta JA} \times I_{LIMIT(NOM)}^2} = \frac{125C - 50C}{10 \frac{C}{W} \times (50A)^2} = 3m\Omega \quad (9)$$

The junction-to-ambient thermal resistance $R_{\theta JA}$, depends upon the package style chosen and the details of heat-sinking and cooling including the PCB. Actual “in-system” temperature measurements will be required to validate heat-sinking and cooling performance.

3. Choose the Power Limit P_{LIM} and the PROG Resistors, R_{PROG1} and R_{PROG2}

M1 dissipates large amounts of power during power-up or output short circuit. Power limit, P_{LIM} should be set to prevent M1 die temperature from exceeding a short term maximum temperature, $T_{J(MAX2)}$. Short term $T_{J(MAX2)}$ may be set as high as 150°C while still leaving ample margin for the typical manufacturer's rating of 175°C. P_{LIM} can be estimated as follows:

$$T_{J(MAX2)} = 150^{\circ}C, T_{A(MAX)} = 50^{\circ}C, R_{\theta CA} = 9.8 \frac{C}{W}, R_{\theta JC} = 0.2 \frac{C}{W}, R_{DS(on)} = 1.18 m\Omega \quad (10)$$

$$P_{LIM} = \frac{0.7 * (T_{J(MAX2)} - R_{\theta CA} \times I_{LIMIT(NOM)}^2 \times R_{DS(on)} - T_{A(MAX)})}{R_{\theta JC}} = 249W \quad (11)$$

Where $R_{\theta CA}$ is M1+PCB case-to-ambient thermal resistance, $R_{\theta JC}$ is M1 junction-to-case thermal resistance, $R_{DS(on)}$ is M1 channel resistance at the maximum operating temperature, and the factor of 0.7 accounts for the tolerance of the constant power engine. The maximum power limit for the constant power engine, $P_{LIM(MAX)}$ and nominal power $P_{OUT(nom)}$ settings for this circuit are calculated with the next equation:

$$V_{REF} = 4V, R_S = 1m\Omega, V_{OUT(NOM)} = 12V, I_{LIMIT(NOM)} = 50A \quad (12)$$

$$P_{LIM(MAX)} = \frac{1V \times V_{REF}}{2 \times R_S} = 2kW \quad (13)$$

$$P_{OUT(NOM)} = V_{OUT(NOM)} \times I_{LIMIT(NOM)} = 12V \times 50A = 600W \quad (14)$$

The PROG resistors should be chosen using the smallest of P_{LIM} , $P_{LIM(MAX)}$, or $P_{LIM(MAX)}$ values. Choose $R_{PROG2} = 20 k\Omega$. Choose R_{PROG1} as shown below.

$$V_{PROG} = \frac{2 \times P_{LIM(ACT)} \times R_S}{1V} = \frac{2 \times 249W \times 1m\Omega}{1V} = 0.498V \quad (15)$$

$$R_{PROG1} = R_{PROG2} \times \left(\frac{V_{REF}}{V_{PROG}} - 1 \right) = 140.6k\Omega \quad (16)$$

- Choose $R_{PROG1} = 140 k\Omega$

The power and current limit curve for this configuration is shown in [Figure 18](#).

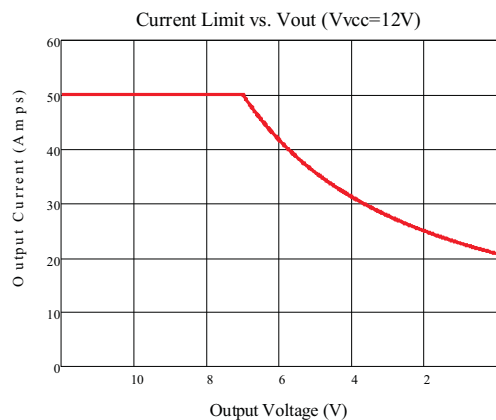


Figure 18. TPS2480/81 Power and Current Limit Curve

4. Choose the Timer Capacitor, C_T and Turn On Time

The turn on time t_{ON} , represents the time it takes the circuit to charge up the output capacitance C_O and load. C_T programs the fault time and should be chosen so that the fault timer does not terminate prior to completion of start up. The turn on time is a function of the type of control; current limit, power limit, or dV/dt control. The next equation calculates t_{ON} for both the power limit and current limit cases and assumes that only C_O draws current during startup.

$$\text{For } P_{LIM(ACT)} < V_{VCC(MAX)} \times I_{LIMIT(NOM)} : t_{ON} = \frac{C_O \times P_{LIM(ACT)}}{2 \times I_{LIMIT(NOM)}^2} + \frac{C_O \times V_{VCC(MAX)}^2}{2 \times P_{LIM(ACT)}} \quad (17)$$

$$\text{For } P_{LIM(ACT)} \geq V_{VCC(MAX)} \times I_{LIMIT(NOM)} : t_{ON} = \frac{C_O \times V_{VCC(MAX)}}{I_{LIMIT(NOM)}} \quad (18)$$

$$t_{ON} = \frac{C_O \times P_{LIM(ACT)}}{2 \times I_{LIMIT(NOM)}^2} + \frac{C_O \times V_{VCC(MAX)}^2}{2 \times P_{LIM(ACT)}} = \frac{1000\mu F \times 249W}{2 \times 50^2 A} + \frac{1000\mu F \times 13.5V^2}{2 \times 249W} = 416\mu s \quad (19)$$

The next equation allows C_T to be selected assuming that only C_O draws current during startup. TPS2480/81 timer current source and capacitor tolerances are accounted for.

$$C_T = \frac{I_{SOURCE(MAX)}}{V_{TMR-TH(MAX)}} \times t_{ON} \times (1 + C_{O-TOL} + C_{T-TOL}) \quad (20)$$

$$C_T = \frac{34\mu A}{4.1V} \times 416\mu s \times (1 + 0.2 + 0.1) = 4.48nF \quad (21)$$

- Choose $C_T = 0.01 \mu F$

5. Choose the Turn On Voltage, V_{ON} and the EN Resistors, R_{EN1} and R_{EN2}

When the EN pin is used as an analog control, the desired turn on voltage, V_{ON} can be used to select the EN resistors. Select R_{EN1} and R_{EN2} taking into account device leakage currents. Choose $R_{EN2} = 10 k\Omega$.

$$R_{EN1} = R_{EN2} \times \left(\frac{V_{ON}}{V_{EN_H(MAX)}} - 1 \right) = 55.22k\Omega \quad (22)$$

- Choose $R_{EN2} = 54.9 k\Omega$

The actual turn on and turn off voltages, $V_{ON(ACT)}$ and $V_{OFF(ACT)}$ can be calculated as follows:

$$V_{ON} = V_{EN_H(MAX)} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}}, V_{OFF} = V_{EN_L(MIN)} \times \frac{R_{EN1} + R_{EN2}}{R_{EN2}} \quad (23)$$

$$V_{ON} = 1.38V \times \frac{54.9k\Omega + 10k\Omega}{10k\Omega} = 8.96V \quad (24)$$

$$V_{OFF} = 1.22V \times \frac{54.9k\Omega + 10k\Omega}{10k\Omega} = 7.92V \quad (25)$$

Alternative Inrush Designs

Gate Capacitor (dV/dt) Control

The TPS2480/81 can be configured to provide a linear dV/dt turn on characteristic. The load capacitor charging current I_{CHARGE} , is controlled by a single capacitor from the GATE terminal to ground. M1 operates as a source follower (following the gate voltage) in this implementation. Choose a charge time, t_{ON} , based on the load capacitor, C_O input voltage V_I , and desired charge current. When power limiting is used ($V_{\text{PROG}} < V_{\text{REF}}$) choose I_{CHARGE} to be less than $P_{\text{LIM}} / V_{\text{VCC}}$ to prevent the fault timer from starting. The fault timer starts only if power or current limit is invoked.

$$t_{\text{ON}} = \frac{C_O \times V_{\text{VCC}}}{I_{\text{CHARGE}}} \quad (26)$$

Use the following equation to select the gate capacitance, C_G . C_{ISS} is the gate capacitance of M1, and I_{GATE} is the TPS2480/81 nominal gate charge current. As shown in [Figure 17](#), a series resistor of about 1 kΩ should be used in series with C_G .

$$C_G = \frac{I_{\text{GATE}} \times t_{\text{ON}}}{V_{\text{VCC}}} - C_{\text{ISS}} \quad (27)$$

If neither power nor current limit faults are invoked during turn on, C_T can be chosen for fast transient turn off response using the M1 SOA curve. Choose the single pulse time conservatively from the M1 SOA curve using maximum operating voltage and maximum trip current.

PROG Inrush Control

A capacitor can be connected from the PROG pin to ground to reduce the initial current step seen in [Figure 12](#). This method maintains a relatively fast turn-on time without the drawbacks of a gate-to-ground capacitor that include increased short circuit response time and less predictable gate clamping.

High Voltage Application Example

The TPS2480/81 can be used to monitor current from a voltage source greater than 26 V by using the OPAMP circuit shown in [Figure 19](#).

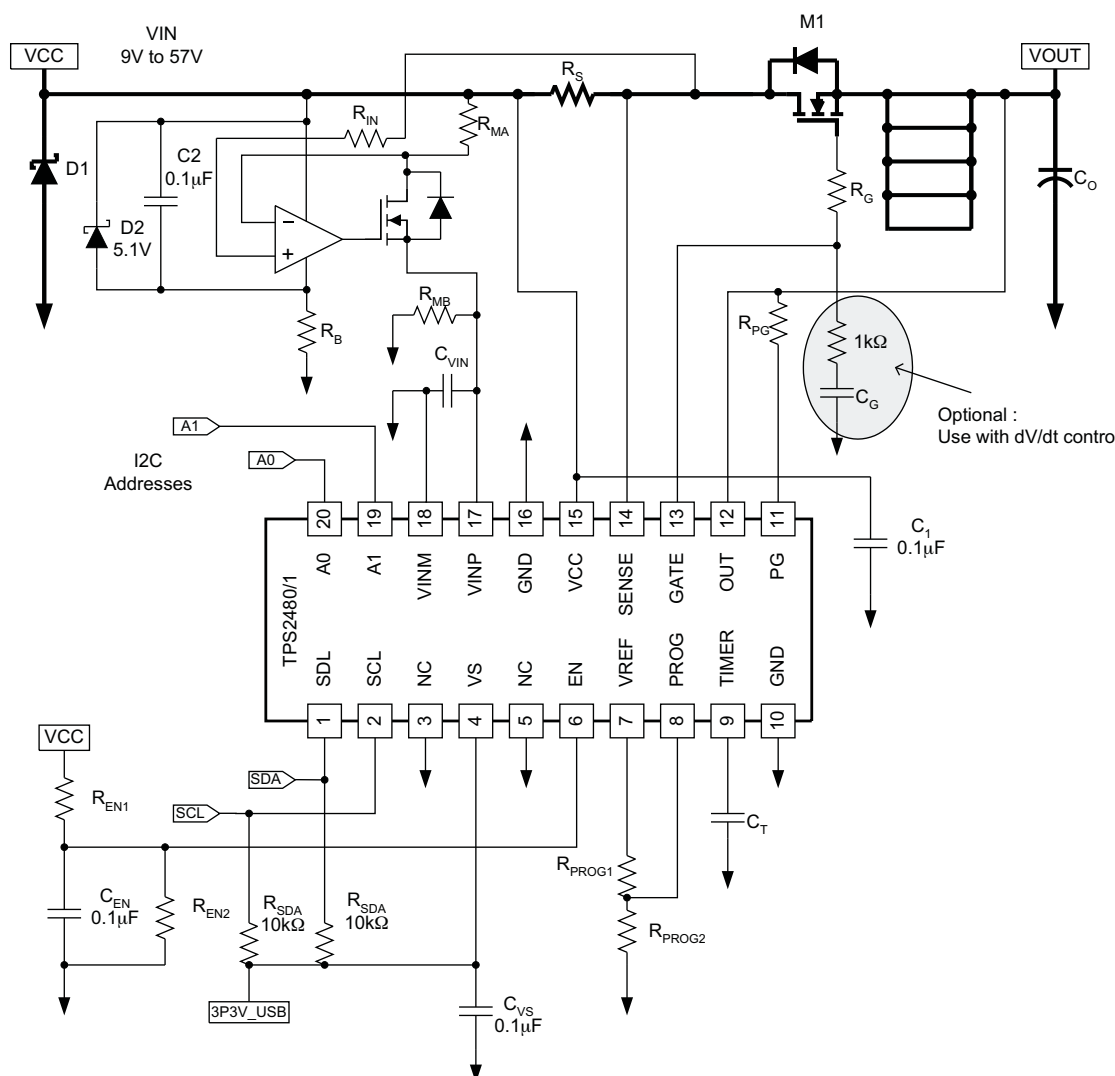


Figure 19. TPS2480/81 High Voltage application

The basic operating principle of U2, Q1, R_{MA}, and R_{MB} is to mirror the voltage seen across R_S from a VCC referenced voltage to a GND referenced voltage. As load current flows through R_S, the voltage input to U2-3 decreases and the output of U2/Q1 as seen at Q1-S follows this sense voltage. Ideally, the voltage drop across R_{MA} mirrors the voltage drop across R_S. Current flow through R_{MB} will mirror current flow through R_{MA}, and if R_{MA} = R_{MB} then the sense voltage across R_S is mirrored at VINP.

Since only a small voltage will be across R_{MA} and R_{MB} , their nominal value should be fairly low to offset input bias current effects (I_{VINP}). TPS2480/1 input bias current sums with the current that flows through R_{MA} increasing the voltage drop across R_{MB} . To block the bias current from R_{MB} , an additional buffer may be inserted between Q1-D and VINP. Using a network type resistor for R_{MA} and R_{MB} designed with temperature coefficient tracking will provide good voltage mirroring.

U2 should be a high quality, low drift operational amplifier. The OPA333AID provides low input voltage offset and very low drift over time and temperature. U2 is referenced to VCC through D2 and R_B and can operate from rail to rail.

Additional Design Considerations

Use of PG

Use the PG pin to control and sequence a downstream DC/DC converter. If this is not done a long time delay may be needed to allow C_O to fully charge before the converter starts.

Output Clamp Diode

Inductive loads on the output may drive the OUT pin below GND when the circuit is unplugged or during current limit. The OUT pin ratings can be maintained with a small diode such as an S1B, between the TPS2480/81 OUT to GND pins.

Gate Clamp Diode

The TPS2480/81 has a relatively well-regulated gate voltage of 12 V to 16 V, even at low supply voltages. A small clamp Zener from gate to source of M1, such as a BZX84C7V5, is recommended if V_{GS} of M1 is rated below this.

High Gate Capacitance Applications

Gate voltage overstress and large fault current spikes can be caused by large gate capacitance. An external gate clamp Zener diode is recommended if the total gate capacitance of M1 exceeds 4000 pF. When gate capacitor dV/dT control is used, a 1-k Ω resistor in series with C_G is recommended, as shown in [Figure 17](#). If the series R-C combination is used for MOSFETs with C_{ISS} less than 3000 pF, then a Zener is not required.

Output Short Circuit Measurements

Repeatable short-circuit testing results are difficult to obtain. The many details of source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to varying results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet since every setup differs.

Applications using the retry feature (TPS2481)

Applications using the retry feature may want to estimate fault retry time. The TPS2481 will retry (enable M1 to attempt turn on) once for every 16 timer charge/discharge cycles (15 cycles between 1 V and 4 V, 1 cycle between 0 V and 4 V).

$$T_{\text{RETRY}} = C_T \times \left[V_{\text{TMRHI(NOM)}} + 15 \times (V_{\text{TMRHI(NOM)}} - V_{\text{TMRLO(NOM)}}) \right] \times \left[\frac{1}{I_{\text{SOURCE(NOM)}}} + \frac{1}{I_{\text{SINK(NOM)}}} \right] \quad (28)$$

$$T_{\text{RETRY}} = C_T \times 21.56 \times 10^6 \quad (29)$$

NOTE

[Equation 29](#) simplified - assumes no error.

Layout Considerations

Good layout practice places the power devices D1, R_S, M1, and C_O so power flows in a sequential, linear fashion. A ground plane under the power and the TPS2480/81 is desirable. The TPS2480/81 should be placed close to the sense resistor and MOSFET using a Kelvin type connection to achieve accurate current sensing across R_S. A low-impedance GND connection is required because the TPS2480/81 can momentarily sink upwards of 100 mA from the gate of M1. The GATE amplifier has high bandwidth while active, so keep the GATE trace length short. The PROG, TIMER, and EN pins have high input impedances, therefore keep their input leads short. Oversize power traces and power device connections to assure low voltage drop and good thermal performance.

Power, Current, and Voltage Monitoring (PIV)

The TPS2480/81 digital current-shunt monitor has an I²C / SMBus-compatible interface. It provides digital current, voltage, and power readings for accurate decision-making in precisely-controlled systems. Programmable registers allow flexible configuration for measurement resolution, and continuous versus-triggered operation. Detailed register information appears in the Register Information Section. See the Register Block Diagram for a block diagram of the TPS2480 / 81 PIV monitoring circuits.

PIV Monitoring - Typical Application Circuit Considerations

[Figure 17](#) shows a typical application circuit for the TPS2480/81. 0.1-μF ceramic capacitors must be placed as close as possible to the supply and ground pins for supply bypassing.

The pull-up resistors shown on the SDA and SCL lines are not needed if there are pull-up resistors on these same lines elsewhere in the system. Resistor values shown are typical: consult the I²C or SMBus specification to determine acceptable values.

I²C Bus Overview

The I²C and SMBus protocols are essentially compatible with each other and the TPS2480/81 are compatible with both. This allows use of the I²C interface throughout this data sheet as the primary example, with SMBus protocol specified only when there is a difference.

Two bidirectional lines, SCL and SDA, connect the TPS2480 / 81 to the bus. Both SCL and SDA are open-drain connections. The device that initiates the transfer is called a master, and the devices controlled by the master are slaves. The bus must be controlled by a master device that generates the serial clock (SCL), controls, the bus access, and generates START and STOP conditions.

To address a specific device, the master initiates a START condition by pulling SDA from a HIGH to a LOW logic level while SCL is HIGH. All slaves on the bus shift in the slave address byte on the rising edge of SCL, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the slave being addressed responds to the master by generating an Acknowledge and pulling SDA LOW.

Data transfer is then initiated and eight bits of data are sent, followed by an Acknowledge bit. During data transfer, SDA must remain stable while SCL is HIGH. Any change in SDA while SCL is HIGH is interpreted as a START or STOP condition.

Once all data have been transferred, the master generates a STOP condition, indicated by pulling SDA from LOW to HIGH while SCL is HIGH. The TPS2480/81 includes a 28-ms timeout on its interface to prevent locking up an SMBus.

Serial Bus Address

To communicate with the TPS2480/81, the master must first address slave devices via a slave address byte. The slave address byte consists of seven address bits, and a direction bit indicating the intent of executing a read or write operation.

The TPS2480/81 have two address pins, A0 and A1. [Table 2](#) describes the pin logic levels for each of the 16 possible addresses. The state of pins A0 and A1 is sampled on every bus communication and should be set before any activity on the interface occurs. The address pins are read at the start of each communication event.

Table 2. TPS2480/81 Address Pins and Slave Addresses

A1	A0	SLAVE ADDRESS
GND	GND	1000000
GND	V _{S+}	1000001
GND	SDA	1000010
GND	SCL	1000011
V _{S+}	GND	1000100
V _{S+}	V _{S+}	1000101
V _{S+}	SDA	1000110
V _{S+}	SCL	1000111
SDA	GND	1001000
SDA	V _{S+}	1001001
SDA	SDA	1001010
SDA	SCL	1001011
SCL	GND	1001100
SCL	V _{S+}	1001101
SCL	SDA	1001110
SCL	SCL	1001111

Serial Interface

The TPS2480/81 operates only as a slave device on the I²C bus and SMBus. Connections to the bus are made via the open-drain I/O lines SDA and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TPS2480/81 support the transmission protocol for fast (1 kHz to 400 kHz) and high-speed (1 kHz to 3.4 MHz) modes. All data bytes are transmitted most significant byte first.

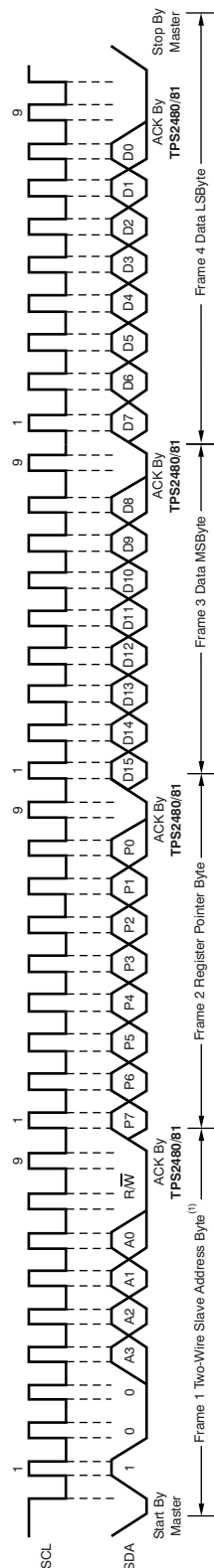
Writing To/Reading From The TPS2480/81

Accessing a particular register on the TPS2480/81 is accomplished by writing the appropriate value to the register pointer. Refer to [Table 4](#) for a complete list of registers and corresponding addresses. The value for the register pointer as shown in [Figure 20](#) is the first byte transferred after the slave address byte with the R/W bit LOW. Every write operation to the TPS2480/81 requires a value for the register pointer.

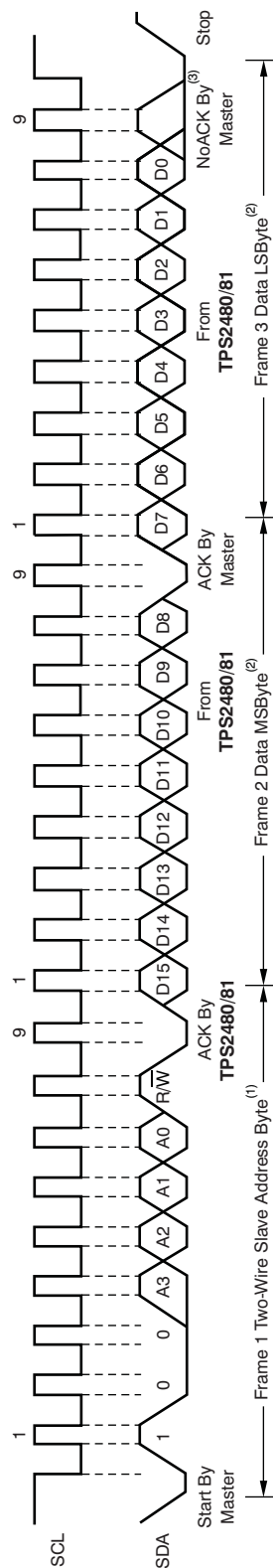
Writing to a register begins with the first byte transmitted by the master. This byte is the slave address, with the R/W bit LOW. The TPS2480/81 then acknowledges receipt of a valid address. The next byte transmitted by the master is the address of the register to which data will be written. This register address value updates the register pointer to the desired register. The next two bytes are written to the register addressed by the register pointer. The TPS2480/81 acknowledges receipt of each data byte. The master may terminate data transfer by generating a START or STOP condition.

When reading from the TPS2480/81, the last value stored in the register pointer by a write operation determines which register is read during a read operation. To change the register pointer for a read operation, a new value must be written to the register pointer. This write is accomplished by issuing a slave address byte with the R/W bit LOW, followed by the register pointer byte. No additional data are required. The master then generates a START condition and sends the slave address byte with the R/W bit HIGH to initiate the read command. The next byte is transmitted by the slave and is the most significant byte of the register indicated by the register pointer. This byte is followed by an Acknowledge from the master; then the slave transmits the least significant byte. The master acknowledges receipt of the data byte. The master may terminate data transfer by generating a Not-Acknowledge after receiving any data byte, or generating a START or STOP condition. If repeated reads from the same register are desired, it is not necessary to continually send the register pointer bytes; the TPS2480/81 retains the register pointer value until it is changed by the next write operation.

[Figure 20](#) and [Figure 21](#) show write and read operation timing diagrams, respectively. Note that register bytes are sent most-significant byte first, followed by the least significant byte. [Figure 22](#) shows the timing diagram for the SMBus Alert response operation. [Figure 23](#) illustrates a typical register pointer configuration.



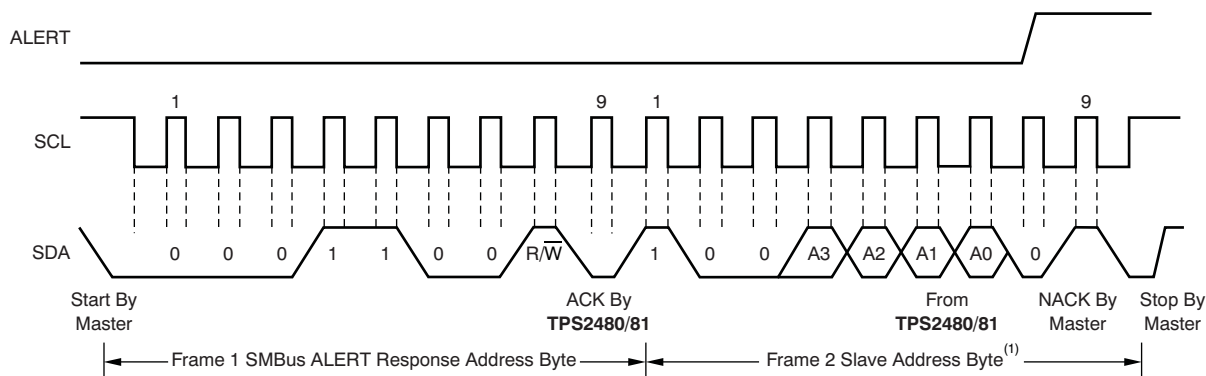
NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.



- NOTES: (1) The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.
(2) Read data is from the last register pointer location. If a new register is desired, the register pointer must be updated. See Figure 19.
(3) ACK by Master can also be sent.

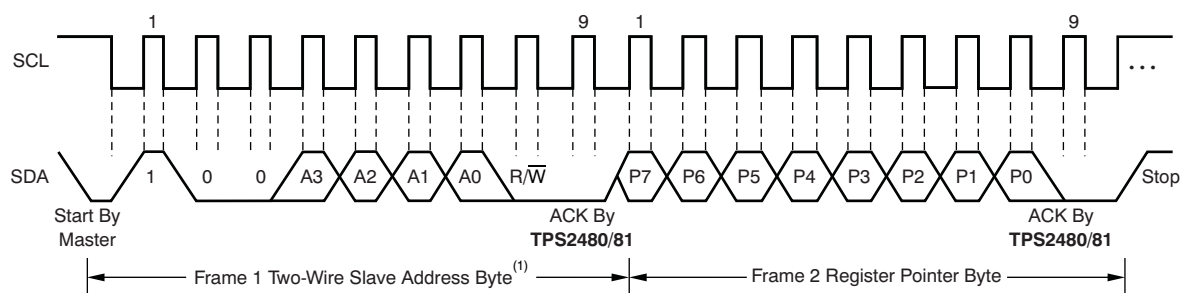
Figure 20. Timing Diagram for Write Word Format

Figure 21. Timing Diagram for Read Word Format



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 22. Timing Diagram for SMBus ALERT



NOTE (1): The value of the Slave Address Byte is determined by the settings of the A0 and A1 pins. Refer to Table 1.

Figure 23. Typical Register Pointer Set

High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pull-up devices. The master generates a start condition followed by a valid serial byte containing High-Speed (HS) master code 00001XXX. This transmission is made in fast (400 kbps) or standard (100 kbps) (F/S) mode at no more than 400 kbps. The TPS2480/81 does not acknowledge the HS master code, but does recognize it and switches its internal filters to support 3.4-Mbps operation.

The master then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 3.4 Mbps are allowed. Instead of using a stop condition, repeated start conditions should be used to secure the bus in HS-mode. A stop condition ends the HS-mode and switches all the internal filters of the TPS2480/81 to support the F/S mode.

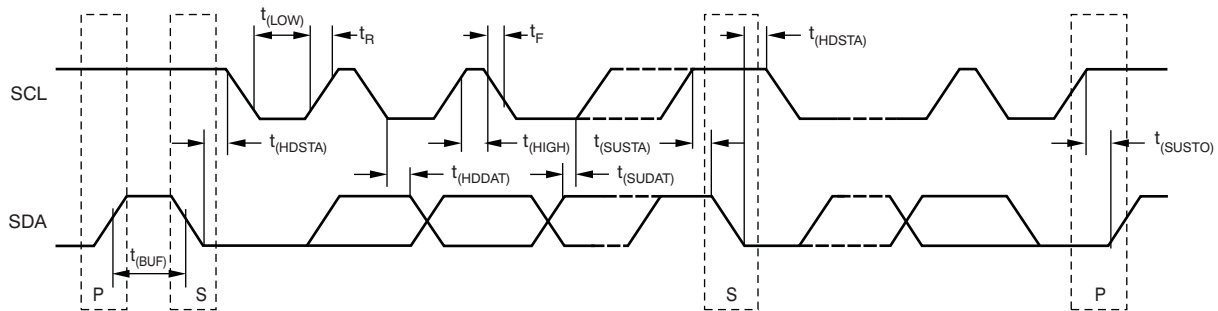


Figure 24.

Table 3.

PARAMETER		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	0.001	0.4	0.001	3.4	MHz
$T_{(BUF)}$	Bus free time between STOP and START condition	600		160		ns
$T_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	100		100		ns
$T_{(SUSTA)}$	Repeated START condition setup time	100		100		ns
$T_{(SUSTO)}$	STOP condition setup time	100		100		ns
$T_{(HDDAT)}$	Data hold time	0		0		ns
$T_{(SUDAT)}$	Data setup time	100		10		ns
$T_{(LOW)}$	SCL clock LOW period	1300		160		ns
$T_{(HIGH)}$	SCL clock HIGH period	600		60		ns
t_F	Clock/data fall time		300		160	ns
t_R / t_R	Clock/data rise time clock/data rise time for SCLK \leq 100kHz		300/1000		160	ns/ns

Power-Up Conditions

Power-up conditions are caused by a software reset via the R_{ST} bit (bit 15) in the Configuration Register, or the I²C bus General Call Reset.

ADC Operation

The two analog inputs to the TPS2480/81, VINP and VINM, connect to a shunt resistor in the bus of interest. The TPS2480/81 is typically powered by a separate supply from 3 V to 5.5V. The bus being sensed can vary from 0 V to 26 V. There are no special considerations for power-supply sequencing (for example, a bus voltage can be present with the supply voltage off, and vice-versa). The TPS2480/81 senses the small drop across the shunt for shunt voltage, and senses the voltage with respect to ground from VIN– for the bus voltage. [Figure 25](#) illustrates this operation.

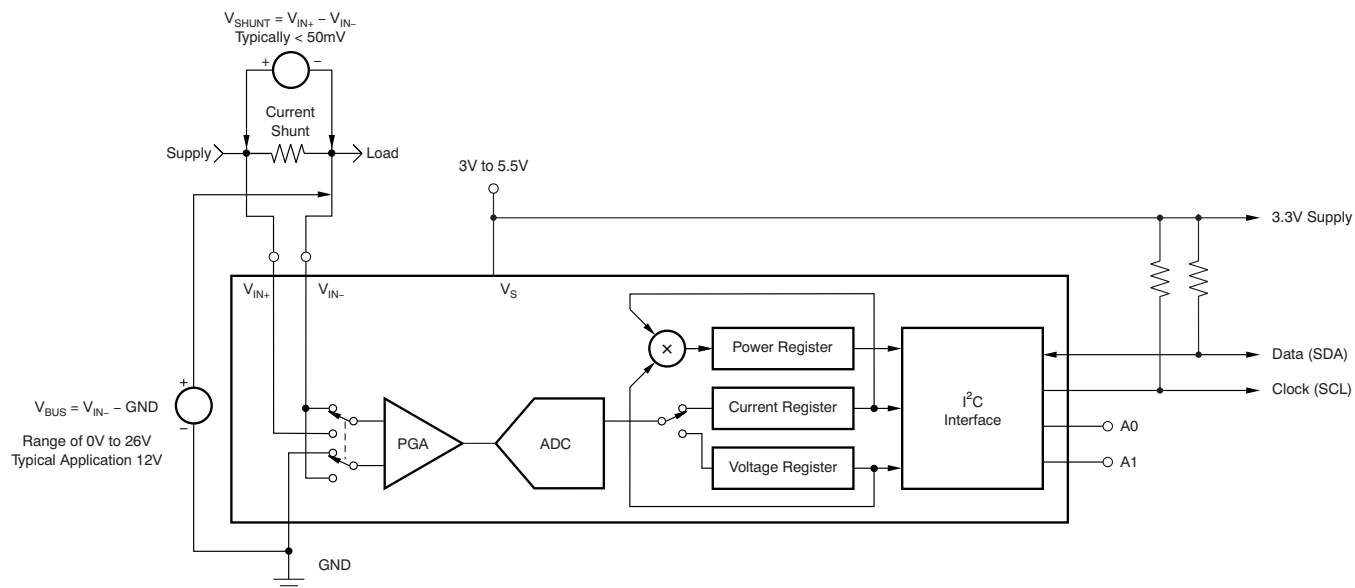


Figure 25. TPS2480/81 Configured For Current and Voltage Measurement

When the TPS2480/81 is in the normal operating mode (that is, MODE bits of the Configuration Register are set to '111'), it continuously converts the shunt voltage up to the number set in the shunt voltage averaging function (Configuration Register, SADC bits). The device then converts the bus voltage up to the number set in the bus voltage averaging (Configuration Register, BADC bits). The Mode control in the Configuration Register also permits selecting modes to convert only voltage or current, either continuously or in response to an event (triggered).

All current and power calculations are performed in the background and do not contribute to conversion time; conversion times shown in the Electrical Characteristics table can be used to determine the actual conversion time.

Power-Down mode reduces the quiescent current and turns off current into the TPS2480/81 inputs, avoiding any supply drain. Full recovery from Power-Down requires 40 μ s. ADC Off mode (set by the Configuration Register, MODE bits) stops all conversions.

In triggered mode, the external Convert line becomes active. Convert commands are initiated by taking the Convert line low for a minimum of 4 μ s. The Convert line may be connected high when unused. Any re-trigger of the Convert line during a conversion is ignored, and the Convert line state is disregarded until the conversion ends. There are several available triggered modes; however, all conversions are performed repeatedly up to the number set in the Averaging function (Configuration Register, BADC and SADC bits).

If the Convert line is held low, writing any of the triggered convert modes into the Configuration Register (even if the desired mode is already programmed into the register) triggers a single-shot conversion.

Although the TPS2480/81 can be read at any time, and the data from the last conversion remain available, the Conversion Ready bit (Status Register, CNVR bit) is provided to help co-ordinate one-shot or triggered conversions. The Conversion Ready bit is set after all conversions, averaging, and multiplication operations are complete.

The Conversion Ready bit clears under these conditions:

1. Writing to the Configuration Register, except when configuring the MODE bits for Power Down or ADC off (Disable) modes;
2. Reading the Status Register; or
3. Triggering a single-shot conversion with the Convert pin.

Power Measurement

Current and bus voltage are converted at different points in time, depending on the resolution and averaging mode settings. For instance, when configured for 12-bit and 128 sample averaging, up to 68 ms in time between sampling these two values is possible. Again, these calculations are performed in the background and do not add to the overall conversion time.

PGA Function

If larger full-scale shunt voltages are desired, the TPS2480/81 provides a PGA function that increases the full-scale range up to 2, 4, or 8 times (320 mV). Additionally, the bus voltage measurement has two full-scale ranges: 16 V or 32 V.

Filtering and Input Considerations

Measuring current can be noisy, and such noise can be difficult to define.

The internal ADC has a delta-sigma ($\Delta\Sigma$) front-end with a 500-kHz ($\pm 30\%$) typical sampling rate. This architecture has good inherent noise rejection. However, transients that occur at or very close to the sampling rate harmonics can cause problems. Because these signals are at 1 MHz and higher, they can be dealt with by incorporating filtering at the input of the TPS2480/81. The high frequency enables the use of low-value series resistors on the filter for reducing effects on measurement accuracy. In general, filtering the TPS2480/81 input is only necessary if there are transients at exact harmonics of the 500-kHz ($\pm 30\%$) sampling rate (>1 MHz). Filter using the lowest possible series resistance and ceramic capacitor. Recommended values are 0.1 μF to 1.0 μF .

Overload conditions are another consideration for the TPS2480/81 inputs. The TPS2480/81 inputs are specified to tolerate 26 V across the inputs. A large differential scenario might be a short to ground on the load side of the shunt. This type of event can result in full power-supply voltage across the shunt (as long the power supply or energy storage capacitors support it). It must be remembered that removing a short to ground can result in inductive kickbacks that could exceed the 26-V differential and common-mode rating of the TPS2480/81. Inductive kickback voltages are best dealt with by zener-type transient-absorbing devices (commonly called transzorbs) combined with sufficient energy storage capacitance.

In applications that do not have large energy storage electrolytics on one or both sides of the shunt, an input overstress condition may result from an excessive dV/dt of the voltage applied to the input. A hard physical short is the most likely cause of this event, particularly in applications with no large electrolytics present. This problem occurs because an excessive dV/dt can activate the ESD protection in the TPS2480/81 in systems where large currents are available.

Simple Current Shunt Monitor Usage (No Programming Necessary)

The TPS2480/81 can be used without any programming if it is only necessary to read a shunt voltage drop and bus voltage with the default 12-bit resolution, 320-mV shunt full-scale range (PGA = $\div 8$), 32-V bus full-scale range, and continuous conversion of shunt and bus voltage.

Without programming, current is measured by reading the shunt voltage. The Current Register and Power Register are only available if the Calibration Register contains a programmed value.

Programming the TPS2480/81

The default power-up states of the registers are shown in the register information section. These registers are volatile, and if programmed to other than default values, must be re-programmed at every device power-up. Detailed information on programming the Calibration Register specifically is given in the Programming the TPS2480/81 Power Measurement Engine section.

Programming The TPS2480/81 Power Measurement Engine

Calibration Register and Scaling

The Calibration Register makes it possible to set the scaling of the Current and Power Registers to whatever values are most useful for a given application. One strategy may be to set the Calibration Register such that the largest possible number is generated in the Current Register or Power Register at the expected full-scale point; this approach yields the highest resolution. The Calibration Register can also be selected to provide values in the Current and Power Registers that either provide direct decimal equivalents of the values being measured, or yield a round LSB number. After these choices have been made, the Calibration Register also offers possibilities for end user system-level calibration, where the value is adjusted slightly to cancel total system error.

Below are two examples for configuring the TPS2480/81 calibration. Both examples are written so the information directly relates to the calibration setup found in the TPS2480/81EVM software.

Calibration Example 1: Calibrating the TPS2480/81 With No Possibility for Overflow

NOTE

The numbers used in this example are the same used with the TPS2480/81EVM software as shown in [Figure 26](#). This does not mean the input can go over 26 V!

1. Establish the following parameters:

$$V_{BUS_MAX} = 32, \text{ This does not mean the input can go over 26 V!}$$

$$V_{SHUNT_MAX} = 0.32$$

$$R_{SHUNT} = 0.5$$

2. Using [Equation 30](#), determine the maximum possible current .

$$\text{MaxPossible_I} = \frac{V_{SHUNT_MAX}}{R_{SHUNT}}$$

$$\text{MaxPossible_I} = 0.64$$

(30)

3. Choose the desired maximum current value. This value is selected based on system expectations.

$$\text{Max_Expected_I} = 0.6$$

4. Calculate the possible range of current LSBs. To calculate this range, first compute a range of LSBs that is appropriate for the design. Next, select an LSB within this range. Note that the results will have the most resolution when the minimum LSB is selected. Typically, an LSB is selected to be the nearest round number to the minimum LSB value.

$$\text{Minimum_LSB} = \frac{\text{Max_Expected_I}}{32767}$$

$$\text{Minimum_LSB} = 18.311 \times 10^{-6}$$

(31)

$$\text{Maximum_LSB} = \frac{\text{Max_Expected_I}}{4096}$$

$$\text{Maximum_LSB} = 146.520 \times 10^{-6}$$

(32)

Choose an LSB in the range: Minimum_LSB < Selected_LSB < Maximum_LSB

$$\text{Current_LSB} = 20 \times 10^{-6}$$

NOTE

This value was selected to be a round number near the Minimum_LSB. This selection allows for good resolution with a rounded LSB.

5. Compute the Calibration Register value using [Equation 33](#):

$$\text{Cal} = \text{trunc} \left(\frac{0.04096}{\text{Current_LSB} \times R_{\text{SHUNT}}} \right)$$

$$\text{Cal} = 4096 \quad (33)$$

6. Calculate the Power LSB, using [Equation 34](#). [Equation 34](#) shows a general formula; because the bus voltage measurement LSB is always 4 mV, the power formula reduces to the calculated result.

$$\text{Power_LSB} = 20 \times \text{Current_LSB}$$

$$\text{Power_LSB} = 400 \times 10^{-6} \quad (34)$$

7. Compute the maximum current and shunt voltage values (before overflow), as shown by [Equation 35](#) and [Equation 36](#). Note that both [Equation 35](#) and [Equation 36](#) involve an *If - then* condition:

$$\text{Max_Current} = \text{Current_LSB} \times 32767$$

$$\text{Max_Current} = 0.65534 \quad (35)$$

If $\text{Max_Current} \geq \text{Max Possible_I}$ then

$$\text{Max_Current_Before_Overflow} = \text{MaxPossible_I}$$

Else

$$\text{Max_Current_Before_Overflow} = \text{Max_Current}$$

End If

NOTE

(Max_Current is greater than MaxPossible_I in this example.)

Max_Current_Before_Overflow = 0.64 (Note: This result is displayed by software as seen in [Figure 26](#).)

$$\text{Max_ShuntVoltage} = \text{Max_Current_Before_Overflow} \times R_{\text{SHUNT}}$$

$$\text{Max_ShuntVoltage} = 0.32 \quad (36)$$

If Max_ShuntVoltage \geq V_{SHUNT_MAX}

$$\text{Max_ShuntVoltage_Before_Overflow} = V_{\text{SHUNT_MAX}}$$

Else

$$\text{Max_ShuntVoltage_Before_Overflow} = \text{Max_ShuntVoltage}$$

End If

$$\text{Max_ShuntVoltage_Before_Overflow} = 0.32$$

NOTE

This result is displayed by software as seen in [Figure 26](#).

(Max_ShuntVoltage is greater than V_{SHUNT_MAX} in this example.)

8. Compute the maximum power with [Equation 37](#).

$$\text{MaximumPower} = \text{Max_Current_Before_Overflow} \times V_{\text{BUS_MAX}}$$

$$\text{MaximumPower} = 20.48 \quad (37)$$

9. (Optional second Calibration step.) Compute corrected full-scale calibration value based on measured current.

$$\text{TPS2480/81_Current} = 0.0504$$

$$\text{MeasShuntCurrent} = 0.05006$$

$$\text{Corrected_Full_Scale_Cal} = \text{trunc} \left(\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{TPS2480/81_Current}} \right)$$

$$\text{Corrected_Full_Scale_Cal} = 4068 \quad (38)$$

Figure 26 illustrates how to perform the same procedure discussed in this example using the automated TPS2480/81EVM software.

NOTE

The same numbers used in the nine-step example are used in the software example in Figure 26. Also note that Figure 26 illustrates which results correspond to which step (for example, the information entered in Step 1 is enclosed in a box in Figure 26 and labeled). This does not mean the input can go over 26 V!

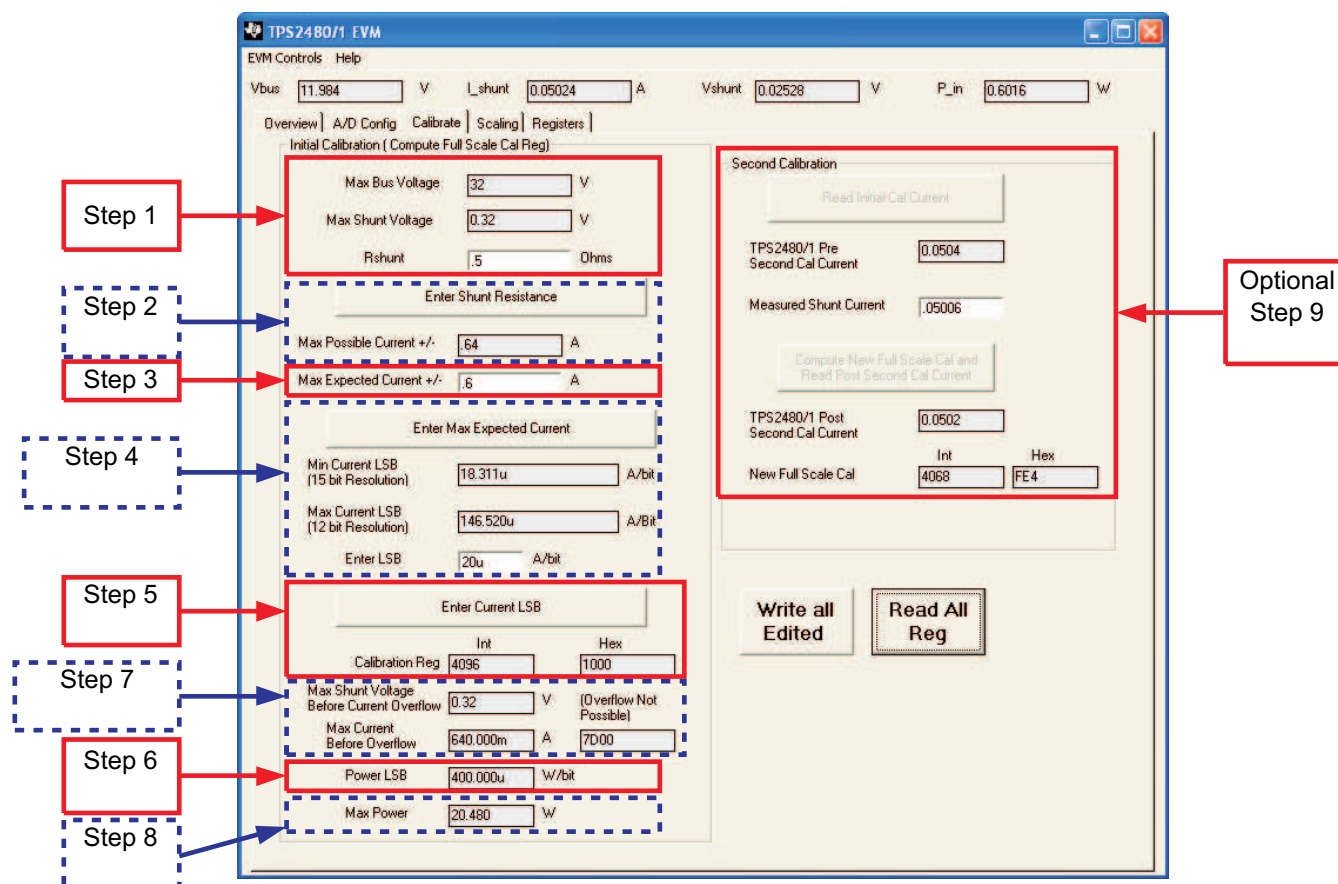


Figure 26. TPS2480/81 Calibration Software Automatically Computes Calibration Steps 1-9

Calibration Example 2 (Overflow Possible)

This design example uses the nine-step procedure for calibrating the TPS2480/81 where overflow is possible. [Figure 27](#) illustrates how the same procedure is performed using the automated TPS2480/81EVM software.

NOTE

(The same numbers used in the nine-step example are used in the software example in [Figure 27](#). Also note that [Figure 27](#) illustrates which results correspond to which step (for example, the information entered in Step 1 is circled in [Figure 27](#) and labeled).

1. Establish the following parameters:

$V_{BUS_MAX} = 32$, This does not mean the input can go over 26 V!

$V_{SHUNT_MAX} = 0.32$

$R_{SHUNT} = 0.001$

2. Determine the maximum possible current using [Equation 39](#):

$$\text{MaxPossible_I} = \frac{V_{SHUNT_MAX}}{R_{SHUNT}}$$

$$\text{MaxPossible_I} = 320$$

(39)

3. Choose the desired maximum current value: $\text{Max_Expected_I}, \leq \text{MaxPossible_I}$. This value is selected based on system expectations.

$$\text{Max_Expected_I} = 60$$

4. Calculate the possible range of current LSBs. This calculation is done by first computing a range of LSB's that is appropriate for the design. Next, select an LSB withing this range. Note that the results will have the most resolution when the minimum LSB is selected. Typically, an LSB is selected to be the nearest round number to the minimum LSB.

$$\text{Minimum_LSB} = \frac{\text{Max_Expected_I}}{32767}$$

$$\text{Minimum_LSB} = 1.831 \times 10^{-3}$$

(40)

$$\text{Maximum_LSB} = \frac{\text{Max_Expected_I}}{4096}$$

$$\text{Maximum_LSB} = 14.652 \times 10^{-3}$$

(41)

Choose an LSB in the range: $\text{Minimum_LSB} < \text{Selected_LSB} < \text{Maximum_LSB}$

$$\text{Current_LSB} = 1.9 \times 10^{-3}$$

NOTE

This value was selected to be a round number near the Minimum_LSB. This section allows for good resolution with a rounded LSB.

5. Compute the calibration register using [Equation 42](#):

$$\text{Cal} = \text{trunc} \left[\frac{0.04096}{\text{Current_LSB} \times R_{SHUNT}} \right] \quad \text{Cal} = 21557$$

(42)

6. Calculate the Power LSB using [Equation 43](#). [Equation 43](#) shows a general formula; because the bus voltage measurement LSB is always 4mV, the power formula reduces to calculate the result.

$$\text{Power_LSB} = 20 \times \text{Current_LSB}$$

$$\text{Power_LSB} = 38 \times 10^{-3}$$

(43)

7. Compute the maximum current and shunt voltage values (before overflow), as shown by [Equation 44](#) and [Equation 45](#). Note that both [Equation 44](#) and [Equation 45](#) involve an *If - then* condition.

$$\text{Max_Current} = \text{Current_LSB} \times 32767$$

$$\text{Max_Current} = 62.2573 \quad (44)$$

If $\text{Max_Current} \geq \text{Max Possible_I}$ then

$$\text{Max_Current_Before_Overflow} = \text{MaxPossible_I}$$

Else

$$\text{Max_Current_Before_Overflow} = \text{Max_Current}$$

End If

(Note that Max_Current is less than MaxPossible_I in this example.)

$\text{Max_Current_Before_Overflow} = 62.2573$ (Note: This result is displayed by software as seen in [Figure 27](#).)

$$\text{Max_ShuntVoltage} = \text{Max_Current_Before_Overflow} \times R_{\text{SHUNT}}$$

$$\text{Max_ShuntVoltage} = 0.0622573 \quad (45)$$

If $\text{Max_ShuntVoltage} \geq V_{\text{SHUNT_MAX}}$

$$\text{Max_ShuntVoltage_Before_Overflow} = V_{\text{SHUNT_MAX}}$$

Else

$$\text{Max_ShuntVoltage_Before_Overflow} = \text{Max_ShuntVoltage}$$

End If

(Note that Max_ShuntVoltage is less than $V_{\text{SHUNT_MAX}}$ in this example.)

$\text{Max_ShuntVoltage_Before_Overflow} = 0.0622573$ (Note: This result is displayed by software as seen in [Figure 27](#).)

8. Compute the maximum power with equation 8.

$$\text{MaximumPower} = \text{Max_Current_Before_Overflow} \times V_{\text{BUS_MAX}}$$

$$\text{MaximumPower} = 1992 \quad (46)$$

9. (Optional second calibration step.) Compute the corrected full-scale calibration value based on measured current.

$$\text{TPS2480/81_Current} = 25.2472$$

$$\text{MeasShuntCurrent} = 25.09$$

$$\text{Corrected_Full_Scale_Cal} = \text{trunc} \left(\frac{\text{Cal} \times \text{MeasShuntCurrent}}{\text{TPS2480/81_Current}} \right)$$

$$\text{Corrected_Full_Scale_Cal} = 21422 \quad (47)$$

Figure 27 illustrates how to perform the same procedure discussed in this example using the automated TPS2480/81EVM software.

NOTE

(The same numbers used in the nine-step example are used in the software example in Figure 27. Also note that Figure 27 illustrates which results correspond to which step (for example, the information entered in Step 1 is enclosed in a box in Figure 27 and labeled).

The screenshot shows the TPS2480/1 EVM software interface. The 'Initial Calibration (Compute Full Scale Cal Reg)' section contains the following steps:

- Step 1:** Max Bus Voltage: 32 V, Max Shunt Voltage: 0.32 V, Rshunt: 0.001 Ohms.
- Step 2:** Enter Shunt Resistance.
- Step 3:** Max Possible Current +/-: 320 A, Max Expected Current +/-: 60 A.
- Step 4:** Enter Max Expected Current.
- Step 5:** Enter Current LSB.
- Step 7:** Calibration Reg: 21557 (Int), 5435 (Hex).
- Step 6:** Power LSB: 38.000m W/bit.
- Step 8:** Max Power: 1.992K W.

The 'Second Calibration' section includes:

- Read Initial Cal Current: TPS2480/1 Pre Second Cal Current: 25.2472.
- Measured Shunt Current: 25.09.
- Compute New Full Scale Cal and Read Post Second Cal Current: TPS2480/1 Post Second Cal Current: 25.1009.
- New Full Scale Cal: 21422 (Int), 53AE (Hex).

Buttons at the bottom include 'Write all Edited' and 'Read All Reg'.

Figure 27. Calibration Software Automatically Computes Calibration Steps 1-9

REGISTER INFORMATION

The TPS2480/81 uses a bank of registers for holding configuration settings, measurement results, maximum/minimum limits, and status information. [Table 4](#) summarizes the TPS2480/81 registers; illustrates registers.

Register contents are updated 4 μ s after completion of the write command. Therefore, a 4- μ s delay is required between completion of a write to a given register and a subsequent read of that register (without changing the pointer) when using SCL frequencies in excess of 1 MHz.

Table 4. Summary of Register Set

POINTER ADDRESS HEX	REGISTER NAME	FUNCTION	POWER-ON RESET		TYPE ⁽¹⁾
			BINARY	HEX	
00	Configuration Register	All-register reset, settings for bus voltage range, PGA Gain, ADC resolution/averaging.	00111001 10011111	399F	R/ \overline{W}
01	Shunt Voltage	Shunt voltage measurement data.	Shunt voltage	—	R
02	Bus Voltage	Bus voltage measurement data.	Bus voltage	—	R
03	Power ⁽²⁾	Power measurement data.	00000000 00000000	0000	R
04	Current ⁽²⁾	Contains the value of the current flowing through the shunt resistor.	00000000 00000000	0000	R
05	Calibration	Sets full-scale range and LSB of current and power measurements. Overall system calibration.	00000000 00000000	0000	R/ \overline{W}

(1) Type: **R** = Read-Only, **R/ \overline{W}** = Read/Write.

(2) The Power Register and Current Register default to '0' because the Calibration Register defaults to '0', yielding a zero current value until the Calibration Register is programmed.

Register Details

All TPS2480/81 16-bit registers are actually two 8-bit registers.

Configuration Register 00h (Read/Write)

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	RST	—	BRNG	PG1	PG0	BADC4	BADC3	BADC2	BADC1	SADC4	SADC3	SADC2	SADC1	MODE3	MODE2	MODE1
POR VALUE	0	0	1	1	1	0	0	1	1	0	0	1	1	1	1	1

Bit Descriptions

RST: **Reset Bit**

Bit 15
Setting this bit to '1' generates a system reset that is the same as power-on reset. Resets all registers to default values; this bit self-clears.

BRNG: **Bus Voltage Range**

Bit 13
0 = 16-V FSR
1 = 32-V FSR (default value)

PG: **PGA (Shunt Voltage Only)**

Bits 11, 12
Sets PGA gain and range. Note that the PGA defaults to ÷8 (320-mV range). [Table 5](#) shows the gain and range for the various product gain settings.

Table 5. PG Bit Settings⁽¹⁾

PG1	PG0	GAIN	RANGE
0	0	1	±40 mV
0	1	÷2	±80 mV
1	0	÷4	±160 mV
1	1	÷8	±320 mV

(1) Shaded values are default.

BADC: **BADC Bus ADC Resolution/Averaging**

Bits 7–10
These bits adjust the Bus ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Bus Voltage Register (02h).

SADC:

Bits 3–6

SADC Shunt ADC Resolution/Averaging

These bits adjust the Shunt ADC resolution (9-, 10-, 11-, or 12-bit) or set the number of samples used when averaging results for the Shunt Voltage Register (01h).
BADC (Bus) and SADC (Shunt) ADC resolution/averaging and conversion time settings are shown in [Table 6](#).

Table 6. ADC Settings⁽¹⁾

ADC4	ADC3	ADC2	ADC1	MODE/SAMPLES	CONVERSION TIME
0	X ⁽²⁾	0	0	9-bit	84 µs
0	X ⁽²⁾	0	1	10-bit	148 µs
0	X ⁽²⁾	1	0	11-bit	276 µs
0	X ⁽²⁾	1	1	12-bit	532 µs
1	0	0	0	12-bit	532 µs
1	0	0	1	2	1.06 ms
1	0	1	0	4	2.13 ms
1	0	1	1	8	4.26 ms
1	1	0	0	16	8.51 ms
1	1	0	1	32	17.02 ms
1	1	1	0	64	34.05 ms
1	1	1	1	128	68.10 ms

(1) Shaded values are default.

(2) X = Don't care.

MODE:

Bits 0–2

Operating Mode

Selects continuous, triggered, or power-down mode of operation. These bits default to continuous shunt and bus measurement mode. The mode settings are shown in [Table 7](#).

Table 7. Mode Settings⁽¹⁾

MODE3	MODE2	MODE1	MODE
0	0	0	Power-down
0	0	1	Shunt voltage, triggered
0	1	0	Bus voltage, triggered
0	1	1	Shunt and bus, triggered
1	0	0	ADC off (disabled)
1	0	1	Shunt voltage, continuous
1	1	0	Bus voltage, continuous
1	1	1	Shunt and bus, continuous

(1) Shaded values are default.

Data Output Registers

Shunt Voltage Register 01h (Read-Only)

The Shunt Voltage Register stores the current shunt voltage reading, V_{SHUNT} . Shunt Voltage Register bits are shifted according to the PGA setting selected in the Configuration Register (00h). When multiple sign bits are present, they will all be the same value. Negative numbers are represented in two's complement format. Generate the two's complement of a negative number by complementing the absolute value binary number and adding 1. Extend the sign, denoting a negative number by setting the MSB = '1'. Extend the sign to any additional sign bits to form the 16-bit word.

Example: For a value of $V_{SHUNT} = -320$ mV:

1. Take the absolute value (include accuracy to 0.01mV) ==> 320.00
2. Translate this number to a whole decimal number ==> 32000
3. Convert it to binary ==> 111 1101 0000 0000
4. Complement the binary result : 000 0010 1111 1111
5. Add 1 to the Complement to create the Two's Complement formatted result ==> 000 0011 0000 0000
6. Extend the sign and create the 16-bit word: 1000 0011 0000 0000 = 8300h (Remember to extend the sign to all sign-bits, as necessary based on the PGA setting.)

At PGA = $\div 8$, full-scale range = ± 320 mV (decimal = 32000, positive value hex = 7D00, negative value hex = 8300), and LSB = 10 μ V.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SD14_8	SD13_8	SD12_8	SD11_8	SD10_8	SD9_8	SD8_8	SD7_8	SD6_8	SD5_8	SD4_8	SD3_8	SD2_8	SD1_8	SD0_8
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = $\div 4$, full-scale range = ± 160 mV (decimal = 16000, positive value hex = 3E80, negative value hex = C180), and LSB = 10 μ V.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SD13_4	SD12_4	SD11_4	SD10_4	SD9_4	SD8_4	SD7_4	SD6_4	SD5_4	SD4_4	SD3_4	SD2_4	SD1_4	SD0_4
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = $\div 2$, full-scale range = ± 80 mV (decimal = 8000, positive value hex = 1F40, negative value hex = E0C0), and LSB = 10 μ V.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SIGN	SD12_2	SD11_2	SD10_2	SD9_2	SD8_2	SD7_2	SD6_2	SD5_2	SD4_2	SD3_2	SD2_2	SD1_2	SD0_2
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At PGA = $\div 1$, full-scale range = ± 40 mV (decimal = 4000, positive value hex = 0FA0, negative value hex = F060), and LSB = 10 μ V.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	SIGN	SIGN	SIGN	SIGN	SD11_1	SD10_1	SD9_1	SD8_1	SD7_1	SD6_1	SD5_1	SD4_1	SD3_1	SD2_1	SD1_1	SD0_1
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 8. Shunt Voltage Register Format⁽¹⁾

V _{SHUNT} Reading (mV)	Decimal Value	PGA = ÷ 8 (D15.....D0)	PGA = ÷ 4 (D15.....D0)	PGA = ÷ 2 (D15.....D0)	PGA = ÷ 1 (D15.....D0)
320.02	32002	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.01	32001	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
320.00	32000	0111 1101 0000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.99	31999	0111 1100 1111 1111	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
319.98	31998	0111 1100 1111 1110	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
-	-	-	-	-	-
160.02	16002	0011 1110 1000 0010	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.01	16001	0011 1110 1000 0001	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
160.00	16000	0011 1110 1000 0000	0011 1110 1000 0000	0001 1111 0100 0000	0000 1111 1010 0000
159.99	15999	0011 1110 0111 1111	0011 1110 0111 1111	0001 1111 0100 0000	0000 1111 1010 0000
159.98	15998	0011 1110 0111 1110	0011 1110 0111 1110	0001 1111 0100 0000	0000 1111 1010 0000
-	-	-	-	-	-
80.02	8002	0001 1111 0100 0010	0001 1111 0100 0010	0001 1111 0100 0000	0000 1111 1010 0000
80.01	8001	0001 1111 0100 0001	0001 1111 0100 0001	0001 1111 0100 0000	0000 1111 1010 0000
80.00	8000	0001 1111 0100 0000	0001 1111 0100 0000	0001 1111 0100 0000	0000 1111 1010 0000
79.99	7999	0001 1111 0011 1111	0001 1111 0011 1111	0001 1111 0011 1111	0000 1111 1010 0000
79.98	7998	0001 1111 0011 1110	0001 1111 0011 1110	0001 1111 0011 1110	0000 1111 1010 0000
-	-	-	-	-	-
40.02	4002	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0010	0000 1111 1010 0000
40.01	4001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0001	0000 1111 1010 0000
40.00	4000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000	0000 1111 1010 0000
39.99	3999	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111	0000 1111 1001 1111
39.98	3998	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110	0000 1111 1001 1110
-	-	-	-	-	-
0.02	2	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010	0000 0000 0000 0010
0.01	1	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001	0000 0000 0000 0001
0	0	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000	0000 0000 0000 0000
-0.01	-1	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111	1111 1111 1111 1111
-0.02	-2	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110	1111 1111 1111 1110
-	-	-	-	-	-
-39.98	-3998	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010	1111 0000 0110 0010
-39.99	-3999	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001	1111 0000 0110 0001
-40.00	-4000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000	1111 0000 0110 0000
-40.01	-4001	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0101 1111	1111 0000 0110 0000
-40.02	-4002	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0101 1110	1111 0000 0110 0000
-	-	-	-	-	-
-79.98	-7998	1110 0000 1100 0010	1110 0000 1100 0010	1110 0000 1100 0010	1111 0000 0110 0000
-79.99	-7999	1110 0000 1100 0001	1110 0000 1100 0001	1110 0000 1100 0001	1111 0000 0110 0000
-80.00	-8000	1110 0000 1100 0000	1110 0000 1100 0000	1110 0000 1100 0000	1111 0000 0110 0000
-80.01	-8001	1110 0000 1011 1111	1110 0000 1011 1111	1110 0000 1100 0000	1111 0000 0110 0000
-80.02	-8002	1110 0000 1011 1110	1110 0000 1011 1110	1110 0000 1100 0000	1111 0000 0110 0000
-	-	-	-	-	-
-159.98	-15998	1100 0001 1000 0010	1100 0001 1000 0010	1110 0000 1100 0000	1111 0000 0110 0000
-159.99	-15999	1100 0001 1000 0001	1100 0001 1000 0001	1110 0000 1100 0000	1111 0000 0110 0000
-160.00	-16000	1100 0001 1000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
-160.01	-16001	1100 0001 0111 1111	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
-160.02	-16002	1100 0001 0111 1110	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
-	-	-	-	-	-
-319.98	-31998	1000 0011 0000 0010	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
-319.99	-31999	1000 0011 0000 0001	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
-320.00	-32000	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
-320.01	-32001	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000
-320.02	-32002	1000 0011 0000 0000	1100 0001 1000 0000	1110 0000 1100 0000	1111 0000 0110 0000

(1) Out-of-range values are shown in grey shading.

Bus Voltage Register 02h (Read-Only)

The Bus Voltage Register stores the most recent bus voltage reading, V_{BUS} .

At full-scale range = 32 V (decimal = 8000, hex = 1F40), and LSB = 4 mV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	BD12	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

At full-scale range = 16 V (decimal = 4000, hex = 0FA0), and LSB = 4 mV.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	0	BD11	BD10	BD9	BD8	BD7	BD6	BD5	BD4	BD3	BD2	BD1	BD0	—	CNVR	OVF
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CNVR:

Conversion Ready

Bit 1

Although the data from the last conversion can be read at any time, the TPS2480/81 Conversion Ready bit (CNVR) indicates when data from a conversion is available in the data output registers. The CNVR bit is set after all conversions, averaging, and multiplications are complete. CNVR will clear under the following conditions:

- 1) Writing a new mode into the Operating Mode bits in the Configuration Register (except for Power-Down or Disable)
- 2.) Reading the Power Register

OVF:

Math Overflow Flag

Bit 0

The Math Overflow Flag (OVF) is set when the Power or Current calculations are out of range. It indicates that current and power data may be meaningless.

Power Register 03h (Read-Only)

Full-scale range and LSB are set by the Calibration Register. See the *TPS2480/81 Power Measurement Engine* section.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	PD15	PD14	PD13	PD12	PD11	PD10	PD9	PD8	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The Power Register records power in watts by multiplying the values of the current with the value of the bus voltage according to the equation:

$$\text{Power} = \frac{\text{Current} \times \text{BusVoltage}}{5000}$$

Current Register 04h (Read-Only)

Full-scale range and LSB depend on the value entered in the Calibration Register. See the *TPS2480/81 Power Measurement Engine* section. Negative values are stored in two's complement format.

BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
BIT NAME	CSIGN	CD14	CD13	CD12	CD11	CD10	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The value of the Current Register is calculated by multiplying the value in the Shunt Voltage Register with the value in the Calibration Register according to the equation:

$$\text{Current} = \frac{\text{ShuntVoltage} \times \text{Calibration Register}}{4096}$$

Calibration Register

Calibration Register 05h (Read/Write)

Current and power calibration are set by bits D15 to D1 of the Calibration Register. Note that bit D0 is not used in the calculation. This register sets the current that corresponds to a full-scale drop across the shunt. Full-scale range and the LSB of the current and power measurement depend on the value entered in this register. See the *TPS2480/81 Power Measurement Engine* section. This register is suitable for use in overall system calibration. Note that the '0' POR values are all default.

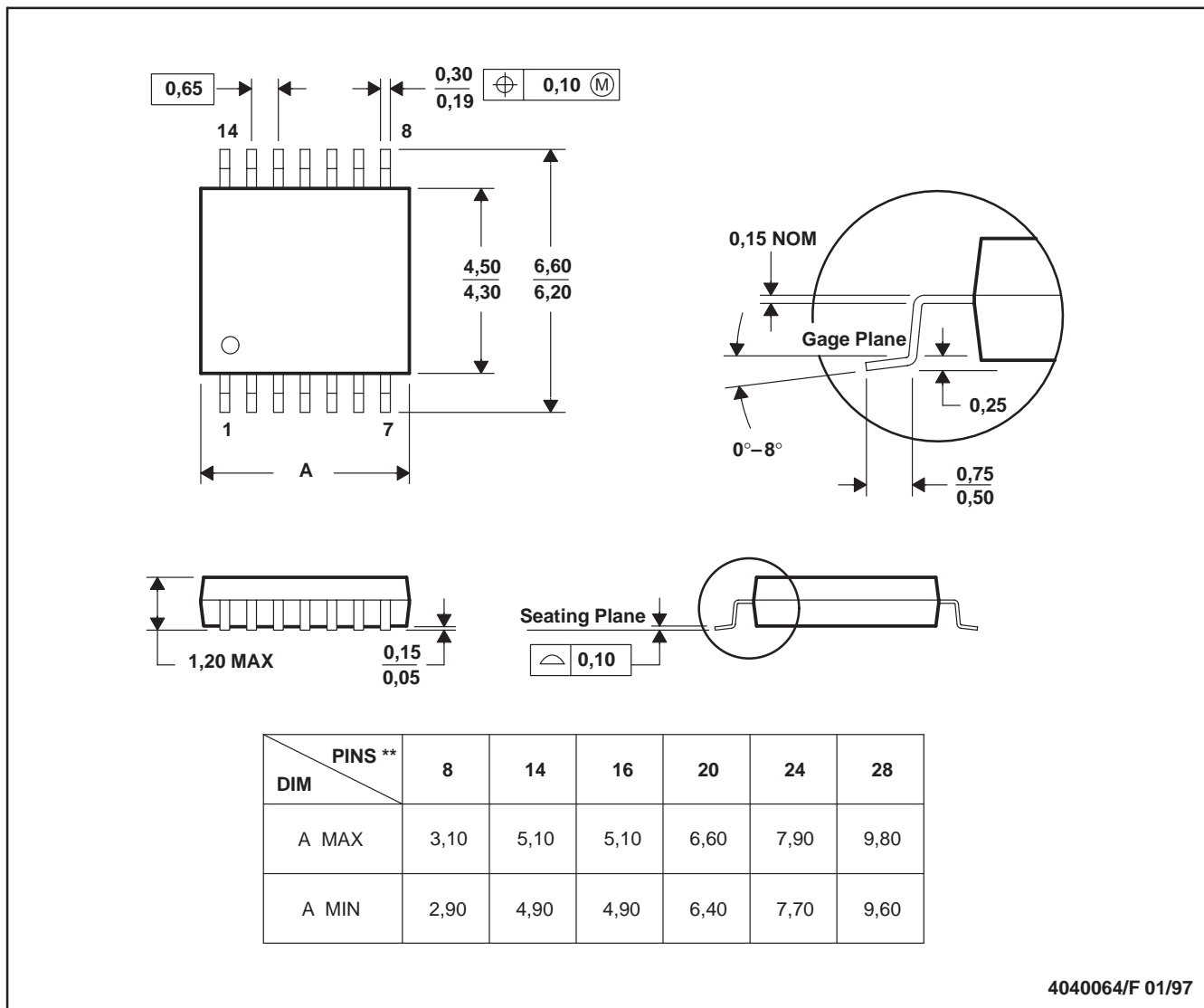
BIT #	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0 ⁽¹⁾
BIT NAME	FS15	FS14	FS13	FS12	FS11	FS10	FS9	FS8	FS7	FS6	FS5	FS4	FS3	FS2	FS1	FS0
POR VALUE	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(1) D0 is a *void* bit and will always be '0'. It is not possible to write a '1' to D0. CALIBRATION is the value stored in D15:D1.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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