

## Features

- Four Short-circuit-protected High-side Drivers with a Maximum Current Capability of 50 mA Each
- Four Short-circuit-protected Low-side Drivers with a Maximum Current Capability of 50 mA Each
- ON Resistance High Side  $R_{on} < 10\Omega$  Versus Total Temperature Range
- ON Resistance Low Side  $R_{on} < 7\Omega$  Versus Total Temperature Range
- Short-circuit Detection of Each Driver Stage
- Disabling of Driver Stages in the Case of Short-circuit and Overtemperature Detection
- Independent Control of Each Driver Stage via an 8-bit Shift Register
- Status Output Reports Short-circuit Condition
- Status Output Reports when All Loads Are Switched Off
- Timing of Status Output Reset Signalizes Failure Mode
- Temperature Protection in Conjunction with Short-circuit Detection



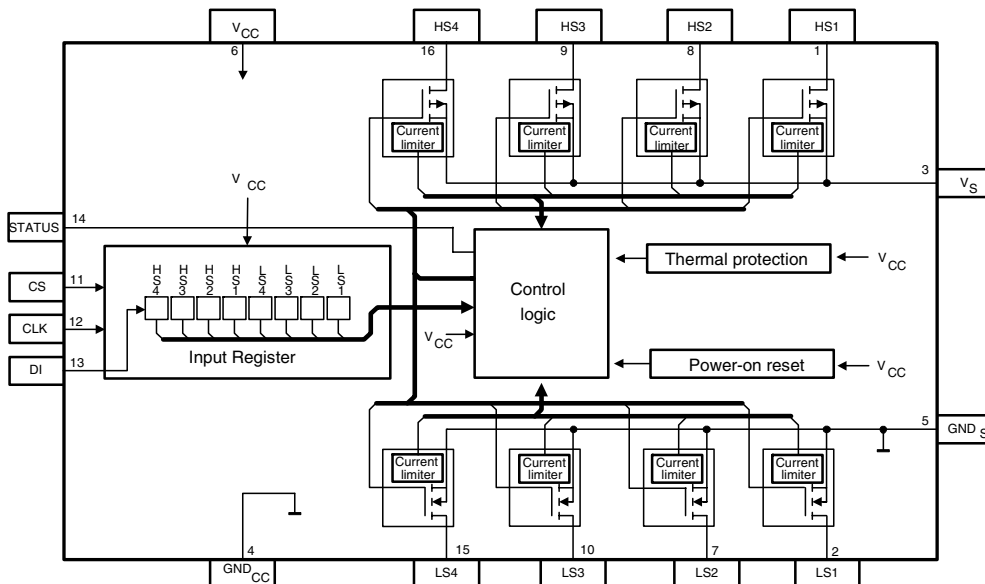
## Dual Quad BCDMOS Driver IC

## U6820BM

## 1. Description

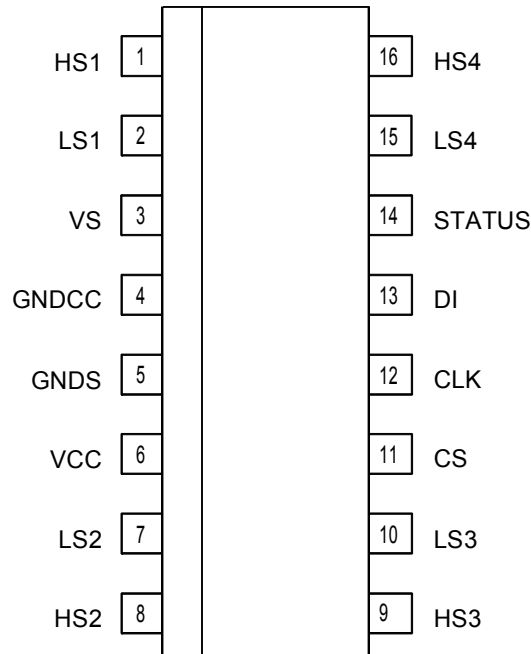
The U6820BM is a driver interface in BCDMOS technology with 8 independent driver stages having a maximum current capability of 50 mA each. Its partitioning into 4 high-side and 4 low-side driver stages allows an easy connection of either 4 half-bridges or 2 H-bridges on the pc board. The U6820BM communicates with a micro-controller via an 8-bit serial interface. Integrated protection against short circuit and overtemperature give added value. EMI protection and 2-kV ESD protection together with automotive qualification referring to conducted interference (ISO/TR 7637/1) make this IC ideal for both automotive and industrial applications.

**Figure 1-1.** Block Diagram



# 2. Pin Configuration

**Figure 2-1.** Pinning SO16



**Table 2-1.** Pin Description

Pin	Symbol	Function
1	HS1	Output high side 1
2	LS1	Output low side 1
3	VS	Supply voltage 6V to 18V
4	GNDCC	Digital ground
5	GNDS	Power ground
6	VCC	Supply voltage 5V (external)
7	LS2	Output low side 2
8	HS2	Output high side 2
9	HS3	Output high side 3
10	LS3	Output low side 3
11	CS	Set supply status (chip select)
12	CLK	Clock line for 8-bit control shift register
13	DI	Data line for 8-bit control shift register
14	STATUS	Status output (H = fault, diagnostic "H" if all driver stages are switched off)
15	LS4	Output low side 4
16	HS4	Output high side 4

### 3. Description of the Control Interface to the Microcontroller

The serial-parallel interface basically includes an 8-bit shift register (SR), an 8-bit command register (CR) and a 4-bit counter.

The data input takes place with commands at pins DI (data input), CS (chip select) and CLK (clock). With a falling edge at CLK, the information at DI is transferred into the SR. The first information written into the SR is the least significant bit (LSB). The pin STATUS is used for diagnostic purposes and reports any fault condition to the microcontroller.

The input CS in accordance with the CR controls the serial interface. A high level at CS disables the SR. With a falling edge at CS, the SR is enabled. The CR control allows only the first 8 bits to be transferred into the SR, and further clocks at CLK are ineffective. If a rising edge occurs at CS after 8 clocks precisely, the information from the SR is transferred into the CR. If the number of clock cycles during the low phase of CS was less or more than eight transitions, no transfer will take place. A new command switches the output stages on or off immediately.

Each output stage is controlled by one specific bit of the CR. Low level means "supply off" or inactive, and high level means "supply on" or active. If all 8 bits are at a low level, the output stages will be set into standby mode.

If one of the output stages detects a short circuit and additionally overtemperature condition, the corresponding control bit in the CR is set to low. This reset has priority over an external command to CR, thus, this does not affect the 1<sup>st</sup> control bit. The priority protects the IC against overtemperature by activating the temperature shut down immediately.

### 4. The STATUS Output

The STATUS output is at low level during normal operation. If one or more output stages detect short circuit or if overtemperature is indicated, the STATUS output changes to high level (OR-connection).

For diagnostic purposes (self test of the status output), the status output can also be brought into high level during standby mode.

#### 4.1 Timing of the Status Output Reset Signalizes the Failure Mode

The use of different reset conditions at the STATUS output simplifies the failure analysis during normal operation, and is also beneficial during testing.

The storage content can be used for STATUS output. It is indicated and latched immediately with the rising edge of CS at STATUS output if less than 8 clocks were received during the low phase of CS. The reset is initiated by the falling edge of the 8<sup>th</sup> clock (bit 7) of the next data input.

Also, the appearance of more than 8 clocks is latched and indicated at STATUS by the rising edge of the 9<sup>th</sup> clock. The reset is initiated by the falling edge of the 2<sup>nd</sup> clock (bit 1) of the next data input.

The detection of overtemperature is latched internally. It is reset by the falling edge of the 4<sup>th</sup> clock (bit 3) of a data transfer if overtemperature is no longer present.

## 4.2 Power-on Reset

After switching on the supply voltage, all data latches are reset and the outputs are switched off. The typical power-on reset threshold is  $V_{CC} = 3.7V$ . The outputs are activated after the first data transfer.

## 4.3 Short-circuit Protection

The current of the output stages is limited by an active feedback control. Short circuit at one output stage sets the diagnostic pin 14 (STATUS) to high. In case of both conditions, short circuit at one of the outputs and temperature detection, the affected output is switched off selectively. It will be activated again after the first new data transfer.

## 4.4 Inductance Protection

Clamping diodes and FETs are integrated to protect the IC against too high or too low voltages at the outputs. They prevent the IC from latch up and parasitic currents which may exceed power dissipation.

## 4.5 Temperature Protection

The IC is protected by an overtemperature detection. As soon as the junction temperature  $T_j = 155^\circ C$  typically is exceeded, the diagnostic pin 14 (STATUS) is set "high". General overtemperature detection along with short-circuit condition at a specific output result in temperature shut down at that specific output. After temperature shut down, the data input register has to be set again with a hysteresis of typically  $\Delta T = 15K$  ( $T_j = 140^\circ C$ ).

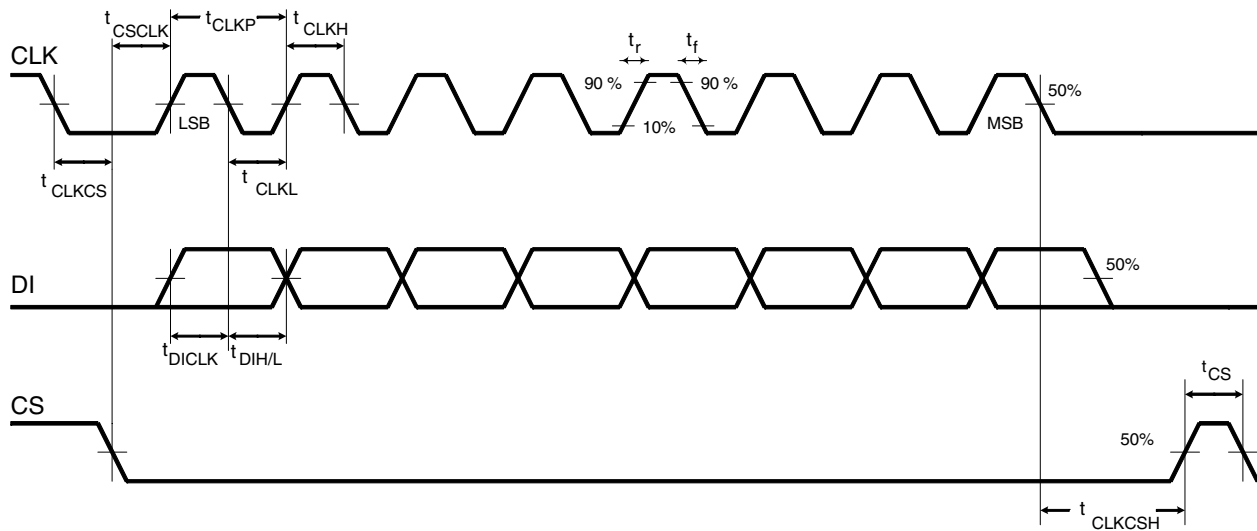
## 4.6 ESD Protection

All output stages are protected against electrostatic discharge up to 5 kV (HBM) with external components (see [Figure 8-1](#)), all other pins are protected up to 2 kV (HBM).

**Table 4-1.** Timing of the STATUS Output

Shift Register								Command Register								Condition				Low-side Switch				High-side Switch				Status	
																				LS1	LS2	LS3	LS4	HS1	HS2	HS3	HS4	Set	Reset
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	All out = OK			off	off	off	off	off	off	off	off	H	New CS
1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	All on = OK			on	on	on	on	on	on	on	on	L	
0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	E.g. one on = OK			off	off	off	off	off	off	off	on	L	
0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	1	Short at LS3			off	on	on	on	on	on	on	on	H	No short
1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	Temp & short at HS4			on	on	on	off	on	on	on	on	H	New CS4
1	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	$V_{VCC} < 3.7 V = P-ON$			off	off	off	off	off	off	off	off	H	P-ON, CS
1	1	1	0	0	0	1	1	x	x	x	x	x	x	x	x	x	CS with less 8 CLK			x	x	x	x	x	x	x	x	H	New CS 8
0	0	0	1	1	1	0	0	x	x	x	x	x	x	x	x	x	CS with more 8 CLK			x	x	x	x	x	x	x	x	H	New CS 2

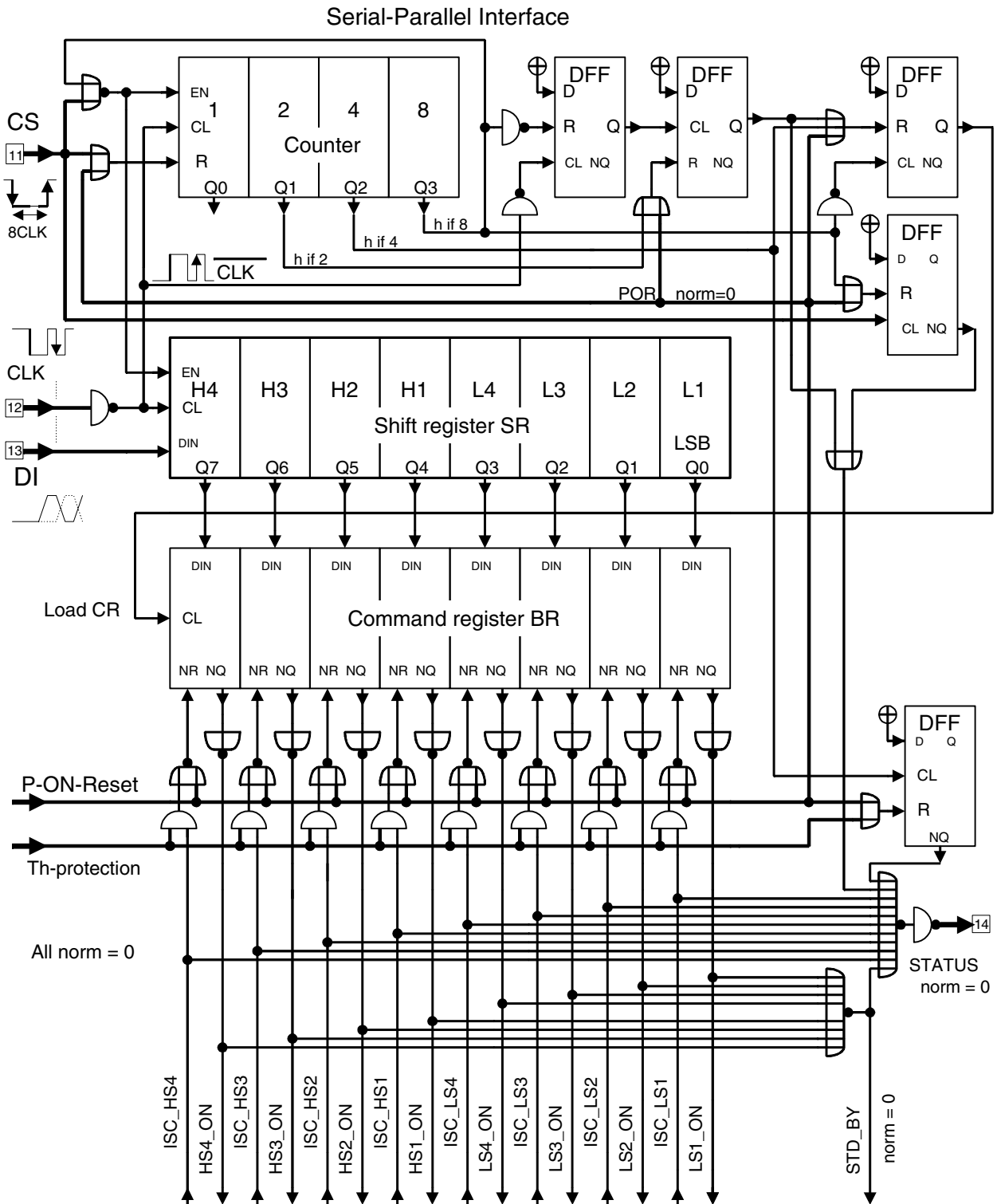
**Figure 4-1.** Data Transfer Timing Diagram



**Table 4-2.** AC Characteristics for Testing

Specification	Conditions	Minimum	Maximum	Unit
$t_r$ (rise)	10% to 90% $V_{CC}$ on CLK, DI and CS		10	ns
$t_f$ (fall)	10% to 90% $V_{CC}$ on CLK, DI and CS		10	ns
$t_{CLKP}$	$1/2 V_{CC}$	250		ns
$t_{CLKH}$	$1/2 V_{CC}$	100		ns
$t_{CLKL}$	$1/2 V_{CC}$	100		ns
$t_{CLKCS}$	$1/2 V_{CC}$	150		ns
$t_{CSCLK}$	$1/2 V_{CC}$	100		ns
$t_{DCLK}$	$1/2 V_{CC}$	80		ns
$t_{DIH/L}$	$1/2 V_{CC}$	100		ns
$t_{CLKCSH}$	$1/2 V_{CC}$	100		ns
$t_{CS}$	$1/2 V_{CC}$	250		ns

**Figure 4-2.** Block Diagram of the Control Interface



## 5. Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameters	Pin	Symbol	Minimum	Maximum	Unit
Supply voltage	3	$V_{VS}$	-0.3	+40	V
Logic supply voltage	6	$V_{VCC}$	-0.3	+7	V
Logic input voltage	11, 12, 13	CS, CLK, DI	-0.3	$V_{VCC} + 0.5$	V
Logic output voltage	14	STATUS	-0.3	$V_{VCC} + 0.3$	V
Input current	3	$I_{VS}$		0.2	mA
	6	$I_{VCC}$		5	mA
Output current (internally limited)	1-2, 8-11, 15-16	$I_{1H-4H}$ and $I_{1L-4L}$	30	65	mA
Junction temperature range		$T_j$	-40	+150	°C
Storage temperature range		$T_{stg}$	-55	+150	°C

## 6. Thermal Resistance

Parameters	Symbol	Value	Unit
Junction ambient	$R_{thJA}$	110	K/W
Junction case	$R_{thJC}$	26	K/W

## 7. Operating Range

Parameters	Pin	Symbol	Value	Unit
Supply voltage	3	$V_{VS}$	6 to 18	V
Logic supply voltage	6	$V_{VCC}$	4.5 to 5.5	V
Logic input voltage low	11, 12, 13	CS, CLK, DI	-0.2 to $(0.2 \times V_{VCC})$	V
Logic input voltage high	11, 12, 13	CS, CLK, DI	$(0.7 \times V_{VCC})$ to $(V_{VCC} + 0.3)$	V
Logic output voltage (1 mA load)	14	STATUS	0.5 to $(V_{VCC} - 1)$	V
Clock frequency		$f_{CLK}$	5	MHz
Junction temperature range		$T_j$	-40 to +150	°C

## 8. Electrical Characteristics

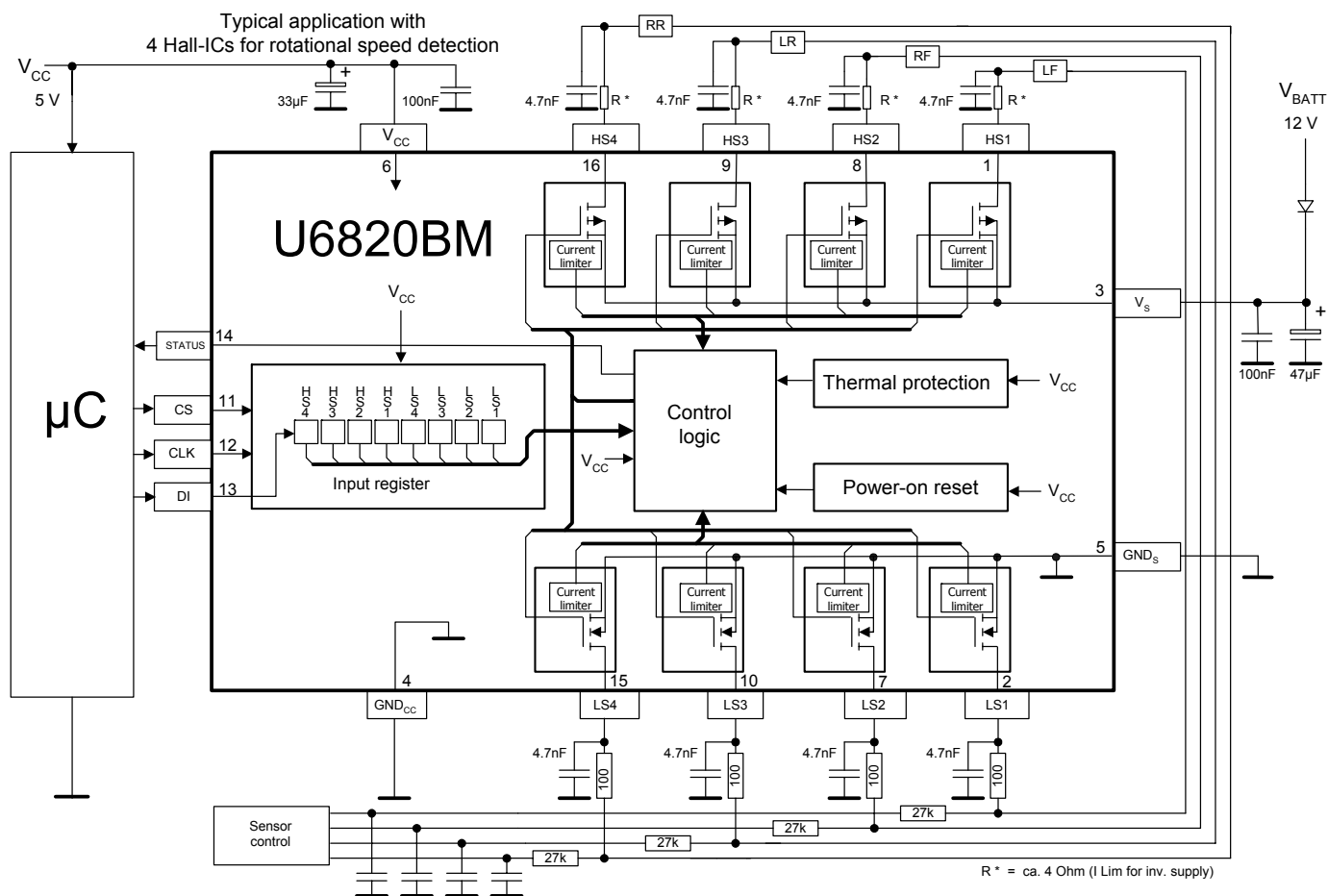
7V < V<sub>VS</sub> < 40V; 4.5V < V<sub>VCC</sub> < 5.5V; -40°C < T<sub>j</sub> < 150°C; unless otherwise specified

No.	Parameters	Test Conditions	Pin	Symbol	Min.	Typ.	Max.	Unit	Type*
<b>1</b>	<b>Current Consumption</b>								
1.1	Supply current VS	No external load	3	I <sub>VS</sub>			0.2	mA	A
1.2	Supply current VCC	No external load	6	I <sub>VCC</sub>			5	mA	A
1.3	Power-on reset threshold		6	V <sub>CC POR</sub>	3.4	3.7	4.0	V	A
1.4	Power-on reset delay time	After switching on V <sub>CC</sub>	6	T <sub>d POR</sub>	60	95	130	μs	D
<b>2</b>	<b>Thermal Shutdown</b>								
2.1	Thermal shutdown set			t <sub>j PW set</sub>	140	155	165	°C	A
2.2	Thermal shutdown reset			t <sub>j PW reset</sub>	130	135	155	°C	A
2.3	Thermal hysteresis			Dt		20		K	A
<b>3</b>	<b>Output Specifications (1L - 4L, 1H - 4H)</b>								
3.1	On-resistance low	I <sub>out</sub> = 26 mA, T <sub>j</sub> = 125°C	2, 7, 10, 15	R <sub>DSONLOW</sub>	3	4	7	Ω	A
3.2	On-resistance high	I <sub>out</sub> = 26 mA, T <sub>j</sub> = 125°C	1, 8, 9, 16	R <sub>DSONHIGH</sub>	4	6.25	10	Ω	A
3.3	Output leakage current lowside	V <sub>LSIDE 1-4</sub> = 17.5V	2, 7, 10, 15	I <sub>LOWSIDE</sub>			5	μA	A
3.4	Output leakage current highside	V <sub>HSIDE 1-4</sub> = 0.5V	1, 8, 9, 16	I <sub>HIGHSIDE</sub>			-5	μA	A
3.5	Output leakage steepness		1-2, 7-10, 15-16	dV <sub>OUT</sub> /dt	50	200	400	mV/μs	D
3.6	Over current limitation highside		1, 8, 9, 16	I <sub>HIGHSIDE</sub>	27	45	95	mA	A
3.7	Over current limitation lowside		2, 7, 10, 15	I <sub>LOWSIDE</sub>	27	45	80	mA	A
<b>4</b>	<b>Serial Interface – Inputs: CS, CLK and DATA</b>								
4.1	Input voltage low level threshold		11-13	V <sub>ILOW</sub>			0.2× V <sub>VCC</sub>	V	A
4.2	Input voltage high level threshold		11-13	V <sub>IHIGH</sub>	0.7× V <sub>VCC</sub>			V	A
4.3	Hysteresis of input voltage		11-13	ΔV <sub>i</sub>		300		mV	A
4.4	Pull-down current	(internal pull-up resistor: 30 kΩ to 140 kΩ)	11-13	I <sub>i</sub>			300	μA	A
<b>5</b>	<b>Serial Interface – Output: STATUS</b>								
5.1	Output voltage low level	I = 1 mA		V <sub>OLOW</sub>			0.5	V	A
5.2	Output voltage high level	I = 1 mA		V <sub>OHIGH</sub>	V <sub>VCC</sub> - 1		V <sub>VCC</sub>	V	A

\*) Type means: A = 100% tested, B = 100% correlation tested, C = Characterized on samples, D = Design parameter



**Figure 8-1. Application Circuit**



**Note:** It is strongly recommended to connect the blocking capacitors at  $V_S$  and  $V_{CC}$  as close as possible to the power supply and GND pins. Recommended value for  $V_S$  is less than 100 μF electrolytic in parallel with 100 nF ceramic. Value for electrolytic capacitor depends on external loads, noise and surge immunity efforts. Recommended value for  $V_{CC}$  is 33 μF electrolytic in parallel with 100 nF ceramic. The 4-Ω resistors connected to the pins HS1 - HS4 support the protection in case of a short circuit of these pins to  $V_{Batt}$ .





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