250mA, Ultralow I_Q, Fast Transient Response, RF LOW-DROPOUT LINEAR REGULATOR

FEATURES

- **Very Low Dropout:**
  - **65mV Typical at 100mA**
  - **130mV Typical at 200mA**
  - **163mV Typical at 250mA**
- **2% Accuracy Over Load/Line/Temperature**
- **Ultralow I_Q: 7.9µA**
- **Excellent Load Transient Performance:±50mV for 200mA Loading/Unloading Transient**
- **Available in Fixed-Output Voltages From 0.9V to 5V Using Innovative Factory EEPROM Programming**
- **High PSRR: 70dB at 1kHz**
- **Stable with a 1.0µF Ceramic Capacitor**
- **Thermal Shutdown and Overcurrent Protection**
- **Available in 4-Ball, 0,4mm Pitch Wafer-Level Chip Scale and 1,5mm x 1,5mm SON Packages**

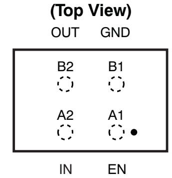
APPLICATIONS

- **Wireless Handsets, Smart Phones, PDAs**
- **MP3 Players and Other Handheld Products**
- **Wireless LAN, Bluetooth®, Zigbee®**
- **Remote Controls**
- **Portable Consumer Products**

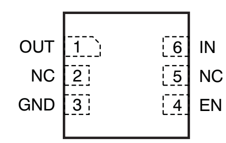
DESCRIPTION

The TPS727xx family of low-dropout (LDO) linear regulators are ultralow quiescent current LDOs with excellent line and ultra-fast load transient performance and are designed for power-sensitive applications. The LDO output voltage level is preset by the use of innovative factory EEPROM programming. A precision bandgap and error amplifier provides overall 2% accuracy over load, line, and temperature extremes. The TPS727xx family is available in 1,5mm x 1,5mm SON and wafer chip-scale (WCSP) packages that make it ideal for handheld applications. This family of devices is fully specified over a temperature range of T_J = –40°C to +125°C.

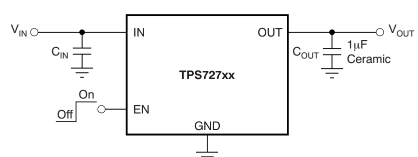
YFF PACKAGE
WCSP-4
(Top View)



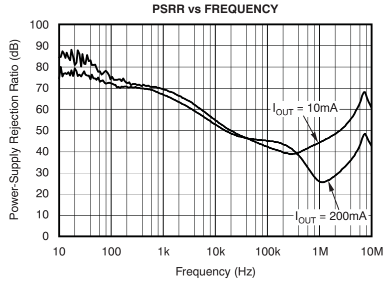
DSE PACKAGE
1,5mm × 1,5mm SON-6
(Top View)



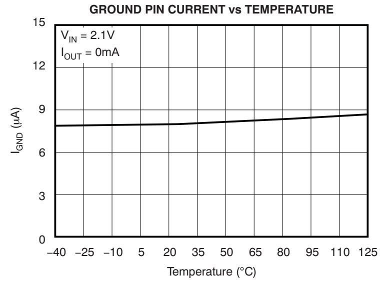
TYPICAL APPLICATION CIRCUIT



PSRR vs FREQUENCY



GROUND PIN CURRENT vs TEMPERATURE



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION(1)

PRODUCT	V_{OUT} (2)
TPS727**xxx** ***yyy z***	**XXX** is the nominal output voltage. **YYY** is package designator. **Z** is package tape and reel quantity (R = 3000, T = 250).

(1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.
(2) Output voltages from 0.9V to 5.0V in 50mV increments are available through the use of innovative factory EEPROM programming; minimum order quantities may apply. Contact factory for details and availability.

ABSOLUTE MAXIMUM RATINGS(1)

At T_J = –40°C to +125°C (unless otherwise noted). All voltages are with respect to GND.

PARAMETER		TPS727xx	UNIT
Input voltage range, V_{IN}		–0.3 to +6.0	V
Enable voltage range, V_{EN}		–0.3 to +6.0(2)	V
Output voltage range, V_{OUT}		–0.3 to +6.0	V
Maximum output current, I_{OUT}		Internally limited	
Output short-circuit duration		Indefinite	
Total continuous power dissipation, P_{DISS}		See Dissipation Ratings Table	
ESD rating	Human body model (HBM)	2	kV
	Charged device model (CDM)	500	V
Operating junction temperature range, T_J		–55 to +150	°C
Storage temperature range, T_{STG}		–55 to +150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) V_{EN} absolute maximum rating is V_{IN} or 6.0V, whichever is less.

DISSIPATION RATINGS

BOARD	PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	T_A < +25°C	T_A = +70°C	T_A = +85°C
High-K(1)	DSE	—	206°C/W	4.85mW/°C	485mW	269mW	194mW
High-K(1)	YFF	85°C/W	268°C/W	3.7mW/°C	370mW	205mW	150mW

(1) The JEDEC high-K (2s2p) board used to derive this data was a 3-inch × 3-inch, multilayer board with 1-ounce internal power and ground planes and 2-ounce copper traces on top and bottom of the board.

ELECTRICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.0V, whichever is greater; I_{OUT} = 10mA, V_{EN} = 0.9V, and C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_J = +25°C.

PARAMETER		TEST CONDITIONS	TPS727xx MIN	TYP	MAX	UNIT
V_{IN}	Input voltage range		2.0		5.5	V
V_O	Output voltage range		0.9		5.0	V
V_{OUT} (1)	DC output accuracy	T_J = +25°C	–2.5		+2.5	mV
		V_{OUT} + 0.3V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 200mA	–2.0	±1.0	+2.0	%
		V_{OUT} + 0.3V ≤ V_{IN} ≤ 5.5V, 0mA ≤ I_{OUT} ≤ 250mA		±1.0		%
ΔV_{OUT}	Load transient	1mA to 200mA or 200mA to 1mA in 1µs, C_{OUT} = 1µF		±50.0		mV
		1mA to 250mA or 250mA to 1mA in 1µs, C_{OUT} = 1µF		±65		mV
$\Delta V_O/\Delta V_{IN}$	Line regulation	$V_{OUT(NOM)}$ + 0.3V ≤ V_{IN} ≤ 5.5V, I_{OUT} = 10mA		8		µV/V
$\Delta V_O/\Delta I_{OUT}$	Load regulation	0mA ≤ I_{OUT} ≤ 250mA		20		µV/mA
V_{DO}	Dropout voltage (2)	V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 10mA		6.5		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 50mA		32.5		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 100mA		65		mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 200mA		130	200	mV
		V_{IN} = 0.98 × $V_{OUT(NOM)}$, I_{OUT} = 250mA		162.5		mV
I_{CL}	Output current limit	V_{OUT} = 0.9 × $V_{OUT(NOM)}$	300	400	550	mA
I_{GND}	Ground pin current	I_{OUT} = 0mA, T_J = –40°C to +125°C		7.9	12	µA
		I_{OUT} = 200mA		110		µA
		I_{OUT} = 250mA		130		µA
I_{SHDN}	Shutdown current (I_{GND})	V_{EN} ≤ 0.4V, V_{IN} = 2V, T_J = +25°C		0.12		µA
		V_{EN} ≤ 0.4V, 2.0V < V_{IN} ≤ 4.5V, T_J = –40°C to +85°C		0.55	2	µA
PSRR	Power-supply rejection ratio	V_{IN} = 2.3V, V_{OUT} = 1.8V, I_{OUT} = 10mA; f = 10Hz		85		dB
		f = 100Hz		75		dB
		f = 1kHz		70		dB
		f = 10kHz		55		dB
		f = 100kHz		40		dB
		f = 1MHz		45		dB
V_N	Output noise voltage	BW = 100Hz to 100kHz, V_{IN} = 2.1V, V_{OUT} = 1.8V, I_{OUT} = 10mA		33.5		μV_{RMS}
t_{STR}	Startup time (3)	C_{OUT} = 1.0µF, 0 ≤ I_{OUT} ≤ 250mA		100		µs
V_{HI}	Enable pin high (enabled)		0.9		V_{IN}	V
V_{LO}	Enable pin low (disabled)		0		0.4	V
I_{EN}	Enable pin current	EN = 5.5V		40	500	nA
UVLO	Undervoltage lock-out	V_{IN} rising	1.85	1.90	1.95	V
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		+160		°C
		Reset, temperature decreasing		+140		°C
T_J	Operating junction temperature		–40		+125	°C

(1) The output voltage is programmed at the factory.
(2) V_{DO} is measured for devices with $V_{OUT(NOM)}$ ≥ 2.35V so that V_{IN} ≥ 2.3V.
(3) Startup time: Time from EN assertion to 0.98 × $V_{OUT(NOM)}$.

DEVICE INFORMATION

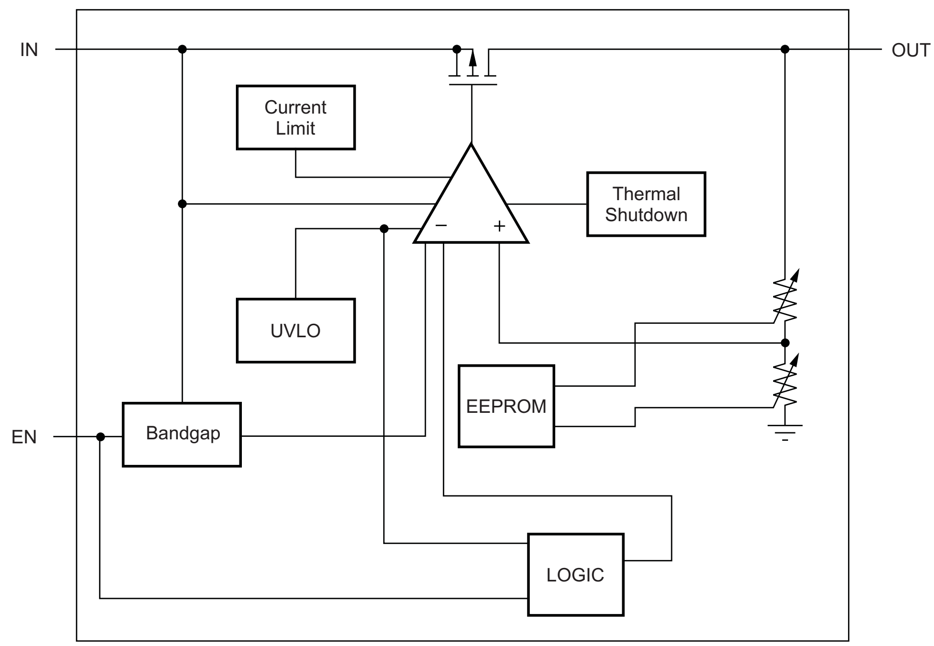
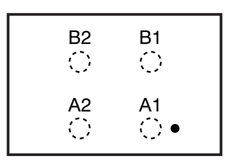


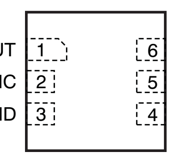
Figure 1. Functional Block Diagram

PIN CONFIGURATIONS

YFF PACKAGE
WCSP-4
(TOP VIEW)



DSE PACKAGE
1,5mm × 1,5mm SON-6
(TOP VIEW)



Note: EN pin marked with dot on YFF package.

PIN DESCRIPTIONS

TPS727xx			
NAME	**YFF**	**DSE**	**DESCRIPTION**
OUT	B2	1	Regulated output voltage pin. A small 1μF ceramic capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.
NC	—	2	No connection. This pin can be tied to to ground to improve thermal dissipation.
GND	B1	3	Ground pin.
EN	A1	4	Enable pin. Driving EN over 0.9V turns on the regulator. Driving EN below 0.4V puts the regulator into shutdown mode, thus reducing the operating current to 120nA, nominal.
NC	—	5	No connection. This pin can be tied to to ground to improve thermal dissipation.
IN	A2	6	Input pin. A small capacitor is needed from this pin to ground to assure stability. See *Input and Output Capacitor Requirements* in the *Application Information* section for more details.

TYPICAL CHARACTERISTICS

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.0V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

LINE REGULATION (TPS72718)

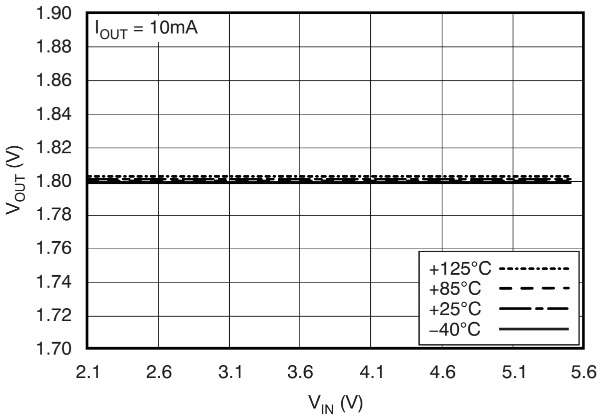


Figure 2.

LINE REGULATION (TPS72718)

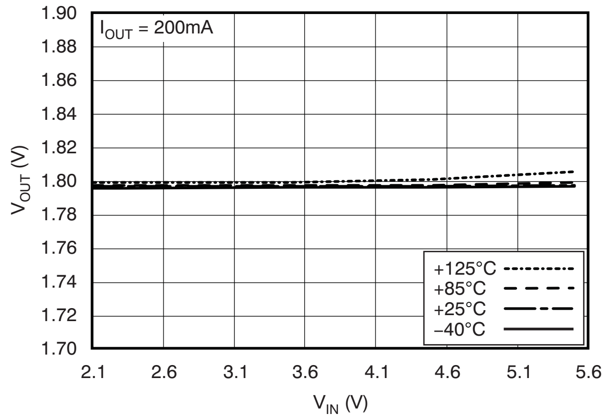


Figure 3.

LOAD REGULATION UNDER LIGHT LOADS (TPS72718)

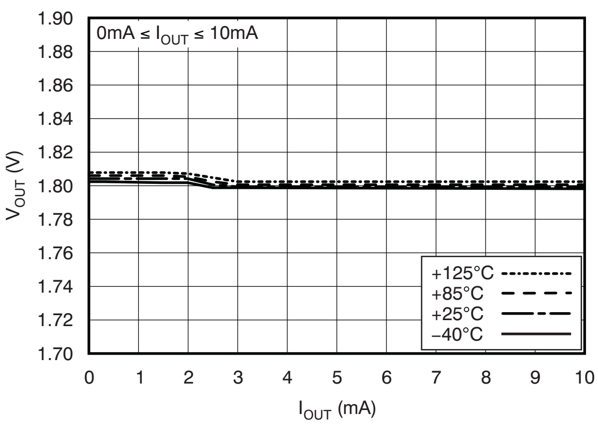


Figure 4.

LOAD REGULATION (TPS72718)

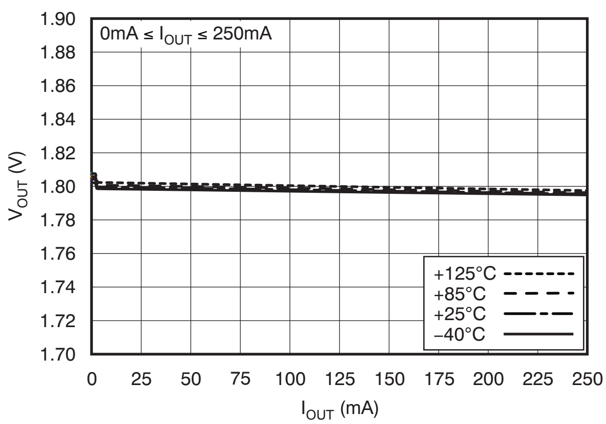


Figure 5.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.0V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

DROPOUT VOLTAGE vs OUTPUT CURRENT (TPS72750)

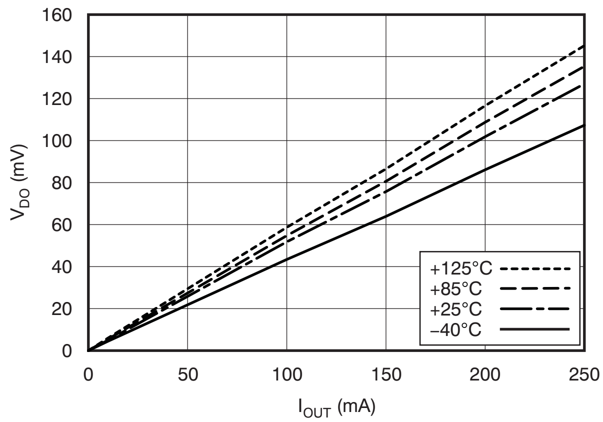


Figure 6.

DROPOUT VOLTAGE vs INPUT VOLTAGE (TPS72750)

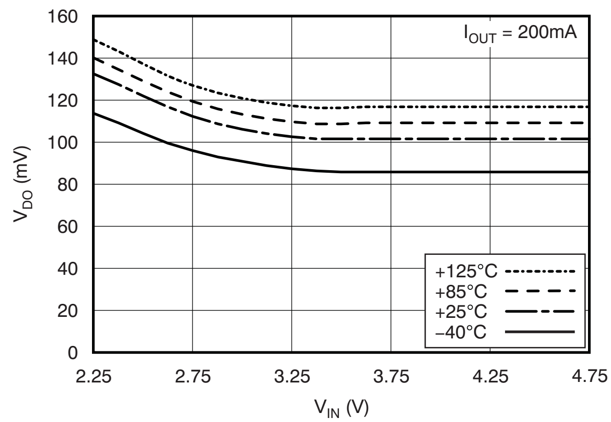


Figure 7.

OUTPUT VOLTAGE vs TEMPERATURE (TPS72718)

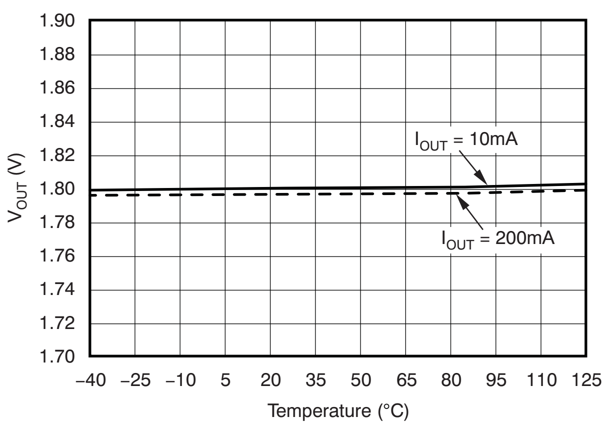


Figure 8.

GROUND PIN CURRENT vs INPUT VOLTAGE (TPS72718)

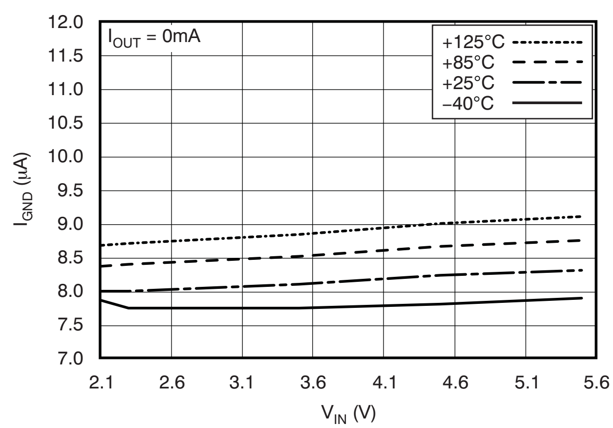


Figure 9.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.0V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_J = +25°C.

GROUND PIN CURRENT vs LOAD (TPS72718)

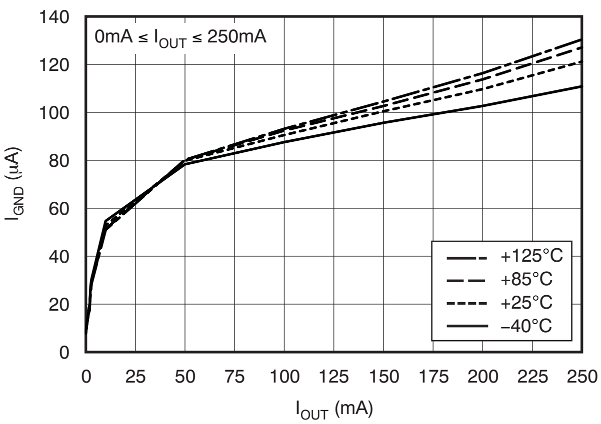


Figure 10.

GROUND PIN CURRENT vs TEMPERATURE (TPS72718)

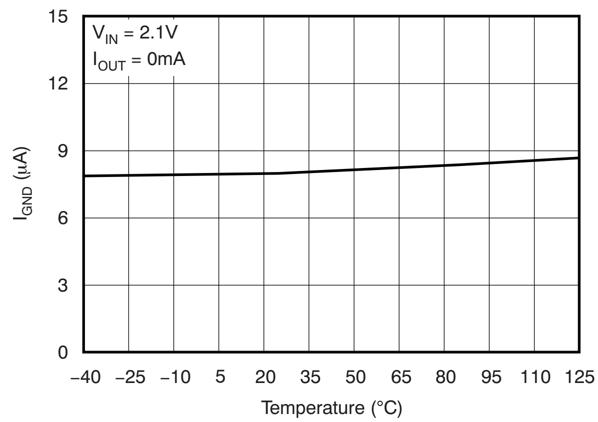


Figure 11.

SHUTDOWN CURRENT vs INPUT VOLTAGE (TPS72718)

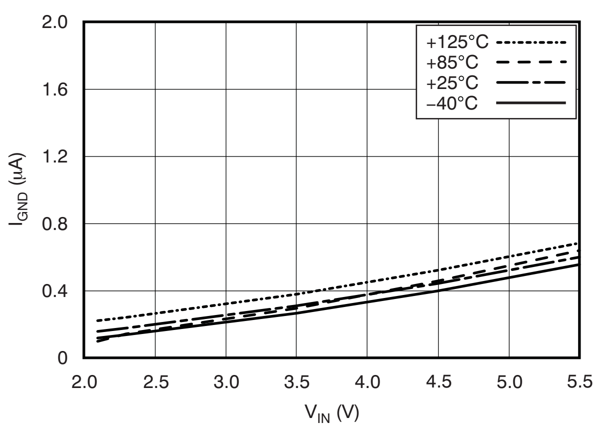


Figure 12.

CURRENT LIMIT vs INPUT VOLTAGE (TPS72718)

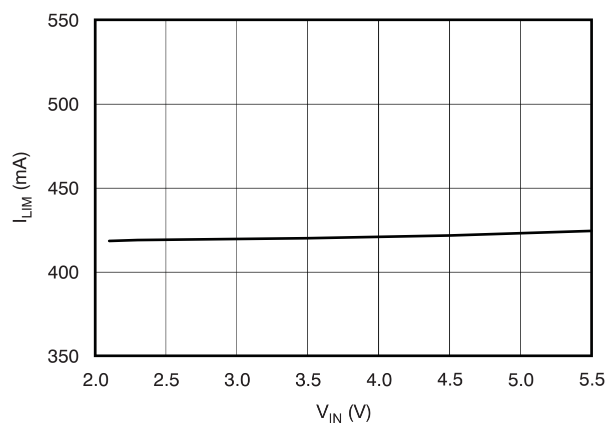


Figure 13.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.0V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0μF, unless otherwise noted. Typical values are at T_J = +25°C.

PSRR vs FREQUENCY (V_{IN} – V_{OUT} = 0.5V, TPS72718)

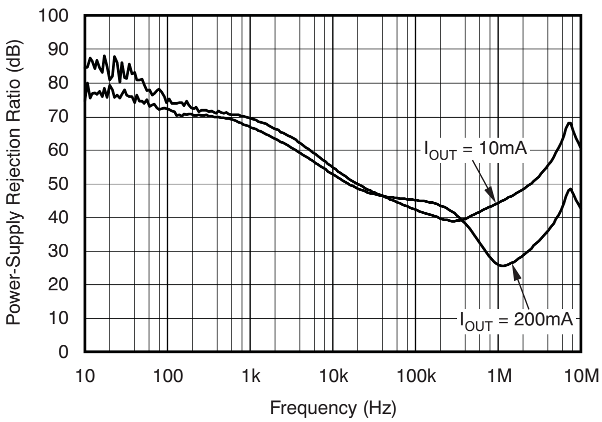


Figure 14.

PSRR vs FREQUENCY (V_{IN} – V_{OUT} = 0.3V, TPS72718)

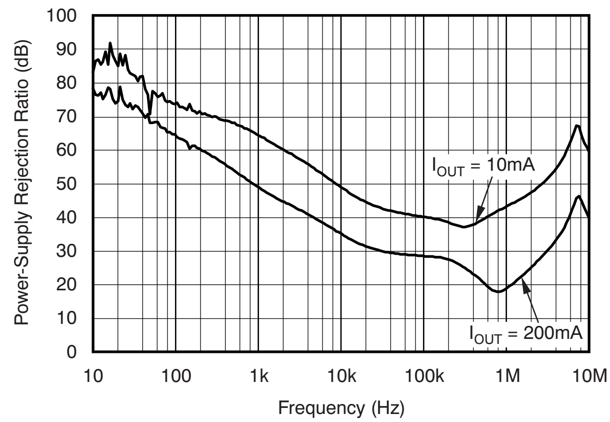


Figure 15.

PSRR vs INPUT VOLTAGE (TPS72718)

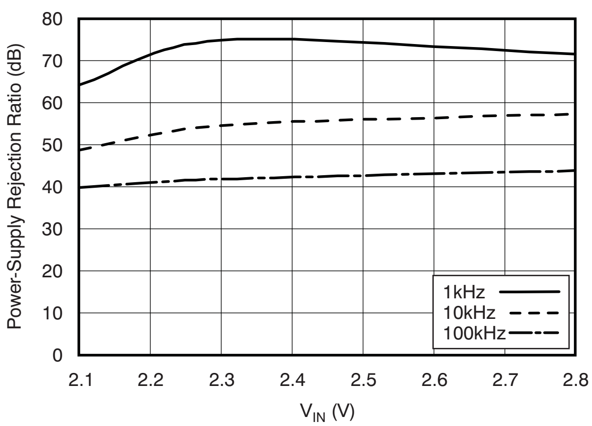


Figure 16.

OUTPUT SPECTRAL NOISE DENSITY vs OUTPUT VOLTAGE (TPS72718)

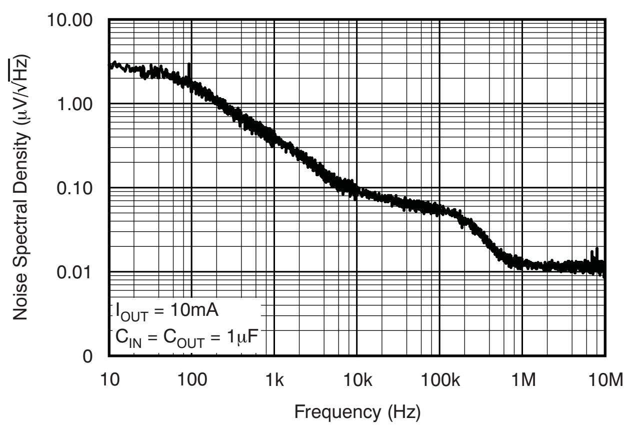


Figure 17.

LOAD TRANSIENT RESPONSE: 0.1mA TO 200mA (TPS72718)

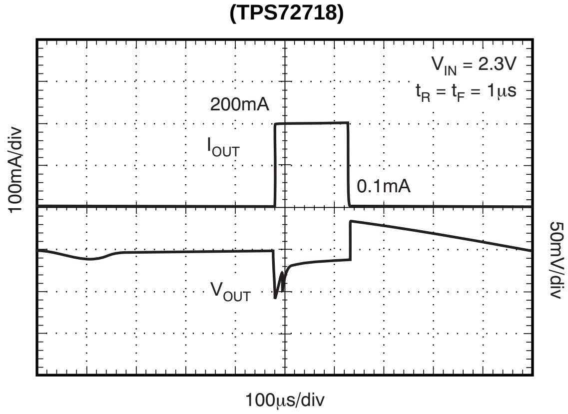


Figure 18.

LOAD TRANSIENT RESPONSE: 1mA TO 200mA (TPS72718)

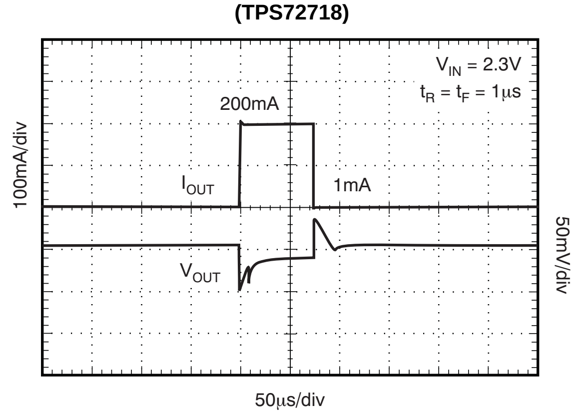


Figure 19.

TYPICAL CHARACTERISTICS (continued)

Over operating temperature range (T_J = –40°C to +125°C), V_{IN} = $V_{OUT(TYP)}$ + 0.3V or 2.0V, whichever is greater; I_{OUT} = 10mA, V_{EN} = V_{IN}, and C_{OUT} = 1.0µF, unless otherwise noted. Typical values are at T_J = +25°C.

LOAD TRANSIENT RESPONSE: 10mA TO 200mA (TPS72718)

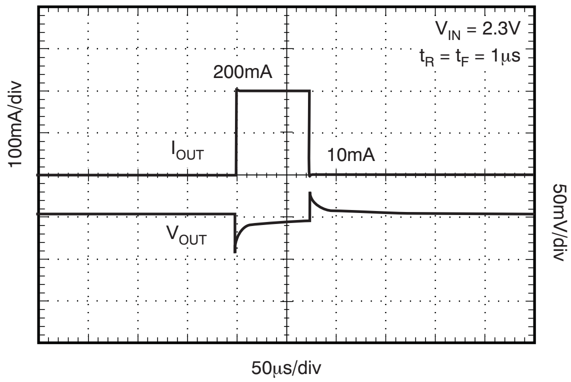


Figure 20.

LINE TRANSIENT RESPONSE (TPS72718)

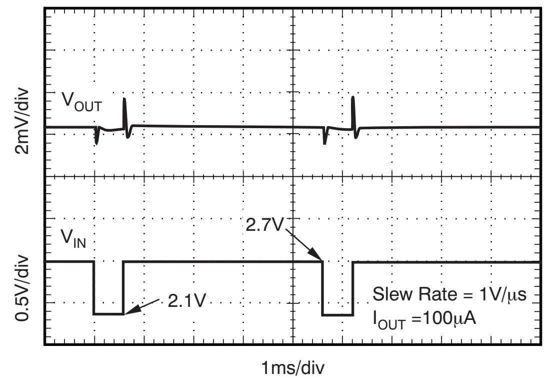


Figure 21.

LINE TRANSIENT RESPONSE (TPS72718)

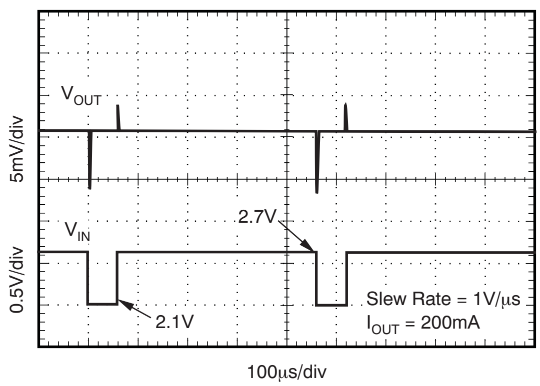


Figure 22.

V_{IN} INRUSH CURRENT (TPS72718)

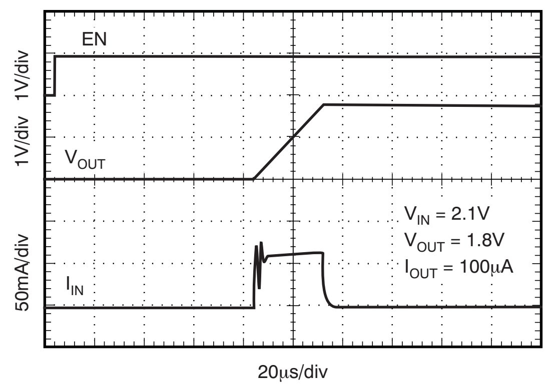


Figure 23.

V_{IN} INRUSH CURRENT (TPS72718)

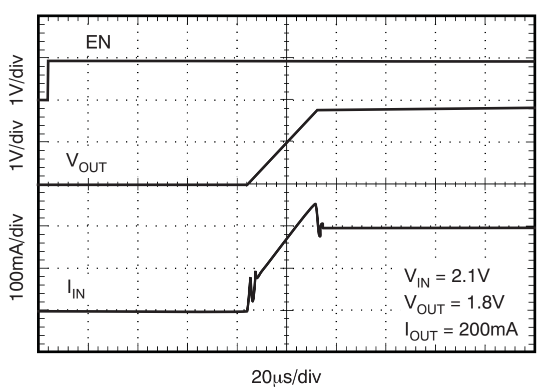


Figure 24.

V_{IN} RAMP UP, RAMP DOWN RESPONSE (TPS72718)

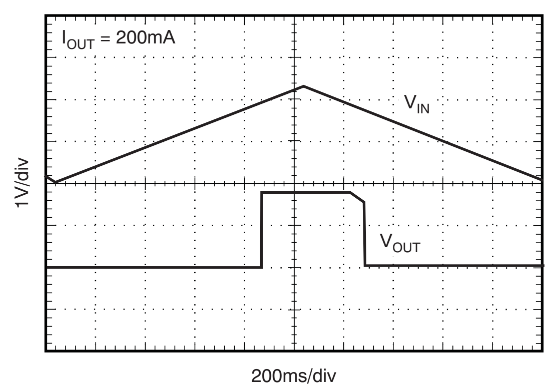


Figure 25.

APPLICATION INFORMATION

The TPS727xx family belongs to a family of new generation LDO regulators that consume extremely low quiescent current while simulatenously delivering excellent PSRR with very little headroom (V_{IN} – V_{OUT} differential voltage), and very good transient response. These features, combined with low noise without a noise reduction pin in an ultrasmall package, make this device ideal for portable applications. This family of regulators offers sub-bandgap output voltages, current limit and thermal protection, and is fully specified from –40°C to +125°C.

INPUT AND OUTPUT CAPACITOR REQUIREMENTS

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1μF to 1.0μF low equivalent series resistance (ESR) capacitor across the IN pin and GND input of the regulator. This capacitor counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated, or if the device is not located close to the power source. If source impedance is not sufficiently low, a 0.1μF input capacitor may be necessary to ensure stability.

The TPS727xx is designed to be stable with standard ceramic capacitors with values of 1.0μF or larger at the output. X5R- and X7R-type capacitors are best because they have minimal variation in value and ESR over temperature. Maximum ESR should be less than 200mΩ.

BOARD LAYOUT RECOMMENDATIONS TO IMPROVE PSRR AND NOISE PERFORMANCE

To improve ac performance such as PSRR, output noise, and transient response, it is recommended that the board be designed with separate ground planes for V_{IN} and V_{OUT}, with the ground plane connected only at the GND pin of the device. In addition, the ground connection for the output capacitor should connect directly to the GND pin of the device. High ESR capacitors may degrade PSRR.

INTERNAL CURRENT LIMIT

The TPS727xx internal current limit helps protect the regulator during fault conditions. During current limit, the output sources a fixed amount of current that is largely independent of output voltage. In such a case, the output voltage is not regulated, and is V_{OUT} = $I_{LIMIT} \times R_{LOAD}$. The PMOS pass transistor dissipates (V_{IN} – V_{OUT}) × I_{LIMIT} until thermal shutdown is triggered and the device is turned off. As the device cools down, it is turned on by the internal thermal shutdown circuit. If the fault condition continues, the device cycles between current limit and thermal shutdown. See the *Thermal Information* section for more details.

The PMOS pass element in the TPS727xx has a built-in body diode that conducts current when the voltage at the OUT pin exceeds the voltage at the IN pin. This current is not limited, so if extended reverse voltage operation is anticipated, external limiting to 5% of rated output current is recommended.

SOFT START

The startup current is given by Equation 1:

$$I_{SOFT\ START}\ (mA) = C_{OUT}(\mu F) \times 0.07(V/\mu s) + I_{LOAD}(mA) \quad (1)$$

This equation shows that soft-start current is directly proportional to C_{OUT}.

The output voltage ramp rate is independent of C_{OUT} and load current, and has a typical value of 0.07V/μs.

The TPS727xx automatically adjusts the soft-start current to supply both the load current and the C_{OUT} charge current. For example, if I_{LOAD} = 0mA upon enabling the LDO, $I_{SOFT\ START}$ = 1μF × 0.07 V/μs + 0mA = 70mA, the current that charges the output capacitor.

If I_{LOAD} = 200mA, $I_{SOFT\ START}$ = 1μF × 0.07V/μs + 200mA = 270mA, the current required for charging output capacitor and supplying the load current.

If the output capacitor and load are increased such that the soft-start current exceeds the output current limit, it is clamped at the typical current limit of 400mA. For example, if C_{OUT} = 10μF and I_{OUT} = 200mA, 10μF × 0.07V/μs + 200mA = 900mA is not supplied. Instead, it is clamped at 400mA.

SHUTDOWN

The enable pin (EN) is active high and is compatible with standard and low voltage, TTL-CMOS levels. When shutdown capability is not required, EN can be connected to the IN pin.

DROPOUT VOLTAGE

The TPS727xx uses a PMOS pass transistor to achieve low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the PMOS pass device is in the linear region of operation and the input-to-output resistance is the $R_{DS(ON)}$ of the PMOS pass element. V_{DO} approximately scales with output current because the PMOS device behaves like a resistor in dropout.

As with any linear regulator, PSRR and transient response are degraded as (V_{IN} – V_{OUT}) approaches dropout. This effect is shown in Figure 16 in the Typical Characteristics section.

TRANSIENT RESPONSE

As with any regulator, increasing the size of the output capacitor reduces over/undershoot magnitude but increases duration of the transient response.

UNDERVOLTAGE LOCK-OUT (UVLO)

The TPS727xx uses an undervoltage lock-out circuit that keeps the output shut off until the input voltage reaches the UVLO threshold voltage.

THERMAL INFORMATION

Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately +160°C, allowing the device to cool. When the junction temperature cools to approximately +140°C the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to +125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least +35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of +125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS727xx has been designed to protect against overload conditions. It is not intended to replace proper heatsinking. Continuously running the TPS727xx into thermal shutdown degrades device reliability.

Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the printed circuit board (PCB) layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data for JEDEC low- and high-K boards are given in the *Dissipation Ratings* table. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers also improves the heatsink effectiveness.

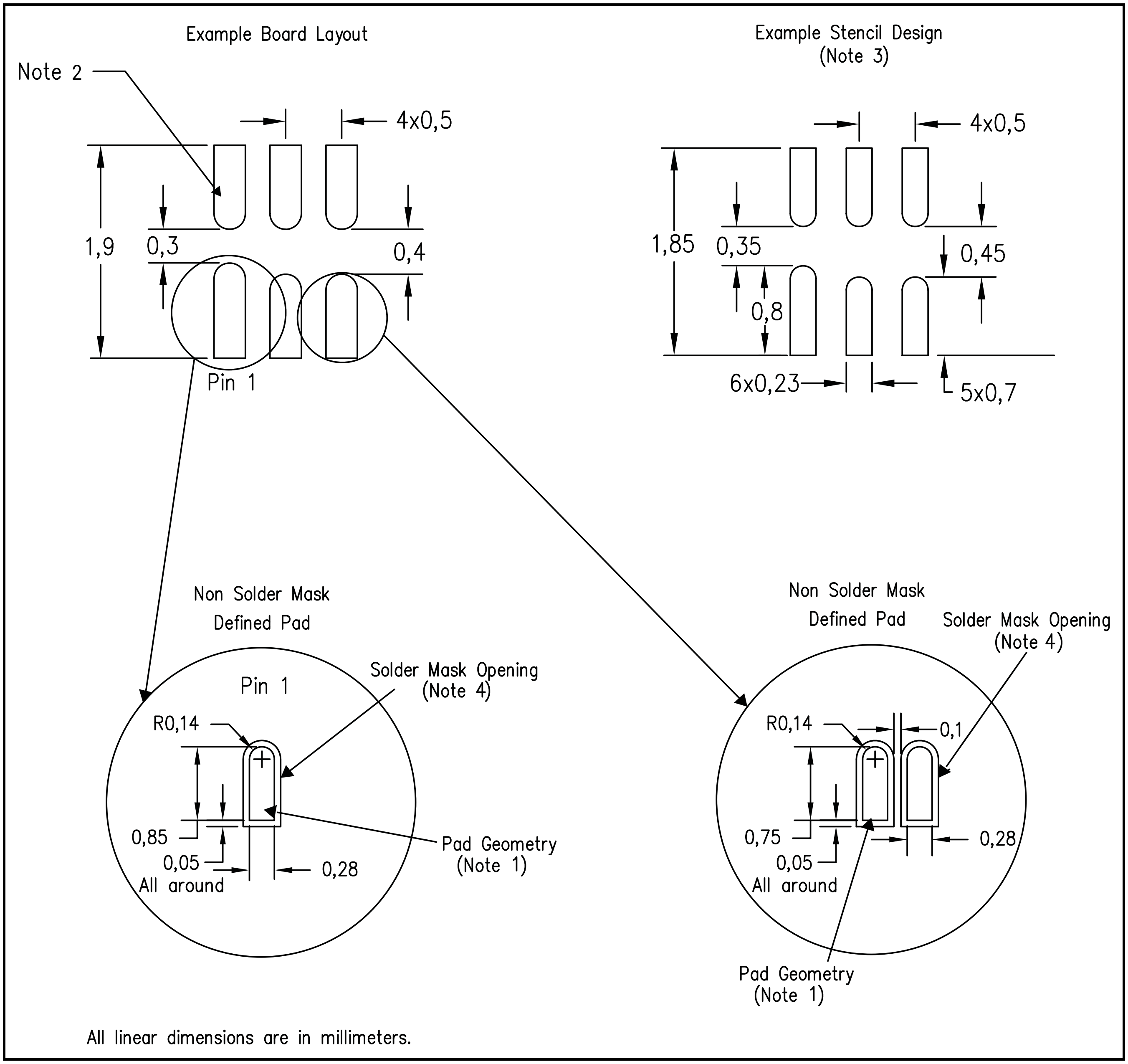
Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}), as shown in Equation 2:

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \qquad (2)$$

Package Mounting

Solder pad footprint recommendations for the TPS727xx are available from the Texas Instruments web site at www.ti.com.

The recommended land pattern for the DSE package is shown in Figure 26. Figure 27 shows the dimensions of the YFF package.



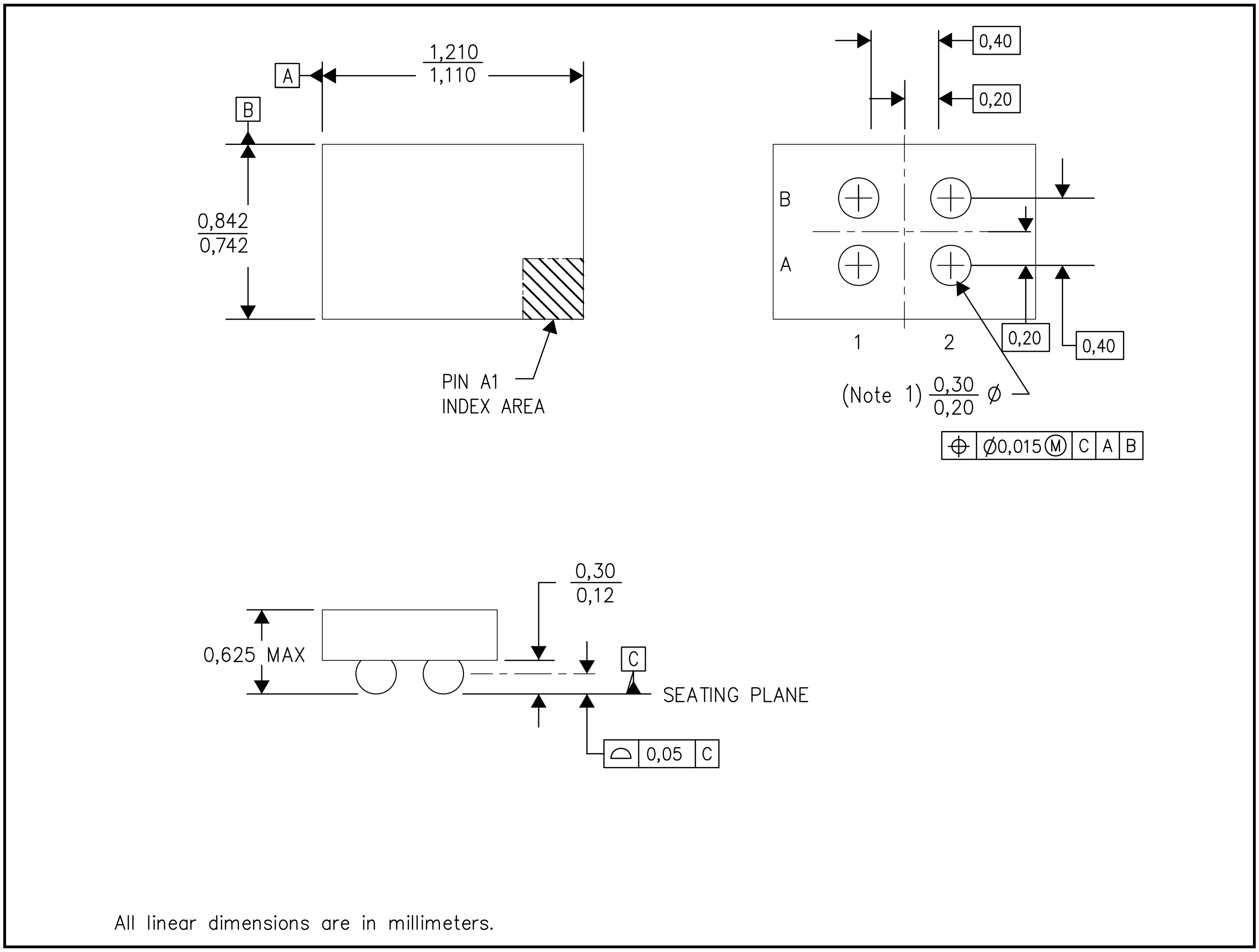
(1) Publication IPC-7351 is recommended for alternate designs.

(2) For more information, refer to TI application notes SCBA017 and SLUA271 (*Quad Flatpack No-Lead Logic Packages* and *QFN/SON PCB Attachment*, respectively) for specific thermal information, via requirements, and additional recommendations for board layout. These documents are available at the Texas Instruments web site (http://www.ti.com) by searching for the literature number.

(3) Laser-cutting apertures with trapedzoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for stencil design considerations.

(4) Customers should contact their board fabrication site for minimum solder mask tolerances between signal pads.

Figure 26. Recommended Land Pattern for DSE Package



(1) Devices in a YFF package can have a dimension that ranges within a specified tolerance. To determine the exact measurements, contact a local Texas Instruments representative.

Figure 27. YFF Package Dimensions

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September, 2009) to Revision B **Page**

Changes from Original (June, 2009) to Revision A **Page**

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPS72711YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples
TPS72711YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples
TPS72715DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS72715DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS72715YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples
TPS72715YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples
TPS72718DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS72718DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS72718YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples
TPS72718YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples
TPS72725DSER	PREVIEW	WSON	DSE	6	3000	TBD	Call TI	Call TI	Samples Not Available
TPS72725DSET	PREVIEW	WSON	DSE	6	250	TBD	Call TI	Call TI	Samples Not Available
TPS727285DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS727285DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS72728DSER	ACTIVE	WSON	DSE	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Purchase Samples
TPS72728DSET	ACTIVE	WSON	DSE	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	Request Free Samples
TPS72728YFFR	ACTIVE	DSBGA	YFF	4	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Purchase Samples
TPS72728YFFT	ACTIVE	DSBGA	YFF	4	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	Request Free Samples

Orderable Device	Status [(1)]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [(2)]	Lead/ Ball Finish	MSL Peak Temp [(3)]	Samples (Requires Login)
TPS72730DSER	PREVIEW	WSON	DSE	6	3000	TBD	Call TI	Call TI	Samples Not Available
TPS72730DSET	PREVIEW	WSON	DSE	6	250	TBD	Call TI	Call TI	Samples Not Available
TPS72733DSER	PREVIEW	WSON	DSE	6	3000	TBD	Call TI	Call TI	Samples Not Available
TPS72733DSET	PREVIEW	WSON	DSE	6	250	TBD	Call TI	Call TI	Samples Not Available

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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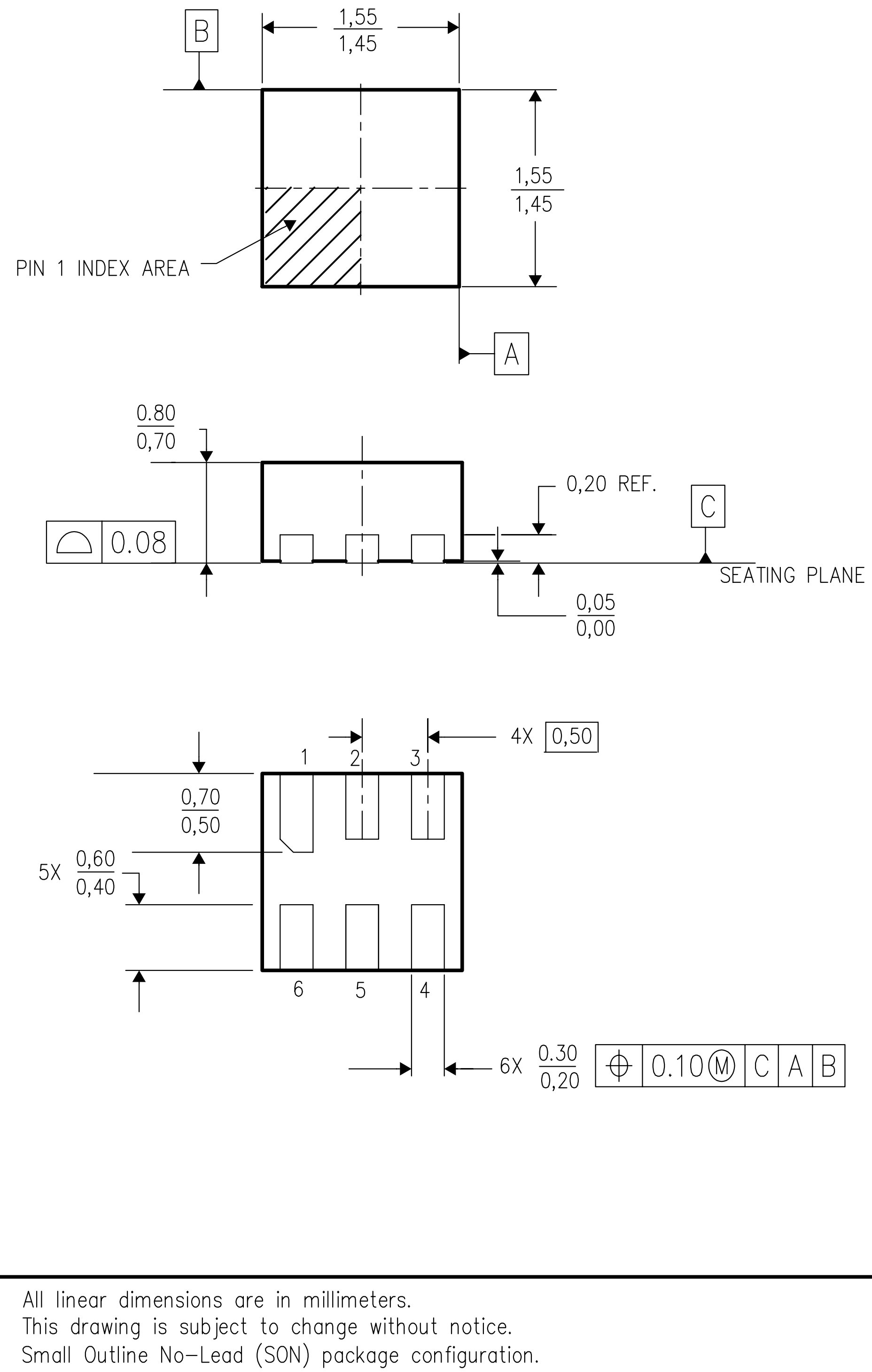
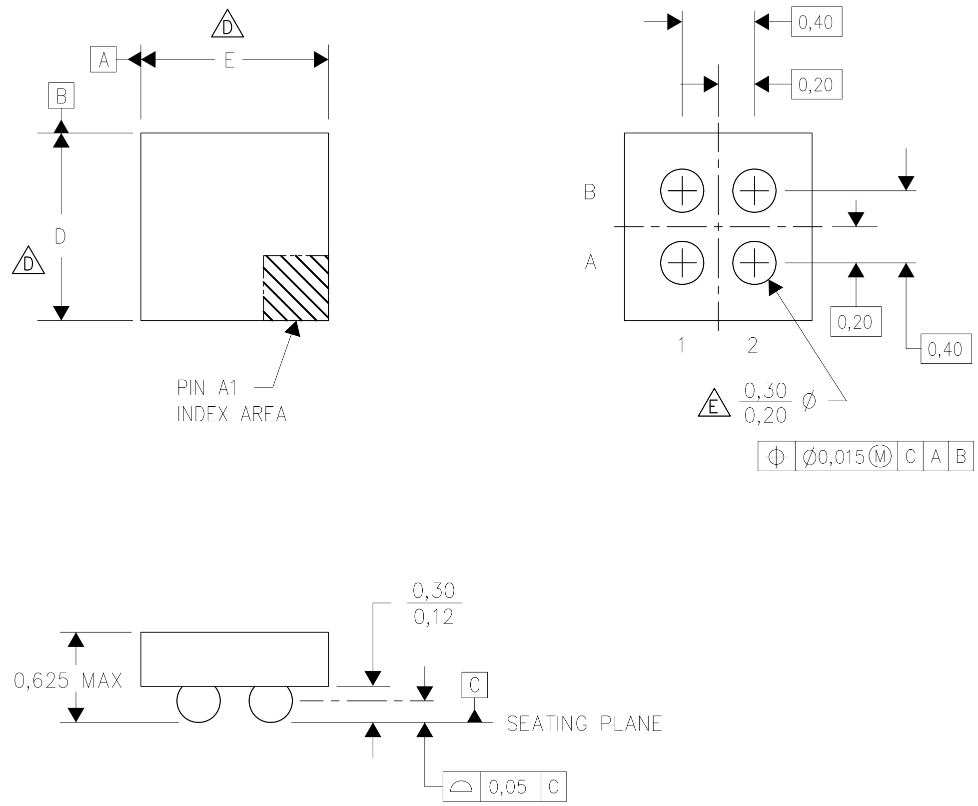
DSE (S-PDSO-N6) PLASTIC SMALL OUTLINE



4207810/A 03/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Small Outline No-Lead (SON) package configuration.
D. This package is lead-free.

YFF (S–XBGA–N4) DIE–SIZE BALL GRID ARRAY



X: Max = 1210 µm, Min = 1110 µm

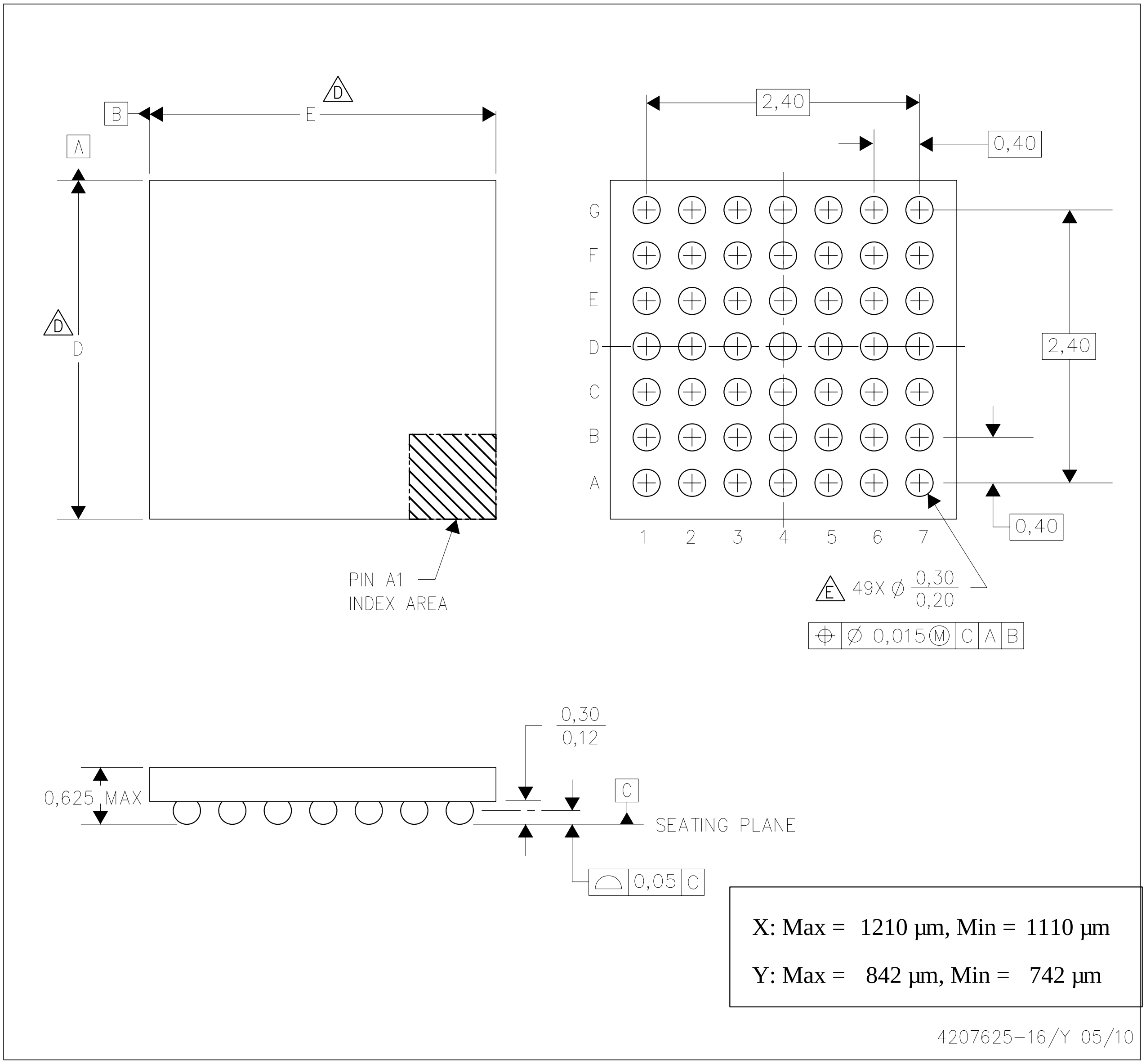
Y: Max = 842 µm, Min = 742 µm

4207625–2/Y 05/10

NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
- B. This drawing is subject to change without notice.
- C. NanoFree™ package configuration.
- D. Devices in YFF package can have dimensions D ranging from 0.76 to 1.45 mm and dimension E ranging from 0.76 to 1.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
- E. Reference Product Data Sheet for array population. 2 x 2 matrix pattern is shown for illustration only.
- F. This package contains Pb–free balls.

NanoFree is a trademark of Texas Instruments.

YFF (R–XBGA–N49) DIE–SIZE BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. Devices in YFF package can have dimension D ranging from 2.73 to 3.45 mm and dimension E ranging from 2.73 to 3.45 mm. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. Reference Product Data Sheet for array population. 7 x 7 matrix pattern is shown for illustration only.
F. This package contains Pb–free balls.

NanoFree is a trademark of Texas Instruments.