

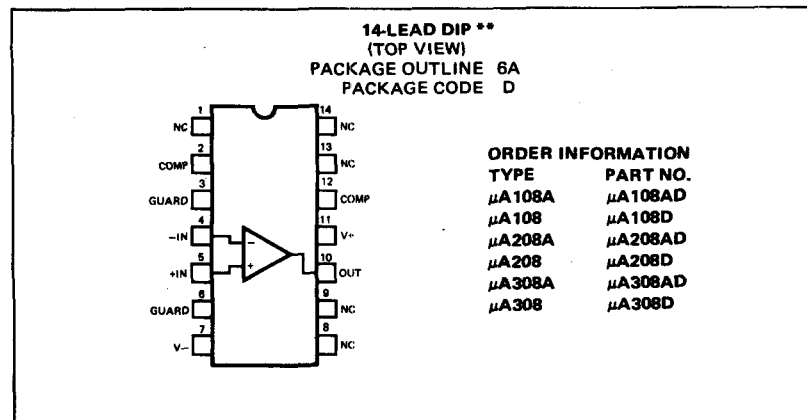
μ A108A • μ A208A • μ A308A μ A108 • μ A208 • μ A308 SUPER BETA OPERATIONAL AMPLIFIERS FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION — The 108 Super Beta Operational Amplifier series is constructed using the Fairchild Planar* epitaxial process. High input impedance, low noise, input offsets, and temperature drift are made possible through use of super beta processing, making the device suitable for applications requiring high accuracy and low drift performance. The 108A series is specially selected for extremely low offset voltage and drift, and high common mode rejection, giving superior performance in applications where offset nulling is undesirable. Increased slew rate without performance compromise is available through use of feedforward compensation techniques, maximizing performance in high speed sample-and-hold circuits and precision high speed summing amplifiers. The wide supply range and excellent supply voltage rejection assure maximum flexibility in voltage follower, summing, and general feedback applications.

- GUARANTEED LOW INPUT OFFSET CHARACTERISTICS
- HIGH INPUT IMPEDANCE
- LOW OFFSET CURRENT
- LOW BIAS CURRENT
- OPERATION OVER WIDE SUPPLY RANGE

ABSOLUTE MAXIMUM RATINGS

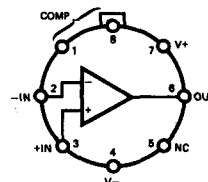
Supply Voltage	
μ A108A, μ A108, μ A208A, μ A208	± 20 V
μ A308A, μ A308	± 18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Current (Note 2)	± 10 mA
Input Voltage (Note 3)	± 15 V
Storage Temperature Range	-65°C to $+150^{\circ}\text{C}$
Operating Temperature Range	
Military (μ A108A, μ A108)	-55°C to $+125^{\circ}\text{C}$
Industrial (μ A208A, μ A208)	-25°C to $+85^{\circ}\text{C}$
Commercial (μ A308A, μ A308)	0°C to $+70^{\circ}\text{C}$
Lead Temperature (Soldering, 60 Seconds)	300°C
Output Short Circuit Duration (Note 4)	Indefinite



See notes on following pages.

CONNECTION DIAGRAMS

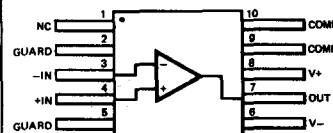
8-LEAD METAL CAN (TOP VIEW) PACKAGE OUTLINE 6S PACKAGE CODE H



ORDER INFORMATION

TYPE	PART NO.
μ A108A	μ A108AH
μ A108	μ A108H
μ A208A	μ A208AH
μ A208	μ A208H
μ A308A	μ A308AH
μ A308	μ A308H

10-LEAD FLATPAK** (TOP VIEW) PACKAGE OUTLINE 3F PACKAGE CODE F



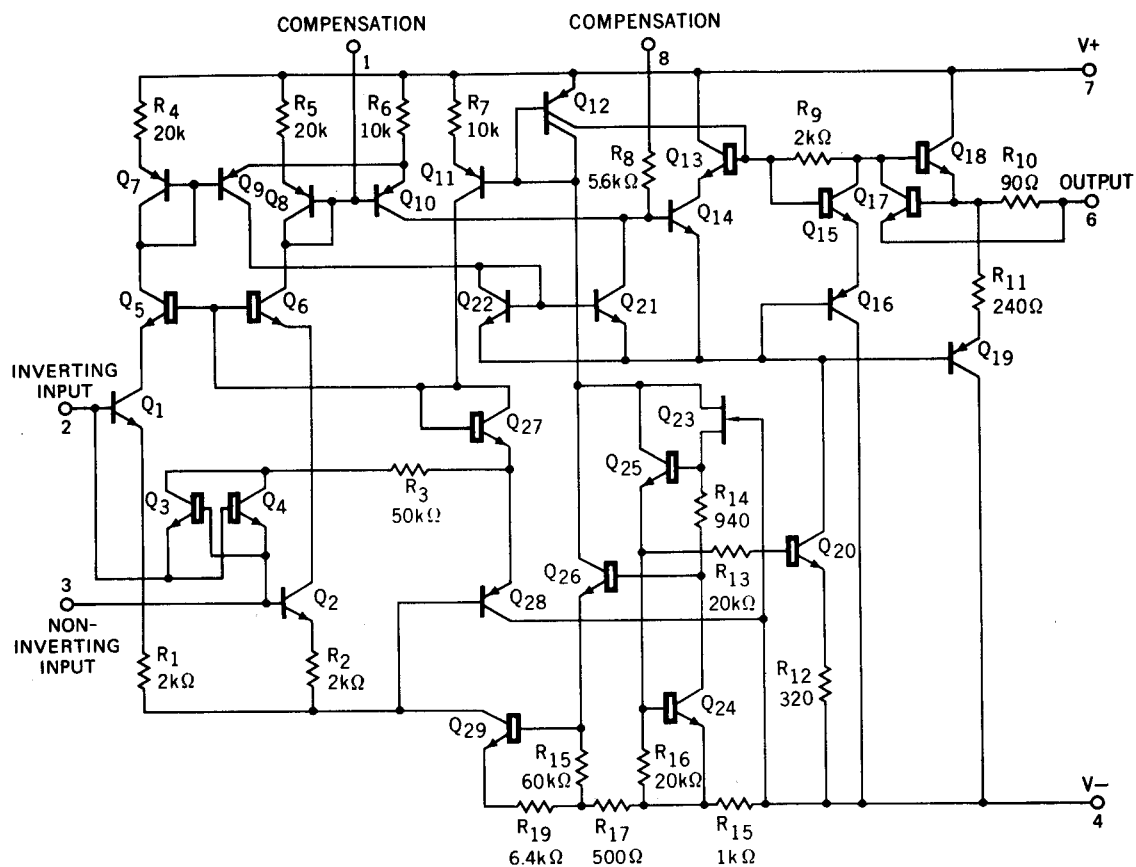
ORDER INFORMATION

TYPE	PART NO.
μ A108A	μ A108AF
μ A108	μ A108F
μ A208A	μ A208AF
μ A208	μ A208F

** Available on special order

*Planar is a patented Fairchild process.

EQUIVALENT CIRCUIT



Pin numbers are for metal can only

FAIRCHILD LINEAR IC μ A108A • μ A208A • μ A308A • μ A108 • μ A208 • μ A308

ELECTRICAL CHARACTERISTICS FOR μ A108A AND μ A208A ($\pm 5\text{ V} < V_S < \pm 20\text{ V}$, $T_A = 25^\circ\text{C}$, $C_C = 30\text{ pF}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		0.3	0.6	mA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L > 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	80,000	300,000		V/V

The following specifications apply for $-55^\circ\text{C} < T_A < +125^\circ\text{C}$ (Note 5)

Input Offset Voltage				1.0	mV
Average Input Offset Voltage Drift			1.0	5.0	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	$\text{pA}/^\circ\text{C}$
Input Bias Current			0.8	3.0	nA
Supply Current	$T_A = +125^\circ\text{C}$		0.15	0.4	mA
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L > 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	40,000			V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L > 10\text{ k}\Omega$	± 13	± 14		V

ELECTRICAL CHARACTERISTICS FOR μ A308A ($\pm 5\text{ V} < V_S < \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $C_C = 30\text{ pF}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.3	0.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L > 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	80,000	300,000		V/V

The following specifications apply for $0^\circ\text{C} < T_A < +70^\circ\text{C}$

Input Offset Voltage				0.73	mV
Average Input Offset Voltage Drift			1.0	5.0	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	$\text{pA}/^\circ\text{C}$
Input Bias Current				10	nA
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 13.5			V
Common Mode Rejection Ratio		96	110		dB
Supply Voltage Rejection Ratio		96	110		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L > 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	60,000			V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L > 10\text{ k}\Omega$	± 13	± 14		V

NOTES:

- The maximum junction temperature of the 108A/108 is 150°C , while that of the 208A/208 is 100°C , and 308A/308 is 85°C . For operating at elevated temperatures, devices in the TO-99 package must be derated based on thermal resistance of $150^\circ\text{C}/\text{W}$, junction to ambient, or $45^\circ\text{C}/\text{W}$, junction to case. For the flatpak a maximum rating of 300 mW applies and derating is based on a thermal resistance of $185^\circ\text{C}/\text{W}$ when mounted on a 1/16 inch thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the Dual In-line Package is $100^\circ\text{C}/\text{W}$, junction to ambient.
- The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1 V is applied between the inputs unless adequate limiting resistance is used.
- For supply voltages less than $\pm 15\text{ V}$, the absolute maximum input voltage is equal to the supply voltage.
- Short circuit may be to either supply or ground. Rating applies to operation up to the maximum operating temperature range.
- For the 208A/208, all temperature specifications apply over $-25^\circ\text{C} < T_A < 85^\circ\text{C}$.

ELECTRICAL CHARACTERISTICS FOR μ A108 AND μ A208 ($\pm 5\text{ V} < V_S < \pm 20\text{ V}$, $T_A = 25^\circ\text{C}$, $C_C = 30\text{ pF}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			0.7	2.0	mV
Input Offset Current			0.05	0.2	nA
Input Bias Current			0.8	2.0	nA
Input Resistance		30	70		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		0.3	0.6	mA
Large Signal Voltage Gain	$R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$ $V_S = \pm 15\text{ V}$	50,000	300,000		V/V

The following specifications apply for $-55^\circ\text{C} < T_A \leq 125^\circ\text{C}$ (Note 5)

Input Offset Voltage				3.0	mV
Average Input Offset Voltage Drift			3.0	15	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				0.4	nA
Average Input Offset Current Drift			0.5	2.5	$\text{pA}/^\circ\text{C}$
Input Bias Current				3.0	nA
Supply Current	$T_A = +125^\circ\text{C}$		0.15	0.4	mA
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 13.5			V
Common Mode Rejection Ratio		85	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	25,000			V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$	± 13	± 14		V

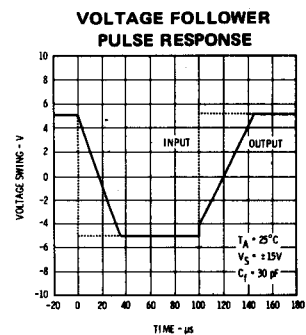
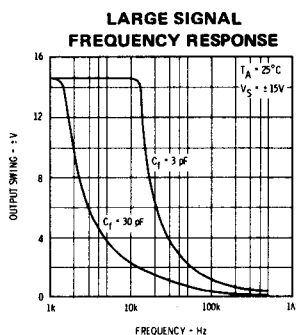
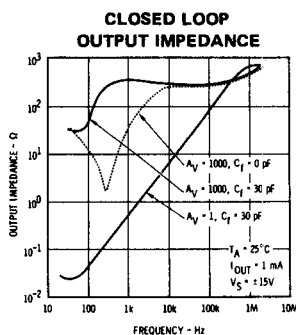
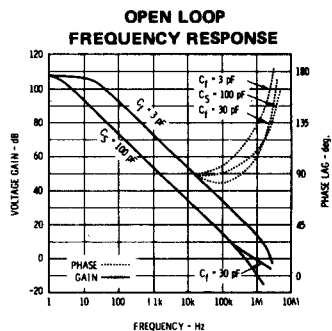
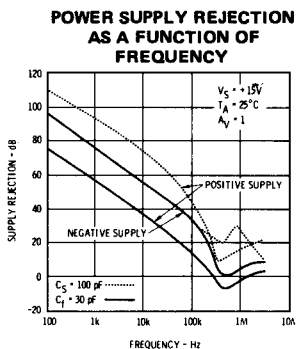
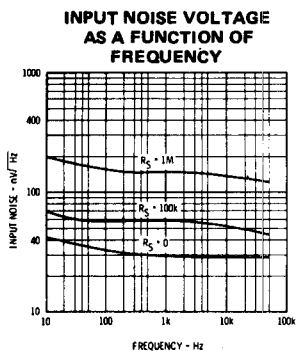
ELECTRICAL CHARACTERISTICS FOR μ A308 ($\pm 5\text{ V} < V_S < \pm 15\text{ V}$, $T_A = 25^\circ\text{C}$, $C_C = 30\text{ pF}$ unless otherwise specified)

PARAMETERS	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage			2.0	7.5	mV
Input Offset Current			0.2	1.0	nA
Input Bias Current			1.5	7.0	nA
Input Resistance		10	40		M Ω
Supply Current	$V_S = \pm 15\text{ V}$		0.3	0.8	mA
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	25,000	300,000		V/V

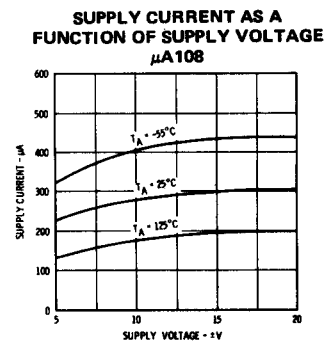
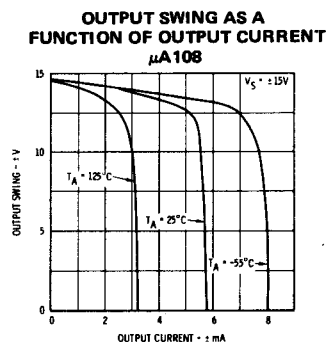
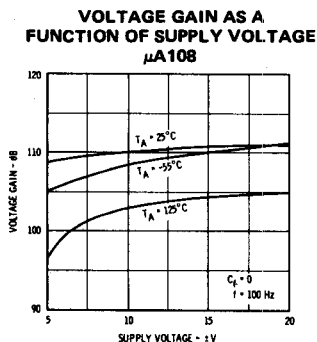
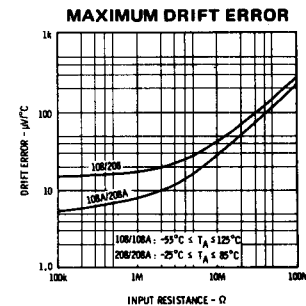
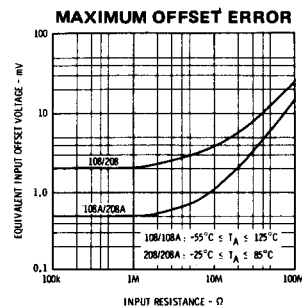
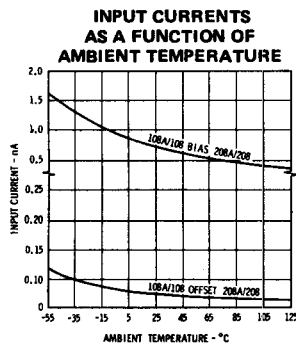
The following specifications apply for $0^\circ\text{C} < T_A \leq +70^\circ\text{C}$

Input Offset Voltage				10	mV
Average Input Offset Voltage Drift			6.0	30	$\mu\text{V}/^\circ\text{C}$
Input Offset Current				1.5	nA
Average Input Offset Current Drift			2.0	10	$\text{pA}/^\circ\text{C}$
Input Bias Current				10	nA
Input Voltage Range	$V_S = \pm 15\text{ V}$	± 13.5			V
Common Mode Rejection Ratio		80	100		dB
Supply Voltage Rejection Ratio		80	96		dB
Large Signal Voltage Gain	$V_S = \pm 15\text{ V}$, $R_L \geq 10\text{ k}\Omega$, $V_{OUT} = \pm 10\text{ V}$	15,000			V/V
Output Voltage Swing	$V_S = \pm 15\text{ V}$, $R_L = 10\text{ k}\Omega$	± 13	± 14		V

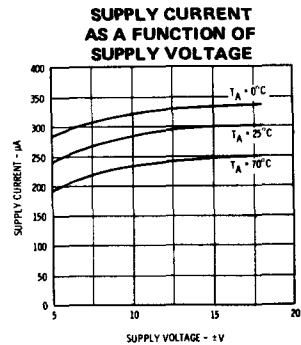
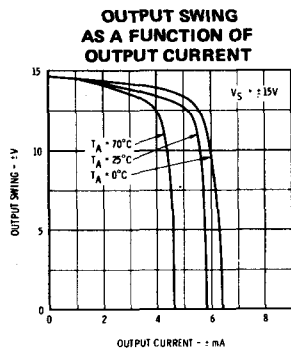
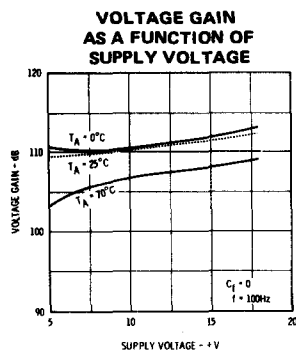
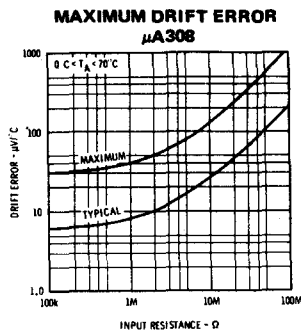
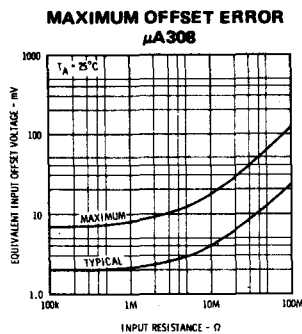
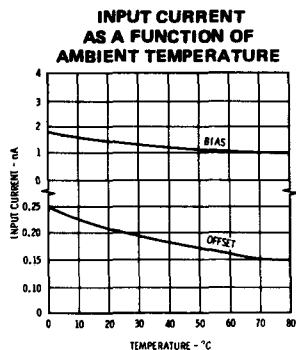
TYPICAL PERFORMANCE CURVES FOR μ A108 SERIES



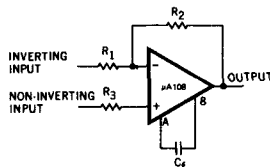
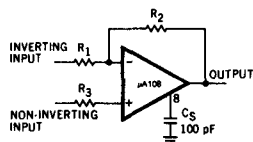
TYPICAL PERFORMANCE CURVES FOR μ A108A • μ A208A • μ A108 • μ A208 (Unless Otherwise Specified)



TYPICAL PERFORMANCE CURVES FOR $\mu A308A$ AND $\mu A308$ (Unless Otherwise Specified)



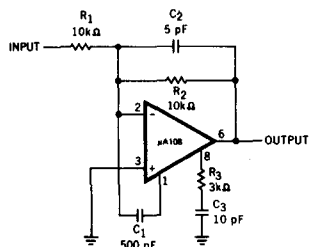
STANDARD COMPENSATION CIRCUITS



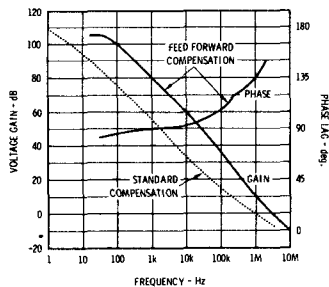
$$C_f \geq 30 \left(\frac{1}{1 + \frac{R_2}{R_1}} \right)$$

FEEDFORWARD COMPENSATION
HIGHER SLEW RATES AND WIDER BANDWIDTH

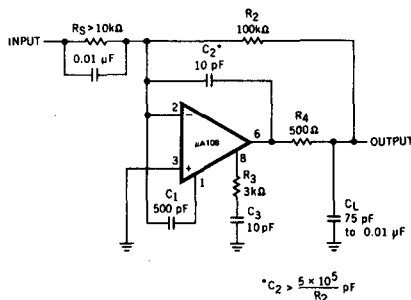
STANDARD FEEDFORWARD



OPEN LOOP VOLTAGE GAIN



FEEDFORWARD COMPENSATION
FOR DECOUPLING LOAD CAPACITANCE



$$C_2 > \frac{5 \times 10^5}{R_2} \text{ pF}$$

GUARDING

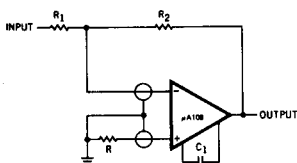
Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage as the inputs. Leakage currents from high voltage pins are then absorbed by the guard.

The pin configuration of the Dual In-line Package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard $\mu A741$ and 101A pin configuration).

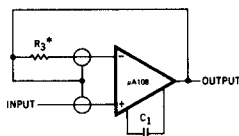
CONNECTION OF INPUT GUARDS

INVERTING AMPLIFIER



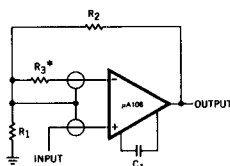
$$R = \frac{R_1 R_2}{R_1 + R_2}$$

FOLLOWER



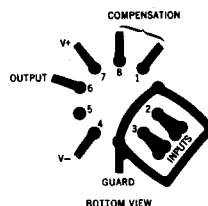
* Use to compensate for large source resistances.

NON-INVERTING AMPLIFIER



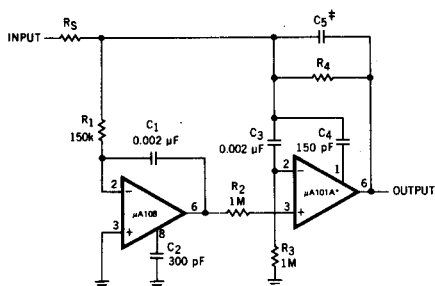
NOTE: $\frac{R_1 R_2}{R_1 + R_2}$ Must be low impedance

BOARD LAYOUT FOR INPUT GUARDING WITH TO-99 PACKAGE (BOTTOM VIEW)



TYPICAL APPLICATIONS

FAST[†] SUMMING AMPLIFIER WITH LOW INPUT CURRENT

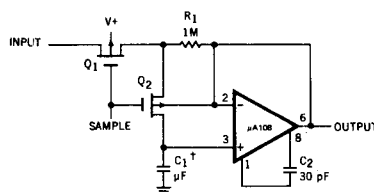


* In addition to increasing speed, the 101A raises high and low frequency gain, increases output drive capability and eliminates thermal feedback.

[†] Power Bandwidth: 250 kHz
Small Signal Bandwidth: 3.5 MHz
Slew Rate: 10 V/μs

$$\ddagger C_5 = \frac{6 \times 10^{-8}}{R_1}$$

SAMPLE AND HOLD



* Worst case drift less than 2.5 mV/s

[†] Teflon, Polyethylene or Polycarbonate Dielectric Capacitor