5041 series

High-stability Crystal Oscillator IC with Frequency Adjustment Function

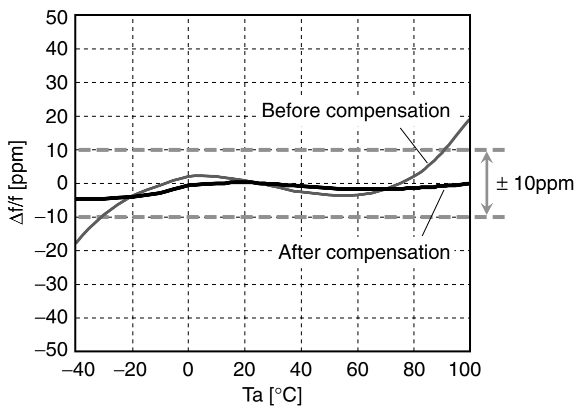
OVERVIEW

The 5041 series are high-stability clock oscillator ICs with built-in frequency adjustment functions. The frequency adjustment functions can be optimized, by the addition of a minimal adjustment process, to improve the frequency stability. The function is implemented using frequency adjustment data written to a built-in EEPROM over a 1-wire serial interface. The ICs are ideal for compact crystal oscillators for use in applications such as WiMAX (Worldwide Interoperability for Microwave Access) and PLC (Power Line Communication) that require high frequency stability in the order of ±30 to ±10ppm. They use a pad layout suitable for flip chip bonding mounting.

FEATURES

- Realizing frequency stability improvement with minimal additional process
- Temperature compensation range/ operating temperature range: –40°C to +85°C
- Frequency adjustment functions built-in
  - Frequency-temperature characteristics compensation function
    AT-cut crystal, 3rd order harmonic frequency-temperature characteristics compensation, with independent low-temperature and high-temperature range compensation settings
    - Center frequency adjustment function
    - Temperature rotation compensation function
    - Low-temperature characteristics compensation
    - High-temperature characteristics compensation
- Rewritable EEPROM built-in
- 6 pads: same as general clock oscillator ICs
- Operating supply voltage range
  - 5041A××: 2.25V to 3.63V
  - 5041B×A: 1.60V to 2.25V
- Recommended oscillation frequency range:
  20MHz to 55MHz (for fundamental oscillation)
- Frequency divider built-in:
  - Selectable by version: f_O, $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$, $f_O/32$
  - Frequency divider output for 0.625MHz (min) low frequency output
- Standby function
  High-impedance in standby mode, oscillator stops
- CMOS output
- 15pF output load
- Pad layout for flip chip bonding
- Wafer form (WF5041×××)

FREQUENCY CHARACTERISTICS COMPENSATION BEFORE and AFTER ADJUSTMENT



APPLICATIONS

- 3.2mm × 2.5mm, 2.5mm × 2.0mm, 2.0mm × 1.6mm size miniature crystal oscillator modules
- WiMAX, WiBro, PLC and applications requiring high-stability clock oscillators

ORDERING INFORMATION

Device	Package
WF5041×××–4	Wafer form

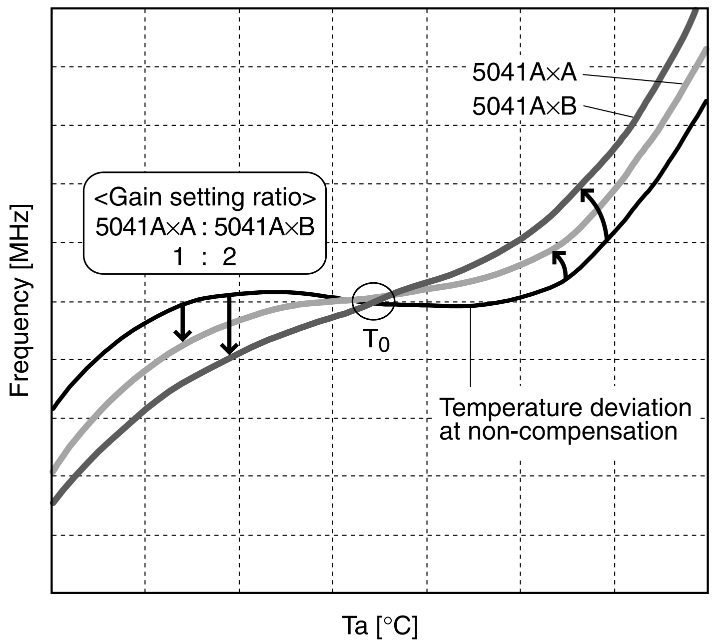
SERIES CONFIGURATION

Pad layout	Recommended oscillation frequency range[*1] [MHz]	Operating supply voltage range [V]	Temperature adjustment function gain setting ratio[*2]	Output frequency and version name[*3]					
				f_O	$f_O/2$	$f_O/4$	$f_O/8$	$f_O/16$	$f_O/32$
for flip chip bonding	20 to 55	2.25 to 3.63	1	5041A1A	5041A2A	5041A3A	5041A4A	5041A5A	5041A6A
			2	5041A1B	5041A2B	5041A3B	5041A4B	5041A5B	5041A6B
		1.60 to 2.25	(1)	(5041B1A)	(5041B2A)	(5041B3A)	(5041B4A)	(5041B5A)	(5041B6A)

*1. The recommended oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.
*2. Values in parentheses ( ) are provisional only.
*3. Versions in parentheses ( ) are under development.

TEMPERATURE ADJUSTMENT FUNCTION GAIN SETTING RATIO

Temperature adjustment function gain setting ratio of 5041A×A and 5041A×B differs. In the case of temperature adjustment function that rotates temperature characteristics on T_0 origin, adjustment sensitivity of 5041A×B is designed twice as higher than that of 5041A×A based on non-compensation temperature deviation in same register value setting.

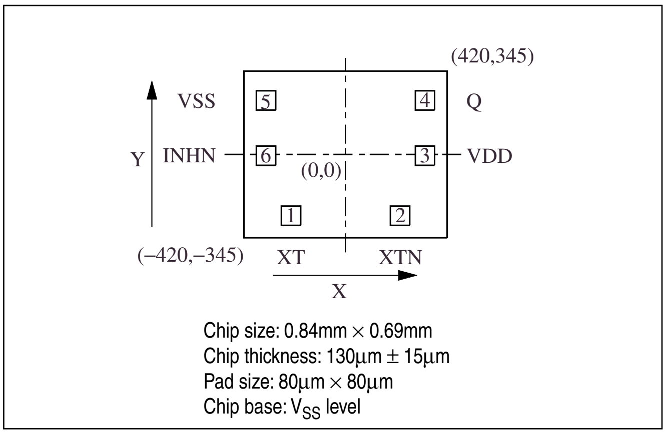


VERSION NAME

Device	Package	Version name
WF5041×××–4	Wafer form	WF5041□□□ –4 Form WF: Wafer form Temperature adjustment function gain setting ratio Frequency divider function (output frequency) Operating supply voltage

PAD LAYOUT

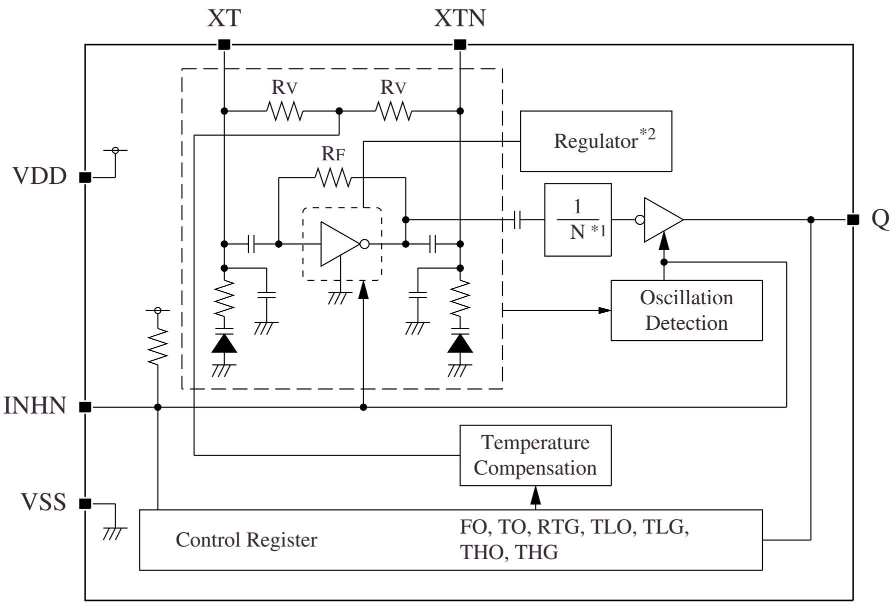
(Unit: µm)



PAD DIMENSIONS　PIN DESCRIPTION

Pad No.	Pin	I/O	Name	Description	Pad dimensions [µm]	
					X	Y
1	XT	I	Amplifier input	Crystal connection pins. Crystal is connected between XT and XTN.	–225.2	–253.5
2	XTN	O	Amplifier output		225.2	–253.5
3	VDD	–	(+) supply voltage	–	328.5	–5.0
4	Q	O	Output	Output frequency determined by internal circuit to one of f_O, $f_O/2$, $f_O/4$, $f_O/8$, $f_O/16$, $f_O/32$. High impedance in standby mode	328.5	223.8
5	VSS	–	(–) ground	–	–328.5	223.8
6	INHN	I	Output state control input	High impedance when LOW (oscillator stops). Power-saving pull-up resistor built-in.	–328.5	–5.0

BLOCK DIAGRAM



*1. N = 1, 2, 4, 8, 16, 32 (mask option)
*2. 5041A×× version only

ABSOLUTE MAXIMUM RATINGS

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Conditions	Rating	Unit
Supply voltage range	V_{DD}	Between VDD and VSS	–0.3 to +4.0	V
Program read/write supply voltage range	V_{PP}	Between INHN and VSS	–0.3 to +16.5	V
Input voltage range*1	V_{IN}	Input pins	–0.3 to V_{DD} + 0.3	V
Output voltage range*1	V_{OUT}	Output pins	–0.3 to V_{DD} + 0.3	V
Output current	I_{OUT}	Q pin	± 20	mA
Storage temperature range	T_{STG}	Wafer form	–65 to +150	°C
EEPROM maximum writes	N_{EW}		100	times

*1. V_{DD} is a V_{DD} value of recommended operating conditions.

Note. Absolute maximum ratings are the values that must never exceed even for a moment. This product may suffer breakdown if any one of these parameter ratings is exceeded. Operation and characteristics are guaranteed only when the product is operated at recommended supply voltage range.

RECOMMENDED OPERATING CONDITIONS

V_{SS} = 0V unless otherwise noted.

Parameter	Symbol	Conditions		Rating*1			Unit
				Min	Typ	Max	
Supply voltage	V_{DD}	Between VDD and VSS	5041A××	2.25	–	3.63	V
			5041B×A	1.60	–	2.25	V
Input voltage	V_{IN}	Input pins (XT, INHN)		V_{SS}	–	V_{DD}	V
Operating temperature	T_{OPR}			–40	–	+85	°C
Oscillation frequency*2	fo	5041A××		20	–	55	MHz
		5041B×A		(20)	–	(55)	MHz
Output frequency*2	f_{OUT}	Q pin	5041A××	0.625	–	55	MHz
			5041B×A	(0.625)	–	(55)	MHz
Output load capacitance	C_{LOUT}	Q pin		–	–	15	pF

*1. Values in parentheses ( ) are provisional only.
*2. The recommended oscillation frequency is a yardstick value derived from the crystal used for NPC characteristics authentication. However, the oscillation frequency range is not guaranteed. Specifically, the characteristics can vary greatly due to crystal characteristics and mounting conditions, so the oscillation characteristics of components must be carefully evaluated.

ELECTRICAL CHARACTERISTICS

DC Characteristics (5041A1× to A6×)

V_{DD} = 2.25V to 3.63V, V_{SS} = 0V, Ta = −40°C to +85°C, C_{LOUT} = 15pF unless otherwise noted.

Parameter	Symbol	Conditions		Rating			Unit
				MIN	TYP	MAX	
Operating-mode current consumption*1	I_{DD}	5041A1× (f_{OUT} = fo), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz	V_{DD} = 2.5V	–	1.4	2.8	mA
			V_{DD} = 3.3V	–	1.7	3.4	mA
		5041A2× (f_{OUT} = fo/2), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz	V_{DD} = 2.5V	–	1.1	2.2	mA
			V_{DD} = 3.3V	–	1.4	2.7	mA
		5041A3× (f_{OUT} = fo/4), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz	V_{DD} = 2.5V	–	1.0	1.9	mA
			V_{DD} = 3.3V	–	1.2	2.4	mA
		5041A4× (f_{OUT} = fo/8), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz	V_{DD} = 2.5V	–	0.9	1.7	mA
			V_{DD} = 3.3V	–	1.0	2.1	mA
		5041A5× (f_{OUT} = fo/16), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz	V_{DD} = 2.5V	–	0.8	1.7	mA
			V_{DD} = 3.3V	–	1.0	2.0	mA
		5041A6× (f_{OUT} = fo/32), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz	V_{DD} = 2.5V	–	0.8	1.6	mA
			V_{DD} = 3.3V	–	1.0	2.0	mA
Standby-mode current consumption	I_{ST}	Measurement circuit 1, INHN = LOW		–	–	10	μA
HIGH-level output voltage	V_{OH}	Q pin, Measurement circuit 3, I_{OH} = −4mA		V_{DD}−0.4	–	–	V
LOW-level output voltage	V_{OL}	Q pin, Measurement circuit 3, I_{OL} = 4mA		–	–	0.4	V
Output leakage current	I_Z	Measurement circuit 4, INHN = LOW	Q = V_{DD}	–	–	10	μA
			Q = V_{SS}	−10	–	–	μA
HIGH-level input current	V_{IH}	INHN pin, Measurement circuit 5		0.7V_{DD}	–	–	V
LOW-level input current	V_{IL}			–	–	0.3V_{DD}	V
INHN pull-up resistance	R_{PU1}	Measurement circuit 6	INHN = V_{SS}	0.4	1.5	10	MΩ
	R_{PU2}		INHN = 0.7V_{DD}	50	100	200	kΩ

*1. The consumption current I_{DD} (C_{LOUT}) with a load capacitance (C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.
I_{DD} (C_{LOUT}) [mA] = I_{DD} [mA] + C_{LOUT} [pF] × V_{DD} [V] × f_{OUT} [MHz] × 10^{-3}

DC Characteristics (5041B1A to B6A)

V_{DD} = 1.60V to 2.25V, V_{SS} = 0V, Ta = –40°C to +85°C, C_{LOUT} = 15pF unless otherwise noted.

Parameter	Symbol	Conditions		Rating			Unit
				MIN	TYP	MAX	
Operating-mode current consumption*1	I_{DD}	5041B1A (f_{OUT} = fo), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz, V_{DD} = 1.8V		–	1.7	3.4	mA
		5041B2A (f_{OUT} = fo/2), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz, V_{DD} = 1.8V		–	1.5	3.3	mA
		5041B3A (f_{OUT} = fo/4), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz, V_{DD} = 1.8V		–	1.4	3.2	mA
		5041B4A (f_{OUT} = fo/8), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz, V_{DD} = 1.8V		–	1.4	3.1	mA
		5041B5A (f_{OUT} = fo/16), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz, V_{DD} = 1.8V		–	1.3	3.1	mA
		5041B6A (f_{OUT} = fo/32), Measurement circuit 1, no load, INHN = HIGH, fo = 48MHz, V_{DD} = 1.8V		–	1.3	3.0	mA
Standby-mode current consumption	I_{ST}	Measurement circuit 1, INHN = LOW		–	–	10	µA
HIGH-level output voltage	V_{OH}	Q pin, Measurement circuit 3, I_{OH} = –4mA		V_{DD}–0.4	–	–	V
LOW-level output voltage	V_{OL}	Q pin, Measurement circuit 3, I_{OL} = 4mA		–	–	0.4	V
Output leakage current	I_Z	Measurement circuit 4, INHN = LOW	Q = V_{DD}	–	–	10	µA
			Q = V_{SS}	–10	–	–	µA
HIGH-level input current	V_{IH}	INHN pin, Measurement circuit 5		0.7V_{DD}	–	–	V
LOW-level input current	V_{IL}			–	–	0.3V_{DD}	V
INHN pull-up resistance	R_{PU1}	Measurement circuit 6	INHN = V_{SS}	0.4	1.5	10	MΩ
	R_{PU2}		INHN = 0.7V_{DD}	50	100	200	kΩ

*1. The consumption current I_{DD} (C_{LOUT}) with a load capacitance (C_{LOUT}) connected to the Q pin is given by the following equation, where I_{DD} is the no-load consumption current and f_{OUT} is the output frequency.
I_{DD} (C_{LOUT}) [mA] = I_{DD} [mA] + C_{LOUT} [pF] × V_{DD} [V] × f_{OUT} [MHz] × 10^{-3}

AC Characteristics

Clock output characteristics (5041A1× to A6×, Q pin)

V_{DD} = 2.25V to 3.63V, V_{SS} = 0V, Ta = −40°C to +85°C, C_{LOUT} = 15pF unless otherwise noted.

Parameter	Symbol	Conditions	Rating			Unit
			MIN	TYP	MAX	
Output rise time	t_r	Measurement circuit 1, $0.1V_{DD} \rightarrow 0.9V_{DD}$	–	–	4.5	ns
Output fall time	t_f	Measurement circuit 1, $0.9V_{DD} \rightarrow 0.1V_{DD}$	–	–	4.5	ns
Output duty cycle*1	Duty	Measurement circuit 1, threshold voltage $0.5V_{DD}$, Duty = Tw/T × 100	45	50	55	%
Output disable delay time	t_{OD}	Measurement circuit 2, INHN = HIGH → LOW	–	–	100	ns

*1. This parameter is measured using the NPC's standard crystal. Note that the values will vary with the crystal characteristics used or mounting conditions.

Clock output characteristics (5041B1A to B6A, Q pin)

V_{DD} = 1.60V to 2.25V, V_{SS} = 0V, Ta = −40°C to +85°C, C_{LOUT} = 15pF unless otherwise noted.

Parameter	Symbol	Conditions	Rating*1			Unit
			MIN	TYP	MAX	
Output rise time	t_r	Measurement circuit 1, $0.1V_{DD} \rightarrow 0.9V_{DD}$	–	–	5	ns
Output fall time	t_f	Measurement circuit 1, $0.9V_{DD} \rightarrow 0.1V_{DD}$	–	–	5	ns
Output duty cycle*2	Duty	Measurement circuit 1, threshold voltage $0.5V_{DD}$, Duty = Tw/T × 100	(45)	(50)	(55)	%
Output disable delay time	t_{OD}	Measurement circuit 2, INHN = HIGH → LOW	–	–	100	ns

*1. Values in parentheses ( ) are provisional only.
*2. This parameter is measured using the NPC's standard crystal. Note that the values will vary with the crystal characteristics used or mounting conditions.

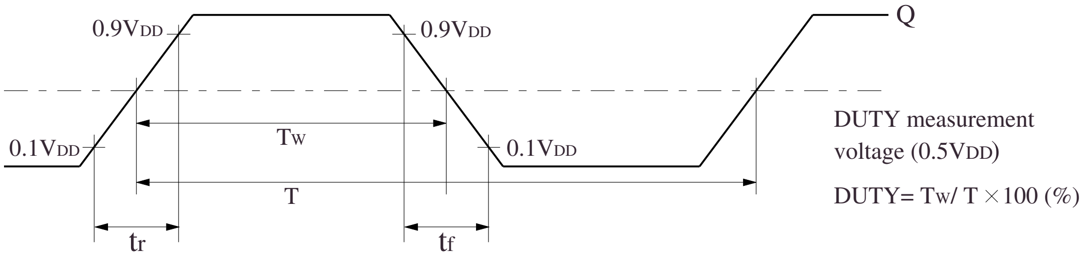
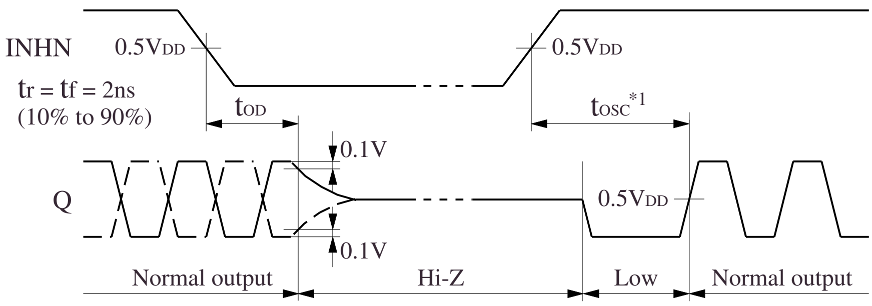


Figure 1. Output switching waveform



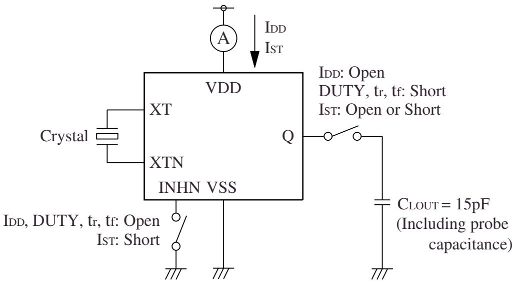
*1. t_{OSC} is oscillator start-up time. It is interval of time until the oscillation is stabilized and varies with the crystal used. Please contact us for further details.

Figure 2. Output disable timing chart

MEASUREMENT CIRCUITS

Measurement Circuit 1

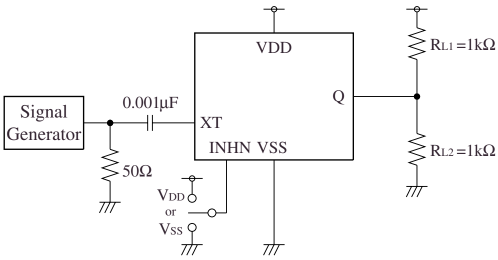
Parameters: I_{DD}, I_{ST}, Duty, t_r, t_f



Note: The AC characteristics are observed using an oscilloscope on pin Q.

Measurement Circuit 2

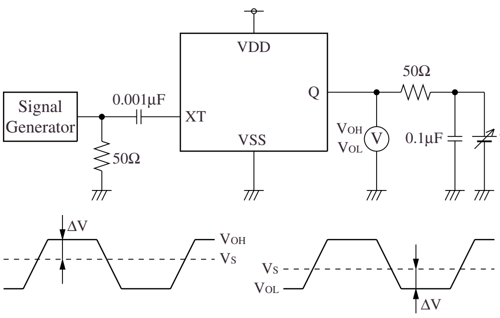
Parameters: t_{OD}



XT input signal: 1Vp-p, sine wave

Measurement Circuit 3

Parameters: V_{OH}, V_{OL}



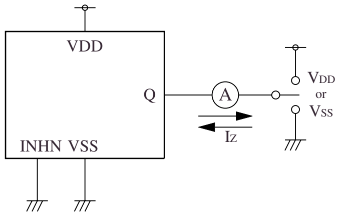
V_S adjusted such that $\Delta V = 50 \times I_{OH}$.

V_S adjusted such that $\Delta V = 50 \times I_{OL}$.

XT input signal: 1Vp-p, sine wave

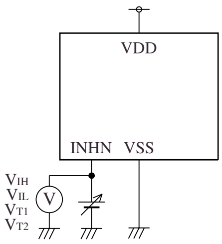
Measurement Circuit 4

Parameters: I_Z



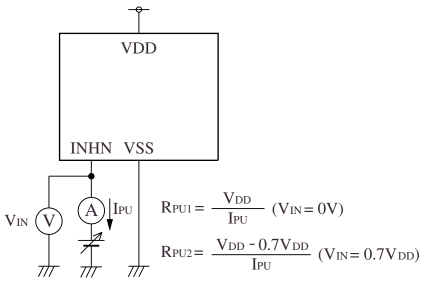
Measurement Circuit 5

Parameters: V_{IH}, V_{IL}



Measurement Circuit 6

Parameters: R_{PU1}, R_{PU2}



FUNCTIONAL DESCRIPTION

Frequency Adjustment Function

The 5041 series ICs have a built-in oscillator frequency adjustment function. The frequency adjustment settings are written to and stored in internal EEPROM, making the devices easy to setup. A typical compensation sequence is shown below.

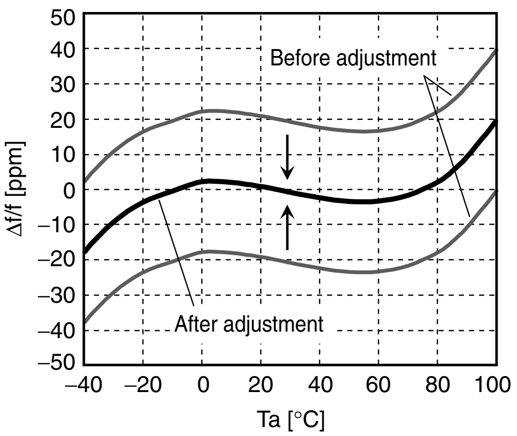


Figure 3. Center frequency adjustment

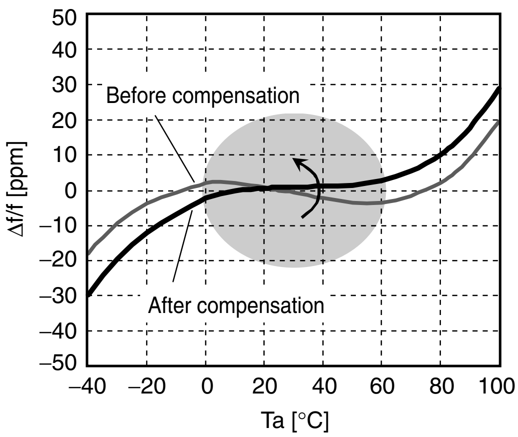


Figure 4. Temperature rotation compensation

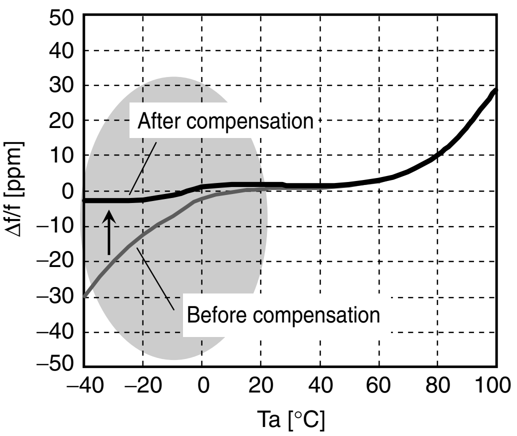


Figure 5. Low-temperature characteristics compensation

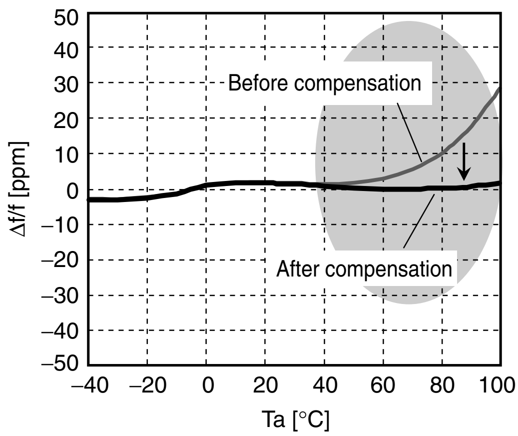


Figure 6. High-temperature characteristics compensation

Power-saving Pull-up Resistor

The INHN pin pull-up resistance R_{PU1} or R_{PU2} changes in response to the input level (open, HIGH, or LOW). When INHN is tied LOW level, the pull-up resistance is large (R_{PU1}), reducing the current consumed by the resistance. When INHN is left open circuit (HIGH), the pull-up resistance is small (R_{PU2}), which increases the input susceptibility to external noise. However, the pull-up resistance ties the INHN pin HIGH level to prevent external noise from unexpectedly stopping the output.

Oscillation Detector Function

The 5041 series also feature an oscillation detector circuit. This circuit functions to disable the outputs until the oscillator circuit starts and oscillation becomes stable. This alleviates the danger of abnormal oscillator output at oscillator start-up when power is applied or when INHN is switched.

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