

NLX1G125

Non-Inverting 3-State Buffer

The NLX1G125 is an advanced high-speed 2-input CMOS non-inverting 3-state buffer in ultra-small footprint.

The NLX1G125 input structures provide protection when voltages up to 7.0 V are applied, regardless of the supply voltage.

Features

- High Speed: $t_{PD} = 2.7 \text{ ns}$ (Typ) @ $V_{CC} = 5.0 \text{ V}$
- Designed for 1.65 V to 5.5 V V_{CC} Operation
- Low Power Dissipation: $I_{CC} = 1 \mu\text{A}$ (Max) at $T_A = 25^\circ\text{C}$
- 24 mA Balanced Output Source and Sink Capability
- Balanced Propagation Delays
- Overvoltage Tolerant (OVT) Input Pins
- Ultra-Small Packages
- These are Pb-Free Devices

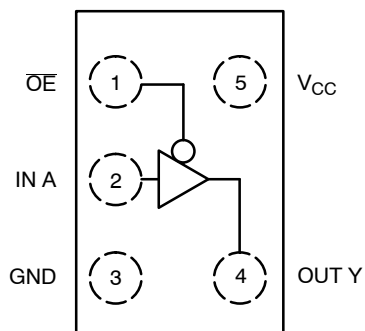


Figure 1. Pinout (Top View)

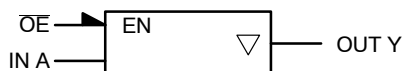


Figure 2. Logic Symbol



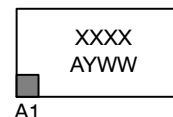
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM



**5 PIN FLIP-CHIP
CASE 499BG**



XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week

PIN ASSIGNMENT

	PIN ASSIGNMENT
1	OE
2	IN A
3	GND
4	OUT Y
5	V _{CC}

FUNCTION TABLE

A Input	OE Input	Y Output
L	L	L
H	L	H
X	H	Z

X = Don't Care

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

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MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	−0.5 to +7.0	V
V _{IN}	DC Input Voltage	−0.5 to +7.0	V
V _{OUT}	DC Output Voltage	−0.5 to +7.0	V
I _{IK}	DC Input Diode Current V _{IN} < GND	−50	mA
I _{OK}	DC Output Diode Current V _{OUT} < GND	−50	mA
I _{OUT}	DC Output Sink Current	±50	mA
I _{CC}	DC Supply Current per Supply Pin	±100	mA
I _{GND}	DC Ground Current per Ground Pin	±100	mA
T _{STG}	Storage Temperature Range	−65 to +150	°C
T _L	Lead Temperature, 1 mm from Case for 10 Seconds	TBD	°C
T _J	Junction Temperature Under Bias	TBD	°C
θ _{JA}	Thermal Resistance (Note 1)	TBD	°C/W
P _D	Power Dissipation in Still Air at 85°C	TBD	mW
MSL	Moisture Sensitivity	Level 1	
F _R	Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in	
V _{ESD}	ESD Withstand Voltage Human Body Model (Note 2) Machine Model (Note 3) Charged Device Model (Note 4)	> 2000 > 200 N/A	V
I _{LATCHUP}	Latchup Performance Above V _{CC} and Below GND at 125 °C (Note 5)	±500	mA

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Measured with minimum pad spacing on an FR4 board, using 10 mm-by-1 inch, 2 ounce copper trace with no air flow.
2. Tested to EIA/JESD22-A114-A.
3. Tested to EIA/JESD22-A115-A.
4. Tested to JESD22-C101-A.
5. Tested to EIA / JESD78.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	Positive DC Supply Voltage Operating Data Retention Only	1.65 1.5	5.5 5.5	V
V _{IN}	Digital Input Voltage (Note 6)	0	5.5	V
V _{OUT}	Output Voltage	0	5.5	V
T _A	Operating Free-Air Temperature	−55	+125	°C
Δt/ΔV	Input Transition Rise or Fall Rate V _{CC} = 1.8 V ± 0.15 V V _{CC} = 2.5 V ± 0.2 V V _{CC} = 3.3 V ± 0.3 V V _{CC} = 5.0 V ± 0.5 V	0 0 0 0	20 20 10 5.0	ns/V

6. Unused inputs may not be left open. All inputs must be tied to a high or low-logic input voltage level.

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DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = 25 °C			T _A = -55°C to +125°C		Unit
				Min	Typ	Max	Min	Max	
V _{IH}	Low-Level Input Voltage		1.65	0.75 x V _{CC}			0.75 x V _{CC}		V
			2.3 to 5.5	0.70 x V _{CC}			0.70 x V _{CC}		
V _{IL}	Low-Level Input Voltage		1.65			0.25 x V _{CC}		0.25 x V _{CC}	V
			2.3 – 5.5			0.30 x V _{CC}		0.30 x V _{CC}	
V _{OH}	High-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OH} = -100 µA	1.65 – 5.5	V _{CC} -0.1	V _{CC}		V _{CC} -0.1		V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = -4 mA	1.65	1.29	1.52		1.29		
		I _{OH} = -8 mA	2.3	1.9	2.15		1.9		
		I _{OH} = -12 mA	2.7	2.2	2.4		2.2		
		I _{OH} = -16 mA	3.0	2.4	2.8		2.4		
		I _{OH} = -24 mA	3.0	2.3	2.68		2.3		
		I _{OH} = -32 mA	4.5	3.8	4.2		3.8		
V _{OL}	Low-Level Output Voltage	V _{IN} = V _{IH} or V _{IL} I _{OL} = 100 µA	1.65 – 5.5			0.1		0.1	V
		V _{IN} = V _{IH} or V _{IL} I _{OH} = 4 mA	1.65		0.08	0.24		0.24	
		I _{OH} = 8 mA	2.3		0.1	0.3		0.3	
		I _{OH} = 12 mA	2.7		0.12	0.4		0.4	
		I _{OH} = 16 mA	3.0		0.15	0.4		0.4	
		I _{OH} = 24 mA	3.0		0.22	0.55		0.55	
		I _{OH} = 32 mA	4.5		0.22	0.55		0.55	
I _{IN}	Input Leakage Current	0 ≤ V _{IN} ≤ 5.5V	0 to 5.5			±0.1		±1.0	µA
I _{OZ}	3-State Output Leakage Current	V _{IN} = V _{IH} or V _{IL} 0 ≤ V _{OUT} ≤ 5.5V	0			±0.5		±5.0	µA
I _{OFF}	Power-Off Output Leakage Current	V _{IN} = 5.5 V	0			1.0		10	µA
I _{CC}	Quiescent Supply Current	0 ≤ V _{IN} ≤ V _{CC}	5.5			1.0		10	µA

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AC ELECTRICAL CHARACTERISTICS (Input $t_r = t_f = 2.5$ ns)

Symbol	Parameter	V_{CC} (V)	Test Condition	$T_A = 25\text{ }^{\circ}\text{C}$			$T_A = -55^{\circ}\text{C to } +125^{\circ}\text{C}$		Unit
				Min	Typ	Max	Min	Max	
t_{PLH} , t_{PHL}	Propagation Delay, Input to Output (Figures 3 and 4, Table 1)	1.65–1.95	$R_L = 1\text{ M}\Omega$, $C_L = 15\text{ pF}$	2.0	6.0	10	2.0	10.5	ns
		2.3–2.7	$R_L = 1\text{ M}\Omega$, $C_L = 15\text{ pF}$	1.0	3.4	7.5	1.0	8.0	
		3.0–3.6	$R_L = 1\text{ M}\Omega$, $C_L = 15\text{ pF}$	0.8	2.5	5.2	0.8	5.5	
			$R_L = 500\text{ }\Omega$, $C_L = 50\text{ pF}$	1.2	3.1	5.7	1.2	6.0	
		4.5–5.5	$R_L = 1\text{ M}\Omega$, $C_L = 15\text{ pF}$	0.5	1.8	4.5	0.5	4.8	
			$R_L = 500\text{ }\Omega$, $C_L = 50\text{ pF}$	0.8	2.3	5.0	0.8	5.3	
t_{PZH} , t_{PZL}	Output Enable Time (Figures 5, 6 and 7, Table 1)	1.65–1.95	$R_L = 250\text{ }\Omega$, $C_L = 50\text{ pF}$	2.0	7.6	9.5	2.0	10	ns
		2.3–2.7		1.8		8.5	1.8	9.0	
		3.0–3.6		1.2		6.2	1.2	6.5	
		4.5–5.5		0.8		5.5	0.8	5.8	
t_{PHZ} , t_{PLZ}	Output Disable Time (Figures 5, 6 and 7, Table 1)	1.65–1.95	$R_L = R_1 = 5\text{--}0\text{ }\Omega$, $C_L = 50\text{ pF}$	2.0	8.0	10	2.0	10.5	ns
		2.3–2.7		1.5		8.0	1.5	8.5	
		3.0–3.6		0.8		5.7	0.8	6.0	
		4.5–5.5		0.3		4.7	0.3	5.0	
C_{IN}	Input Capacitance	5.5	$V_{IN} = 0\text{ V or } V_{CC}$		2.5				pF
C_{OUT}	Output Capacitance	5.5	$V_{IN} = 0\text{ V or } V_{CC}$		2.5				pF
C_{PD}	Power Dissipation Capacitance (Note 7)	3.3	10 MHz		9.0				pF
		5.5	$V_{IN} = 0\text{ V or } V_{CC}$		11				

7. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the dynamic operating current consumption without load. Average operating current can be obtained by the equation $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$. C_{PD} is used to determine the no-load dynamic power consumption: $P_D = C_{PD} \cdot V_{CC}^2 \cdot f_{in} + I_{CC} \cdot V_{CC}$.

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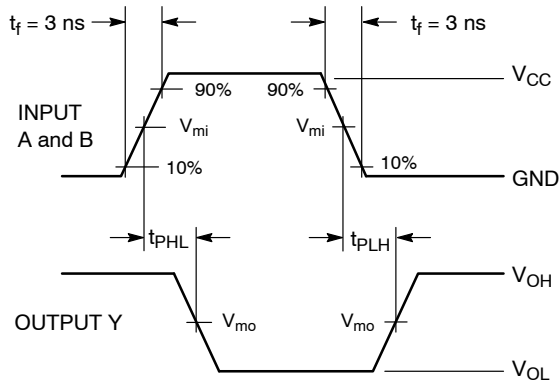
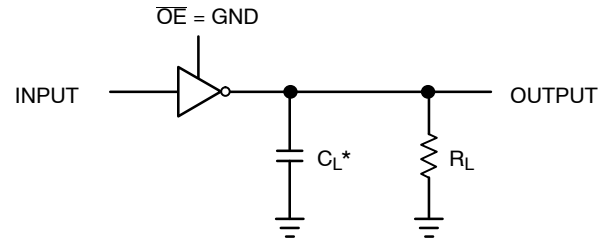
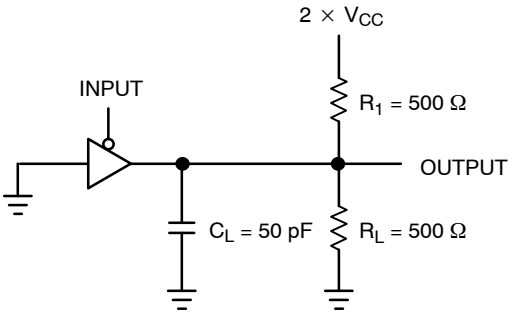


Figure 3. Switching Waveform



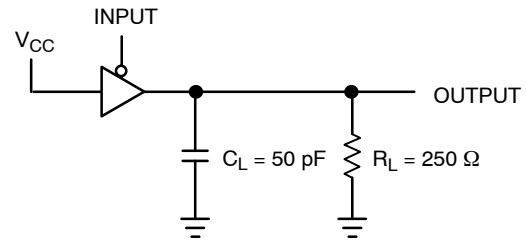
*Includes all probe and jig capacitance.
A 1 MHz square input wave is recommended for propagation delay tests.

Figure 4. T_{PLH} or T_{PHL}



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 5. T_{PZL} or T_{PL}



A 1 MHz square input wave is recommended for propagation delay tests.

Figure 6. T_{PZH} or T_{PHZ}

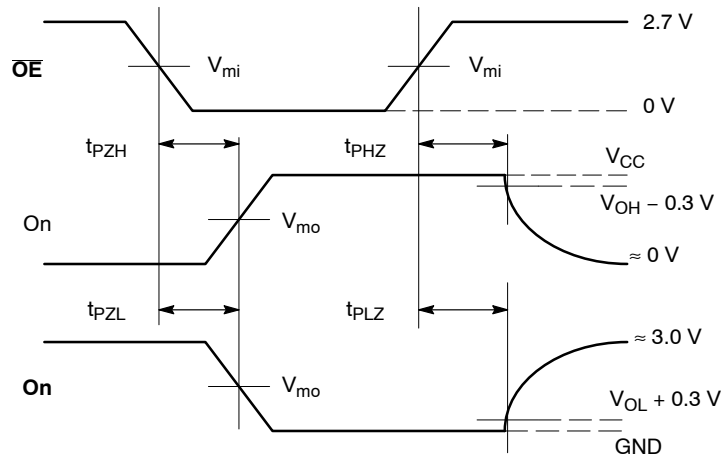


Figure 7. AC Output Enable and Disable Waveform

Table 1. OUTPUT ENABLE AND DISABLE TIMES

$t_R = t_F = 2.5$ ns, 10% to 90%; $f = 1$ MHz; $t_W = 500$ ns

Symbol	V_{CC}		
	$3.3\text{ V} \pm 0.3\text{ V}$	2.7 V	$2.5\text{ V} \pm 0.2\text{ V}$
V_{mi}	1.5 V	1.5 V	$V_{CC}/2$
V_{mo}	1.5 V	1.5 V	$V_{CC}/2$

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DEVICE ORDERING INFORMATION

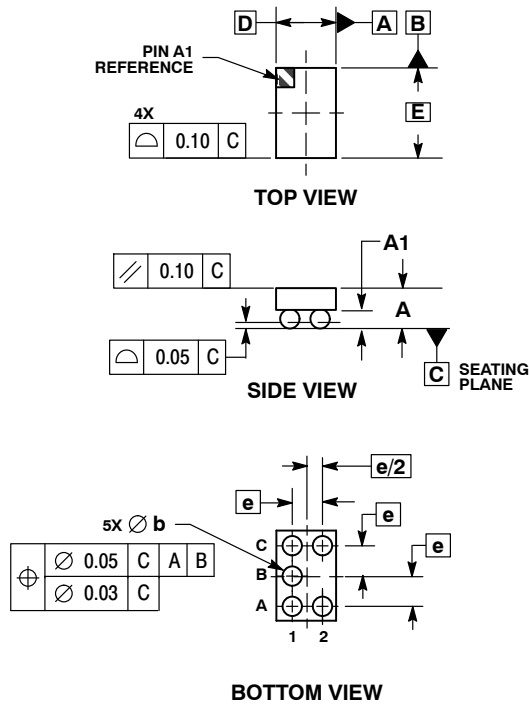
Device	Package	Shipping†
NLX1G125FCT1G	Flip-Chip 5 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

5 PIN FLIP-CHIP CASE 499BG-01 ISSUE O

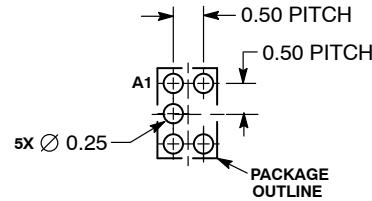


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. COPLANARITY APPLIES TO SPHERICAL CROWNS OF SOLDER BALLS.

MILLIMETERS		
DIM	MIN	MAX
A	0.44	0.50
A1	0.15	0.19
b	0.21	0.25
D	0.90 BSC	
E	1.40 BSC	
e	0.50 BSC	

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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