Green Phase-Shifted Full-Bridge Controller With Synchronous Rectification

Check for Samples: UCC28950

FEATURES

- **Enhanced Wide Range Resonant Zero Voltage Switching (ZVS) Capability**
- **Direct Synchronous Rectifier (SR) Control**
- **Light-Load Efficiency Management Including**
  - **Burst Mode Operation**
  - **Discontinuous Conduction Mode (DCM), Dynamic SR On/Off Control with Programmable Threshold**
  - **Programmable Adaptive Delay**
- **Average or Peak Current Mode Control with Programmable Slope Compensation and Voltage Mode Control**
- **Closed Loop Soft Start and Enable Function**
- **Programmable Switching Frequency up to 1 MHz with Bi-Directional Synchronization**
- **(+/-3%) Cycle-by-Cycle Current Limit Protection with Hiccup Mode Support**
- **150-µA Start-Up Current**
- **V_{DD} Under Voltage Lockout**
- **Wide Temperature Range -40°C to 125°C**

APPLICATIONS

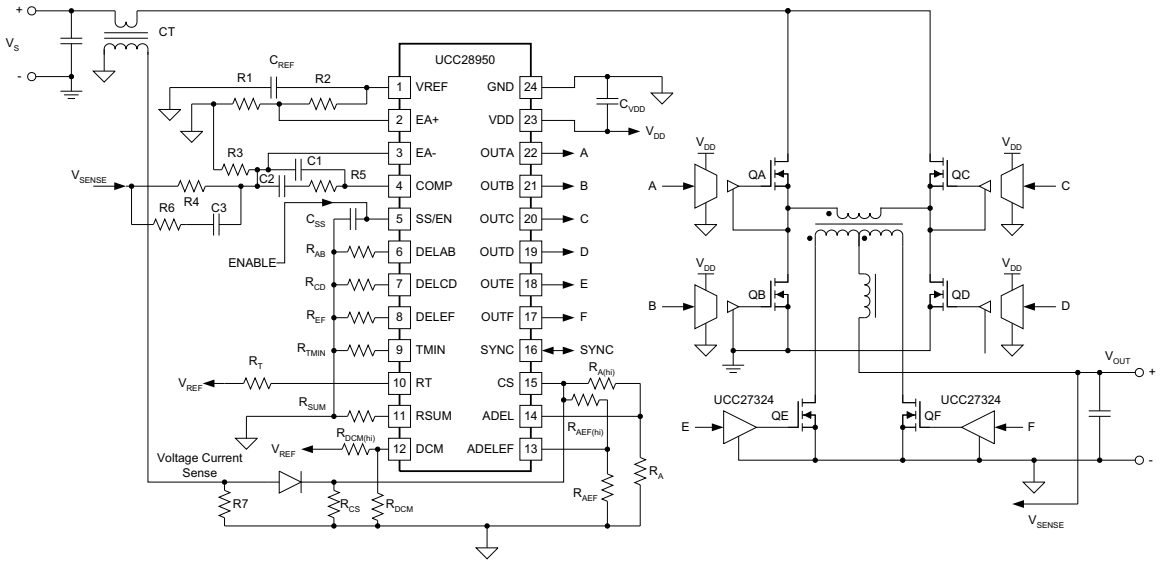
- **Phase-Shifted Full-Bridge Converters**
- **Server, Telecom Power Supplies**
- **Industrial Power Systems**
- **High-Density Power Architectures**
- **Solar Inverters, and Electric Vehicles**

DESCRIPTION

The UCC28950 enhanced phase-shifted controller builds upon Texas Instrument's industry standard UCCx895 phase-shifted controller family with enhancements that offer best in class efficiency in today's high performance power systems. The UCC28950 implements advanced control of the full-bridge along with active control of the synchronous rectifier output stage.

The primary-side signals allow programmable delays to ensure ZVS operation over wide-load current and input voltage range, while the load current naturally tunes the secondary-side synchronous rectifiers switching delays, maximizing overall system efficiency.

UCC28950 Typical Application



DESCRIPTION (CONT.)

The UCC28950 also offers multiple light-load management features including burst mode and dynamic SR on/off control when transitioning in and out of Discontinuous Current Mode (DCM) operation, ensuring ZVS operation is extended down to much lighter loads.

In addition, the UCC28950 includes support for peak current along with voltage mode control, programmable switching frequency up to 1 MHz and a wide set of protection features including cycle-by-cycle current limit, UVLO and thermal shutdown. A 90-degree phase-shifted interleaved synchronized operation can be easily arranged between two converters.

The UCC28950 is available in TSSOP-24 package.

ORDERING INFORMATION

TEMPERATURE RANGE, $T_A = T_J$	PACKAGE	TAPE AND REEL QTY.	PART NUMBER
-40°C to 125°C	Plastic 24-pin TSSOP (PW)	250	UCC28950PW
		2000	UCC28950PWR

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) (1)(2)

PARAMETER	VALUE	UNIT
Input supply voltage range, V_{DD} (3)	-0.4 to 20.0	V
OUTA, OUTB, OUTC, OUTD, OUTE, OUTF	-0.4 to VDD + 0.4	
Inputs voltages on DELAB, DELCD, DELEF, SS/EN, DCM, TMIN, RT, SYNC, RSUM, EA+, EA-, COMP, CS, ADEL, ADELEF	-0.4 to VREF + 0.4	
Output voltage on VREF	-0.4 to 5.6	
ESD rating, HBM	2 k	
ESD rating, CDM	500	
Continuous total power dissipation	See dissipation rating table	
Operating virtual junction temperature range, T_J	-40 to 150	°C
Operating ambient temperature range, T_A	-40 to 125	
Storage temperature, T_{stg}	-65 to 150	
Lead temperature (soldering, 10 sec.)	300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) These devices are sensitive to electrostatic discharge; follow proper device handling procedures.
(3) All voltages are with respect to GND unless otherwise noted. Currents are positive into, negative out of the specified terminal. See Packaging Section of the datasheet for thermal limitations and considerations of packages.

DISSIPATION RATINGS(1)

PACKAGE	$R_{\theta JC}$ (°C/W)	$R_{\theta JA}$ (°C/W)	DERATING FACTOR	POWER RATING		
			ABOVE T_A = 25°C	T_A < 25°C	T_A = 70°C	T_A = 85°C
PW	18.5	89.3	11.2 mW/ °C	1.12 W	0.615 W	0.448 W

(1) These thermal data are taken at standard JEDEC test conditions and are useful for the thermal performance comparison of different packages. The cooling condition and thermal impedance RθJA of practical design is specific.

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

	MIN	TYP	MAX	UNIT
Supply voltage range, V_{DD}	8	12	17	V
Operating junction temperature range	-40		125	°C
Converter switching frequency setting range, $F_{SW(nom)}$	50		1000	kHz
Programmable delay range between OUTA, OUTB and OUTC, OUTD set by resistors DELAB and DELCD and parameter K_A (1)	30		1000	ns
Programmable delay range between OUTA, OUTF and OUTB, OUTE set by resistor DELEF, and parameter K_{EF} (1)	30		1400	
Programmable DCM range as percentage of voltage at CS (1)	5%		30%	
Programmable T_{MIN} range	100		800	ns

(1) Verified during characterization only.

ELECTRICAL CHARACTERISTICS (1)

V_{DD} = 12 V, $T_A = T_J$ = -40°C to 125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, RSUM = 124 kΩ, RMIN = 88.7 kΩ, RT = 59 kΩ connected between RT pin and 5-V voltage supply to set F_{SW} = 100 kHz (F_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from the Typical Application Diagram.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Under Voltage Lockout (UVLO)						
UVLO_RTH	Start threshold		6.75	7.3	7.9	V
UVLO_FTH	Minimum operating voltage after start		6.15	6.7	7.2	
UVLO_HYST	Hysteresis		0.53	0.6	0.75	
Supply Currents						
$I_{DD(off)}$	Startup current	V_{DD} is 5.2 V		150	270	µA
I_{DD}	Operating supply current			5	10	mA
VREF Output Voltage						
V_{REF}	VREF total output range	0 ≤ IR ≤ 20 mA; V_{DD} = from 8 V to 17 V	4.925	5	5.075	V
ISCC	Short circuit current	VREF = 0 V	-53		-23	mA
Switching Frequency (½ of internal oscillator frequency F_{OSC})						
$F_{SW(nom)}$	Total range		92	100	108	KHz
D_{MAX}	Maximum duty cycle			95%	97%	
Synchronization						
PH_{SYNC}	Total range	RT = 59 kΩ between RT and GND; Input pulses 200 kHz, D = 0.5 at SYNC	85	90	95	°PH
F_{SYNC}	Total range	RT = 59 kΩ between RT and 5 V; -40 °C ≤ T_J ≤ 125°C	180	200	220	kHz
T_{PW}	Pulse width		2.2	2.5	2.8	µs

(1) Typical values for T_A = 25°C

ELECTRICAL CHARACTERISTICS(1) (continued)

V_{DD} = 12 V, $T_A = T_J$ = -40°C to 125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, RSUM = 124 kΩ, RMIN = 88.7 kΩ, RT = 59 kΩ connected between RT pin and 5-V voltage supply to set F_{SW} = 100 kHz (F_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from the Typical Application Diagram.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Error Amplifier						
V_{ICM}	Common mode input voltage range	V_{ICM} range ensures parameters, the functionality ensured for 3.6 V < V_{ICM} < VREF + 0.4 V, and -0.4 V < V_{ICM} < 0.5 V	0.5		3.6	V
V_{IO}	Offset voltage		- 7		7	mV
I_{BIAS}	Input bias current		-1		1	µA
EA_{HIGH}	High-level output voltage	(EA+) - (EA-) = 500 mV, I_{EAOUT} = -0.5 mA	3.9	4.25		V
EA_{LOW}	Low-level output voltage	(EA+) - (EA-) = -500 mV, I_{EAOUT} = 0.5 mA		0.25	0.35	
I_{SOURCE}	Error amplifier source current		-8	-3.75	-0.5	mA
I_{SINK}	Error amplifier sink current		2.7	4.6	5.75	
I_{VOL}	Open-loop dc gain			100		dB
GBW	Unity gain bandwidth(2)			3		MHz
Cycle-by-Cycle Current Limit						
V_{CS_LIM}	CS pin cycle-by-cycle threshold		1.94	2	2.06	V
T_{CS}	Propagation delay from CS to OUTC and OUTD outputs	Input pulse between CS and GND from zero to 2.5 V		100		ns
Internal Hiccup Mode Settings						
I_{DS}	Discharge current to set cycle-by-cycle current limit duration	CS = 2.5 V, VSS = 4 V	15	20	25	µA
V_{HCC}	Hiccup OFF Time threshold		3.2	3.6	4.2	V
I_{HCC}	Discharge current to set Hiccup Mode OFF Time		1.90	2.55	3.2	µA
Soft Start/Enable						
I_{SS}	Charge current	V_{SS} = 0 V	20	25	30	µA
V_{SS_STD}	Shutdown/restart/reset threshold		0.25	0.50	0.70	V
V_{SS_PU}	Pull up threshold		3.3	3.7	4.3	
V_{SS_CL}	Clamp voltage		4.20	4.65	4.95	

(2) Verified during characterization only.

ELECTRICAL CHARACTERISTICS(1) (continued)

V_{DD} = 12 V, $T_A = T_J$ = -40°C to 125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, RSUM = 124 kΩ, RMIN = 88.7 kΩ, RT = 59 kΩ connected between RT pin and 5-V voltage supply to set F_{SW} = 100 kHz (F_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from the Typical Application Diagram.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Programmable Delay Time Set Accuracy and Range (3)(4)(5)(6)(7)						
T_{ABSET1}	Short delay time set accuracy between OUTA and OUTB	CS = ADEL = ADELEF = 1.8 V	32	45	56	ns
T_{ABSET2}	Long delay time set accuracy between OUTA and OUTB	CS = ADEL = ADELEF = 0.2 V	216	270	325	
T_{CDSET1}	Short delay time set accuracy between OUTC and OUTD	CS = ADEL = ADELEF = 1.8 V	32	45	56	
T_{CDSET2}	Long delay time set accuracy between OUTC and OUTD	CS = ADEL = ADELEF = 0.2 V	216	270	325	
T_{AFSET1}	Short delay time set accuracy between falling OUTA, OUTF	CS = ADEL = ADELEF = 0.2 V	22	35	48	
T_{AFSET2}	Long delay time set accuracy between falling OUTA, OUTF	CS = ADEL = ADELEF = 1.8 V	190	240	290	
T_{BESET1}	Short delay time set accuracy between falling OUTB, OUTE	CS = ADEL = ADELEF = 0.2 V	22	35	48	
T_{BESET2}	Long delay time set accuracy between falling OUTB, OUTE	CS = ADEL = ADELEF = 1.8 V	190	240	290	
ΔT_{ADBC}	Pulse matching between OUTA rise, OUTD fall and OUTB rise, OUTC fall	CS = ADEL = ADELEF = 1.8 V, COMP = 2 V	-50	0	50	
ΔT_{ABBA}	Half cycle matching between OUTA rise, OUTB rise and OUTB rise, OUTA rise	CS = ADEL = ADELEF = 1.8 V, COMP = 2 V	-50	0	50	
ΔT_{EEFF}	Pulse matching between OUTE fall, OUTE rise and OUTF fall, OUTF rise	CS = ADEL = ADELEF = 0.2 V, COMP = 2 V	-60	0	60	
ΔT_{EFFE}	Pulse matching between OUTE fall, OUTF rise and OUTF fall, OUTE rise	CS = ADEL = ADELEF = 0.2 V, COMP = 2 V	-60	0	60	

(3) See Figure 3 for timing diagram and T_{ABSET1}, T_{ABSET2}, T_{CDSET1}, T_{CDSET2} definitions.
(4) See Figure 6 for timing diagram and T_{AFSET1}, T_{AFSET2}, T_{BESET1}, T_{BESET2} definitions.
(5) Pair of outputs OUTC, OUTE and OUTD, OUTF always going high simultaneously.
(6) Outputs A or B are never allowed to go high if both outputs OUTE and OUTF are high.
(7) All delay settings are measured relatively 50% of pulse amplitude.

ELECTRICAL CHARACTERISTICS(1) (continued)

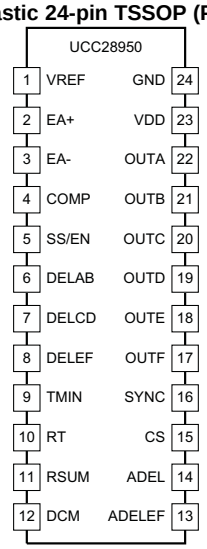
V_{DD} = 12 V, $T_A = T_J$ = -40°C to 125°C, C_{VDD} = 1 µF, C_{REF} = 1 µF, R_{AB} = 22.6 kΩ, R_{CD} = 22.6 kΩ , R_{EF} = 13.3 kΩ, RSUM = 124 kΩ, RMIN = 88.7 kΩ, RT = 59 kΩ connected between RT pin and 5-V voltage supply to set F_{SW} = 100 kHz (F_{OSC} = 200 kHz) (unless otherwise noted). All component designations are from the Typical Application Diagram.

PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNITS
Light Load Efficiency Circuit						
V_{DCM}	DCM threshold, T = 25°C	V_{DCM} = 0.4 V, Sweep CS confirm there are OUTE and OUTF pulses	0.37	0.39	0.41	V
	DCM threshold, T = 0°C to 85°C (8)	V_{DCM} = 0.4 V, Sweep CS, confirm there are OUTE and OUTF pulses	0.364	0.390	0.416	
	DCM threshold, T= -40°C to 125°C (8)	V_{DCM} = 0.4 V, Sweep CS, confirm there are OUTE and OUTF pulses	0.35	0.39	0.43	
$I_{DCM,SRC}$	DCM Sourcing Current	CS < DCM threshold	14	20	26	µA
T_{MIN}	Total range	R_{TMIN} = 88.7 kΩ	425	525	625	ns
OUTPUTS OUTA, OUTB, OUTC, OUTD, OUTE, OUTF						
$I_{SINK/SRC}$	Sink/Source peak current(8)			0.2		A
T_R	Rise time	C_{LOAD} = 100 pF		9	25	ns
T_F	Fall time	C_{LOAD} = 100 pF		7	25	
R_{SRC}	Output source resistance	I_{OUT} = 20 mA	10	20	35	Ω
R_{SINK}	Output sink resistance	I_{OUT} = 20 mA	5	10	30	
THERMAL SHUTDOWN						
	Rising threshold(8)			160		°C
	Falling threshold(8)			140		
	Hysteresis			20		

(8) Verified during characterization only.

DEVICE INFORMATION

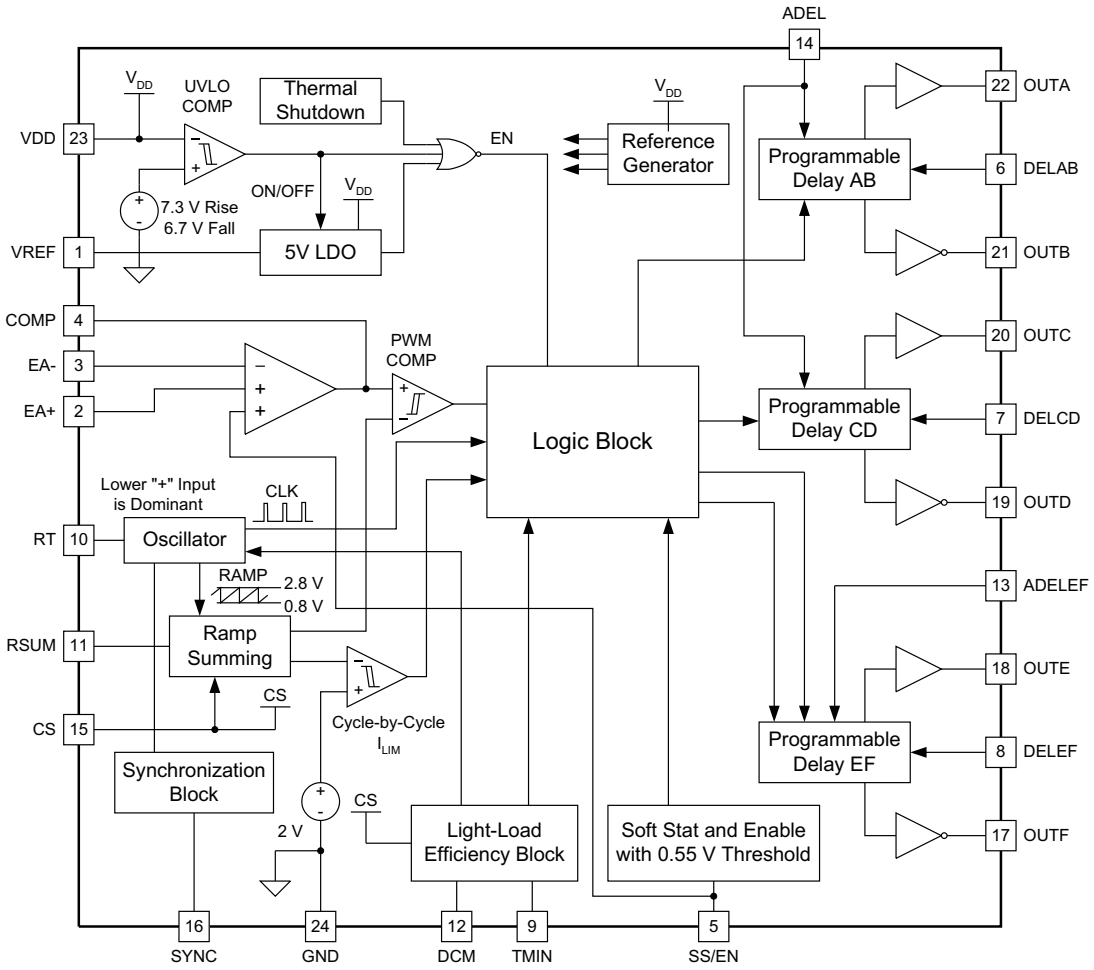
Plastic 24-pin TSSOP (PW)



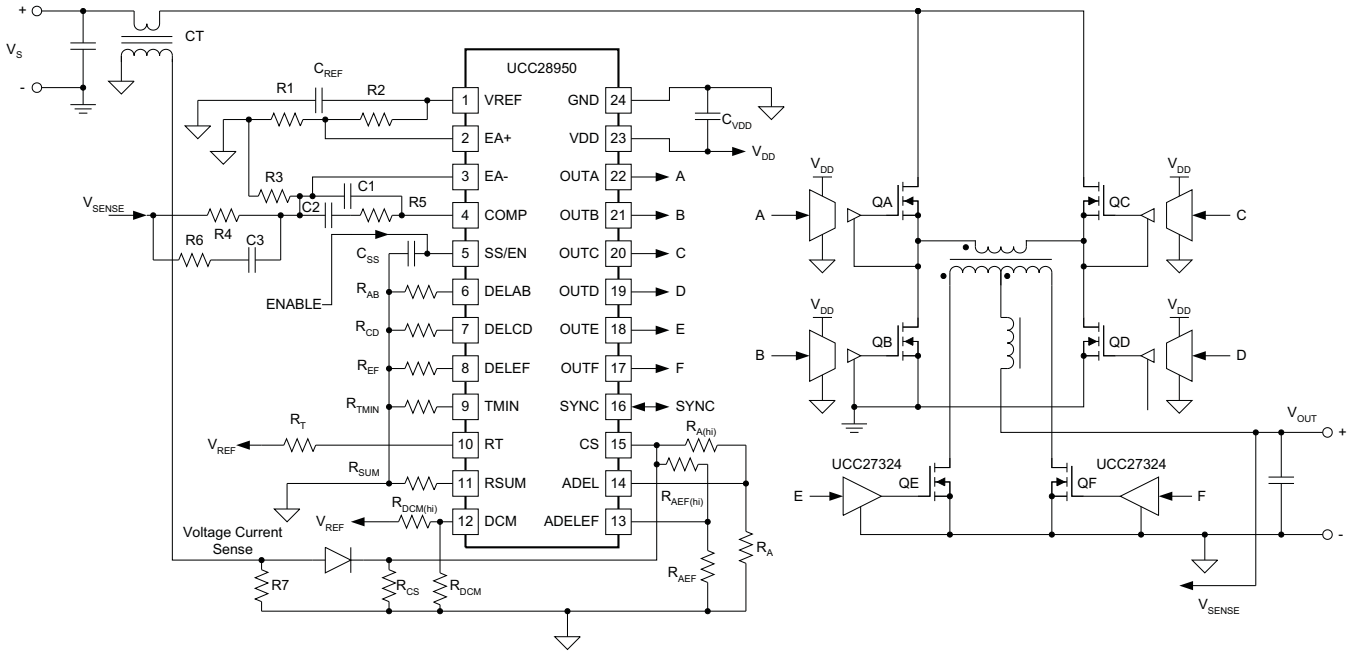
TERMINAL FUNCTIONS

TERMINAL		I/O	FUNCTION
NUMBER	NAME		
1	VREF	O	5-V, ±1.5%, 20-mA reference voltage output.
2	EA+	I	Error amplifier non-inverting input.
3	EA-	I	Error amplifier inverting input.
4	COMP	I/O	Error amplifier output and input to the PWM comparator.
5	SS/EN	I	Soft-start programming, device enable and hiccup mode protection circuit.
6	DELAB	I	Dead-time delay programming between OUTA and OUTB.
7	DELCD	I	Dead-time delay programming between OUTC and OUTD.
8	DELEF	I	Delay-time programming between OUTA to OUTF, and OUTB to OUTE.
9	TMIN	I	Minimum duty cycle programming in burst mode.
10	RT	I	Oscillator frequency set. Master or slave mode setting.
11	RSUM	I	Slope compensation programming. Voltage mode or peak current mode setting.
12	DCM	I	DCM threshold setting.
13	ADELEF	I	Delay-time programming between primary side and secondary side switches, T_{AFSET} and T_{BESET}.
14	ADEL	I	Dead-time programming for the primary switches over CS voltage range, T_{ABSET} and T_{CDSET}.
15	CS	I	Current sense for cycle-by-cycle over-current protection and adaptive delay functions.
16	SYNC	I/O	Synchronization out from Master controller to input of slave controller.
17	OUTF	O	0.2-A sink/source synchronous switching output.
18	OUTE	O	0.2-A sink/source synchronous switching output.
19	OUTD	O	0.2-A sink/source primary switching output.
20	OUTC	O	0.2-A sink/source primary switching output.
21	OUTB	O	0.2-A sink/source primary switching output.
22	OUTA	O	0.2-A sink/source primary switching output.
23	VDD	I	Bias supply input.
24	GND		Ground. All signals are referenced to this node.

Functional Block Diagram



Typical Application Diagram



Startup Timing Diagram

No output delay shown, COMP-to-RAMP offset not included.

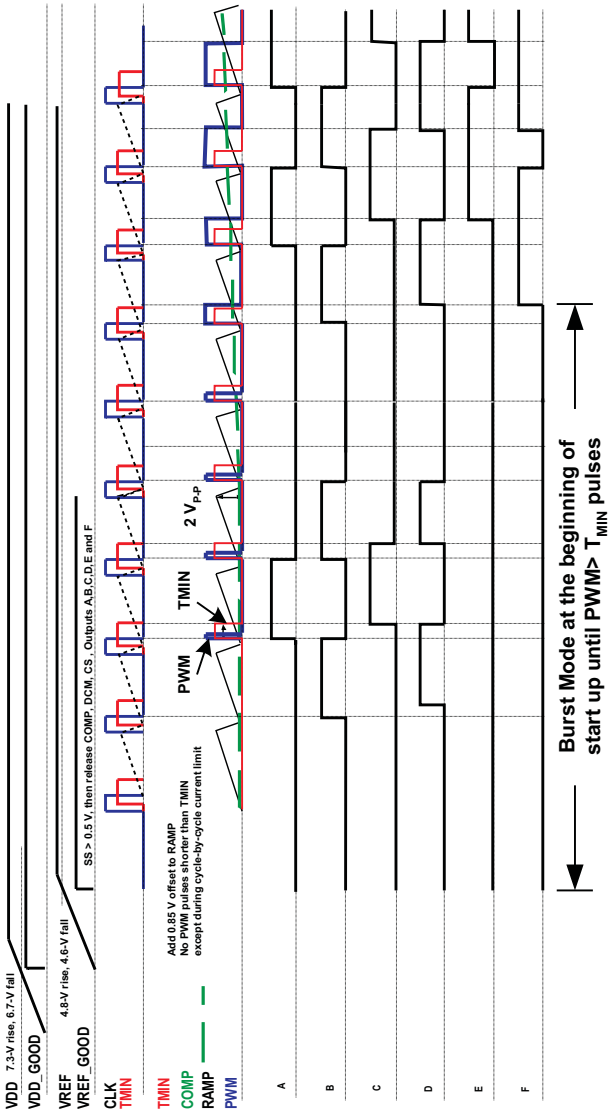


Figure 1. UCC28950 Timing Diagram

NOTE

There is no pulse on OUTE during burst mode at startup. Two falling edge PWM pulses are required before enabling the synchronous rectifier outputs.

Steady State/Shutdown Timing Diagram

No output delay shown, COMP-to-RAMP offset not included.

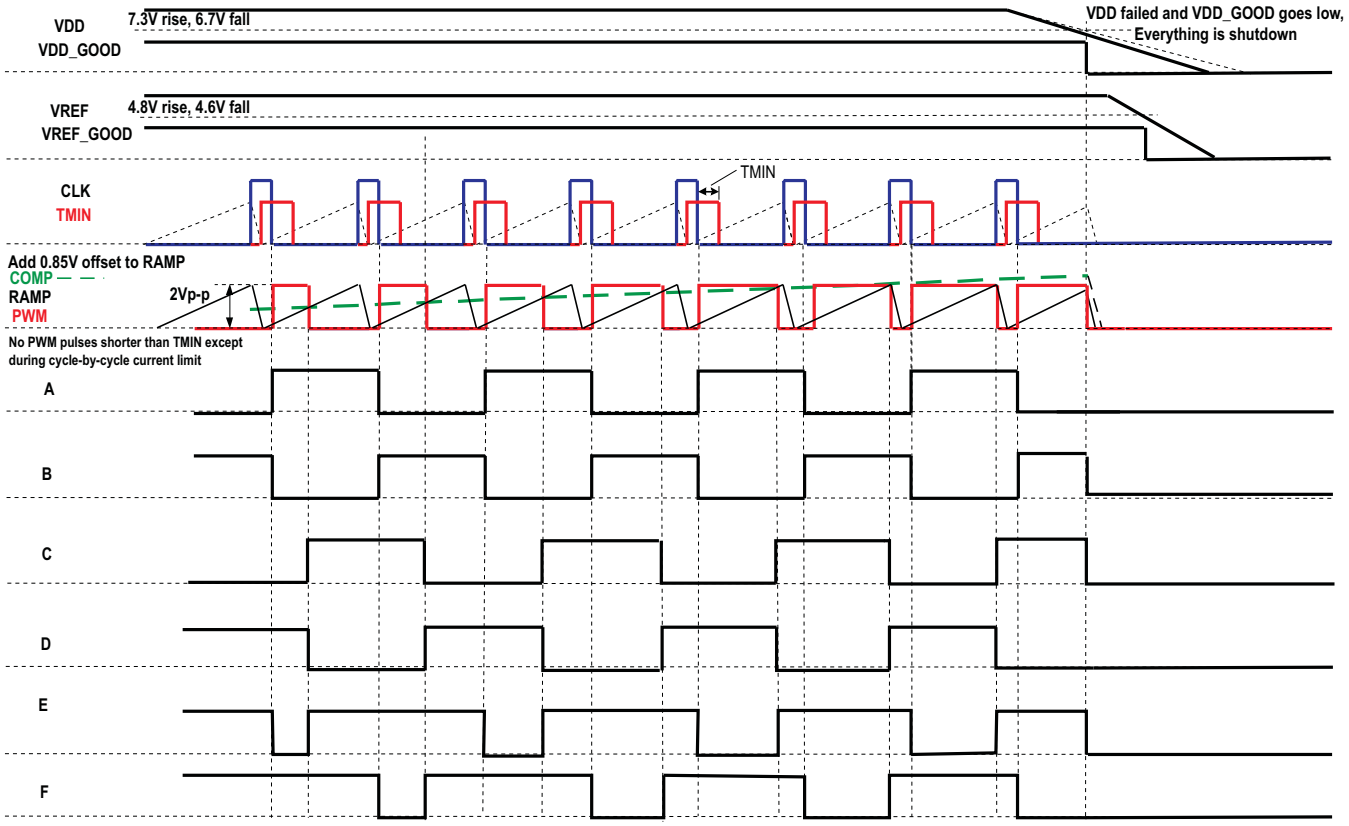


Figure 2. UCC28950 Timing Diagram

DETAILED PIN DESCRIPTION AND PARAMETER SETTINGS

Start-Up Protection Logic

Before the UCC28950 controller will start up, the following conditions must be met:

- VDD voltage exceeds rising UVLO threshold 7.3 V typical.
- The 5-V reference voltage is available.
- Junction temperature is below the thermal shutdown threshold of 140°C.
- The voltage on the soft-start capacitor is not below 0.55 V typical.

If all those conditions are met, an internal enable signal EN is generated that initiates the soft start process. The duty cycle during the soft start is defined by the voltage at the SS pin, and cannot be lower than the duty cycle set by TMIN, or by cycle-by-cycle current limit circuit depending on load conditions.

Voltage Reference (VREF)

The accurate (±1.5%) 5-V reference voltage regulator with the short circuit protection circuit supplies internal circuitry and provides up to 20-mA external output current for setting DC/DC converter parameters. Place low ESR and ESL, preferably ceramic decoupling capacitor C_{REF} in 1 µF to 2.2 µF range from this pin to GND as close to the related pins as possible for best performance. The only condition where the reference regulator is shut down internally is during under voltage lockout.

Error Amplifier (EA+, EA-, COMP)

The error amplifier has two uncommitted inputs, EA+ and EA-, with a 3-MHz unity bandwidth, which allows flexibility in closing the feedback loop. The EA+ is a non-inverting input, the EA- is an inverting input and the COMP is the output of the error amplifier. The input voltage common mode range, where the parameters of error amplifier are guaranteed, is from 0.5 V to 3.6 V. The output of the error amplifier is connected internally to the non-inverting input of the PWM comparator. The range of the error amplifier output of 0.25 V to 4.25 V far exceeds the PWM comparator input ramp-signal range, which is from 0.8 V to 2.8 V. The soft-start signal serves as an additional non-inverting input of the error amplifier. The lower of the two non-inverting inputs of the error amplifier is the dominant input and sets the duty cycle where the output signal of the error amplifier is compared with the internal ramp at the inputs of the PWM comparator.

Soft Start and Enable (SS/EN)

The soft-start pin SS/EN is a multi-function pin used for the following operations:

- Closed loop soft start with the gradual duty cycle increase from the minimum set by TMIN up to the steady state duty cycle required by the regulated output voltage.
- Setting hiccup mode conditions during cycle-by-cycle over current limit.
- On/off control for the converter.

During soft start, one of the voltages at the SS/EN or EA+ pins, whichever is lower (SS/EN - 0.55 V) or EA+ voltage (see Block Diagram), sets the reference voltage for a closed feedback loop. Both SS/EN and EA+ signals are non-inverting inputs of the error amplifier with the COMP pin being its output. Thus the soft start always goes under the closed feedback loop and the voltage at COMP pin sets the duty cycle. The duty cycle defined by COMP voltage can not be shorter than TMIN pulse set by the user. However, if the shortest duty cycle is set by the cycle-by-cycle current limit circuit, then it becomes dominant over the duty cycle defined by COMP voltage or by TMIN block.

The soft-start duration is defined by an external capacitor C_{SS}, connected between SS/EN pin and ground, and the internal charge current that has typical value of 25 µA. Pulling the soft-start pin externally below 0.55 V shuts down the controller. The release of the soft-start pin enables the controller to start, and if there is no current limit condition, the duty cycle applied to the output inductor gradually increases until it reaches the steady state duty cycle defined by the regulated output voltage of the converter. This happens when the voltage at the SS/EN pin reaches and then exceeds the voltage at EA+ pin defined as VNI by 0.55 V. Thus for the given soft-start time T_{SS}, the C_{SS} value can be defined by Equation 1 or Equation 2:

$$C_{SS(master)} = \frac{T_{SS} \times 25\,\mu A}{(VNI + 0.55)} \quad (1)$$

$$C_{SS(slave)} = \frac{T_{SS}}{825K \times Ln\left(\frac{20.6}{20.6 - VNI - 0.55}\right)} \quad (2)$$

For example, in Equation 1, if the soft-start time T_{SS} is selected to be 10 ms, and the VNI is 2.5 V, then the soft-start capacitor C_{SS} is equal to 82-nF.

NOTE

If the converter is configured in Slave Mode, make sure you place an 825-kΩ resistor from SS pin to ground.

Light-Load Power Saving Mode

The UCD28950 offers four different light-load management techniques for improving the efficiency of a power converter over a wide load current range.

1. Adaptive Delay,
   (a) ADEL, which sets and optimizes the dead-time control for the primary switches over wide load current range.
   (b) ADELEF, which sets and optimizes the delay-time control between the primary side switches and the secondary side switches.
2. TMIN, sets the minimum duty cycle as long as the part is not in current limit mode.
3. Dynamic synchronous rectifier on/off control in DCM Mode, For increased efficiency at light loads. The DCM Mode starts when the voltage at CS pin is lower than the threshold set by the user. In DCM Mode, the synchronous output drive signals OUTE and OUTF are brought down low.
4. Burst Mode, for maximum efficiency at very light loads or no load. Burst Mode has an even number of PWM TMIN pulses followed by off time. Transition to the Burst Mode is defined by the TMIN duration set by the user.

Adaptive Delay, (Delay between OUTA and OUTB, OUTC and OUTD (*DELAB, DELCD, ADEL*))

The resistor R_{AB} from the DELAB pin, DELAB to GND, along with the resistor divider R_{AHI} from CS pin to ADEL pin and R_A from ADEL pin to GND sets the delay T_{ABSET} between one of outputs OUTA or OUTB going low and another output going high Figure 3.

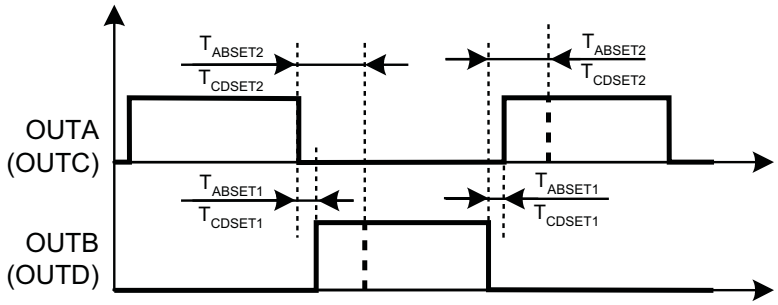


Figure 3. Delay definitions between OUTA and OUTB, OUTC and OUTD

This delay gradually increases as a function of the CS signal from T_{ABSET1}, which is measured at V_{CS} = 1.8 V, to T_{ABSET2}, which is measured at the V_{CS} = 0.2 V. This approach ensures there will be no shoot-through current during the high-side and low-side MOSFET switching and optimizes the delay for ZVS condition over a wide load current range. Depending on the resistor divider R_{AHI} and R_A, the proportional ratio between longest and shortest delay is set. The max ratio is achieved by tying the CS and ADEL pins together. If ADEL is connected to GND, then the delay is fixed, defined only by the resistor R_{AB} from DELAB to GND. The delay T_{CDSET1} and T_{CDSET2} settings and their behaviour for outputs OUTC and OUTD are very similar to the one described for OUTA and OUTB. The difference is that resistor R_{CD} connected between DELCD pin and GND sets the delay T_{CDSET}. Delays for outputs OUTC and OUTD share with the outputs OUTA and OUTB the same CS voltage dependence pin ADEL.

The delay time T_{ABSET} is defined by the following Equation 3.

$$T_{ABSET} = \left(\frac{5 \times R_{AB}}{0.15\,V + CS \times K_A \times 1.46} \right) ns + 5ns \quad (3)$$

The same equation is used to define the delay time T_{CDSET} in another leg except R_{AB} is replaced by R_{CD}.

$$T_{CDSET} = \left(\frac{5 \times R_{CD}}{0.15\,V + CS \times K_A \times 1.46} \right) ns + 5ns \quad (4)$$

In these equations R_{AB} and R_{CD} are in kΩ and CS, the voltage at pin CS, is in volts and K_A is a numerical coefficient in the range from 0 to 1. The delay time T_{ABSET} and T_{CDSET} are in ns. These equations are empirical and they are approximated from measured data. Thus, there is no unit agreement in the equations. As an example, assume R_{AB} = 15 kΩ, CS = 1 V and K_A = 0.5. Then the T_{ABSET} is going to be 90.25 ns. In both Equation 3 and Equation 4, K_A is the same and is defined as:

$$K_A = \frac{R_A}{R_A + R_{AHI}} \quad (5)$$

K_A sets how the delay is sensitive to CS voltage variation. If K_A = 0 (ADEL shorted to GND), the delay is fixed. If K_A = 1 (ADEL is tied to CS), the delay is maximum at CS = 0.2 V and gradually decreases when CS goes up to 1.8 V. The ratio between the maximum and minimum delay can be up to 6:1.

It is recommended to start by setting K_A = 0 and set T_{ABSET} and T_{CDSET} relatively large using equations or plots in the data sheet to avoid hard switching or even shoot through current. The delay between outputs A, B and C, D set by resistors R_{AB} and R_{CS} accordingly. Program the optimal delays at light load first. Then by changing K_A set the optimal delay for the outputs A, B at maximum current. K_A for outputs C, D is the same as for A,D. Usually outputs C, D always have ZVS if sufficient delay is provided.

NOTE

The allowed resistor range on DELAB and DELCD, R_{AB} and R_{CD} are 13 kΩ to 90 kΩ.

R_A and R_{AHI} define the portion of voltage at pin CS applied to the pin ADEL (See Typical Application Diagram). K_A defines how significantly the delay time depends on CS voltage. Ka varies from 0, where ADEL pin is shorted to ground (R_A = 0) and the delay does not depend on CS voltage, to 1, where ADEL is tied to CS (R_{AH} = 0). Setting K_A, R_{AB} and R_{CD} provides the ability to maintain optimal ZVS conditions of primary switches over load current because the voltage at CS pin includes reflected load current to primary side through the current sensing circuit. The plots in Figure 4 and Figure 5 show the delay time settings as a function of CS voltage and K_A for two different conditions: R_{AB} = R_{CD} = 13 kΩ (Figure 4) and R_{AB} = R_{CD} = 90 kΩ (Figure 5).

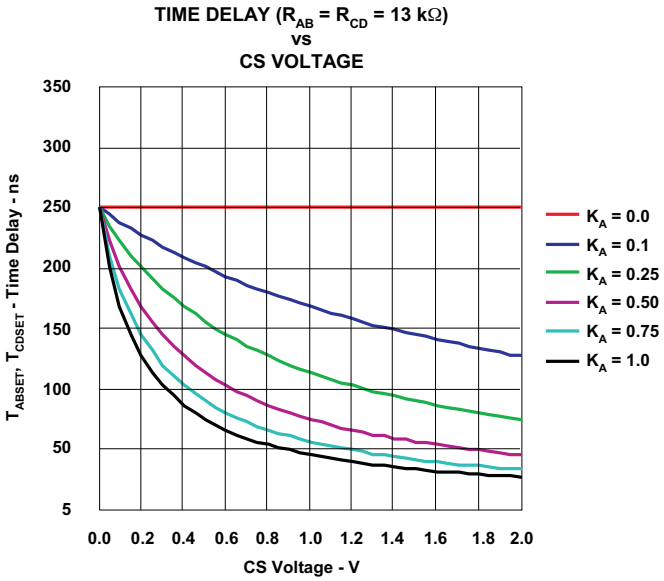


Figure 4. Delay Time Set T_{ABSET} and T_{CDSET} (Over CS voltage variation and selected K_A for R_{AB} and R_{CD} equal 13 kΩ)

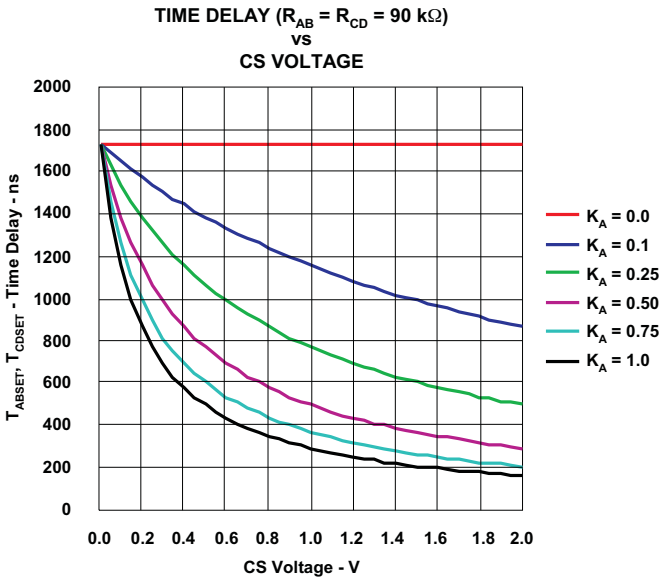


Figure 5. Delay time set T_{ABSET} and T_{CDSET} (Over CS voltage variation and selected K_A for R_{AB} and R_{CD} equal 90 kΩ)

Adaptive Delay (Delay between OUTA and OUTF, OUTB and OUTE (*DELEF, ADELEF*))

The resistor R_{EF} from the DELEF pin to GND along with the resistor divider R_{AEFHI} from CS pin to ADELEF pin and R_{AEF} from ADELEF pin to GND sets equal delays T_{AFSET} and T_{BESET} between outputs OUTA or OUTB going low and related output OUTF or OUTE going low Figure 6.

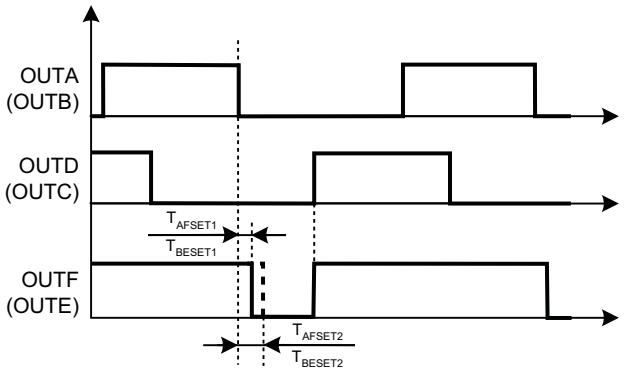


Figure 6. Delay Definitions Between OUTA and OUTF, OUTB and OUTE

These delays gradually increase as function of CS signal from T_{AFSET1}, which is measured at V_{CS} = 0.2 V, to T_{AFSET2}, which is measured at V_{CS} = 1.8 V. Opposite to the DELAB and DELCD behaviour, this delay is longest (T_{AFSET2}) when the signal at CS pin is maximized and shortest (T_{AFSET1}) when the CS signal is minimized. This approach will reduce the synchronous rectifier MOSFET body diode conduction time over a wide load current range thus improving efficiency and reducing diode recovery time. Depending on the resistor divider R_{AEFHI} and R_{AEF}, the proportional ratio between longest and shortest delay is set. If CS and ADELEF are tied, the ratio is maximized. If ADELEF is connected to GND, then the delay is fixed, defined only by resistor R_{EF} from DELEF to GND.

The delay time T_{AFSET} is defined by the following Equation 6. The same defines the delay time T_{BESET}.

$$T_{AFSET} = \left(\left(\frac{5 \times R_{EF}}{2.65\,V - CS \times K_{EF} \times 1.32} \right) ns + 4\,ns \right) \tag{6}$$

In this equation R_{EF} is in kΩ, the CS, which is the voltage at pin CS, is in volts and K_{EF} is a numerical gain factor of CS voltage from 0 to 1. The delay time T_{AFSET} is in ns. This equation is empirical approximation of measured data, thus, there is no unit agreement in it. As an example of calculation, assume R_{EF} = 15 kΩ, CS = 1 V and K_{EF} = 0.5. Then the T_{AFSET} is going to be 41.7 ns. K_{EF} is defined as:

$$K_{EF} = \frac{R_{AEF}}{R_{AEF} + R_{AEF(hi)}} \tag{7}$$

R_{AEF} and R_{AEFHI} define the portion of voltage at pin CS applied to the pin ADELEF (See Typical Application Diagram). K_{EF} defines how significantly the delay time depends on CS voltage. K_{EF} varies from 0, where ADELEF pin is shorted to ground (R_{AEF} = 0) and the delay does not depend on CS voltage, to 1, where ADELEF is tied to CS (R_{AEFHI} = 0).

NOTE

The allowed resistor range on DELEF, R_{EF} is 13 kΩ to 90 kΩ.

The plots in Figure 7 and Figure 8 show delay time settings as function of CS voltage and K_{EF} for two different conditions: R_{EF} = 13 kΩ (Figure 7) and R_{EF} = 90 kΩ (Figure 8)

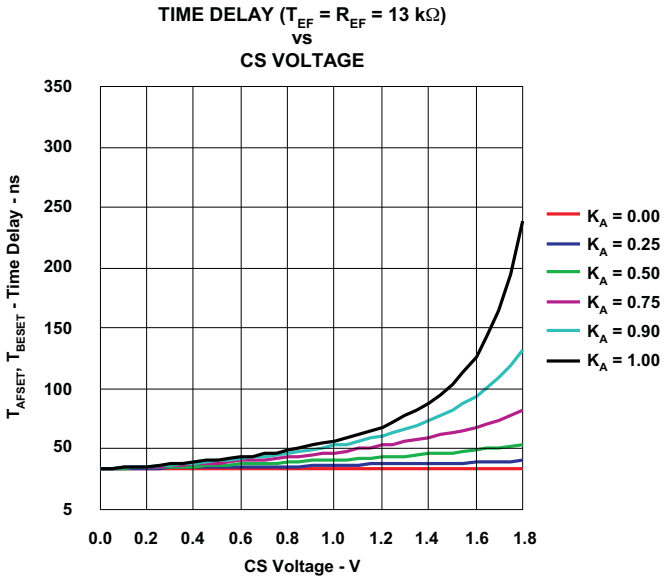


Figure 7. Delay Time T_{AFSET} and TBESET (Over CS voltage and selected K_{EF} for R_{EF} equal 13 kΩ)

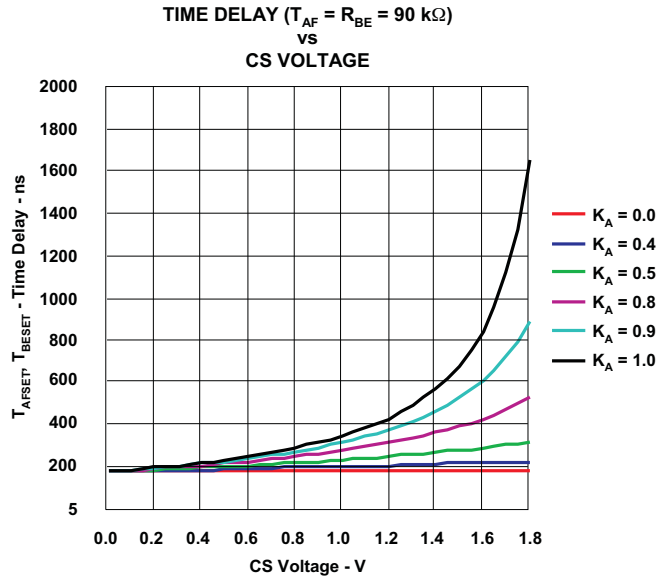


Figure 8. Delay Time T_{AFSET} and T_{BESET} (Over CS voltage and selected K_{EF} for R_{EF} equal 90 kΩ)

Minimum Pulse (TMIN)

The resistor R_{TMIN} from TMIN pin to GND sets fixed minimum pulse TMIN applied to the output rectifier enabling ZVS of the primary switches at light load. If the output PWM pulse demanded by the feedback loop is shorter than TMIN, then controller proceeds to the burst mode of operation where even number of TMIN pulses are followed by the off time dictated by the feedback loop. The proper selection of TMIN duration is dictated by the time it takes to raise the sufficient magnetizing current in the power transformer to maintain ZVS. The minimum pulse TMIN is defined by the following Equation 8.

$$TMIN = \left(5.92 \times R_{TMIN}\right) ns \quad (8)$$

In this equation R_{TMIN} is in kΩ and TMIN is in ns.

NOTE

The minimum allowed resistor on TMIN, R_{TMIN} is 13 kΩ.

The related plot is shown in Figure 9

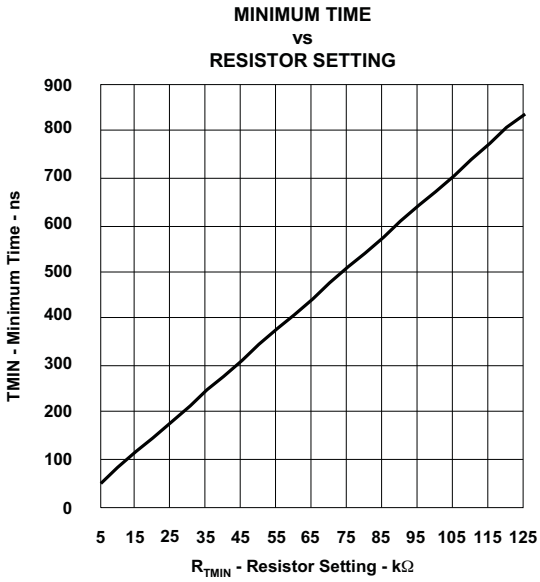


Figure 9. Minimum Time TMIN Over Setting Resistor R_{TMIN}

The value of minimum duty cycle DMIN is determined by Equation 9.

$$DMIN = \left(TMIN \times F_{SW(osc)} \times 10^{-4}\right)\% \quad (9)$$

Here, $F_{SW(osc)}$ is oscillator frequency in kHz, TMIN is the minimum pulse in ns and DMIN is in percents.

Burst Mode

If the converter is commanding a duty cycle lower than TMIN, then the controller will go into Burst Mode. The controller will always deliver even number of Power cycles to Power transformer. The controller always stops its bursts with OUTB and OUTC power delivery cycle. If the controller is still demanding a duty cycle less than TMIN, then the controller goes into shut down mode. Then it waits until the converter is demanding a duty cycle equal or higher than TMIN before the controller puts out TMIN or a PWM duty cycle as dictated by COMP voltage pin.

Switching Frequency Setting (RT)

Connecting an external resistor RT between the RT pin and VREF pins sets the fixed frequency operation and configures the controller as a master providing synchronization output pulses at SYNC pin with 0.5 duty cycle and frequency equal to the internal oscillator. To set the converter in Slave Mode, connect the external resistor RT between RT-pin to GND and place an 825-kΩ resistor form SS pin to GND in parallel to the SS_EN capacitor. This configures the controller as a slave. The slave controller operates with 90° phase shift relatively to the master converter if their SYNC pins are tied together. The switching frequency of the converter is equal to the frequency of output pulses. The following Equation 10 defines the nominal switching frequency of the converter configured as a master (resistor RT between RT-pin and VREF). On the UCC28950 there is an internal clock oscillator frequency which is twice as that of the controller outputs frequency.

$$F_{SW(nom)} = \left(\frac{2.5 \times 10^3}{\left(\frac{RT}{V_{REF} - 2.5\,V} + 1 \times \frac{k\Omega}{V} \right)} \right) kHz \tag{10}$$

In this equation the RT is in kΩ, VREF is in volts and $F_{SW(nom)}$ is in kHz. This is also empirical approximation and thus, there is no unit agreement. Assume for example, VREF = 5 V, RT = 65 kΩ. Then the switching frequency $F_{SW(nom)}$ is going to be 92.6 kHz.

The Equation 11 defines the nominal switching frequency of converter if the converter configured as a slave and the resistor RT is connected between RT pin and GND.

$$F_{SW(nom)} = \left(\frac{2.5 \times 10^3}{\left(\frac{RT}{2.5\,V} + 1 \times \frac{k\Omega}{V} \right)} \right) kHz \tag{11}$$

In this equation the RT is in kΩ, and $F_{SW(nom)}$ is in kHz. Notice that for VREF = 5 V, Equation 10 and Equation 11 yield the same results.

The plot in Figure 10 shows how $F_{SW(nom)}$ depends on the resistor RT value when the VREF = 5 V. As it is seen from Equation 10 and Equation 11, the switching frequency $F_{SW(nom)}$ is set to the same value for either master, of slave configuration provided the same resistor value RT is used.

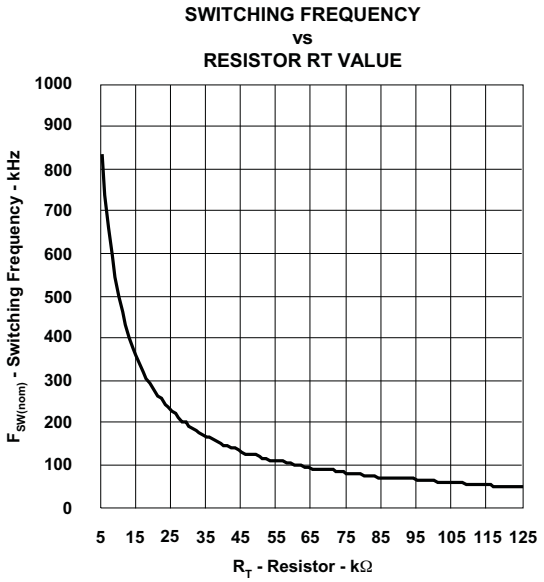


Figure 10. Converter Switching Frequency $F_{SW(nom)}$ Over Resistor RT Value

Slope Compensation (RSUM)

Slope compensation is the technique that adds additional ramp signal to the CS signal and applied to the:

- Input of PWM comparator in case of peak current mode control.
- Input of cycle-by-cycle current limit comparator.

This prevents sub-harmonic oscillation at D > 50% (some publications suggest it might happen even at D < 50%). At low duty cycle and light load, the slope compensation ramp reduces noise sensitivity of Peak Current Mode control.

Too much additional slope compensation ramp reduces benefits of PCM control. In case of cycle-by-cycle current limit, the average current limit becomes lower and this might reduce the start up capability with the large output capacitance. The optimal compensation slope varies depending on duty cycle, L_O and L_M.

The slope compensation is needed for the controller operating at peak current mode control or during the cycle-by-cycle current limit at duty cycle above 50%. Placing a resistor from RSUM pin to ground allows the controller to operate in peak current control mode. Connecting RSUM pin through resistor to VREF switches controller to the voltage mode control with the internal PWM ramp. However, the resistor value still provides CS signal compensation for cycle-by-cycle current limit. In other words, in VMC, the slope compensation is applied only to cycle-by-cycle comparator. While in PCM, the slope compensation applied to both PWM and cycle-by-cycle current limit comparators.

The operation logic of slope compensation circuit is shown in Figure 11.

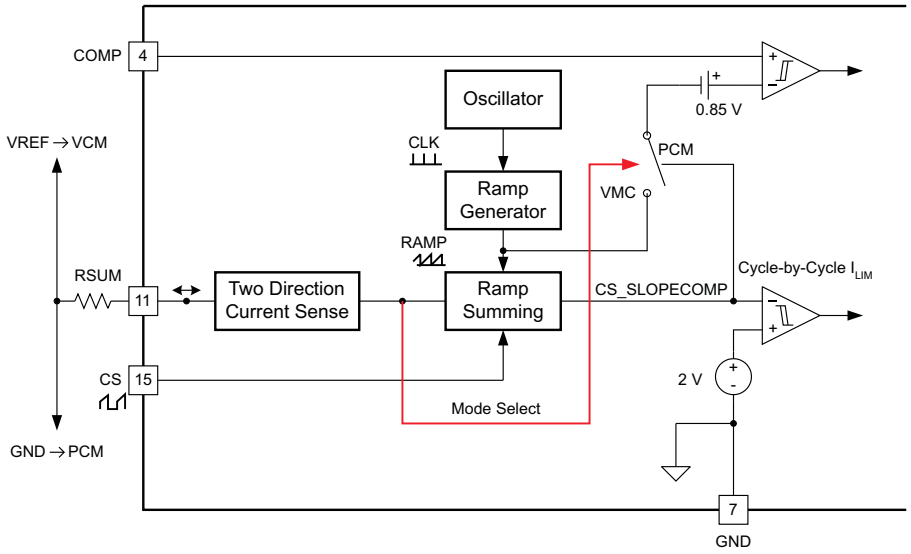


Figure 11. The Operation Logic of Slope Compensation Circuit

The slope of the additional ramp, me, added to CS signal by placing a resistor from RSUM pin to the ground is defined by the following Equation 12.

$$me = \left(\frac{2.5}{0.5 \times R_{SUM}} \right) \frac{V}{\mu s} \quad (12)$$

If the resistor from RSUM pin is connected to VREF pin, then the controller operates in voltage mode control, still having the slope compensation added to CS signal used for cycle-by-cycle current limit. In such a case the slope is defined by the following Equation 13.

$$me = \left(\frac{(V_{REF} - 2.5\,V)}{0.5 \times R_{SUM}} \right) \frac{V}{\mu s} \tag{13}$$

In Equation 12 and Equation 13, the VREF is in volts, RSUM is in kΩ, and me is in V/µs. These are empirical equations without unit agreement. As an example, substituting VREF = 5 V and RSUM = 40 kΩ, yields the result 0.125 V/µs. The related plot of me as function of RSUM is shown in Figure 12. Because VREF = 5 V, the plots generated from Equation 12 and Equation 13 coincide.

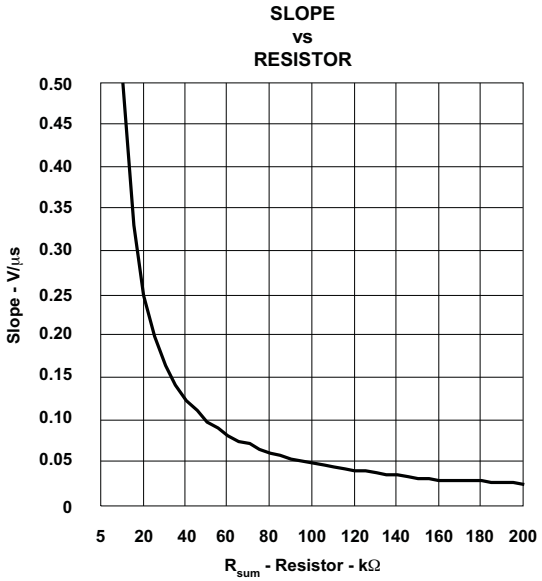


Figure 12. Slope of the Added Ramp Over Resistor RSUM

NOTE

The recommended resistor range for R_{SUM} is 10 kΩ to 1 MΩ.

Dynamic SR ON/OFF Control (DCM Mode)

The voltage at the DCM pin provided by the resistor divider Rdcmhi between VREF pin and DCM, and Rdcm from DCM pin to GND, sets the percentage of 2-V current limit threshold for the Current Sense pin, (CS). If the CS pin voltage falls below the DCM pin threshold voltage, then the controller initiates the light load power saving mode, and shuts down the synchronous rectifiers, OUTE and OUTF. If the CS pin voltage is higher than the DCM pin threshold voltage, then the controller runs in CCM mode. Connecting the DCM pin to VREF makes the controller run in DCM mode and shuts both Outputs OUTE and OUTF. Shorting the DCM pin to GND disables the DCM feature and the controller runs in CCM mode under all conditions.

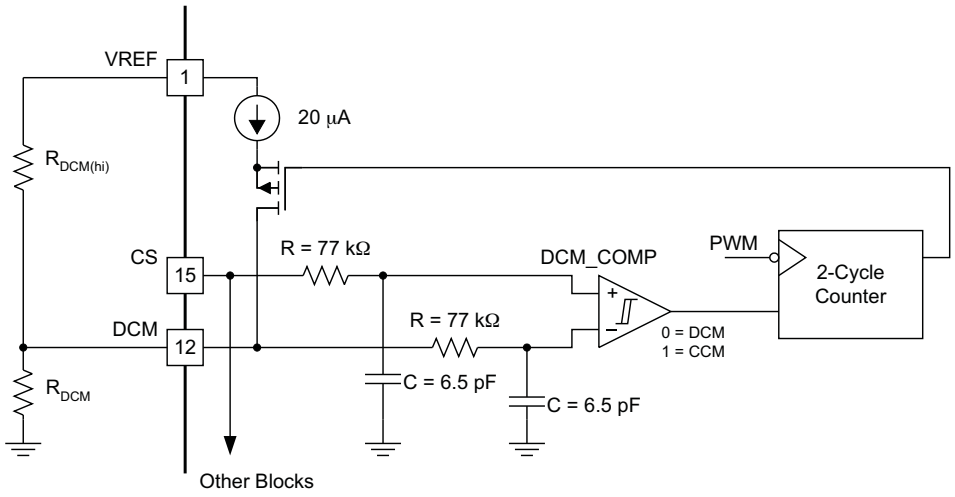


Figure 13. DCM Functional Block

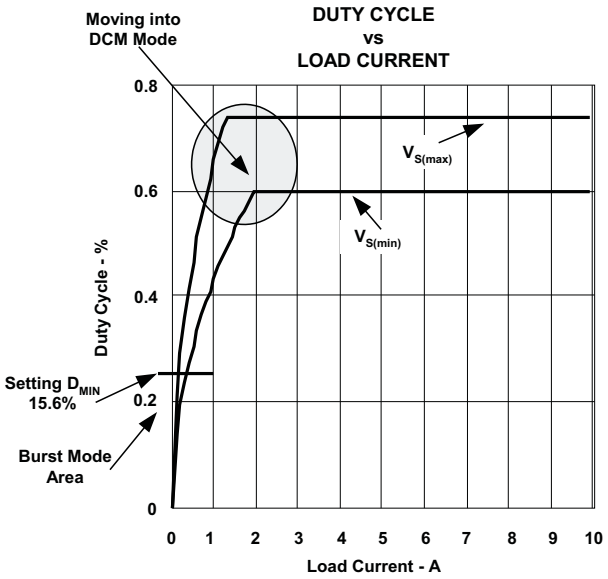


Figure 14. Duty Cycle Change Over Load Current Change

There is a nominal 20-µA switched current source used to create hysteresis. The current source is active only when the system is in DCM Mode. Otherwise, it is inactive and does not affect the node voltage. Therefore, when being in DCM region, the DCM threshold is the voltage divider plus ΔV explained in Equation 14 below. When being in CCM region, the threshold is the voltage set by the resistor divider. When CS pin reaches the threshold set on the DCM pin, the system waits to see two consecutive falling edge PWM cycles before switching from CCM to DCM and vice-versa. The magnitude of the hysteresis is a function of the external resistor divider impedance. The hysteresis can be calculated using the following Equation 14:

$$\Delta V = 2 \times 10^{-5} \frac{R_{DCMHI} \times R_{DCM}}{R_{DCMHI} + R_{DCM}} \quad (14)$$

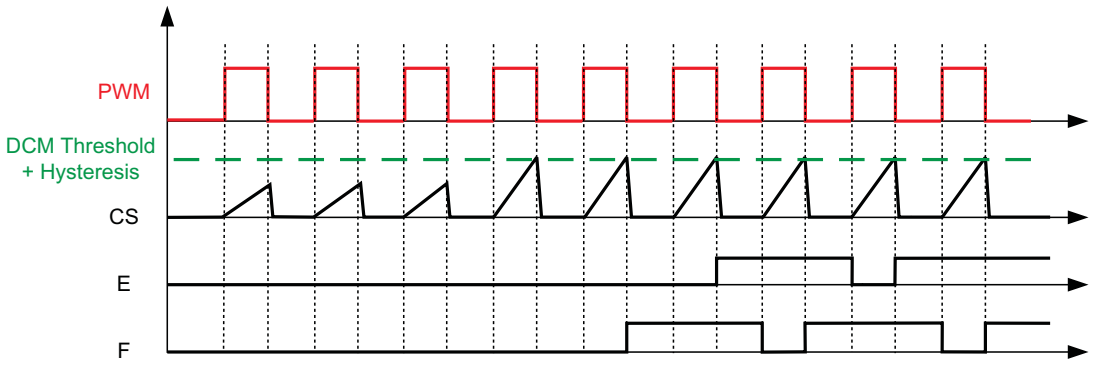


Figure 15. Moving from DCM to CCM Mode

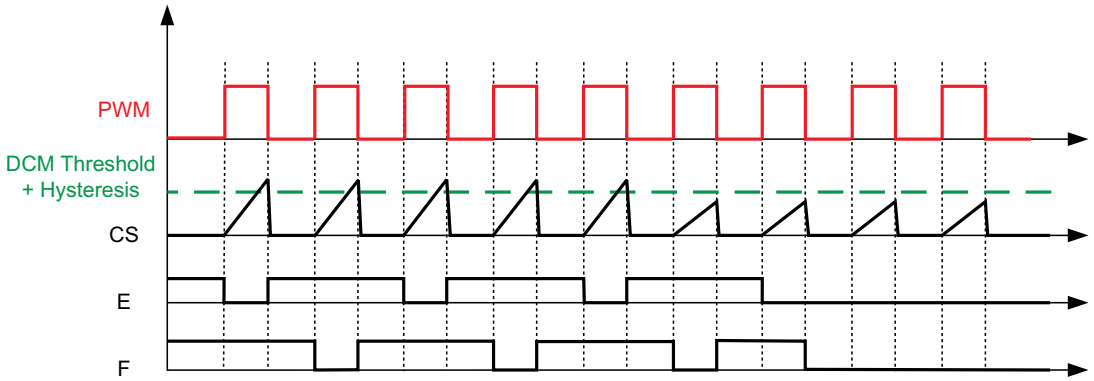


Figure 16. Moving from CCM to DCM Mode

DCM must be used in order to prevent reverse current in the output inductor which could cause the synchronous FETS to fail.

Current Sensing (CS)

The signal from current sense pin is used for cycle-by-cycle current limit, peak-current mode control, light-load efficiency management and setting the delay time for outputs OUTA, OUTB, OUTC, OUTD and delay time for outputs OUTE, OUTF. Connect the current sense resistor R_{CS} between CS and GND. Depending on layout, to prevent a potential electrical noise interference, it is recommended to put a small R-C filter between R_{CS} resistor and CS pin.

Cycle-by-Cycle Current Limit Current Protection and Hiccup Mode

The cycle-by-cycle current limit provides peak current limiting on the primary side of the converter when the load current exceeds its predetermined threshold. For peak current mode control, certain leading edge blanking time is needed to prevent the controller from false tripping due to switching noise. In order to save external RC filter for the blanking time, an internal 30-ns filter at CS input is provided. The total propagation delay TCS from CS pin to outputs is 100 ns. An external RC filter is still needed if the power stage requires more blanking time. The 2.0-V ±3% cycle-by-cycle current limit threshold is optimized for efficient current transformer based sensing. The duration when a converter operates at cycle-by-cycle current limit depends on the value of soft-start capacitor and how severe the over current condition is. This is achieved by the internal discharge current I_{DS} Equation 15 and Equation 16 at SS pin.

$$I_{DS(master)} = \left(-25 \times (1-D) + 5\right)\mu A \quad (15)$$

$$I_{DS(slave)} = \left(-25 \times (1-D)\right)\mu A \quad (16)$$

The soft-start capacitor value also determines the so called hiccup mode off-time duration. The behavior of the converter during different modes of operation, along with related soft start capacitor charge/discharge currents are shown in Figure 17.

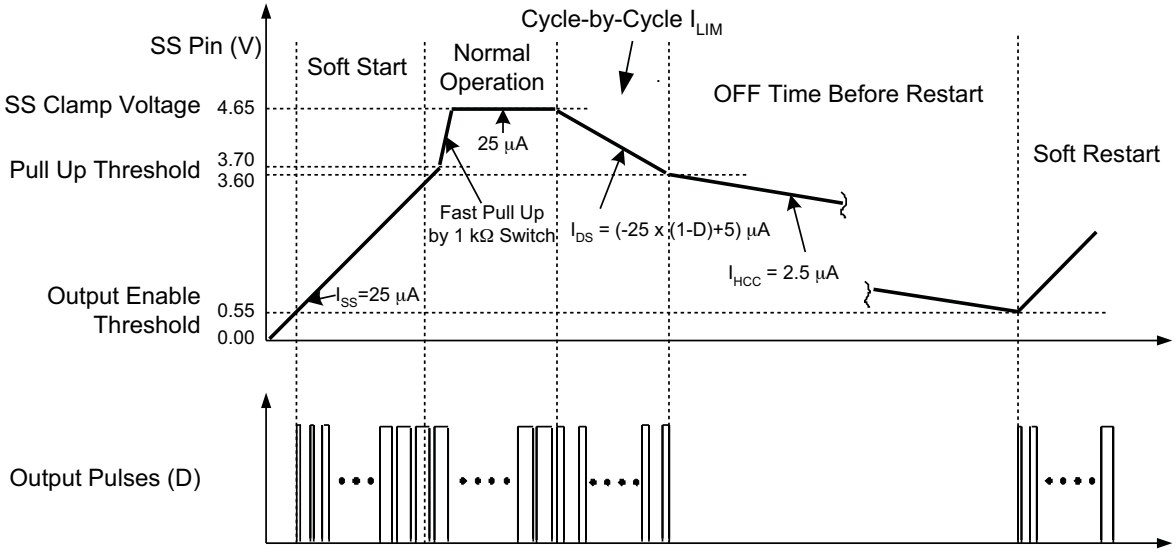


Figure 17. Timing Diagram of Soft-Start Voltage V_{SS}

The largest discharge current of 20 µA is when the duty cycle is close to zero. This current sets the shortest operation time during the cycle-by-cycle current limit which is defined as:

$$T_{CL(on\_master)} = \frac{C_{SS} \times (4.65\,V - 3.7\,V)}{20\,\mu A} \quad (17)$$

$$T_{CL(on\_slave)} = \frac{C_{SS} \times (4.65\,V - 3.7\,V)}{25\,\mu A} \quad (18)$$

Thus, if the soft-start capacitor C_{SS} = 100 nF is selected, then the $T_{CL(on)}$ time will be 5 ms.

To calculate the hiccup off time $T_{CL(off)}$ before the restart, the following Equation 19 or Equation 20 needs to be used:

$$T_{CL(off\_master)} = \frac{C_{SS} \times (3.6\,V - 0.55\,V)}{2.5\,\mu A} \quad (19)$$

$$T_{CL(off\_slave)} = \frac{C_{SS} \times (3.6\,V - 0.55\,V)}{4.9\,\mu A} \quad (20)$$

With the same soft start capacitor value 100 nF, the off time before the restart is going to be 122 ms. Notice, that if the over current condition happens before the soft start capacitor voltage reaches the 3.7-V threshold during start up, the controller limits the current but the soft start capacitor continues to be charged. As soon as the 3.7-V threshold is reached, the soft-start voltage is quickly pulled up to the 4.65-V threshold by an internal 1-kΩ $R_{DS(on)}$ switch and the cycle-by-cycle current limit duration timing starts by discharging the soft start capacitor. Depending on specific design requirements, the user can override default parameters by applying external charge or discharge currents to the soft start capacitor. The whole cycle-by-cycle current limit and hiccup operation is shown in Figure 17. In this example the cycle-by-cycle current limit lasts about 5 ms followed by 122 ms of off time.

Similar to the over current condition, the hiccup mode with the restart can be overridden by the user if a pull up resistor is connected between the SS and VREF pins. If the pull up current provided by the resistor exceeds 2.5 µA, then the controller remains in the latch off mode. In this case, an external soft-start capacitor value should be calculated with the additional pull-up current taken into account. The latch off mode can be reset externally if the soft-start capacitor is forcibly discharged below 0.55 V or the V_{DD} voltage is lowered below the UVLO threshold.

Synchronization (SYNC)

The UCC28950 allows flexible configuration of converters operating in synchronized mode by connecting all SYNC pins together and by configuration of the controllers as master and/or slaves. The controller configured as Master (resistor between RT and VREF) provides synchronization pulses at the SYNC pin with the frequency equal to 2X the converter frequency $F_{SW(nom)}$ and 0.5 duty cycle. The controller configured as a Slave (resistor between RT and GND and 825-kΩ resistor between SS_EN pin to GND) does not generate the synchronization pulses. The Slave controller synchronizes its own clock to the falling edge of synchronization signal thus operating 90° phase shifted versus the master converter's frequency $F_{SW(nom)}$. Because the Slave is synchronized to the falling edge of the SYNC pulses, the slave operates at 180° delayed versus Master's CLK or 90° delayed versus output switching pulses of Master.

Such operation between Master and Slave provides maximum input capacitor and output capacitor ripple cancellation effect if inputs and outputs of converters are tied together. To avoid system issues during the synchronized operation of few converters the following conditions should be taken care of.

- If any converter is configured a as a Slave, the SYNC frequency must be greater than or equal to 1.8 times the converter frequency.
- Slave converter does not start until at least one synchronization pulse has been received.
- If any or all converters are configured as Slaves, then each converter operates at its own frequency without synchronization after receiving at least one synchronization pulse. Thus, If there is an interruption of synchronization pulses at the slave converter, then the controller uses its own internal clock pulses to maintain operation based on the RT value that is connected to GND in the Slave converter.
- In Master mode, SYNC pulses start after SS pin passes its Enable threshold which is 0.55 V.
- Slave starts generating SS/EN voltage even though synchronization pulses have not been received.
- It is recommended that the SS on the Master controller starts before the SS on the Slave controller; therefore SS/EN pin on master converter must reach its Enable threshold voltage before SS/EN on the slave converter starts for proper operation. On the same note, it's recommended that T_{MIN} resistors on both Master and Slave are set at the same value.

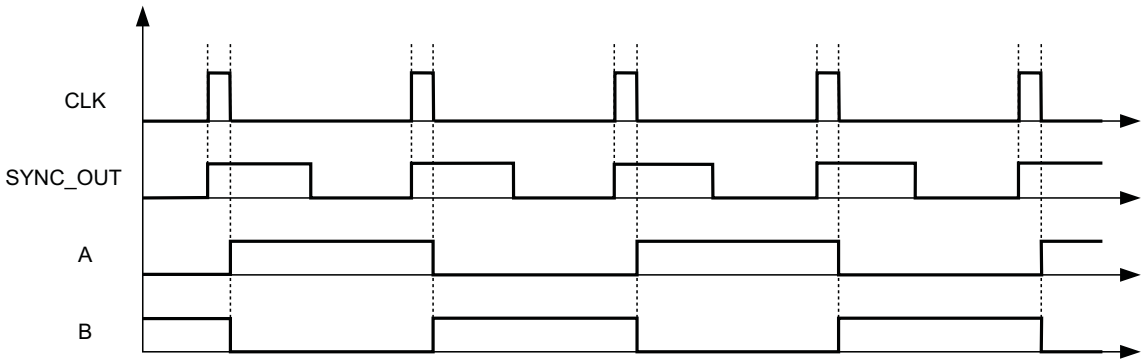


Figure 18. SYNC_OUT (Master Mode) Timing Diagram

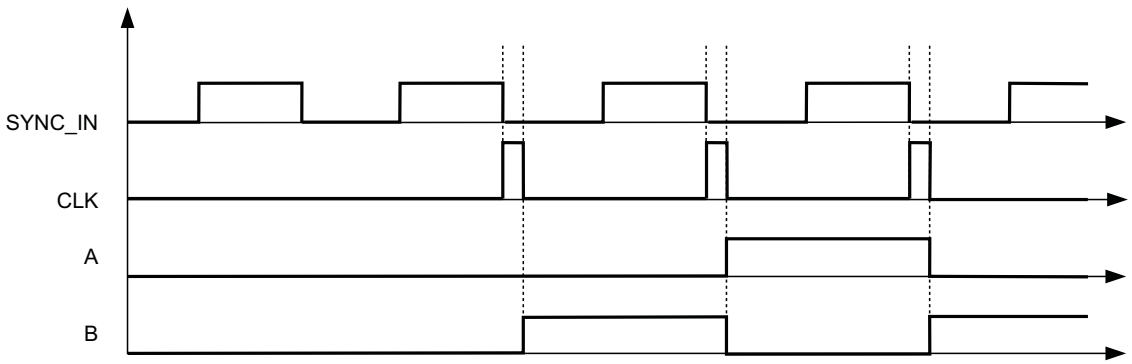


Figure 19. SYNC_IN (Slave Mode) Timing Diagram

Outputs (OUTA, OUTB, OUTC, OUTD, OUTE, OUTF)

- All MOSFET control outputs have 0.2-A drive capability.
- The control outputs are configured as P-MOS and N-MOS totem poles with typical $R_{DS(on)}$ 20 Ω and 10 Ω accordingly.
- The control outputs are capable of charging 100-pF capacitor within 12 ns and discharge within 8 ns.
- The amplitude of output control pulses is equal to V_{DD}.
- Control outputs are designed to be used with external gate MOSFET/IGBT drivers.
- The design is optimized to prevent the latch up of outputs and verified by extensive tests.

The UCC28950 has outputs OUTA, OUTB driving the active leg, initiating the duty cycle leg of power MOSFETs in phase-shifted full bridge power stage, and outputs OUTC, OUTD driving the passive leg, completing the duty cycle leg, as it is shown in typical timing diagram in Figure 47. Outputs OUTE and OUTF are optimized to drive the synchronous rectifier MOSFETs (Figure 20). These outputs have 200-mA peak-current capabilities and are designed to drive relatively small capacitive loads like inputs of external MOSFET or IGBT drivers. Recommended load capacitance should not exceed 100 pF. The amplitude of output signal is equal to V_{DD} voltage.

The capacitors C_{OSS} shown in Figure 20 are internal MOSFET capacitances that must be taken into account during design procedure to estimate zero voltage condition and switching losses.

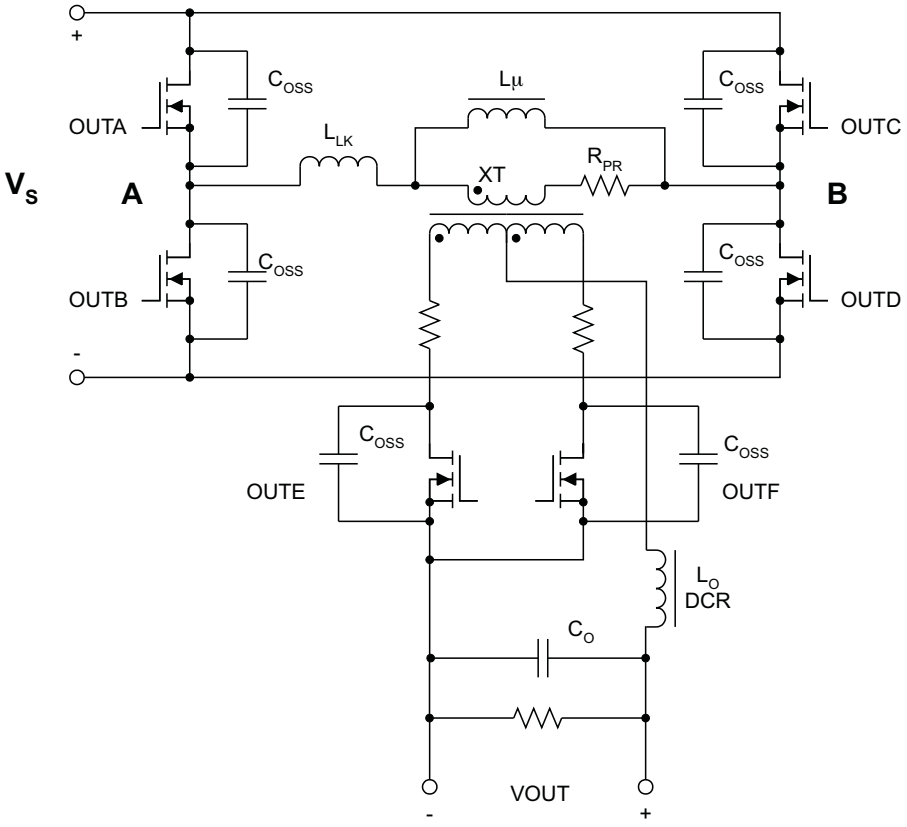


Figure 20. Power Stage

Supply Voltage (VDD)

Connect this pin to bias supply from 8 V to 17 V range. Place high quality, low ESR and ESL, at least 1-µF ceramic bypass capacitor C_{VDD} from this pin to GND. It is recommended to use 10-Ω resistor in series to VDD pin to form RC filter with C_{VDD} capacitor.

Ground (GND)

All signals are referenced to this node. It is recommended to have a separate quite analog plane connected in one place to the power plane. The analog plane combines the components related to the pins VREF, EA+, EA-, COMP, SS/EN, DELAB, DELCD, DELEF, TMIN, RT, RSUM. The power plane combines the components related to the pins DCM, ADELEF, ADEL, CS, SYNC, OUTF, OUTE, OUTD, OUTC, OUTB, OUTA, and VDD. An example of layout and ground planes connection is shown in Figure 21.

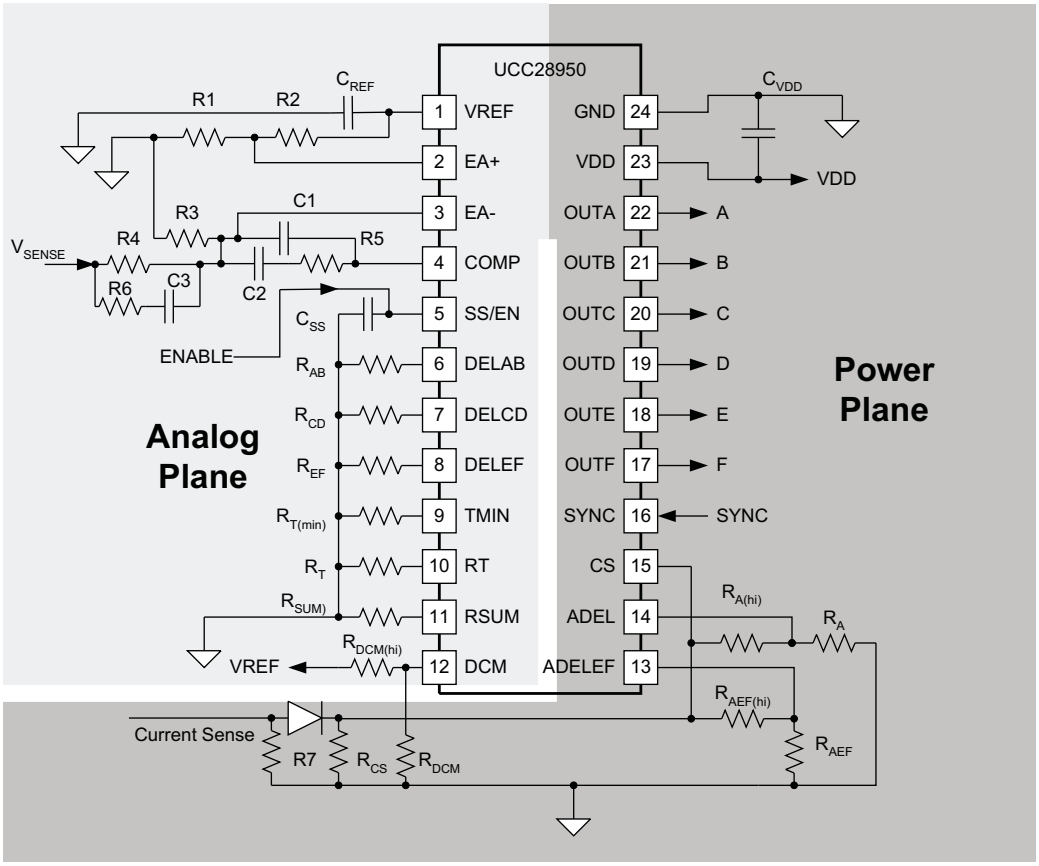


Figure 21. Layout Recommendation for Analog and Power Planes

TYPICAL CHARACTERISTICS

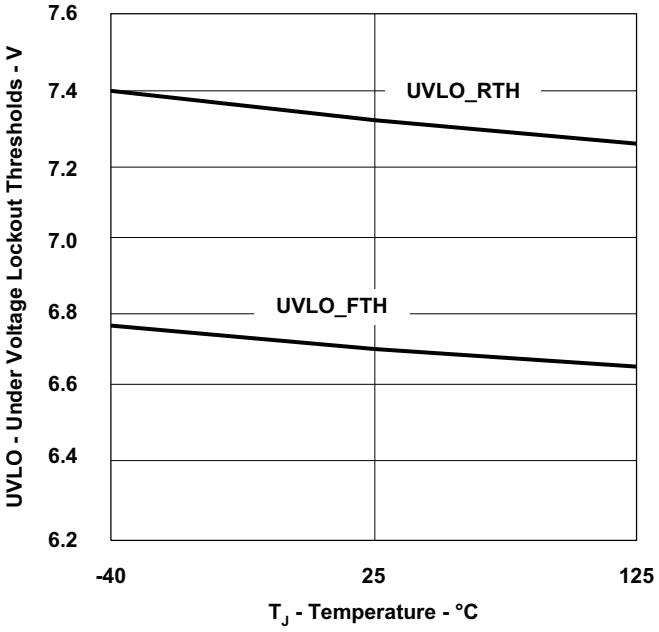


Figure 22.

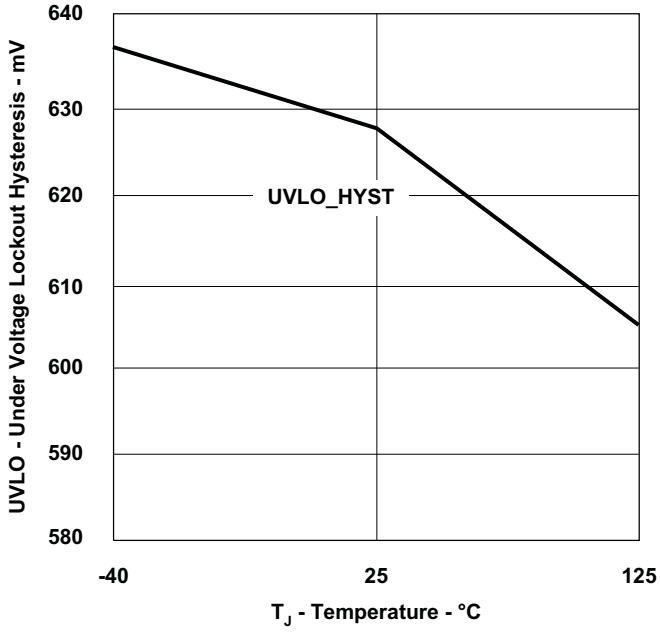


Figure 23.

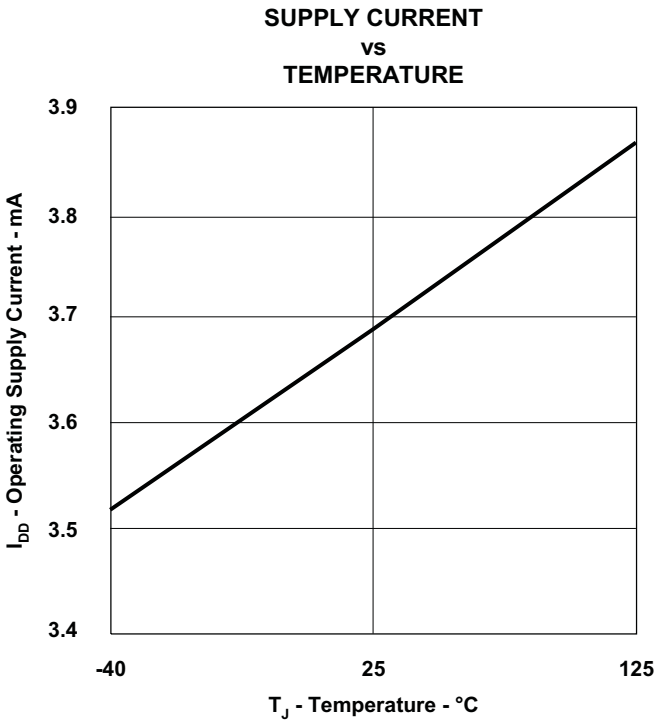


Figure 24.

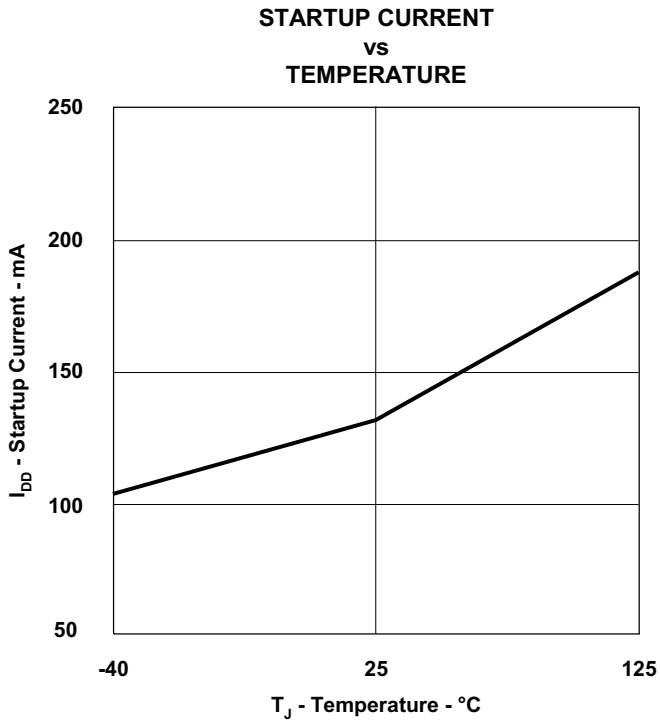


Figure 25.

TYPICAL CHARACTERISTICS (continued)

VOLTAGE REFERENCE (VDD = 12 V) vs TEMPERATURE

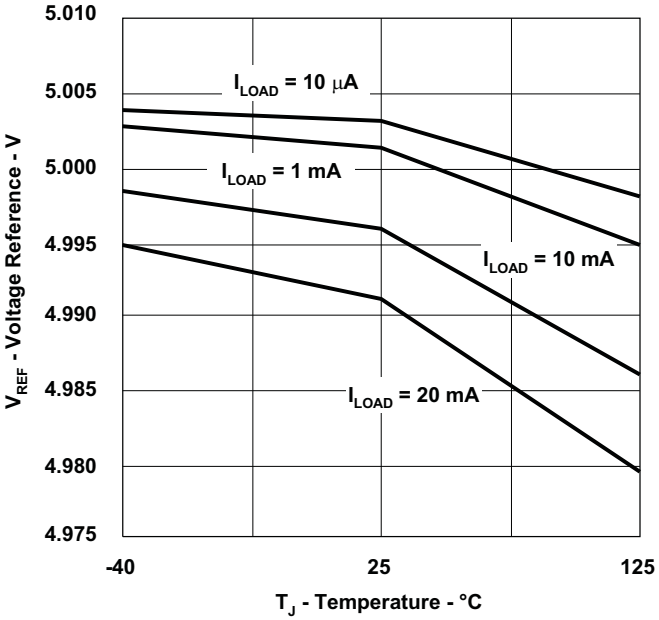


Figure 26.

LINE VOLTAGE REGULATION (I_{LOAD} = 10 mA) vs TEMPERATURE

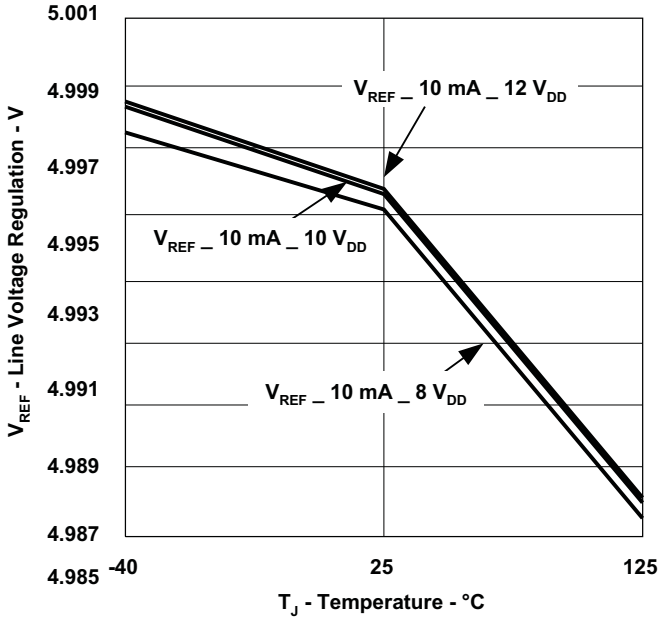


Figure 27.

SHORT CIRCUIT CURRENT vs TEMPERATURE

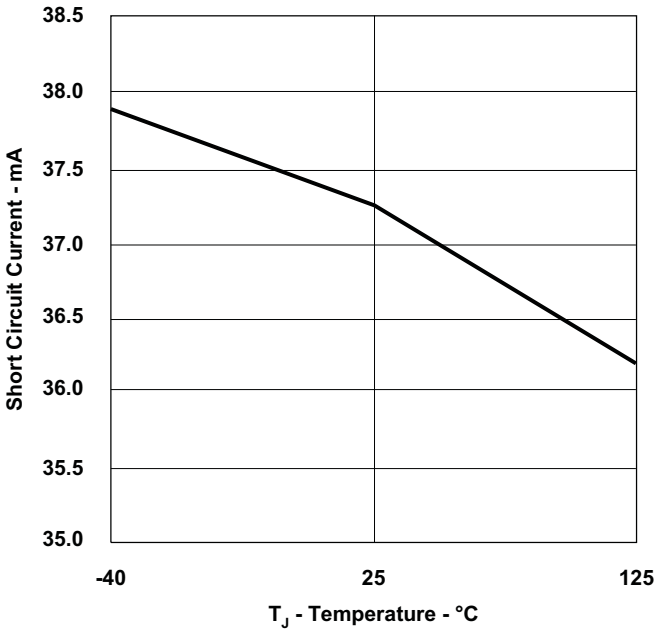


Figure 28.

MAXIMUM DUTY CYCLE vs TEMPERATURE

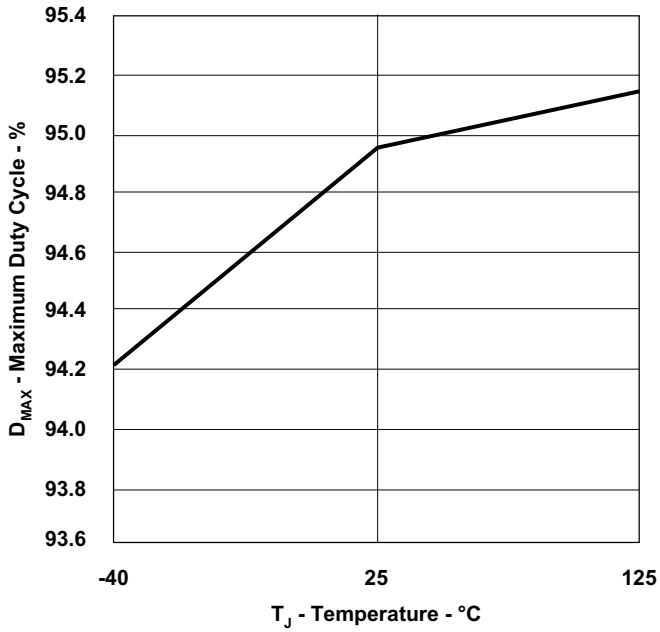


Figure 29.

TYPICAL CHARACTERISTICS (continued)

NOMINAL SWITCHING FREQUENCY vs TEMPERATURE

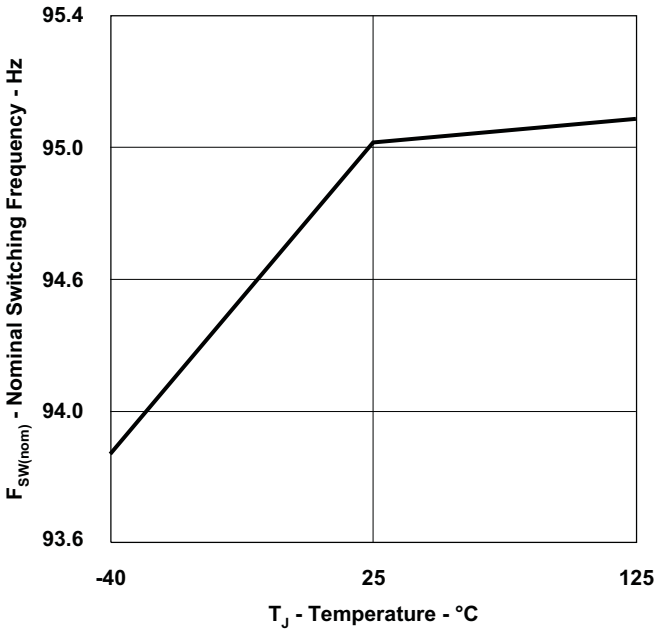


Figure 30.

MAXIMUM SWITCHING FREQUENCY vs TEMPERATURE

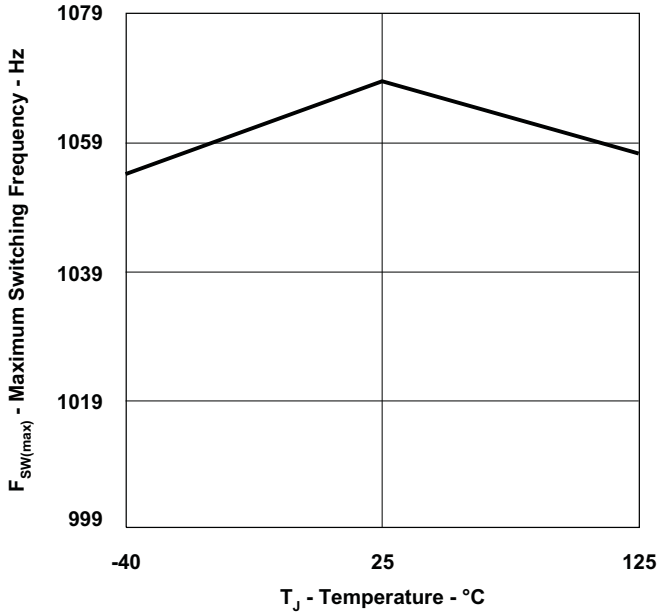


Figure 31.

ERROR AMPLIFIER OFFSET VOLTAGE vs TEMPERATURE

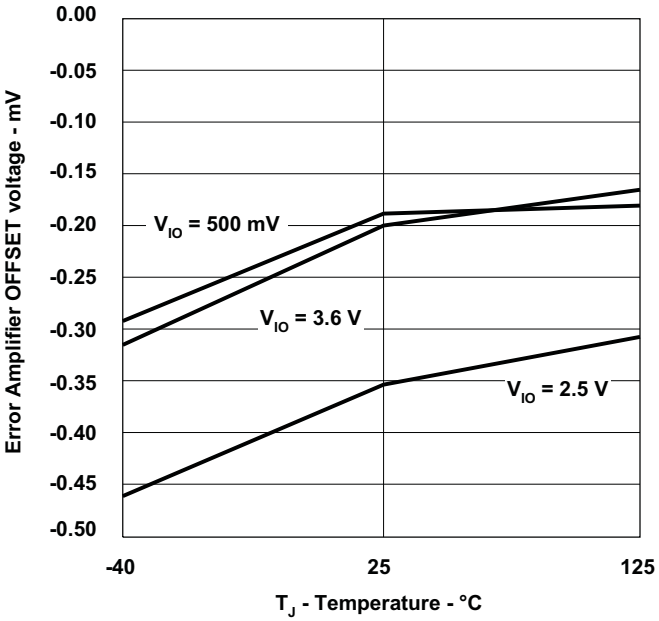


Figure 32.

VOLTAGE ERROR AMPLIFIER (Open Loop Gain) vs TEMPERATURE

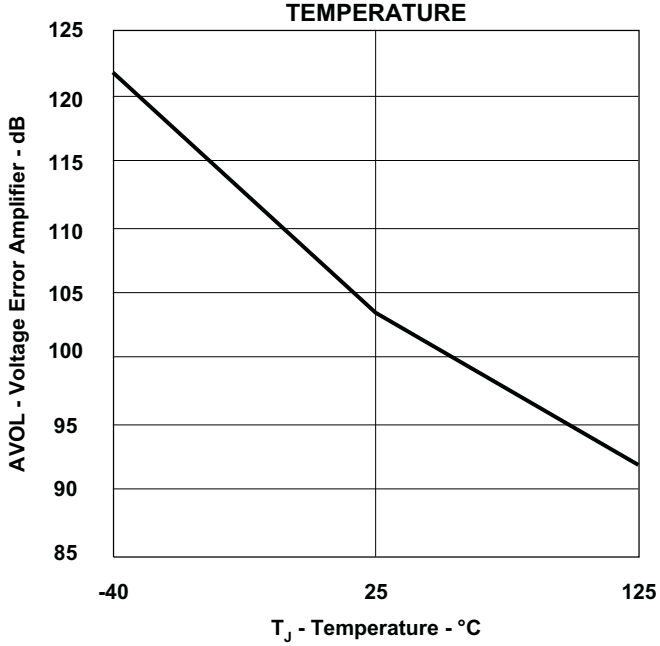


Figure 33.

TYPICAL CHARACTERISTICS (continued)

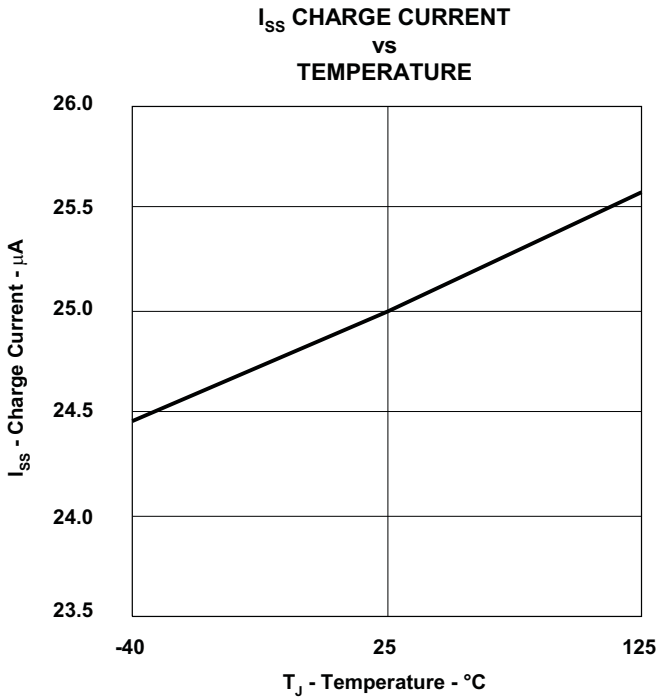


Figure 34.

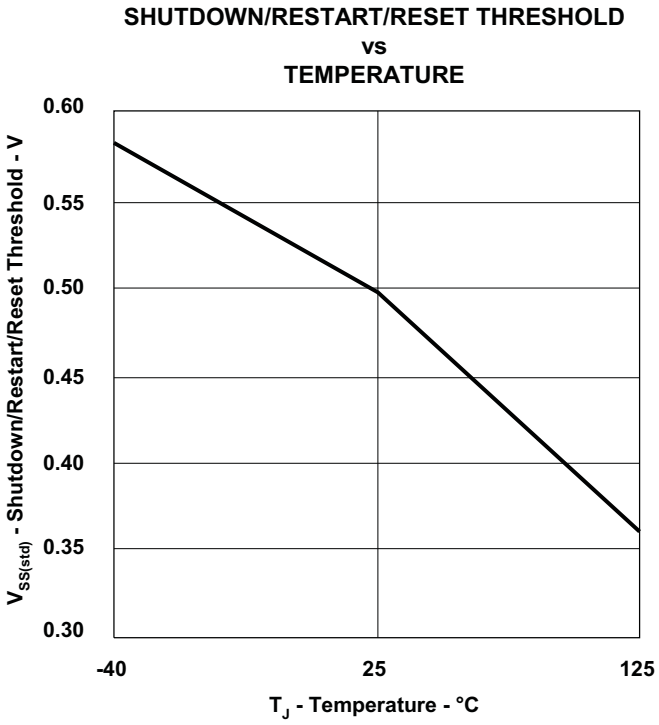


Figure 35.

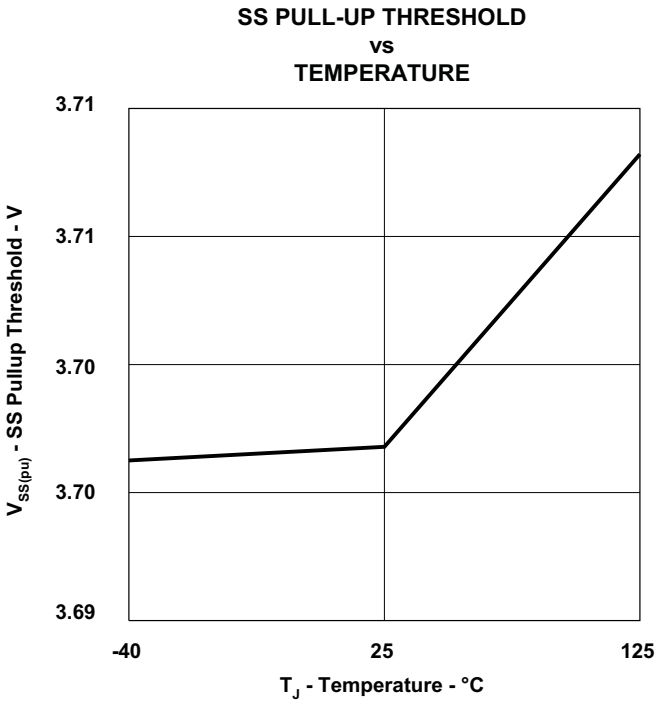


Figure 36.

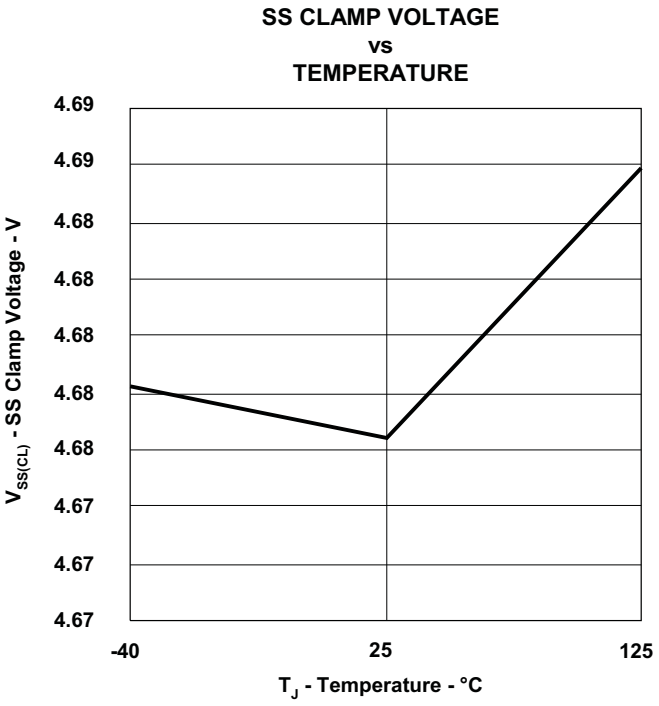


Figure 37.

TYPICAL CHARACTERISTICS (continued)

CURRENT SENSE CYCLE-BY-CYCLE LIMIT vs TEMPERATURE

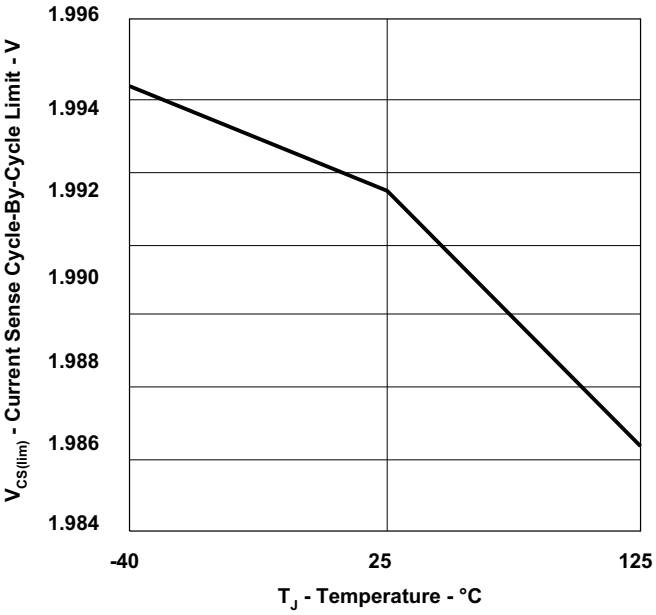


Figure 38.

CURRENT SENSE PROPAGATION DELAY vs TEMPERATURE

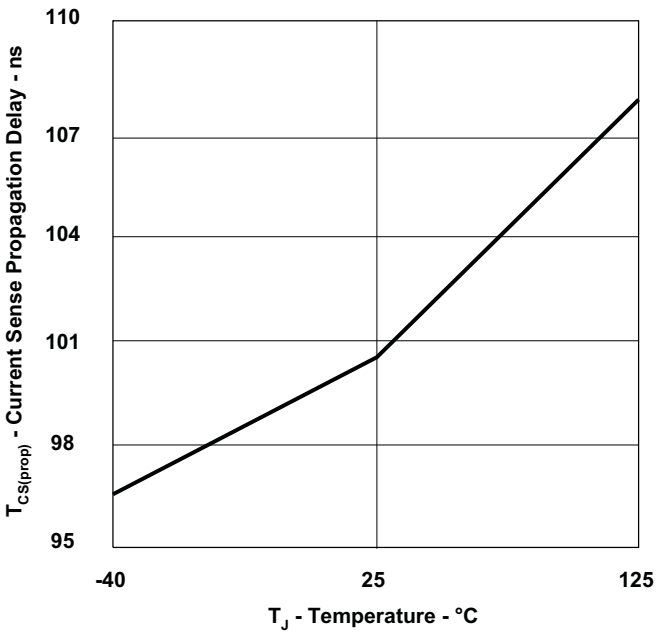


Figure 39.

OUTPUTS SINK RESISTANCE vs TEMPERATURE

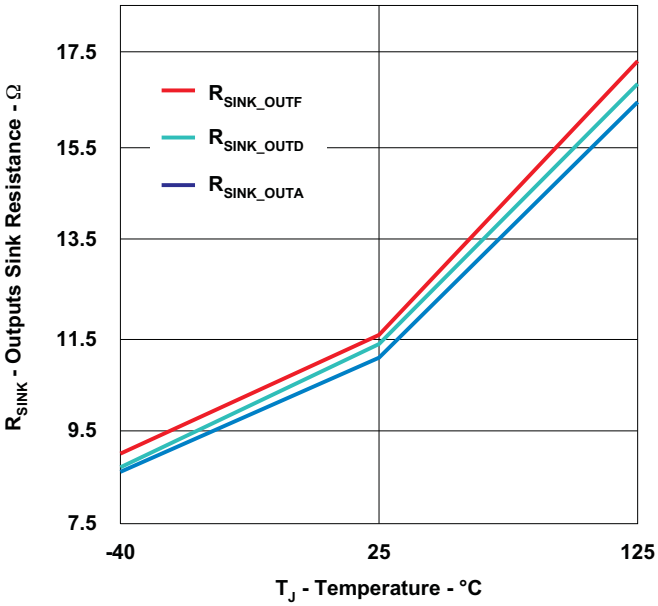


Figure 40.

OUTPUTS SINK RESISTANCE vs TEMPERATURE

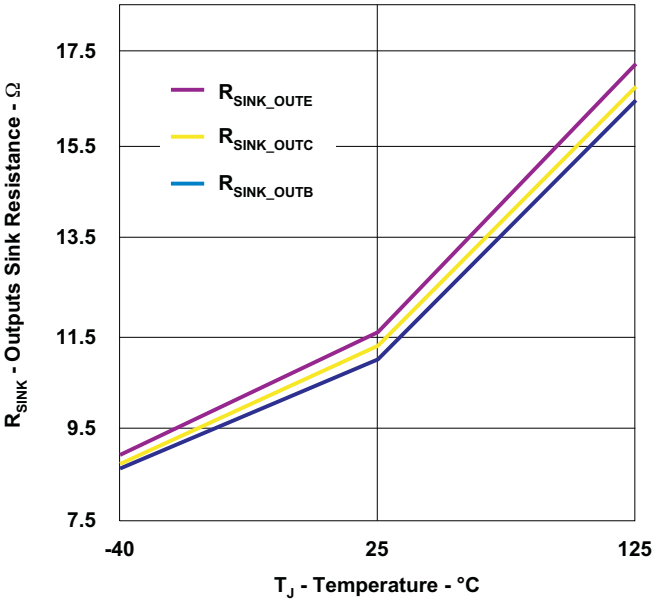


Figure 41.

TYPICAL CHARACTERISTICS (continued)

OUTPUTS SOURCE RESISTANCE vs TEMPERATURE

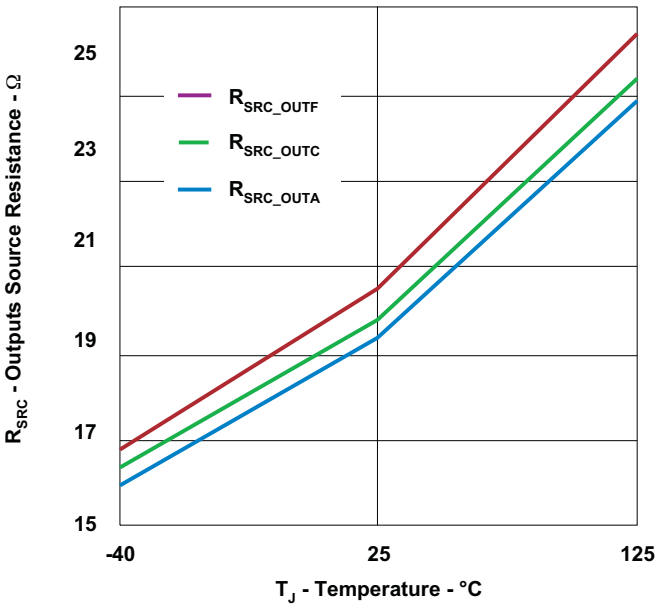


Figure 42.

OUTPUTS SOURCE RESISTANCE vs TEMPERATURE

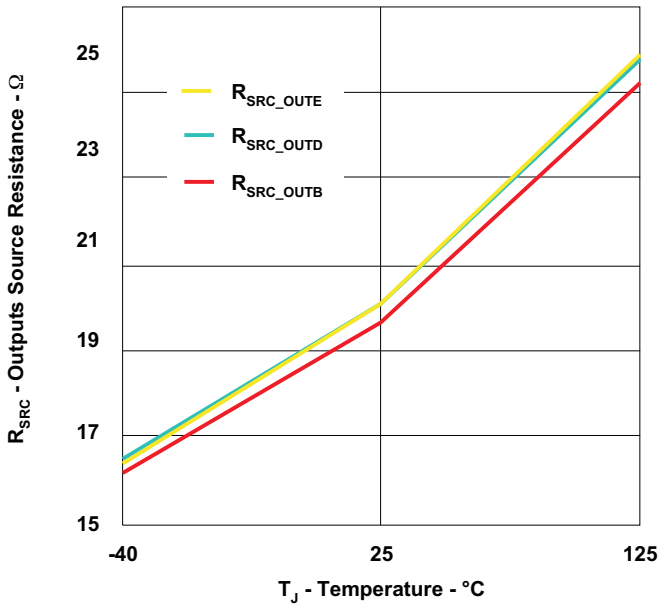


Figure 43.

DEAD TIME DELAY vs TEMPERATURE

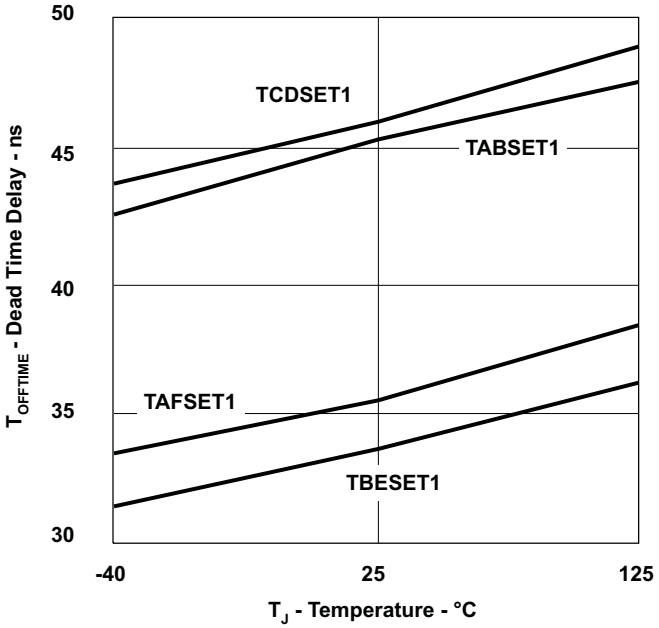


Figure 44.

DEAD TIME DELAY vs TEMPERATURE

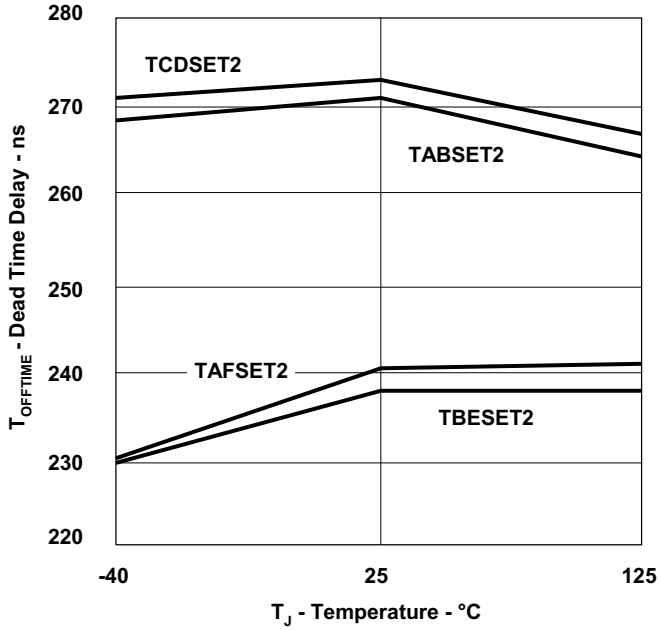


Figure 45.

TYPICAL CHARACTERISTICS (continued)

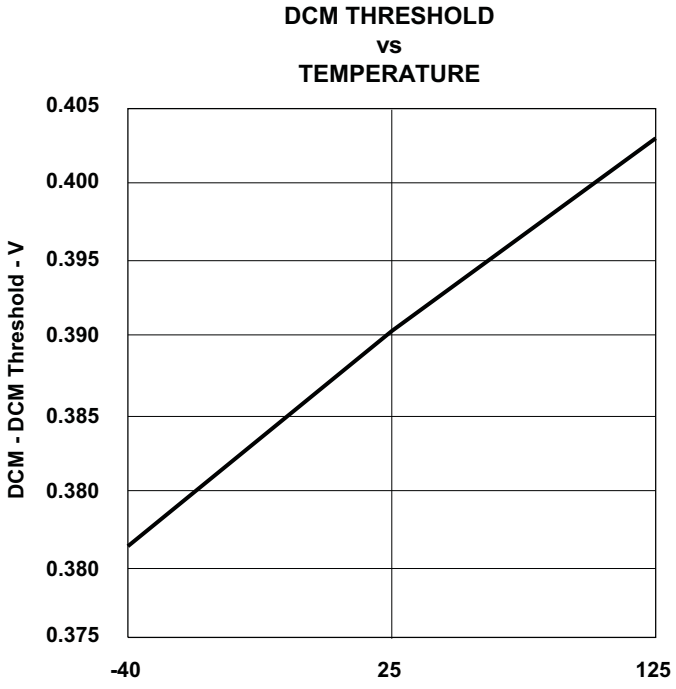


Figure 46.

APPLICATION INFORMATION

UCC28950 Application Description

The efficiency improvement of phase-shifted full-bridge DC/DC converter with UCC28950 is achieved by using the synchronous rectification technique, control algorithm providing ZVS condition over the entire load current range, accurate adaptive timing of the control signals between primary and secondary FETs and special operating modes at light load for the highest efficiency and power saving. The simplified electrical diagram of this converter is shown in Figure 47. The controller device is located on the secondary side of converter, although it could be located on primary side as well. The location on secondary side allows easy power system level communication and better handling of some transient conditions that require fast direct control of the synchronous rectifier MOSFETs. The power stage includes primary side MOSFETs, QA, QB, QC, QD and secondary side synchronous rectifier MOSFETs, QE and QF. For example, for the 12-V output converters in server power supplies use of the center-tapped rectifier scheme with L-C output filter is a popular choice.

To maintain high efficiency at different output power conditions, the converter operates in nominal synchronous rectification mode at mid and high output power levels, with transitioning to the diode rectifier mode at light load and further followed by the burst mode, as the output power becomes even lower. All these transitions are based on the current sensing on the primary side using the current sense transformer in this specific case.

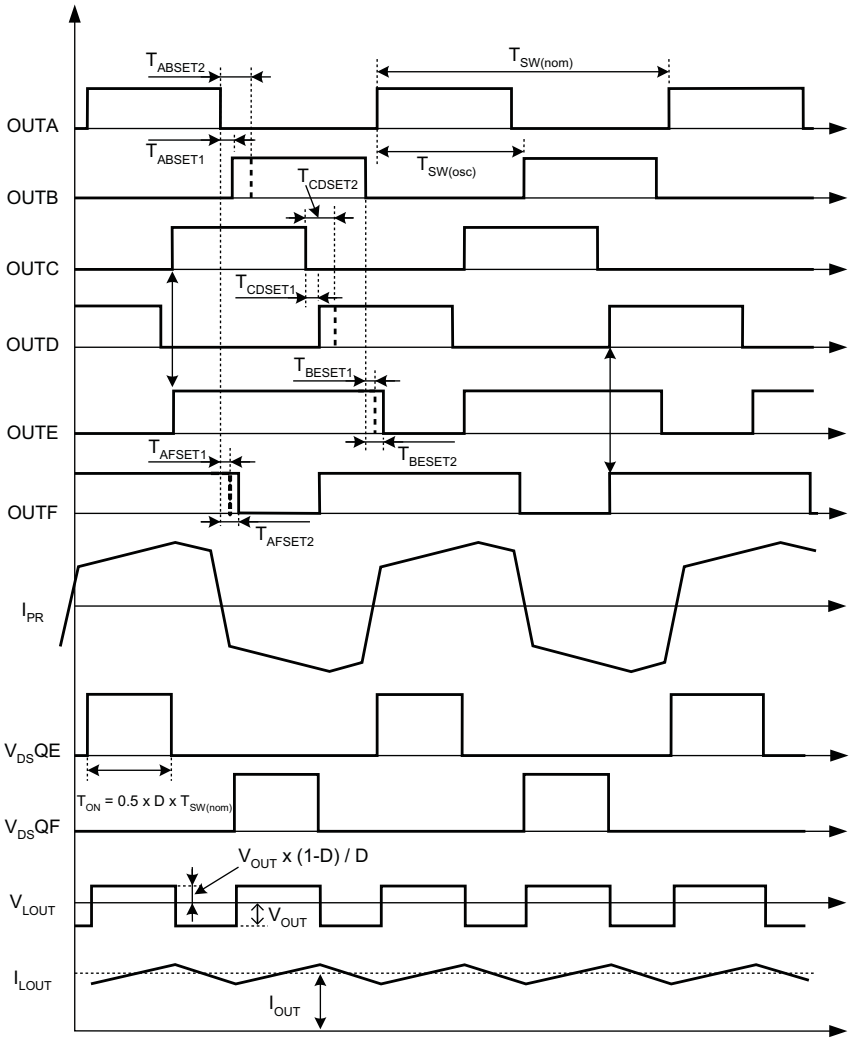


Figure 47. Major Waveforms of Phase-Shifted Converter

Major waveforms of the phase-shifted converter during nominal operation mode are shown in Figure 47. Upper six waveforms in the Figure 47 show the output drive signals of the controller. At nominal mode, the outputs OUTE and OUTF overlap during the part of the switching cycle when the both rectifier MOSFETs are conducting and the windings of power transformer are shorted. Current, I_{PR}, is the current flowing through the primary winding of power transformer. The bottom four waveforms show the drain-source voltages of rectifier MOSFETs, V_{DS_QE} and V_{DS_QF}, the voltage at the output inductor, V L_{OUT}, and the current through the output inductor, I L_{OUT}. Proper timing between the primary switches and synchronous rectifier MOSFETs is critical to achieve highest efficiency and reliable operation in this mode. The controller device adjusts the turn OFF timing of rectifier MOSFETs as function of load current to ensure the minimum conduction time and reverse recovery losses of their internal body diodes.

ZVS is an important feature of relatively high input voltage converters to reduce switching losses associated with the internal parasitic capacitances of power switches and transformers. The controller ensures ZVS conditions over the entire load current range by adjusting the delay time between the primary MOSFETs switching in the same leg in accordance to the load variation. Controller also limits the minimum ON-time pulse applied to the power transformer at light load, allowing the storage of sufficient energy in the inductive components of power stage for the ZVS transition.

As soon as the load current keeps reducing from the mid load current down to no-load condition, the controller selects the most efficient power saving mode by moving the converter from the nominal operation mode to the discontinuous-current diode-rectification mode and, eventually, at very light-load and at no-load condition, to the burst mode. These modes and related output signals, OUTE, OUTF, driving the rectifier MOSFETs, are shown in Figure 48.

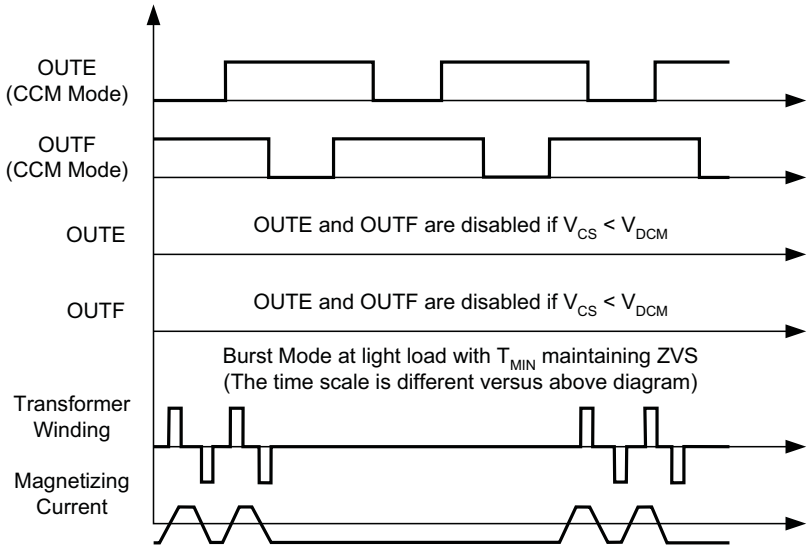


Figure 48. Major Waveforms During Transitions Between Different Operating Modes

It is necessary to prevent the reverse current flow through the synchronous rectifier MOSFETs and output inductor at the light load, during parallel operation and at some transient conditions. Such reverse current results in circulating of some extra energy between the input voltage source and the load and, therefore, causes increased losses and reduces efficiency. Another negative effect of such reverse current is the loss of ZVS condition. The suggested control algorithm prevents reverse current flow, still maintaining most of the benefits of synchronous rectification by switching off the drive signals of rectifier MOSFETs in a predetermined way. At some pre-determined load current threshold, the controller disables outputs OUTE and OUTF by bringing them down to zero.

Synchronous rectification using MOSFETs requires some electrical energy to drive the MOSFETs. There is a condition below some light-load threshold when the MOSFET drive related losses exceed the saving provided by the synchronous rectification. At such light load, it is best to disable the drive circuit and use the internal body diodes of rectifier MOSFETs, or external diodes in parallel with the MOSFETs, for more efficient rectification. In most practical cases, the drive circuit needs to be disabled close to DCM mode. This mode of operation is called discontinuous-current diode-rectification mode.

At very light-load and no-load condition, the duty cycle, demanded by the closed-feedback-loop control circuit for output voltage regulation, can be very low. This could lead to the loss of ZVS condition and increased switching losses. To avoid the loss of ZVS, the control circuit limits the minimum ON-time pulse applied to the power transformer using resistor from TMIN pin to GND. Therefore, the only way to maintain regulation at very light load and at no-load condition is to skip some pulses. The controller skips pulses in a controllable manner to avoid saturation of the power transformer. Such operation is called burst mode. In Burst Mode there are always an even number of pulses applied to the power transformer before the skipping off time. Thus, the flux in the core of the power transformer always starts from the same point during the start of every burst of pulses.

Voltage Loop Compensation Recommendation

For best results in the voltage loop it is recommended to use Type 2 or Type 3 compensation network (Figure 49). A type 2 compensation network does not require passive components C_{Z2} and R_{Z2}. Type 1 compensation is not versatile enough for a phase shifted full bridge. When evaluating the COMP for best results it is recommended to put a 1-kΩ resistor between the scope probe and the COMP pin of the UCC28950.

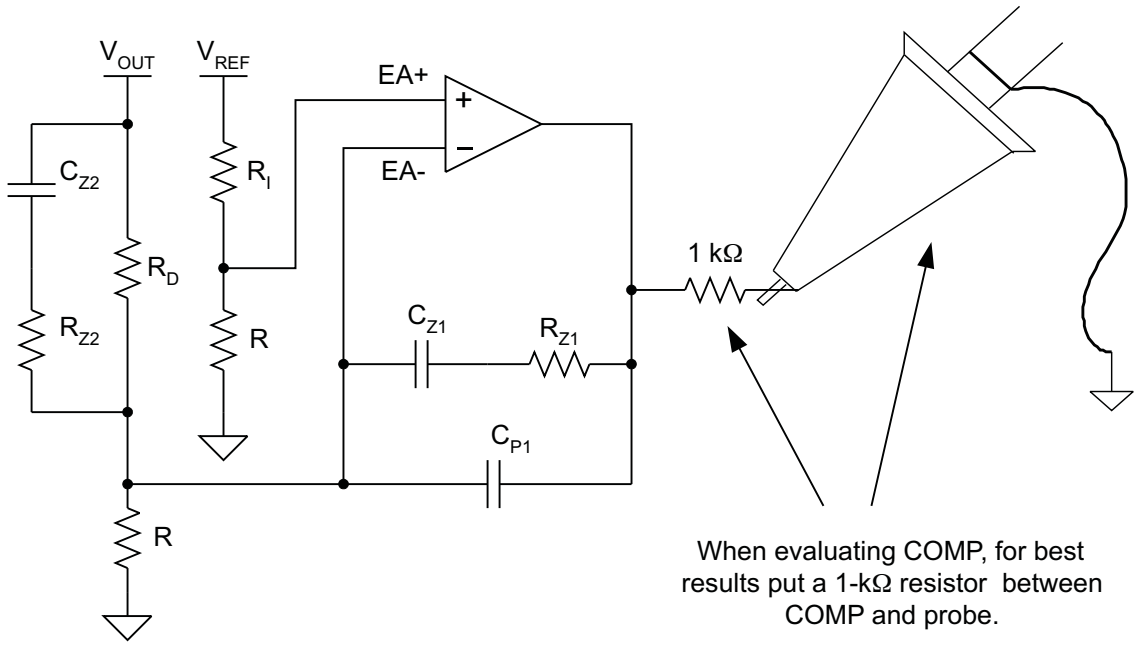


Figure 49. Type 3 Compensation Evaluation

Experimental Results Example

The following experimental results are based on 660-W output power prototype of phase shifted full-bridge DC/DC converter. The input voltage is 300 V to 400 V and the output is 12 V, 55 A. The primary MOSFETs are SPA11N60CFD and the synchronous rectifier MOSFETs are FDP047AN08A0, two in parallel. The measured efficiency of the prototype is shown in Figure 50.

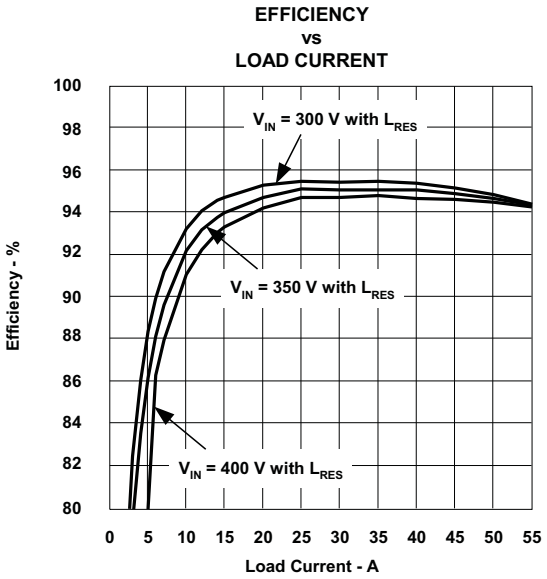


Figure 50. Efficiency of the Prototype Phase-Shifted Converter (V_{IN} = 300 V, 350 V and 400 V, V_{OUT} = 12 V)

Because of the power saving need even at very light and no-load conditions, careful optimization of operation at light load condition is required to set the proper boundaries between different operation modes. The result of this optimization is shown in Figure 51. This plot demonstrates the power savings while moving from the synchronous rectification mode above 1-A load current, into the discontinuous current mode with the diode rectification between 0.3-A and 1-A load current, and eventually into the burst mode operation at load current below 0.3 A.

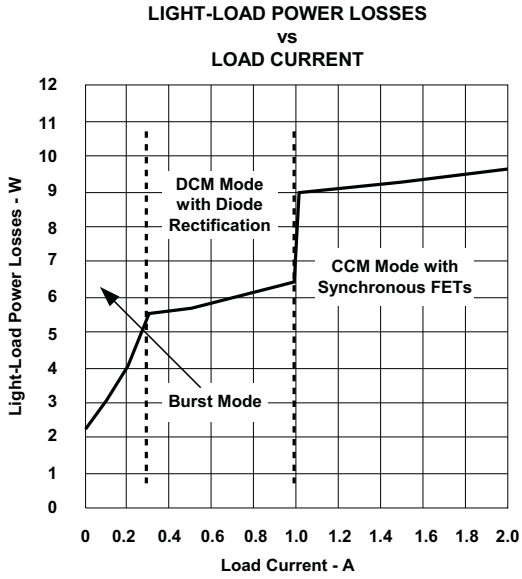


Figure 51. Power Losses of the Prototype at Light-Load and No-Load Conditions

REVISION HISTORY

Changes from Original (March 2010) to Revision A **Page**

- Changed UCC28950 Typical Application Diagram 1
- Changed Converter switching frequency from 1400 kHz to 1000 kHz 3
- Changed Functional Block Diagram 8
- Changed Typical Application Diagram 8
- Added Figure 5 15
- Changed Equation 16
- Added Typical Application Diagram 16
- Added always deliver even number of Power cycles to Power transformer. 18
- Deleted deliver either one or two power delivery cycle pulses. If controller delivers a power delivery cycle for OUTB and OUTC, then it stops. If it starts delivering to OUTA and OUTD, then it continues with another power delivery cycle to OUTB and OUTC, and then it stops. 18

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
UCC28950PW	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC28950PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

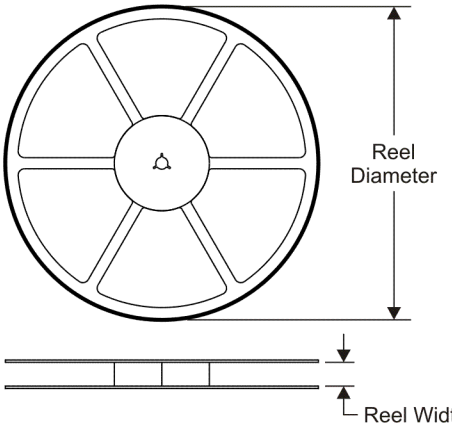
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

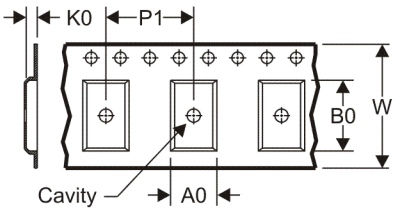
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

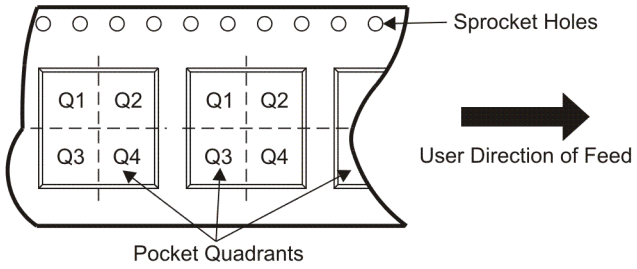


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

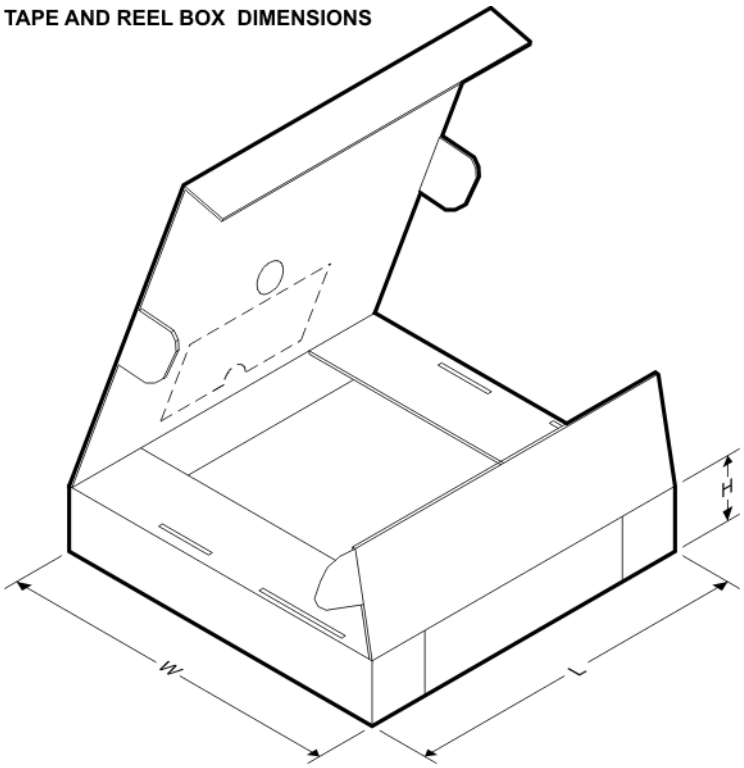
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC28950PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS

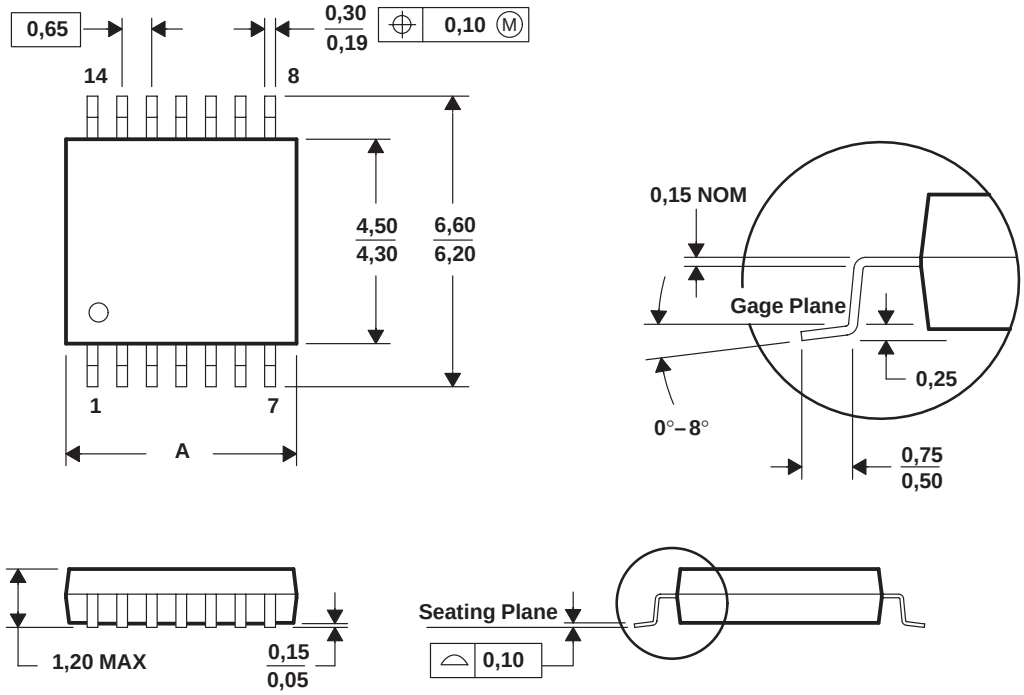


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC28950PWR	TSSOP	PW	24	2000	346.0	346.0	33.0

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

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NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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